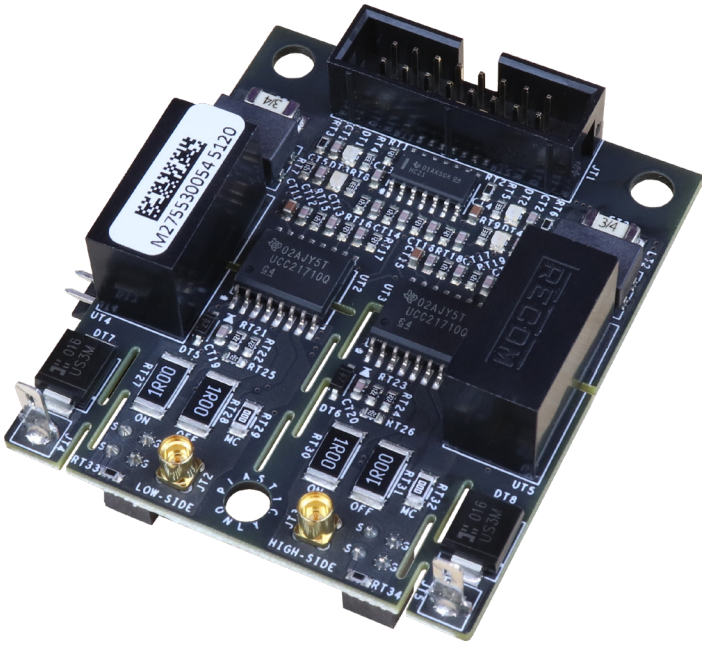
User Guide PRD-06992

CGD1700HB2M-UNA Gate Driver User Guide



Part Number	Description
CGD1700HB2M-UNA	Unregulated Output (+15 V / -3 V)
CGD1700HB2M-UNA-R1	Regulated Output (+15 V / -4 V)
CGD1700HB2M-UNA-R2	Regulated Output (+18 V / -4 V)

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请勿在通电情况下接触板子，在操作板子前应使大容量电容器的电荷完全释放。接通电源后，该评估板上通常会存在危险的高电压，板子上一些组件的温度可能超过50摄氏度。此外，移除电源后，上述情况可能会短时持续，直至大容量电容器电量完全释放。

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死亡 ▲ 严重伤害 ▲ 触电 ▲ 电击 ▲ 电灼伤 ▲ 严重的热烧伤

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通電している時、ボードに接触するのは禁止です。ボードを処分する前に、大容量のコンデンサーで電力を完全に釈放すべきです。通電してから、ボードにひどく高い電圧が存在している可能性があります。ボードのモジュールの温度は50度以上になるかもしれません。また、電源を切った後、上記の状況がしばらく持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。

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CGD1700HB2M-UNA Gate Driver User Guide

Contents

1. Introduction

The CGD1700HB2M-UNA gate driver, shown in Figure 1, is a dual channel isolated gate driver optimized for Wolfspeed's power MOSFETs. The gate driver uses Wolfspeed's universal gate driver board footprint and is compatible with many Wolfspeed power module evaluation boards and the Wolfspeed SpeedVal™ platform. The gate driver is designed for high-frequency operation and can drive high-performance silicon carbide (SiC) MOSFETs in both discrete and module packages. It features separate 2 W isolated power supplies and Texas Instruments® UCC21710 gate drivers for independently operating two channels such as the high- and low-side switch positions of a SiC half bridge. The design includes input voltage protection, differential inputs for increased noise immunity, soft shutdown, anti-overlap functionality, undervoltage lockout, and overcurrent protection. This user guide provides an overview of the gate driver functions and parameters including connector pinouts and operating guidance.

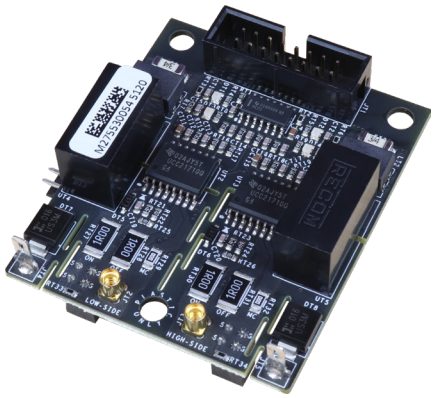

Figure 1: CGD1700HB2M-UNA gate driver

1.1 Gate Driver Variations

There are multiple variations of the CGD1700HB2M-UNA gate driver used to support different applications. The difference between the configurations is the output gate-to-source voltage (V_{GS}) rails which are summarized in Table 1. The default CGD1700HB2M-UNA variant directly uses the output of the onboard isolated DC/DC converters (see Section 4.3) to generate the V_{GS} voltage rails (+15 V / -3 V). These outputs are not well regulated, though this approach would typically be adopted in many end applications. In this configuration, the isolated DC/DC converters provide suitable regulation for safely operating SiC MOSFETs without requiring the cost burden of more components. In applications requiring critical regulation (such as characterization measurements) or alternative voltages, Wolfspeed offers variations with precise output voltages using linear regulators for stable and adjustable output voltages (see Section 4.3.2). Note that regulation can be added later as an upgrade to an unregulated variant (see Section 4.3.3) or modified by an end user (see Section 4.3.4).

Table 1: CGD1700HB2M-UNA gate driver variations

Part Number	Description
CGD1700HB2M-UNA	Unregulated Output (+15 V / -3 V)
CGD1700HB2M-UNA-R1	Regulated Output (+15 V / -4 V)
CGD1700HB2M-UNA-R2	Regulated Output (+18 V / -4 V)

2. Design Features

The CGD1700HB2M-UNA gate driver is designed to operate at DC bus voltages up to 1500 V and includes system benefits such as onboard overcurrent, shoot-through, and reverse polarity protection. The maximum operating parameters of this gate driver design are shown in Table 2 and the full list of electrical parameters are shown in Table 3. Renderings of the board assembly from various views are shown in Figure 2.

2.1 Maximum Operating Parameters

Table 2: Maximum operating parameters (verified by design)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DC}	-0.5 to 13.2	V
Logic Level Input	V_I	-0.5 to 5.5	
Output Peak Current (T_A = 25 °C)	I_O	±10	A
Output Power Per Channel (T_A = 25 °C)	P_{DRIVE}	2	W
Maximum Switching Frequency (MOSFET & V_{GS} Dependent, See Section 4.8)	f_{SW}	1	MHz
Ambient Operating Temperature	T_{OP}	-40 to 70	°C
Storage Temperature	T_{STG}	-40 to 85	

2.2 Assembly

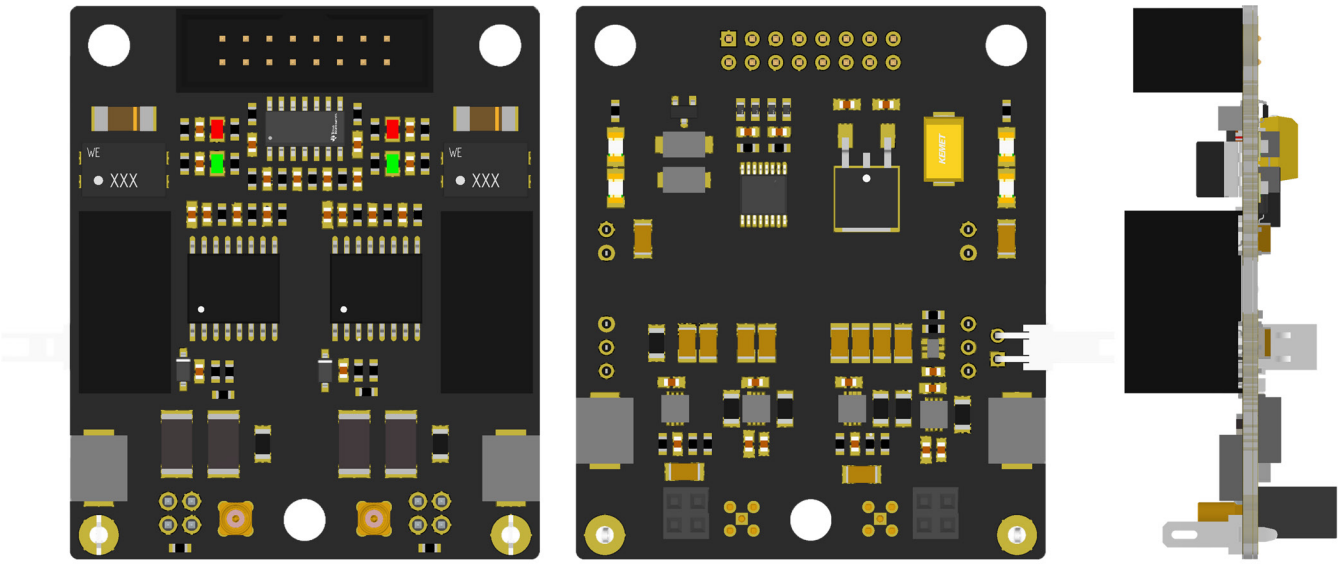

Figure 2: CGD1700HB2M-UNA rendering views

2.3 Electrical Characteristics

Table 3: Electrical characteristics (T = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V_{DC}	10.8	12	13.2		
Secondary Under Voltage Lockout	V_{UVLO}	10.5	12.0	12.8		
Secondary UVLO Hysteresis	V_{HYS}		0.8			
Input Over Voltage Clamping	V_{OVLO}		20			Zener Diode Voltage
High Level Logic Input Voltage	V_{IH}	3.5		5.5		Single-Ended Inputs
Low Level Logic Input Voltage	V_{IL}	0		1.5		(Based on AND Gate Input)
Diff Input Common Mode Range	V_{IDCM}			± 7		Differential Inputs
Positive-going input threshold voltage, differential input	V_{IT+}			0.2	V	$V_{ID} = V_{POS-LINE} – V_{NEG-LINE}$
Negative-going input threshold voltage, differential input	V_{IT-}	-0.2				
High level Output Voltage	$V_{GATE,HIGH}$		+15			-UNA, -UNA-R1 Variants
			+18			-UNA-R2 Variant
Low level Output Voltage	$V_{GATE,LOW}$		-3			-UNA Variant
			-4			-UNA-R1, -UNA-R2 Variants
Working Isolation Voltage	V_{IOWM}		1500			V_{RMS}
Isolation Capacitance	C_{ISO}		4		pF	Per Channel
Common Mode Transient Immunity	CMTI	150			kV/µs	V_{CM} = 1500 V
Output Resistance[1]	$R_{G(IC)-ON}$		0.7		Ω	Tested at 0.1 A
	$R_{G(IC)-OFF}$		0.3			
External Resistance[2]	$R_{G(EXT)-ON}$		1			External SMD Resistor 2512 (6432 Metric)
	$R_{G(EXT)-OFF}$		1			
Output Rise Time	t_{ON}		600		ns	$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF From 10% to 90%
Output Fall Time	t_{OFF}		300			
Propagation Delay (Turn-Off)	t_{PHL}		143			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF From 50% to 50%
Propagation Delay (Turn-On)	t_{PLH}		135			
Over-current Blanking Time	t_{BLANK}		275			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Over-current Propagation Delay to FAULT Signal Low	$t_{PD-FAULT}$		0.4		µs	Does Not Include Blanking
Soft-Shutdown Time	t_{SS}		2.8			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Soft-Shutdown Current[3]	I_{STO}	250	400	570	mA	$V_{DD} – V_{EE}$ = 20 V, $V_{OUTL} – COM$ = 8 V
Miller Clamp Resistance	R_{MC}		0.6		Ω	Tested at 200 mA
Miller Clamp Voltage Threshold	V_{MC}	1.5	2.0	2.5	V	Reference to Source

[1] Output resistance of gate driver integrated circuit (IC).

[2] Additional output resistance is added with surface mount device (SMD) resistors. Separate resistors allow for independent tuning.

[3] Soft-shutdown network will safely turn off the gate if an overcurrent event is detected.

2.4 Block Diagram

A block diagram of the full gate driver is shown in Figure 3. Both channels (high- and low-side) include a dedicated isolated DC/DC converter and gate driver integrated circuit (IC) for independent modulation of the respective channels. The gate driver communicates with a controller via differential signaling for both input and feedback signals. The gate driver combines all onboard fault signals (i.e. overcurrent and power faults for both channels) into a single global fault signal which is transmitted to the controller to indicate the board status. The board includes an overcurrent detection circuit, independent turn-on and turn-off resistors, Miller clamp, and thermistor feedback. Some notable interface features on the board are indicated in Figure 4.

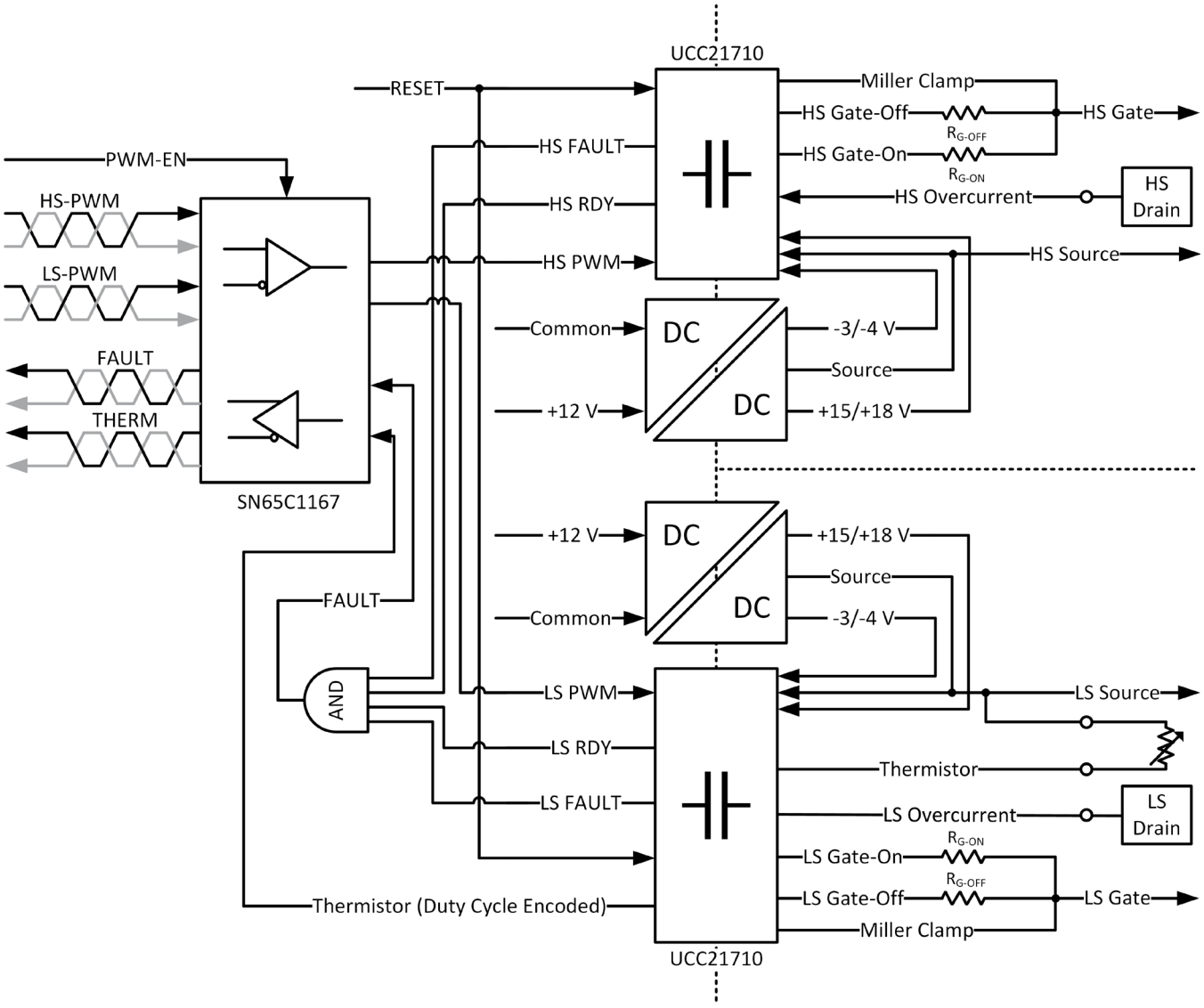

Figure 3: Block diagram of CGD1700HB2M-UNA gate driver

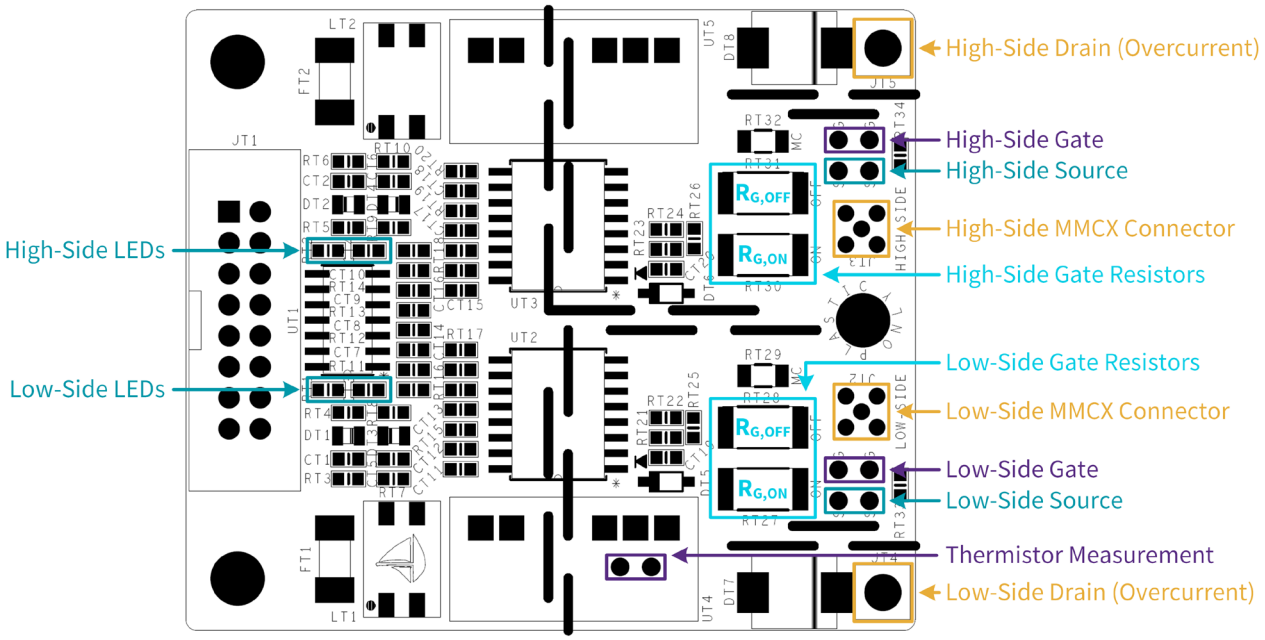

Figure 4: Interface of CGD1700HB2M-UNA gate driver

3. Inputs/Outputs

The CGD1700HB2M-UNA gate driver includes multiple connectors for interfacing with the power module and control signals and to perform measurements. This section details the pinouts and functionalities of each of these connectors. An overview of the purpose of each connector is shown in Table 4 along with the corresponding document section to find additional information.

Table 4: Summary of input/output connectors

Ref. Des.	Side	Description	Section
JT1	Top	Input signals	3.1
JT2	Top	Low-side V_{GS} measurement	3.5
JT3	Top	High-side V_{GS} measurement	3.5
JT4	Top	Low-side overcurrent feedback	3.4
JT5	Top	High-side overcurrent feedback	3.4
JB1	Bottom	Thermistor feedback	3.3
JB2	Bottom	High-side output	3.2
JB3	Bottom	Low-side output	3.2

3.1 Input Connector

The CGD1700HB2M-UNA gate driver is intended to operate with differential signaling for improved noise immunity compared to single-ended signaling (see Section 4.2). All the control and feedback signals with this gate driver are digital and interface through a single input connector (reference designator *JT1*). The connector orientation and the corresponding pin locations are shown in Figure 5. *JT1* uses part number SBH11-NBPC-D08-SM-BK manufactured by Sullins Connector Solutions® and the suggested mating parts are listed in Table 5.

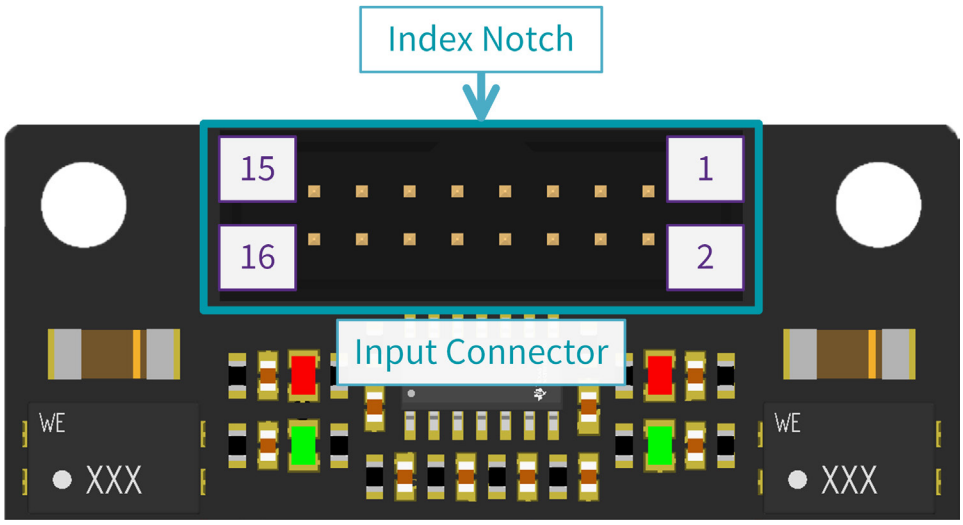

Figure 5: JT1 input connector orientation and pin locations

Table 5: Input connector suggested mating parts

Component	Manufacturer	Part Number	Description
Mating IDC Connector	Sullins Connector Solutions	SBH11-NBPC-D08-SM-BK	16 Position Rectangular Header Connector IDC Gold 28 AWG
Straight Ribbon Cable[1]	3M	HF365/16SF	Flat Ribbon Cable Gray 16 Conductors 0.050" (1.27mm) Flat Cable
Twisted Ribbon Cable[1]	3M	1700/16 100SF	Flat Ribbon Cable Multiple 16 (8 Pair Twisted) Conductors 0.050" (1.27mm)
Mating Vertical (PCB Mount)	Sullins Connector Solutions	SFH11-PBPC-D08-ST-BK	16 Position Header Connector 0.100" (2.54mm) Through Hole Gold
Mating Right-Angle (PCB Mount)	Sullins Connector Solutions	SFH11-PBPC-D08-RA-BK	16 Position Header Connector 0.100" (2.54mm) Through Hole, Right Angle Gold

[1] When using ribbon cable for long connections, it is recommended to use twisted-pair ribbon cable for improved noise immunity.

3.1.1 Pinout

Table 6: Pinout of JT1 input connector

Pin	Name	Description
1	VDC	Power supply input pin (+12 V Nominal Input).
2	Common	Common.
3	HS-PWM-P*	Positive line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
4	HS-PWM-N*	Negative line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
5	LS-PWM-P*	Positive line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
6	LS-PWM-N*	Negative line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
7	$\overline{\text{FAULT}}$-P*	Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA. A low state on FAULT indicates when a desaturation fault has occurred. The presence of a fault precludes the gate drive output from going high.
8	$\overline{\text{FAULT}}$-N*	Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA.
9	THERM-P*	Positive line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via duty cycle.
10	THERM-N*	Negative line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via duty cycle.
11	NC	No connect.
12	Common	Common.
13	No	No connect.
14	Common	Common.
15	$\overline{\text{RESET}}$/EN	Pull up or leave floating to enable the gate driver. Onboard 10 kΩ pull up. When a fault exists, bring this pin low for >1000 ns to clear the fault on the rising edge.
16	Common	Common.

* Inputs 3-10 are differential pairs.

3.1.2 Signal Descriptions

PWM Signals: High-side and low-side pulse-width modulation (PWM) signals are RS-422 compatible differential inputs. The termination impedance of the differential receiver is 120 Ω. Overlap protection is provided to prevent both the high-side and low-side gates from turning on simultaneously. The overlap protection should not be used as a dead time generator.

$\overline{FAULT}$ Signal: The fault signal is a RS-422 compatible differential output with a maximum drive strength of 20 mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. This signal will be low if an overcurrent fault or undervoltage-lockout (UVLO) fault condition is detected on either channel. After an overcurrent fault, this signal will latch low until the gate driver is reset via the $\overline{RESET}/EN$ signal. The presence of a fault precludes the gate drive output from going high. The onboard light-emitting diodes (LEDs) will also indicate the fault condition. See Sections 3.6 and 4.4 for more details.

THERM Signal: THERM output is a differential signal that returns the resistance of an attached thermistor. It is a duty cycle signal that encodes the resistance of the temperature sensor. The approximate temperature of the module can be determined from this resistance. The signal operates at 400 kHz with a duty cycle ranging from 10% to 88%. See the Sections 3.3 and 4.7 for further details.

$\overline{RESET}$/EN Signal: This is a single-ended input that can be used to enable the gate driver and clear overcurrent faults on the gate driver. During normal operating, this signal should be held high or left floating to enable the gate driver. This signal is held high by default with an onboard 10 kΩ resistor. When this signal is low, both gate driver channel outputs will be held off. To clear an overcurrent fault, this signal must be commanded low for at least 1000 ns. The gate driver overcurrent fault will be cleared at the following rising edge of the signal. This signal enables and resets both channels of the gate driver.

3.2 Output Connectors

The output connectors on the CGD1700HB2M-UNA gate driver are four-pin 0.1 inch standard headers designed to attach to a printed circuit board (PCB) with mating connectors very close to the gate and source pins of the target MOSFET. The connections should be as close as possible to the gate and source pins to limit introducing parasitic inductance to the gate loop. An example connection is shown in Figure 6 for the KIT-CRD-CIL23N-GMA Evaluation Board where the gate driver mates directly with the power PCB immediately adjacent to the module gate and source terminals. The gate and source output connections for both channels, *JB2* and *JB3*, are shown in Figure 7. Both connectors use SSW-102-01-G-D manufactured by Samtec® and the recommended mating parts are summarized in Table 7. The high- and low-side output connectors are isolated from each other and do not share a source connection.

Figure 6: Example CGD1700HB2M-UNA attached to a power module evaluation board

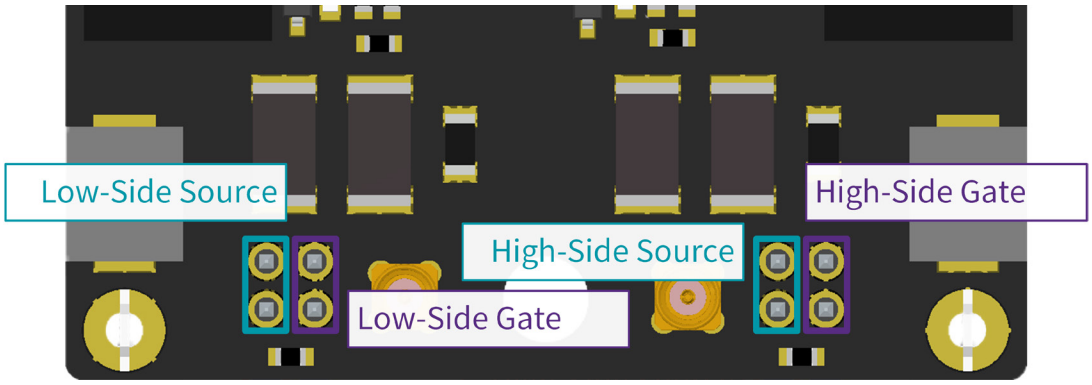

Figure 7: JB2 and JB3 output connectors orientations and pin locations

Table 7: Output connectors suggested mating parts

Component	Manufacturer	Part Number	Description
Mating (Surface Mount)	Samtec	TSM-102-01-SM-DV	Connector Header Surface Mount 4 position 0.100" (2.54mm)
Mating (Through-Hole)	Samtec	TSW-102-07-F-D	Connector Header Through Hole 4 position 0.100" (2.54mm)

3.3 Thermistor Connector

Many Wolfspeed power modules include an integrated negative temperature coefficient (NTC) thermistor for monitoring the baseplate temperature of the module (see **PRD-08376**). The CGD1700HB2M-UNA includes circuitry to directly measure the thermistor and encode the resistance as a duty cycle. This circuitry can also be utilized to measure thermistors attached elsewhere on the MOSFET or PCB, which can be useful for measuring temperatures in systems that do not include an integrated thermistor. The thermistor connector, *JB1*, uses the 22-28-1020 connector manufactured by Molex and is shown in Figure 8. The recommended mating connector is 0022012027 manufactured by Molex with 0008500113 pins from Molex. The polarity of the thermistor does not matter, though the "+" and "-" designators are shown for reference to indicate where the pins connect on the gate driver board. This connector can be left floating when not in use. See Section 4.7 for more information about the thermistor circuit and corresponding duty cycle encoding.

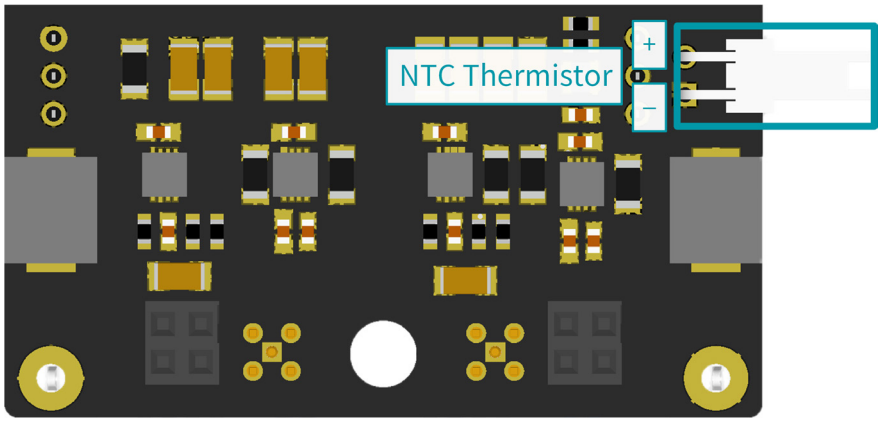

Figure 8: JB1 thermistor connector orientation and pin locations

3.4 Overcurrent Feedback Connectors

The desaturation circuits employed on this design for overcurrent protection (see Section 4.4.3) require accurate feedback of the MOSFET drain terminals to identify when the device is conducting high currents, such as when the device output is shorted. The CGD1700HB2M-UNA gate driver includes dedicated connectors to connect to the drain terminals for overcurrent protection of each channel. The gate driver includes *JT4* for the low-side overcurrent protection and *JT5* for the high-side overcurrent protection. Both connections are 735187-2 connectors manufactured by TE Connectivity and are shown in Figure 9. The recommended mating connectors for these are 7-520365-2 or 2-520272-2 which are both manufactured by TE Connectivity. For the best results, a flying wire should be attached to this connector as close as possible to the drain terminal of the corresponding switch position drain. The flying wire should be kept as short as possible.

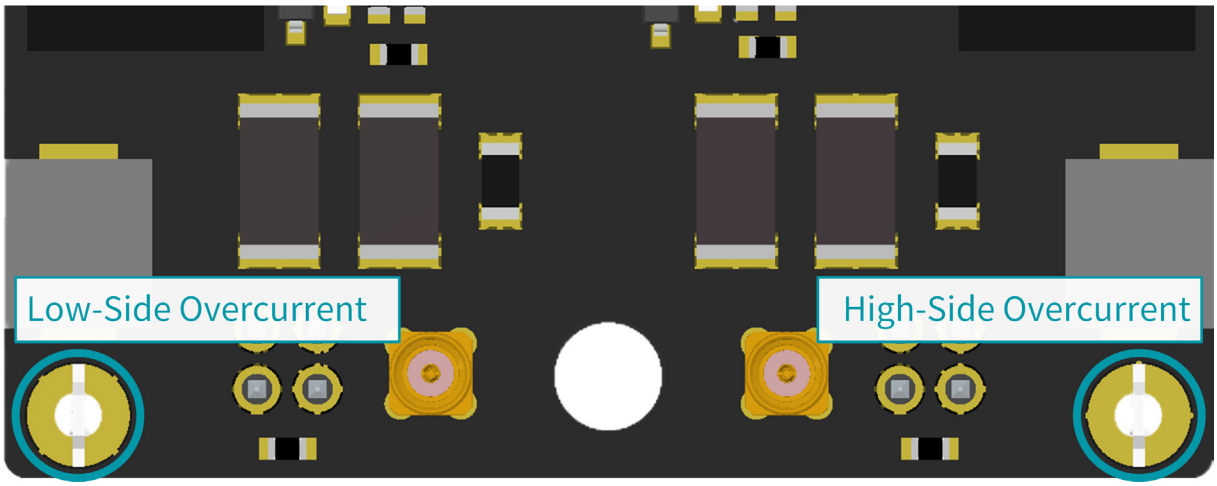

Figure 9: JT4 and JT5 overcurrent feedback connector locations

These connectors cannot be left floating as the overcurrent fault will trip immediately when the associated gate is actuated. If bench-top testing of the gate driver is required, it is acceptable to short the connector to the appropriate source (i.e. connect *JT4* to the low-side source and connect *JT5* to the high-side source) to prevent the overcurrent fault from tripping during testing. **Performing this modification will bypass the overcurrent protection,** so the gate driver will no longer be protecting the MOSFET(s).

3.5 Gate-to-Source Voltage Measurement Connectors

A high-fidelity gate-to-source voltage measurement (V_{GS}) is critical for many applications such as device characterization, system commissioning, and troubleshooting. The CGD1700HB2M-UNA gate driver includes integrated micro-miniature coaxial (MMCX) connectors for measuring the V_{GS} outputs of the gate driver. The pinouts and locations for the measurement connectors are shown in Figure 10. A variety of probes can interface directly with these standard MMCX connectors. Wolfspeed recommends performing these measurements with an optically isolated probe such as the Tektronix® IsoVu™ series of probes to ensure high common-mode rejection during measurements. This is especially critical for the high-side V_{GS} measurement which is referenced to a varying voltage node. In applications where the CGD1700HB2M-UNA is not placed immediately adjacent to the MOSFET gate/source terminals and in applications requiring extremely high-fidelity measurements (such as characterization measurements), it is recommended to include a separate V_{GS} probe location right next to

the MOSFET. The output connectors of the CGD1700HB2M-UNA include some parasitic inductance which can obfuscate dynamics occurring at the MOSFET terminals. In characterization measurements, it is critical that the V_{GS} measurement is as close as possible to the MOSFET terminals. For example, the KIT-CRD-CIL23N-GMA evaluation board shown in Figure 6 includes additional V_{GS} measurement connectors on the power PCB.

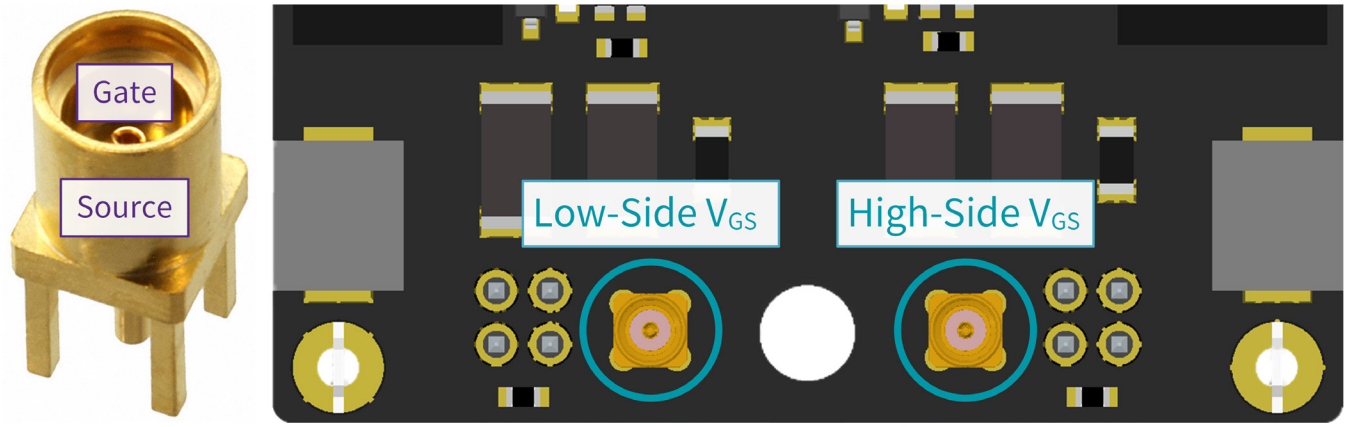

Figure 10: JT2 and JT3 measurement connectors orientations and pin locations

3.6 Status Indicators

The CGD1700HB2M-UNA gate driver includes four LEDs, shown in Figure 11, to indicate the state of the board. The functionality of these LEDs is summarized in Table 8. In normal operation, the green READY LEDs (*DT3* and *DT4*) will be illuminated, indicating that the gate driver board is functioning as expected. When the system faults due to an overcurrent event, the channel(s) where the fault occurred will illuminate the corresponding red FAULT LED (*DT1* and/or *DT2*). When the gate driver has an UVLO event, the READY LED of the relevant channel(s) will be extinguished. The status of the gate driver board depending on the LED states is summarized in Table 9.

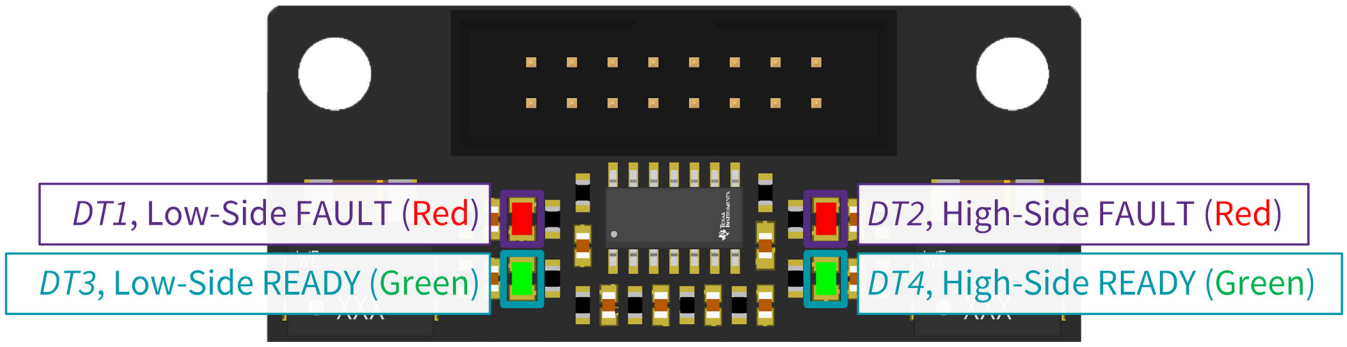

Figure 11: Status LEDs: locations and purposes

Table 8: Status LED descriptions

LED	Color	Description
DT1	Red	Low-Side FAULT
DT2	Red	High-Side FAULT
DT3	Green	Low-Side READY
DT4	Green	High-Side READY

Table 9: Status LED states

READY LED (*DT3* | *DT4*)	FAULT LED (*DT1* | *DT2*)	Description
1	0	Normal operation. No issues.
0	X	Bad power rail(s). Check input power quality, fuses, component failure, and output short-circuit.
X	1	Overcurrent fault. Clear fault condition and reset gate driver.

1 = LED On | 0 = LED Off | X = Irrelevant

4. Features

The CGD1700HB2M-UNA gate driver includes several design features intended to enable it to efficiently and reliably drive high-performance SiC MOSFETs at high frequencies. These features – which enable higher efficiency, noise immunity, flexibility, and protection – are detailed in this section.

4.1 Independent Gate Resistors

The design includes separate external turn-on ($R_{G(EXT),ON}$) and turn-off ($R_{G(EXT),OFF}$) gate resistors for both channels of the gate driver. The different resistors allow for independent tuning of the turn-on and turn-off switching dynamics. This can be useful for optimizing switching losses while staying within the safe operating bounds. By default, the CGD1700HB2M-UNA gate driver includes 1 Ω gate resistors for turn-off and turn-on for both channels, though the resistors can be easily changed to adjust the switching dynamics. The default resistors used are Vishay Dale CRCW25121R00FKEGHP resistors in a surface-mount 2512 (6432 metric) footprint. To maximize performance, it is recommended to use pulse-rated resistors when replacing/changing the gate resistors. The locations of the gate resistors are shown in Figure 12, and the purpose of each resistor is summarized in Table 10. See **PRD-09301** for more information about independent gate resistor tuning.

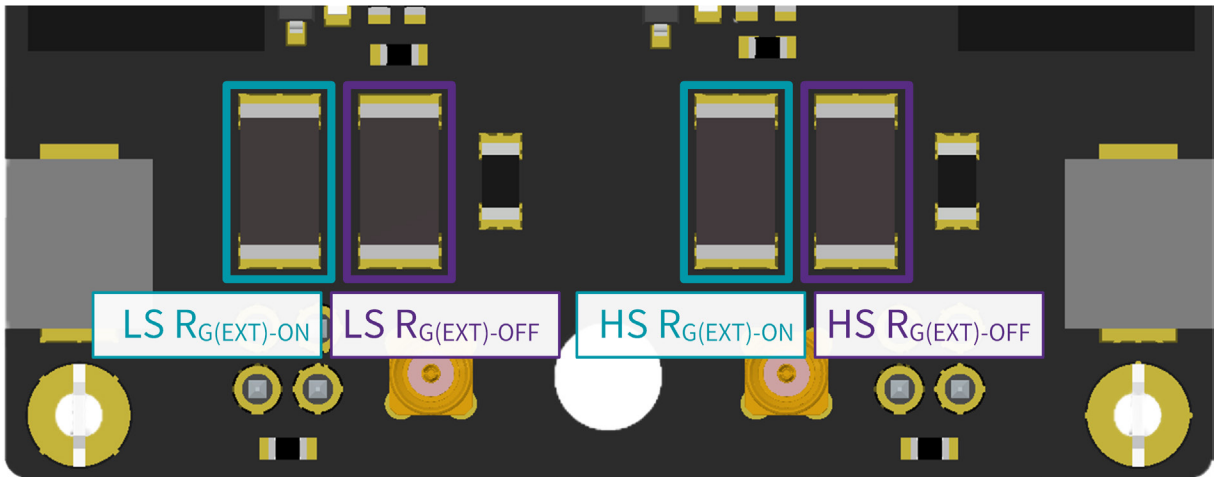

Figure 12: External turn-on and turn-off gate resistor locations

Table 10: External gate resistors descriptions

Ref. Des.	Default	Description
RT27	1 Ω	Low-Side External Turn-On Resistor
RT28	1 Ω	Low-Side External Turn-Off Resistor
RT30	1 Ω	High-Side External Turn-On Resistor
RT31	1 Ω	High-Side External Turn-Off Resistor

4.2 Differential Signaling

Signal integrity is critical when controlling power devices with a gate driver. A gate driver that is susceptible to the powerful interference generated by power devices can induce a shoot-through condition in the module. The extremely fast turn-on and turn-off times during the switching events in a SiC power system can create electromagnetic interference (EMI) that can easily couple onto the gate control signals. For this reason, differential signaling was adopted instead of standard, single-ended connections between the gate driver and control board. More information about differential signaling compared to single-ended connections is provided in **PRD-09301**.

Differential signaling significantly reduces the impact of radiated noise from the switching events of a power module. A single-ended signal can be converted to a differential signal by transmitting both the original signal and its complement in two closely coupled wires. At the receiver, the two signals are compared in order to reconstruct the original signal. Figure 13 illustrates this principle with an example of induced noise forced onto the cable somewhere between the transmitter and receiver. The noise affects both the original signal and the complement by the same magnitude assuming that the cables are consistently coupled. Thus, when the receiver compares the two signals, the difference is unaffected by the noise induced on the line and the intended original signal is created.

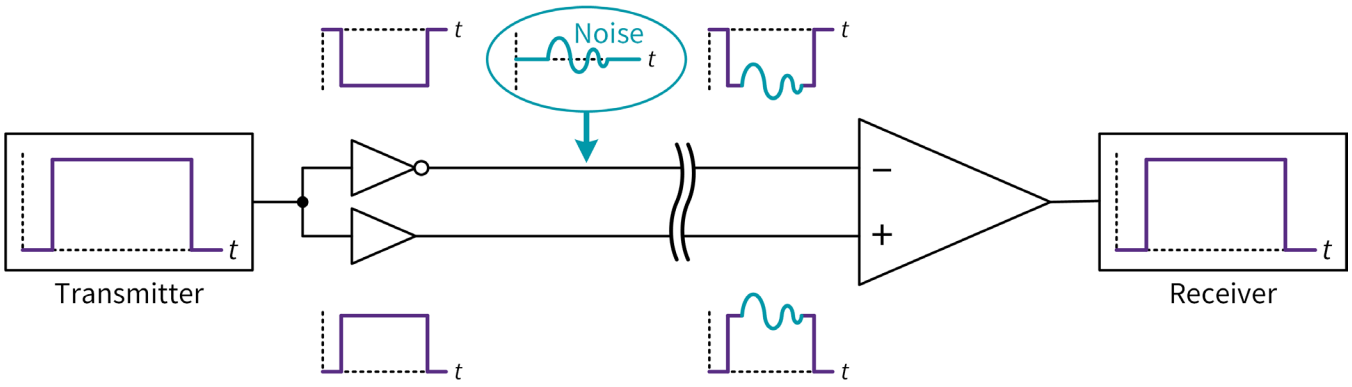

Figure 13: Noise immunity improvement provided by differential signaling

The CGD1700HB2M-UNA gate driver requires differential communication for proper performance. This can be achieved through differential transceivers included directly on a control board or using a single-ended to differential transceiver board. Wolfspeed provides the CGD12HB00D 2-channel differential transceiver companion tool for adding differential signaling to projects. For a reference design which adds differential transceivers directly to the control board, see the control board design from the CRD300DA12E-XM3 inverter. The differential circuit implemented on the CGD1700HB2M-UNA gate driver board is shown in Figure 14.

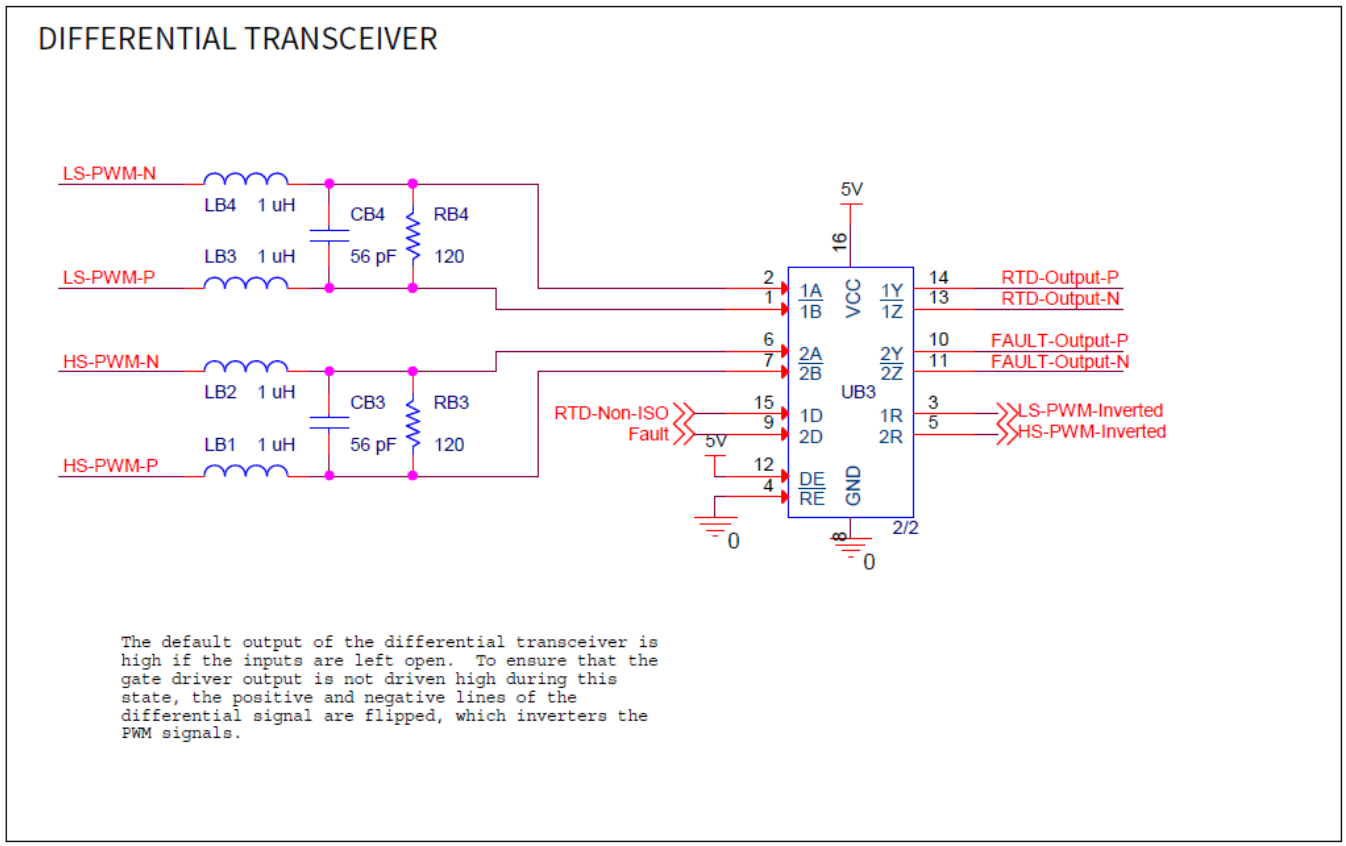

Figure 14: Differential signaling circuit

4.3 Adjustable Output Voltages

As discussed in Section 1, there are multiple configurations of the CGD1700HB2M-UNA which have different output voltages. All the CGD1700HB2M-UNA variants use the same PCB design, with components populated differently. The basic power regulation circuitry is shown in Figure 15.

4.3.1 Isolated DC/DC Converter

All the variants use an isolated DC/DC converter to serve as the isolation barrier and to generate unregulated voltage rails. The isolated DC/DC converter used in each variant along with the corresponding output voltages are summarized in Table 11. The exact implementation of the isolated DC/DC converter on the CGD1700HB2M-UNA designs is shown in Figure 16.

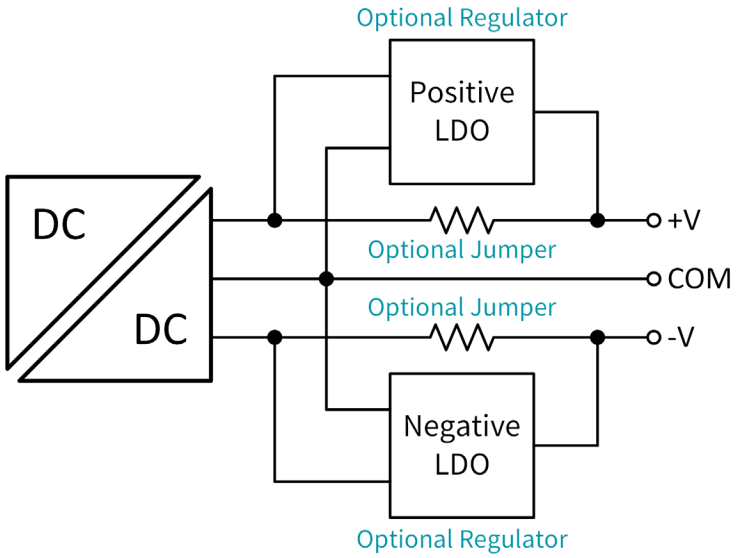

Figure 15: Power regulation circuitry used in all CGD1700HB2M-UNA variants

Table 11: Isolated DC/DC converters used for each CGD1700HB2M-UNA variation

Part Number	Isolated DC/DC Converter	DC/DC Converter Voltages
CGD1700HB2M-UNA (Unregulated +15 V / -3 V)	RECOM® R12P21503D	+15 V / -3 V
CGD1700HB2M-UNA-R1 (Regulated +15 V / -4 V)	Murata® MGJ2D122005SC[1]	+20 V / -5 V*
CGD1700HB2M-UNA-R2 (Regulated +18 V / -4 V)	Murata® MGJ2D122005SC	+20 V / -5 V*

* Not the final output voltages of the gate driver; the design includes further voltage conditioning

[1] Note that the schematic identifies Murata MGJ2D12**15**05SC for +15 V / -4 V operation. This approach will provide an unregulated +15 V rail and a regulated -4 V regulated rail. Using the Murata MGJ2D12**20**05SC – as discussed in this document – will achieve regulation for both the +15 V and -4 V rails.

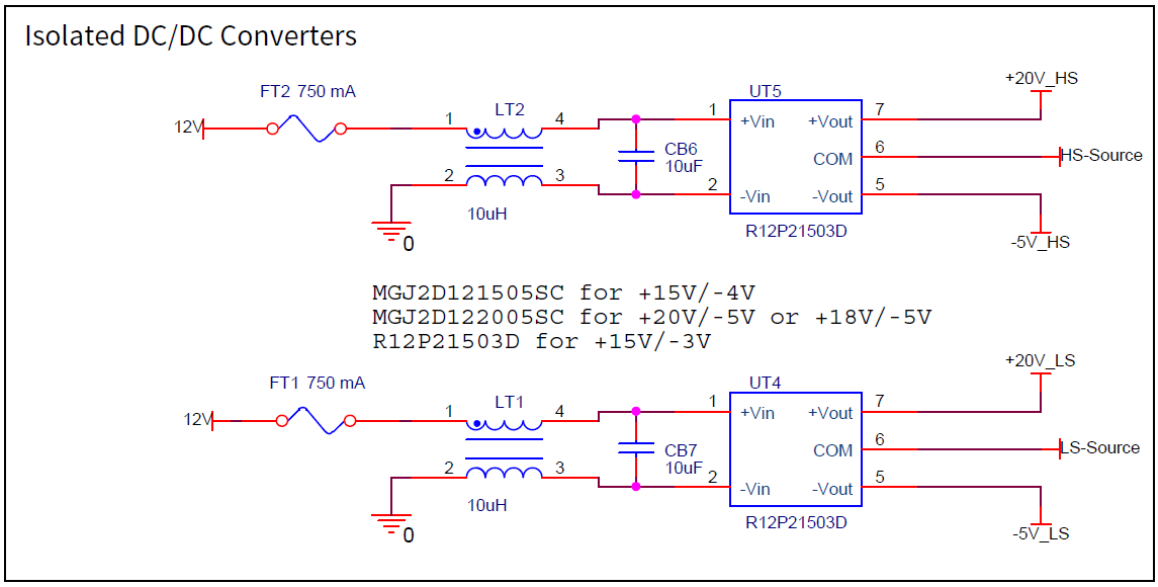

Figure 16: Isolated power supply circuits

4.3.2 Linear Regulators

For the default variant, CGD1700HB2M-UNA, the optional jumpers – shown notionally in Figure 15 – are populated and the low dropout (LDO) linear regulators are not populated, so the isolated DC/DC converter generates the final gate driver output voltages. As discussed previously, this solution is attractive for many applications since it does not require using additional power regulation components, and the generated voltage rail regulation is suitable for most end-applications. However, in some cases, such as MOSFET characterization measurements, an improved voltage rail regulation is required. For these applications, Wolfspeed offers the CGD1700HB2M-UNA-R**x** gate driver variants with high-precision LDOs on the output of the isolated DC/DC converters. These outputs provide improved regulation where precision voltage measurements are critical. These CGD1700HB2M-UNA-R**x** variations also enable modifying the output rails to voltages which are not standard in the isolated DC/DC converter footprint.

For the variants, CGD1700HB2M-UNA-R**x**, the optional jumpers shown notionally in Figure 15 are not populated, and the positive and negative linear regulators are both populated. The circuit implementations of the positive regulators are shown in Figure 17 with the populated components for each variation type shown in Table 12. Similarly, the circuit implementations of the negative regulators are shown in Figure 18 with the populated components for each variation type shown in Table 13. These component values can be modified to create different regulated output voltages as will be discussed in Section 4.3.4.

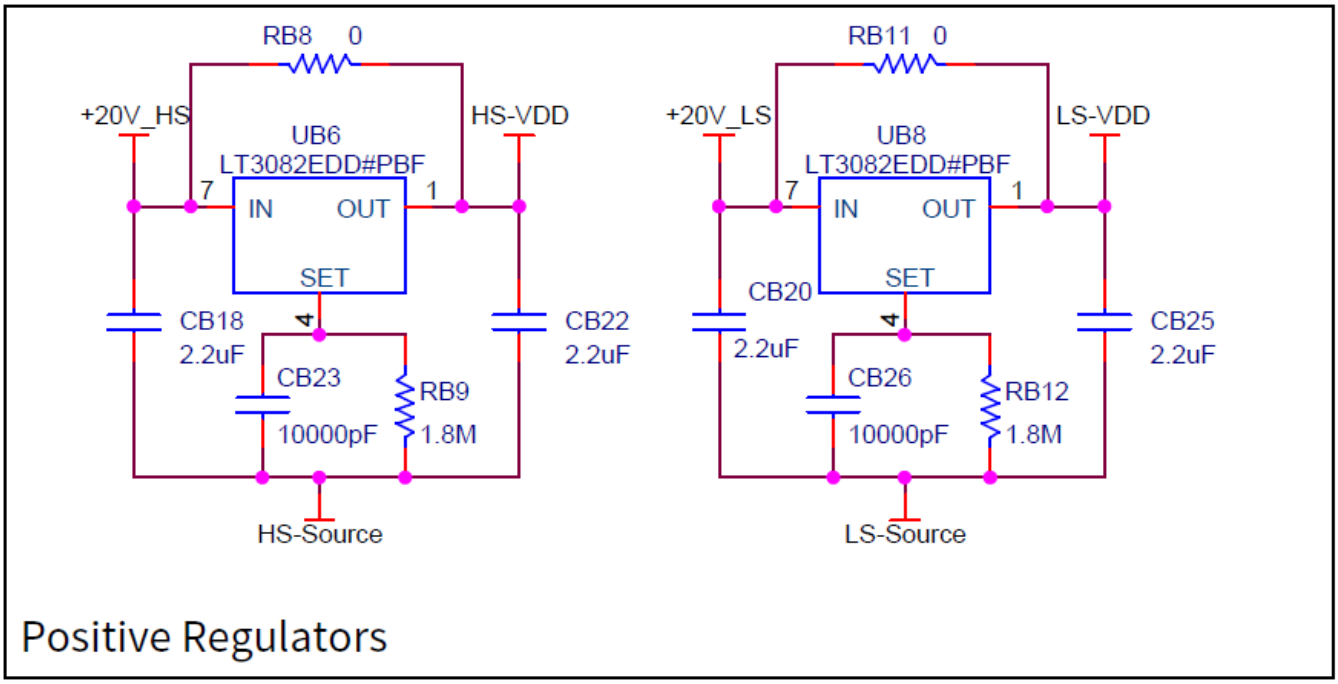

Figure 17: Optional positive linear regulator circuits to generate regulated turn-on voltage

Table 12: Positive linear regulator configuration for each gate driver variant

Part Number	UB6 UB8	RB8 RB11	RB9 RB12	CB18 CB20	CB23 CB26	CB22 CB25
CGD1700HB2M-UNA (Unregulated +15 V / -3 V)	DNP	**0 Ω**	DNP	DNP	DNP	DNP
CGD1700HB2M-UNA-R1 (Regulated +15 V / -4 V)	Analog Devices® LT3082EDD#PBF	DNP	**1.5 MΩ**	2.2 µF	10 nF	2.2 µF
CGD1700HB2M-UNA-R2 (Regulated +18 V / -4 V)	Analog Devices® LT3082EDD#PBF	DNP	**1.8 MΩ**	2.2 µF	10 nF	2.2 µF

* DNP : Do Not Populate

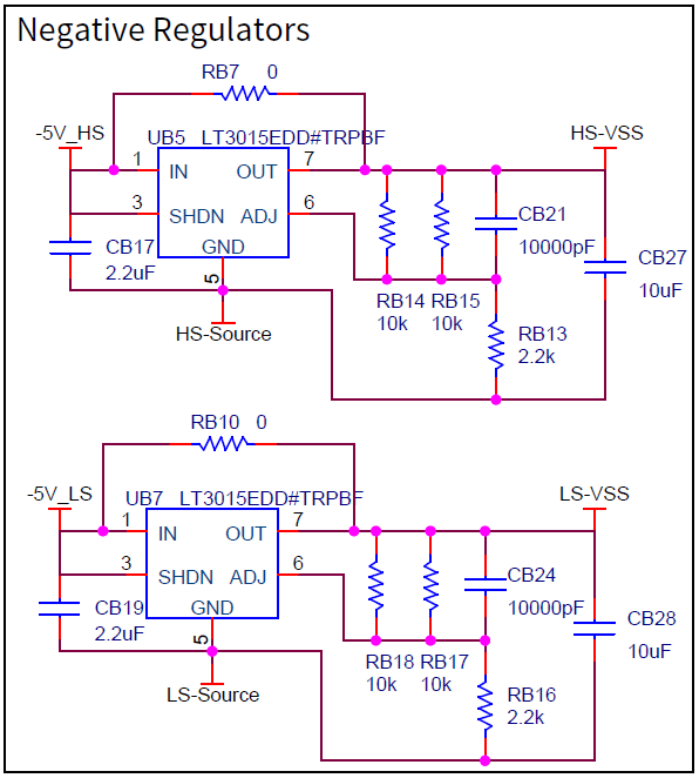

Figure 18: Optional negative linear regulator circuits to generate regulated turn-off voltage

Table 13: Negative linear regulator configuration for each gate driver variant

Part Number	UB5 UB7	RB7 RB10	RB14 RB18	RB15 RB17	RB13 RB16	CB17 CB19	CB21 CB24	CB27 CB28
CGD1700HB2M-UNA (Unregulated +15 V / -3 V)	DNP	**0 Ω**	DNP	DNP	DNP	DNP	DNP	DNP
CGD1700HB2M-UNA-R1 (Regulated +15 V / -4 V)	Analog Devices® LT3015EDD#TRPBF	DNP	54.9 kΩ	54.9 kΩ	12.1 kΩ	2.2 µF	10 nF	2.2 µF
CGD1700HB2M-UNA-R2 (Regulated +18 V / -4 V)	Analog Devices® LT3015EDD#TRPBF	DNP	54.9 kΩ	54.9 kΩ	12.1 kΩ	2.2 µF	10 nF	2.2 µF

* DNP : Do Not Populate

4.3.3 Add Regulation CGD1700HB2M-UNA

Since the default gate driver variation, CGD1700HB2M-UNA, uses the same PCB design as all the model variations, the CGD1700HB2M-UNA can be easily modified to add voltage regulation. Some cases where this could be useful include changing the output voltage to evaluate SiC MOSFET performance in other operating conditions or re-purposing the gate driver for a new application. To add regulation to the default CGD1700HB2M-UNA driver, simply adjust the components listed in Table 11, Table 12, and Table 15 to the values of the intended operation. The exact components used for the different variations are included in the bill of materials (BOM) provided on the CGD1700HB2M-UNA website landing page. To change the output voltage to a non-standard output voltage, follow the steps discussed in Section 4.3.4.

4.3.4 Change Output Regulation Voltages

Once regulation is added to the design (see Section 4.3.3 if starting with the baseline CGD1700HB2M-UNA gate driver), the regulated output voltages can be easily modified to other regulated voltages. Note that the range of the linear regulators is limited by the isolated DC/DC converter outputs. The maximum magnitude of linear regulator output voltages must be 0.3 less than the corresponding DC/DC output voltage. The maximum output range of the linear regulators is therefore (V_{DCDC-} + 0.3 V) to (V_{DCDC+} - 0.3 V).

To change the turn-on voltage, change the feedback resistors, R_{FB+},(*RB9* and *RB12*), on the positive linear regulators (*UB6* and *UB8*). The positive linear regulators generate a 10 µA reference current out of the *SET* pin, so the output voltage of the regulators will be set equal to the following equation. Resistor values for common positive output voltages are summarized in Table 14. See the Analog Devices LT3082EDD#PBF datasheet for more information. Resistors with tolerances less than or equal to 1% should be used for the best performance.

$$V_{GATE,HIGH} = R_{FB+} \cdot 10\mu A$$

Table 14: Positive linear regulator feedback resistors for common output voltages

V+	R_{FB+} (*RB9* and *RB12*)
+15 V	1.5 MΩ
+18 V	1.8 MΩ

To change the turn-off voltage, change the feedback resistor network on the negative linear regulator to adjust the voltage using the equation below. The output voltage of the linear regulator can be adjusted between -1.22 V and (V_{DCDC-} + 0.3 V). See the Analog Devices LT3015EDD#TRPBF datasheet for more information. Resistors with tolerances less than or equal to 1% should be used for the best performance.

$$V_{GATE,LOW} = -1.22\ V\left(1 + \frac{R_2}{R_1}\right) + \left(I_{ADJ}\right)(R_2)$$

where

R_1: bias resistor attached to the common rail [Ω]
R_2: bias resistor attached the output voltage rail [Ω]
I_{ADJ}: bias current (30 nA at 25 °C, see component datasheet for more information) [A]

The calculation for the default circuit configuration of -4 V is shown below for reference.

$$-1.22\ V\left(1 + \frac{(54.9\ k\Omega\ ||\ 54.9\ \text{k}\Omega)}{12.1\ k\Omega}\right) + (30\ nA)(54.9\ k\Omega\ ||\ 54.9\ \text{k}\Omega) = -4\ V$$

The SiC power MOSFETs are not intended to be operated continuously in the linear region, so the user should ensure that the selected voltages are within the safe operating area of the device. Although it is possible to change the output voltage to non-standard voltages, this is not recommended for most applications. This guide is intended to be informative for users testing systems in edge conditions or for evaluating how the system handles faulty conditions. Also, the overcurrent protection circuit blanking time is biased from the output-high

voltage rail (see Section 4.4.4), so modifying this voltage can influence the trip timing of the overcurrent protection circuit.

4.3.5 Unipolar Operation

The CGD1700HB2M-UNA gate driver can support unregulated unipolar operation (i.e. 0 V turn-off voltage). This is not a configuration option currently offered by Wolfspeed, though the modifications can be performed by an end user. To support +15 V / 0 V, use the RECOM R12P215S isolated DC/DC without the output regulators populated (i.e. follow the same configuration as the baseline CGD1700HB2M-UNA variant simply with a different isolated DC/DC converter). In addition, remove *CB8*, *CB9*, *CB12*, and *CB13*, and replace them with jumpers to connect the turn-off rail to the source rail, as shown in Figure 19. This creates an unregulated +15 V high V_{GS} and 0 V low V_{GS}. **The capacitors should not be shorted when operating the gate driver in bipolar mode** (i.e. with a negative turn-off gate voltage).

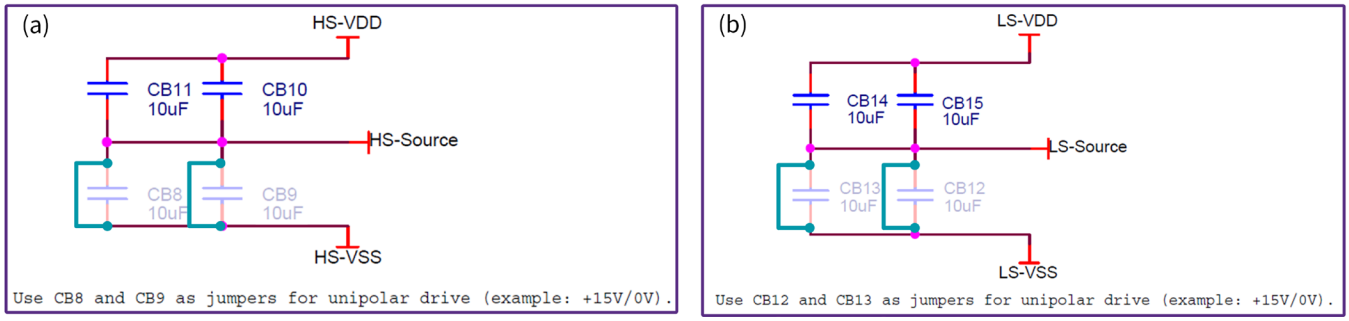

Figure 19: Capacitor removal and jumpers to support unipolar operation: (a) high-side and (b) low-side

4.4 Faults / Protections

The CGD1700HB2M-UNA gate driver is protected from input +12 V power quality issues, isolated power supply issues, signal overlap, and overcurrent events. This section discusses these faults in more detail and how to adjust them. Table 15 provides a logic table summary indicating the state of the gate driver outputs depending on the various input signals and/or fault statuses. The UVLO and overcurrent faults of each channel are combined into a single global fault signal that is transmitted to the controller, as shown in Figure 20.

Table 15: Output logic table depending on inputs and faults

PWM	$\overline{\text{RESET}}$/EN	Overcurrent/ UVLO	FAULT	Output
H	H	No	H	H
L	H	No	H	L
X	L	No	H	L
X	X	No	L	L
X	X	Yes	L	L

H = High | L = Low | X = Irrelevant

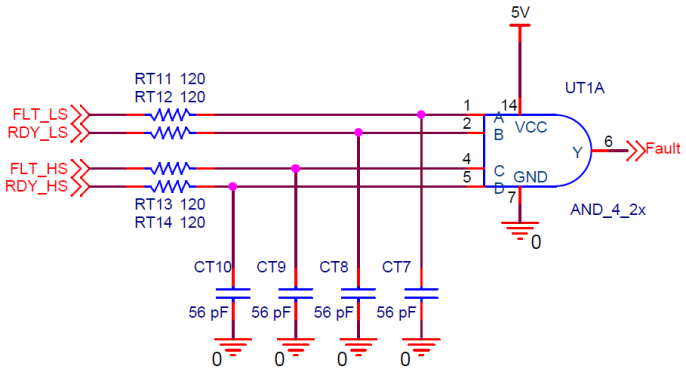

Figure 20: Fault combination into single global fault signal

4.4.1 Input Voltage Protection

The CGD1700HB2M-UNA gate driver includes overvoltage and reverse voltage protection on the +12 V power input (pin 1) of the input connector, *JT1*. The implemented overvoltage and reverse voltage protection circuit is shown in Figure 21. The Zener diode protects from input voltage spikes greater than 20 V (nominal) and the P-channel MOSFET protects from the positive and negative voltage polarities being reversed. Incorrect connections should be avoided when using the CGD1700HB2M-UNA gate driver, though these circuit elements are included to protect the system if it is incorrectly wired.

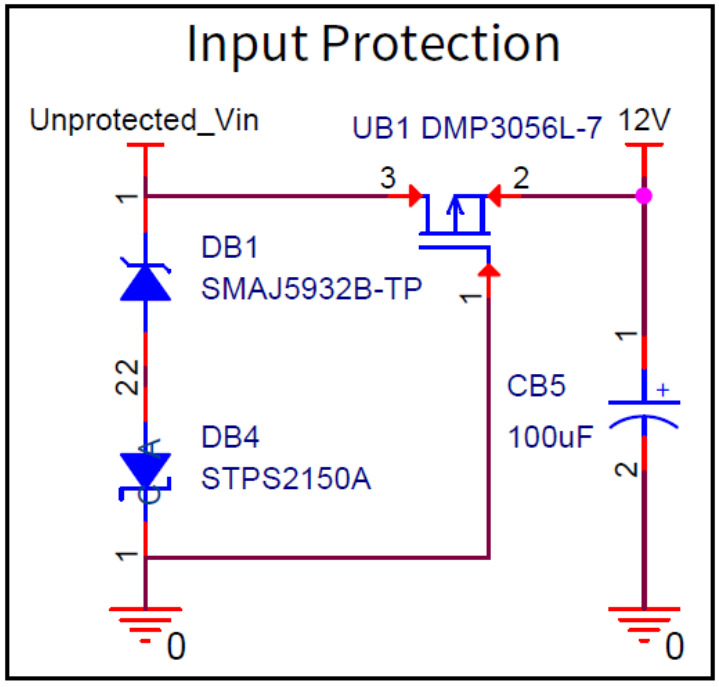

Figure 21: Input overvoltage and reverse voltage protection circuit

4.4.2 Undervoltage Lockout

The Texas Instruments UCC21710 gate driver IC used on this design features integrated UVLO. The UVLO circuit detects when the output rails of the isolated DC/DC converter fall below safe operating conditions for the gate driver or when the gate driver input voltage is too low. An output UVLO fault indicates that the voltage potential between the split output voltage rails has fallen below the UVLO active level. The gate for the channel where the fault occurred will be pulled low through $R_{G(EXT)-OFF}$ for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. There is hysteresis for this fault to ensure safe operating conditions. When there is no UVLO fault present, a green LED indicates a power good state. The LED, *DT4*, indicates a high-side power good status, and *DT3* indicates a low-side power good status.

4.4.3 Overcurrent Fault

An overcurrent (OC) fault is an indication of an overcurrent event in the SiC power module. The overcurrent protection circuit, shown in Figure 22 for the low-side and in Figure 23 for the high-side, measures the drain-to-source voltage (V_{DS}), and the fault will indicate if this voltage has risen above an acceptable current level. When a fault has occurred, the corresponding gate driver channel will be disabled, and the gate will be pulled down through a soft turnoff circuit. The equivalent drain-to-source voltage for a particular overcurrent limit can be configured through onboard resistors. The overcurrent fault is latched upon detection and must be cleared by the user/controller with a low pulse of at least 1000 ns on the $\overline{RESET}/EN$ signal of the gate driver. The various timing and voltage trip levels presented in Table 3 and Section 4.4.4 are defined notionally in the timing diagram shown in Figure 24.

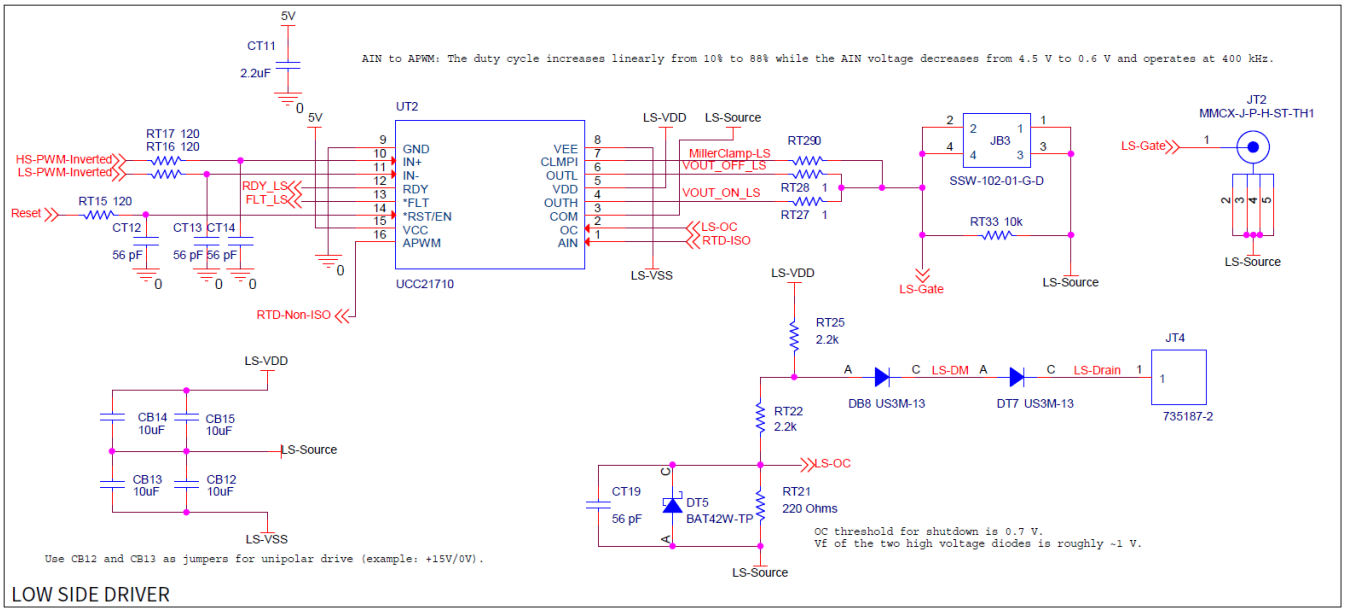

Figure 22: Low-side gate driver circuit with overcurrent protection

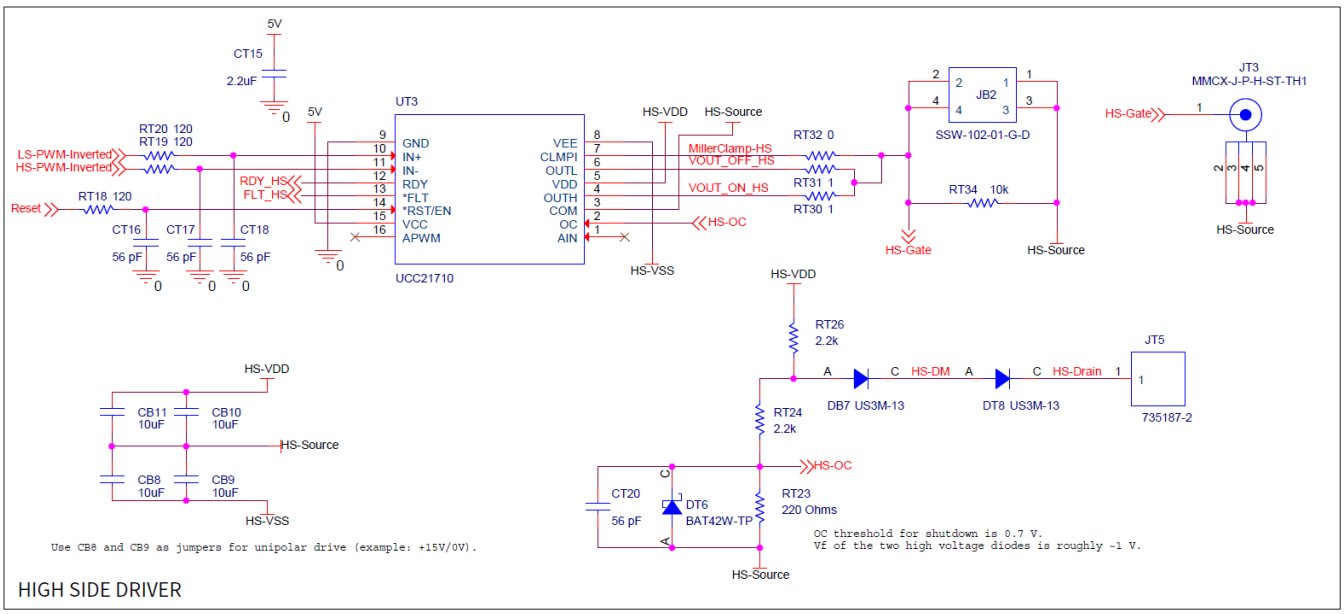

Figure 23: High-side gate driver circuit with overcurrent protection

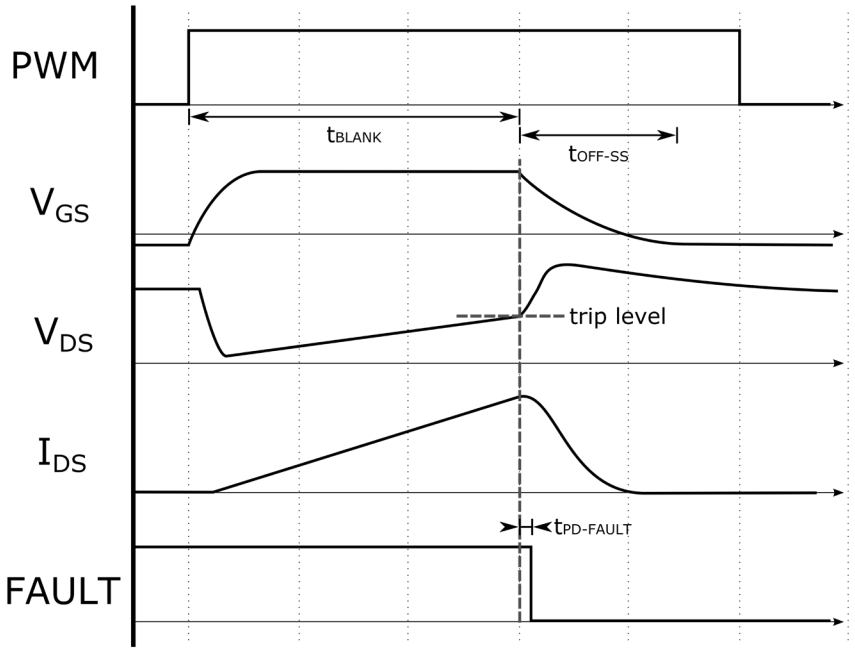

Figure 24: Overcurrent fault timing diagram

4.4.4 Overcurrent Trip Level

The OC fault detection circuit – shown in Figure 22 and Figure 23 for the low-side and high-side positions, respectively – monitors the on-state V_{DS} across each switch position and triggers a fault condition if the voltage rises above the predefined set level for a predefined amount of time (blanking time) while the device is on. The circuit is simplified into the notional diagram shown in Figure 25. Referring to this figure, the corresponding overcurrent trip voltage, $V_{OC-Trip}$ and blanking time, $t_{BLK,EXT}$, can be calculated using the following equations:

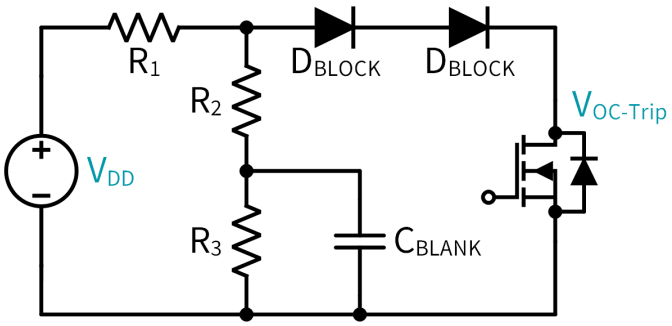

Figure 25: Notional overcurrent fault circuit

$$V_{OC-Trip} = V_{OC-Thres} \cdot \frac{R_2 + R_3}{R_3} - N_D \cdot V_F$$

$$t_{BLK,EXT} = -\frac{R_1 + R_2}{R_1 + R_2 + R_3} \cdot R_3 \cdot C_{BLANK} \cdot \ln\left(1 - \frac{R_1 + R_2 + R_3}{R_3} \cdot \frac{V_{OC-Thres}}{V_{DD}}\right)$$

where

$V_{OC-Trip}$: target overcurrent trip voltage [V]
$V_{OC-Thres}$: internal comparator trip voltage of the gate driver IC [V]
R_1, R_2, R_3: circuit resistor values [Ω]
N_D: number of series high-voltage blocking diodes
V_F: forward voltage of the high-voltage blocking diode(s) [V]
C_{BLANK}: blanking capacitor used to prevent false triggers during switching events [F]
V_{DD}: high output gate-to-source voltage [V]

The calculated blanking time only accounts for the delay due to the external components (using nominal values). The UCC21710 also includes a nominal 120 ns deglitch filter on the overcurrent measurement that adds additional blanking time to the calculated value. The calculated value can be used as a starting point but the precise value should be measured on the hardware. The example calculations are performed below for the default gate driver circuit parameters. Note that the CGD1700HB2M-UNA gate driver is intended to drive a variety of semiconductor devices ranging from single-die discrete devices to multi-die power modules. Because of this, the default overcurrent trip value may not be optimal for all applications. Similarly, operators may want to adjust how aggressively or conservatively the overcurrent protection trips. For these reasons, it is important to perform these calculations for the end application to determine if any of the parameter values need to be changed. See **PRD-09301** for more information about selecting overcurrent trip values.

$V_{OC-Thres}$: 0.7 V (from Texas Instruments UCC21710 datasheet)
R_1: 2.2 kΩ; R_2: 2.2 kΩ; R_3: 220 Ω (from gate driver schematic)
N_D: 2 (from gate driver schematic)
V_F: 0.5 V (from high-voltage diode datasheet)
C_{BLANK}: 56 pF (from gate driver schematic)
V_{DD}: 15 V (from gate driver schematic)

$$V_{OC-Trip} = 0.7\ V \cdot \frac{2200\ \Omega + 220\ \Omega}{220\ \Omega} - 2 \cdot 0.5\ V \rightarrow \boldsymbol{V_{OC-Trip} = \ 6.7\ V}$$

$$t_{BLK,EXT} = -\frac{2200\ \Omega + 2200\ \Omega}{2200\ \Omega + 2200\ \Omega + 220\ \Omega} \cdot 220\ \Omega \cdot (56 \times 10^{-12}\ F) \cdot \ln\left(1 - \frac{2200\ \Omega + 2200\ \Omega + 220\ \Omega}{220\ \Omega} \cdot \frac{0.7\ V}{15\ V}\right)$$

$$\boldsymbol{t_{BLK,EXT} = 46\ ns}$$

By default, CGD1700HB2M-UNA gate driver is configured with a 6.7 V overcurrent trip voltage and 46 ns blanking time. To determine the approximate corresponding trip current value, refer to the I_{DS} vs V_{DS} output characteristic curves of the applicable device. For example, Wolfspeed's C3M0032120J1 output characteristics show that a V_{DS} of 6.7 V occurs at approximately 103 A at V_{GS} = 15 V and T_J = 150 °C. To adjust the overcurrent trip voltage, it is recommended to change the value of R_3. To adjust the blanking time, it is recommended to change the value of C_{BLANK}. As discussed in Section 3.4, **the overcurrent connector, *JT4* and *JT5*, cannot be left floating as the overcurrent fault will trip immediately when the gate is actuated**. If bench-top testing of the gate driver is required, it is acceptable to short this connector to the appropriate source connection to prevent the overcurrent fault from tripping. **Performing this modification will disable the overcurrent protection.**

4.4.5 Miller Clamp

When a switch position is in the off state, high *dV/dt* in other switch positions can cause current flow through the Miller capacitance of a MOSFET and ultimately induce noise into the gate. To prevent false turn-on of the device, it is important that the gate driver has a low-impedance to the turn-off voltage when the device is off to ensure the gate of the MOSFET is held low. The Texas Instruments UCC21710 gate driver IC employed on this design features an integrated Miller clamp circuit. When the gate voltage drops below a 2 V internal reference, the Miller clamp latch is engaged, which is a low-impedance connection to the output-low voltage rail. In this configuration, the external turn-off resistor still controls the turn-off dynamics, and the gate driver has a low-impedance connection to dissipate Miller charge even when a high-valued turn-off resistor is employed.

4.4.6 Interlock Protection

In a half-bridge circuit, commanding both channels on simultaneously short-circuits the bus and can cause extreme currents. While the overcurrent protection circuit discussed in 4.4.3 can prevent catastrophic damage, the Texas Instruments UCC21710 gate driver IC used in this design also includes circuitry that prevents both channels from being commanded on simultaneously. This interlock protection, also commonly referred to as shoot-through or anti-overlap protection, applies XOR logic to the two input control signals, preventing either output from going high if both signals are commanded on simultaneously, as shown in Table 16. This can help with noise rejection if noise causes one of the commanded signals to flip, and it can help prevent issues from a faulty controller. Notably, this protection should not be relied upon for generating dead time.

Table 16: Interlock protection logic table

HS PWM	LS PWM	$V_{GS,HS}$	$V_{GS,LS}$
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

H = High | L = Low

4.5 Soft Shutdown

When an overcurrent fault occurs, hard turn-off of the device (i.e. turning the device off normally) can induce large voltage overshoots due to the enormous *di/dt* event. To prevent the device voltage from exceeding safe operating area, the Texas Instruments UCC21710 includes an integrated soft shutdown feature. When the overcurrent fault is detected, a dedicated 400 mA soft turn-off circuit is used to turn the device off in a controlled manner which limits voltage spikes from large *di/dt* events. The soft-turnoff feature is directly integrated into the UCC21710 IC, so no additional connections are required. More information about the soft turn-off functionality can be found in the gate driver IC datasheet.

4.6 Timing Definitions

Table 3 provides various timing parameters to indicate the propagation delays of the gate driver. These timing parameters are shown visually in Figure 26 for the gate signals.

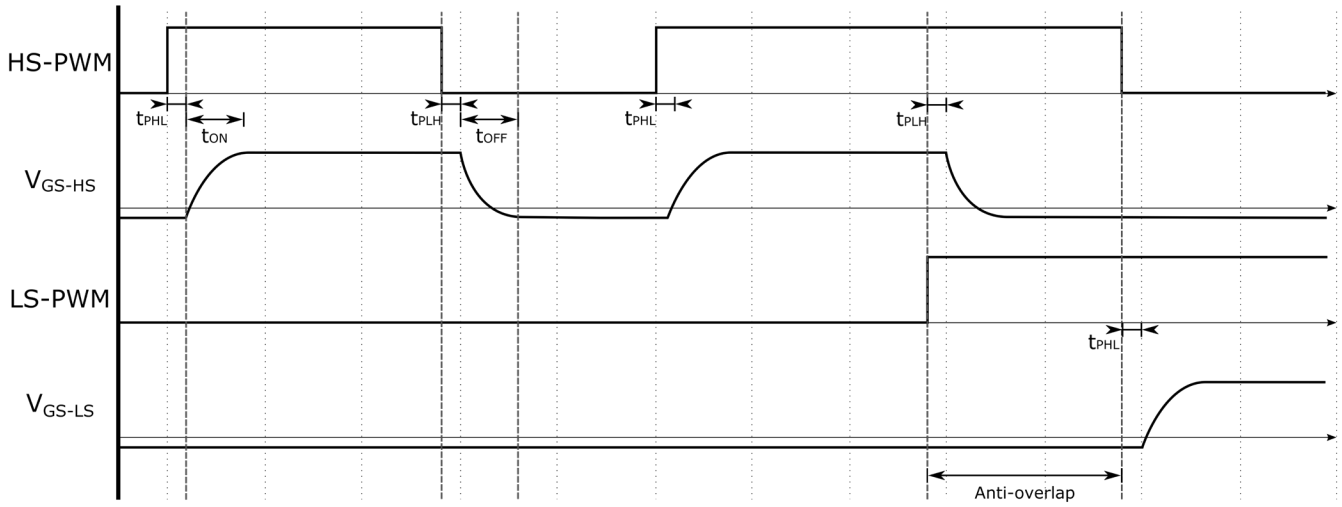

Figure 26: Gate timing diagram

4.7 Thermistor Feedback

The CGD1700HB2M-UNA gate driver includes a connector (*JB1*) for measuring an external thermistor. The gate driver converts the thermistor resistance to a voltage and transmits it as a PWM signal with a varying duty cycle ranging from 10% to 88% at 400 kHz. The measurement is transmitted to the controller as a differential pair on pins 9 and 10 on the input connector, *JT1* (see Section 3.1). The resistance to duty cycle conversion is performed within the Texas Instruments UCC21710 gate driver IC, so it includes the same isolation protection as the rest of the gate driver. This signal can therefore be transmitted to the controller in the same ribbon cable as the rest of the gate driver's signals. The bias circuit for the thermistor connection is shown in Figure 27. The circuit relies on a 200 µA current source from the UCC21710 IC to bias the resistance of the thermistor connection, *JB1*. The current mirror components, *UB4* and *RB6*, are not populated by default.

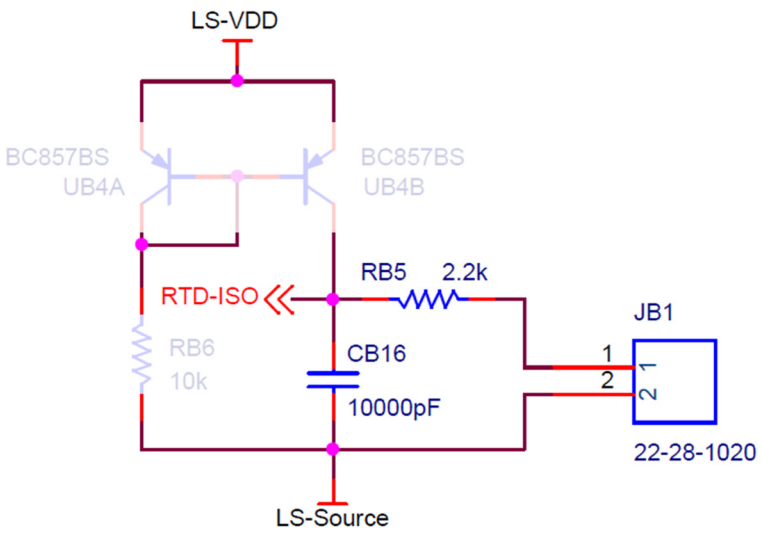

Figure 27: Thermistor resistance to duty cycle conversion circuit

The temperature to duty cycle relationship of the thermistor will be dependent on the thermistor attached to the circuit. For power modules with an integrated thermistor, the thermistor temperature vs resistance characteristics are included in the relevant datasheet. For the Wolfspeed SpeedVal™ platform, many of the daughtercards include a thermistor on the PCB, with the corresponding characterization data included in the associated user guide. To calibrate the temperature to duty cycle relationship, it is recommended to connect a potentiometer to *JB1* and vary the resistance to match various thermistor temperatures and develop an equation to capture the relationship. Figure 28 shows an example duty cycle to temperature relationship for the thermistor found in the Wolfspeed WolfPACK™ family of power modules.

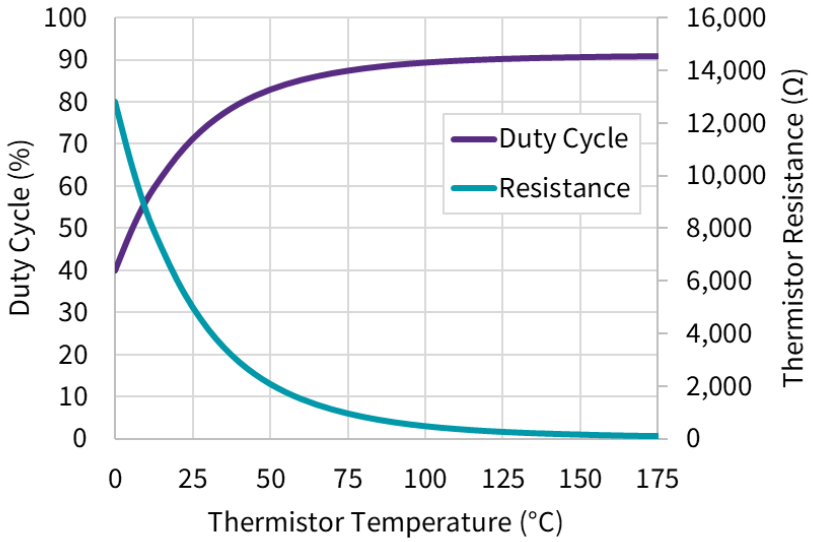

Figure 28: Example duty cycle relationship for Wolfspeed WolfPACK™ power module thermistors

The temperature reported by the thermistor often differs largely from the junction temperature of the SiC MOSFETs and should not be used as an accurate junction temperature measurement (see **PRD-08376**). The

duty cycle-encoded signal is transmitted at 400 kHz. On the controller side, the duty cycle-encoded signal can be interpreted by directly measuring the duty cycle using edge detection or the signal can be converted to an analog signal with a simple resistor-capacitor (RC) circuit. If using the analog approach, the RC circuit should have a long enough time constant to maintain a stable signal and then it can be measured simply with an analog-to-digital converter (ADC). If not used, the thermistor connector, *JB1*, can be left floating with no loss of functionality to other parts of the circuit. Though this circuit is intended to be used with a thermistor, it can alternatively be used to measure any resistive-based sensor. Note that if you are adopting this approach, the attached sensor will be referenced to the low-side switch position source terminal. Only sensors that can tolerate being attached to the isolated side of the gate driver should be measured.

4.8 Power Estimates

The gate driver power required to drive a switch position at a target switching frequency is calculated using the equation below. The gate charge is dependent on the datasheet of the MOSFET being driven. Once the required gate driver power is calculated, the necessary input power can be calculated from the efficiency curves on the datasheet of the applicable power supply. This calculation is for one channel of the gate driver.

$$P_{SW} = Q_G \cdot f_{SW} \cdot \Delta V_{PS}$$

where

P_{SW}: per channel gate driver power [W]
Q_G: total gate charge [C]
f_{SW}: switching frequency [Hz]
ΔV_{PS}: difference in isolated power supply voltage rails ($V_{PS,HIGH} - V_{PS,LOW}$) [V]

This calculation can be manipulated to determine the theoretical maximum switching frequency possible with a gate driver and MOSFET combination (with some margin). An example calculation for the CCB032M12FM3T power module and CGD1700HB2M-UNA gate driver is demonstrated below. Note that the calculated maximum switching frequency is not always achievable or practical in the target application depending on rise/fall times, deadtime, and parasitic inductance/capacitance. This calculation is often most critical in applications using high ampacity power modules or high switching frequencies. This value serves as the theoretical maximum based on the gate driver components. Additionally, all calculated values greater than 1 MHz will be bound to 1 MHz since this is the fastest possible switching frequency of the Texas Instruments UCC21710 gate driver IC employed on this board. Thermal performance of the UCC21710 gate driver IC must also be considered when pushing to elevated switching frequencies. At very high switching frequencies, refer to the UCC21710 datasheet for more information about estimating the temperature of the gate driver IC.

P_{SW}: 2 W (rated output power of the isolated power supplies on the gate driver)
Q_G: 118 nC (provided in CCB032M12FM3T datasheet)
$V_{PS,HIGH}$: 15 V (default positive output voltage of the CGD1700HB2M-UNA)
$V_{PS,LOW}$: -3 V (default negative output voltage of the CGD1700HB2M-UNA)
ΔV_{PS}: 18 V ($V_{PS,HIGH} - V_{PS,LOW}$)

$$f_{SW} \leq \frac{2\ W}{118\ nC \cdot 18\ V} \rightarrow f_{sw} \leq 940\ kHz$$

5. Dimensions

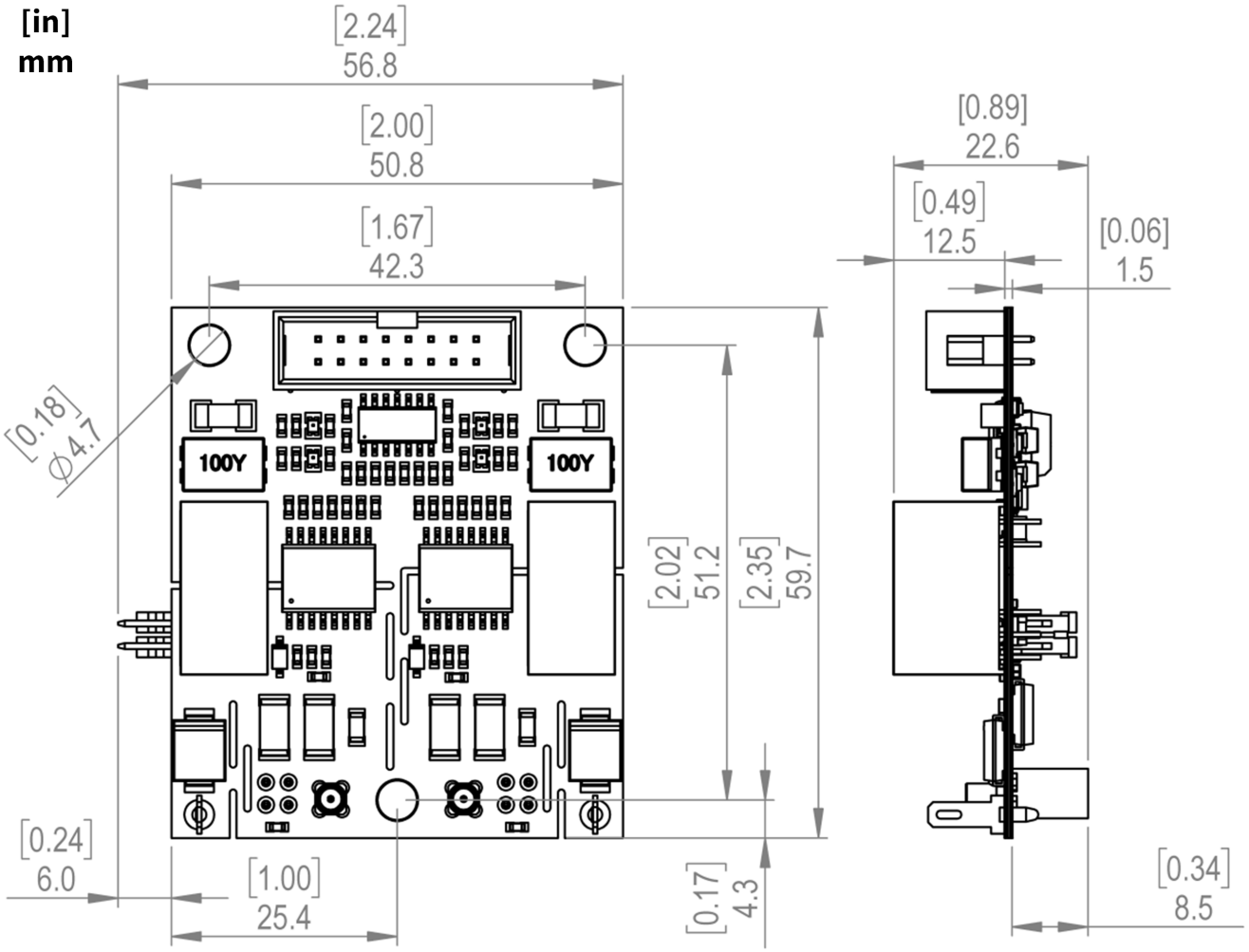

Figure 29: Dimensions of the CGD1700HB2M-UNA gate driver

6. Supporting Links and Tools

The following links provide additional information about gate drivers, SiC power MOSFETs (discrete and module solutions), and design tools for using the devices. Please navigate to the landing page for this design for additional links and support.

6.1 Evaluation Tools and Support

- Discrete MOSFETs
- FM Module Product Family
- GM Module Product Family
- KIT-CRD-CIL12N-FMA: Dynamic Characterization Evaluation Tool Optimized for the Wolfspeed WolfPACK™ Half Bridge Module Platform

- KIT-CRD-CIL12N-FMB: Dynamic Performance Evaluation Board for the Wolfspeed WolfPACK™ Full-Bridge Module Platform
- KIT-CRD-CIL12N-FMC: Dynamic Characterization Evaluation Tool Optimized for the Wolfspeed WolfPACK™ Six-Pack Platform
- KIT-CRD-CIL12N-GMA: Dynamic Characterization Evaluation Tool Optimized for the Wolfspeed WolfPACK™ GM3 Half Bridge Module Platform
- KIT-CRD-CIL23N-GMA: Dynamic Characterization Evaluation Tool Optimized for the Wolfspeed 2300 V WolfPACK™ GM Half Bridge Module Platform
- SpeedVal™: Modular Evaluation Platform
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- All Wolfspeed Gate Drivers

6.2 Dual Channel Gate Driver Board

- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

6.3 Application Notes

- PRD-09301: Gate Driver Design for SiC Power Modules
- PRD-04814: Design Options for Wolfspeed Silicon Carbide MOSFET Gate Bias Power Supplies

Revision History

Date	Revision	Changes
January 2021	0	Initial release.
September 2023	1	Reformatted document and updated images.
October 2025	2	Added -R1 and -R2 variants. Added more operating information.

IMPORTANT NOTES

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- compliance with applicable regulatory or safety compliance or certification standards that may normally be associated with other products, such as those established by EU Directive 2011/65/EU of the European Parliament and of the Council on 8 June 2011 about the Restriction of Use of Hazardous Substances (or the RoHS 2 Directive) and EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (or WEEE). The board is not a finished end product and therefore may not meet such standards. Users are also responsible for properly disposing of a board's components and materials.

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