

## High Performance Stereo Audio ADC

### Features

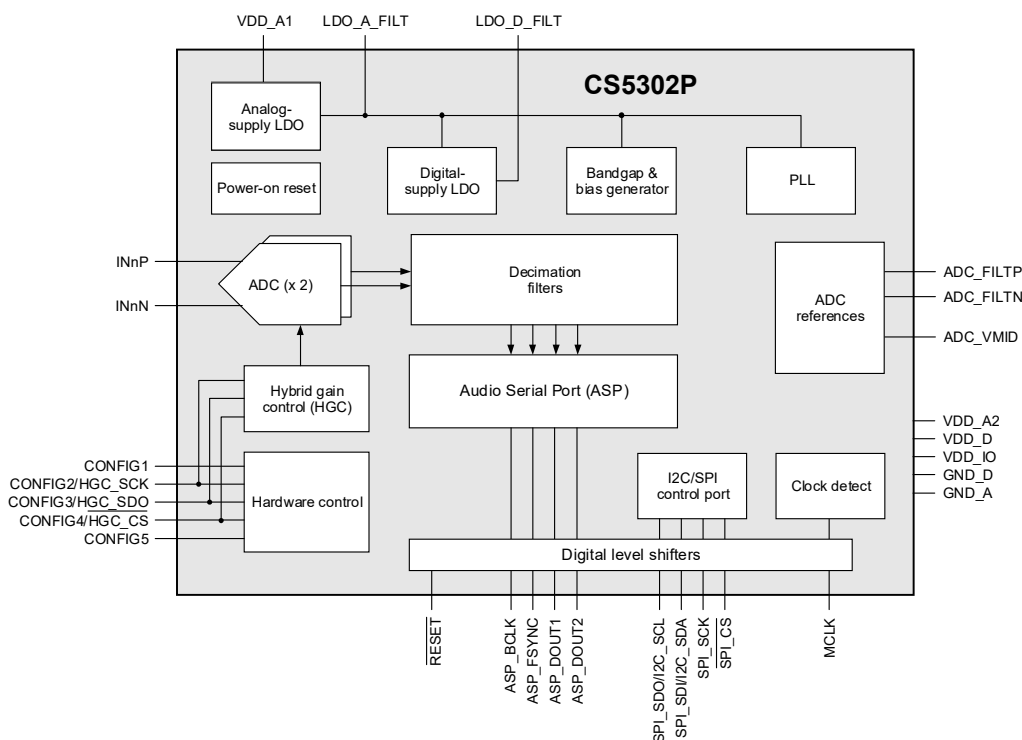
- High performance two-channel ADC
  - Differential analog architecture
  - High-resolution 32-bit digital architecture
  - Advanced multibit sigma-delta ADC
  - Low-latency digital filters and digital volume control
- PLL supports range of external system-clock references
- Sample timing alignment across multiple devices
- Synchronized control of external preamplifier gain
- Audio serial port (ASP) sample rates up to 768 kHz
  - I<sup>2</sup>S, left-justified, and TDM data formats
- Hardware and software control modes
  - I<sup>2</sup>C control port up to 1 MHz
  - SPI control port up to 24 MHz
  - Hardware control with no host processor required
- Single-supply operation at 3.3 V
  - Support for 1.8 V–3.3 V digital input/output
- 48-pin QFN package

### Specifications

- 126 dB dynamic range (A-weighted)
- –110 dB total harmonic distortion + noise (THD+N)
- 4.1/Fs group delay at 96 kHz sample rate (slow roll-off, minimum-phase filter)
- 2 V<sub>RMS</sub> differential analog input
- High-pass filter

### Applications

- A/V receivers
- Digital mixing consoles
- DAW interfaces
- Musical instruments



### Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

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## General Description

The CS5302P is a high-performance, 32-bit resolution, two-channel ADC. The CS5302P supports differential analog input, and 32-bit digital output via the audio serial port (ASP) at sample rates up to 768 kHz. The CS5302P uses a 5th-order, multibit sigma-delta modulator followed by digital filtering and decimation. The ADC uses a differential architecture, optimized for high performance combined with low power consumption.

The CS5302P can be configured using a control interface supporting I<sup>2</sup>C and SPI modes of operation. The device can also be operated in hardware mode, using external resistors to select the required configuration. Multiple hardware-control options are supported, including system clocking, ASP format, sample rate, and digital-filter selection.

The low-latency digital filters are optimized for the applicable sample rate. Fast or slow roll-off filters can be combined with minimum or linear phase responses to support the desired signal characteristics.

The CS5302P supports synchronized control of an external preamplifier associated with each ADC input path. Updates to the external and internal gain settings are fully synchronized, and a transient-masking function provides additional capability to ensure seamless operation across all signal levels.

The ASP supports multichannel operation in I<sup>2</sup>S, left-justified, and TDM data formats. Two data-output pins support 32-bit multichannel operation up to 768 kHz. Tristate control of the data-output pins allows multiple devices to operate on a shared bus.

Clocking for the CS5302P can be derived from the ASP or else provided from a separate clock source. An integrated phase-locked loop (PLL) can be used to reduce jitter and to support a range of reference-clock frequency options. The ADC-sample timing is referenced to the ASP data frame, enabling time-aligned operation across multiple devices sharing a common data bus.

The CS5302P can be powered from a single 3.3 V supply; an integrated regulator provides the 1.2 V digital-core supply. Digital input/output at 1.8 V logic levels is also possible using a separate external supply. The device combines high performance with low power consumption.

The CS5302P is available in a commercial-grade 0.4 mm pitch, 48-pin QFN package for operation from –40° to +85°C.

See [Section 11](#) for ordering information.

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## 1 Pin Assignments and Descriptions

### 1.1 48-Pin QFN (Top View, Through-Package)

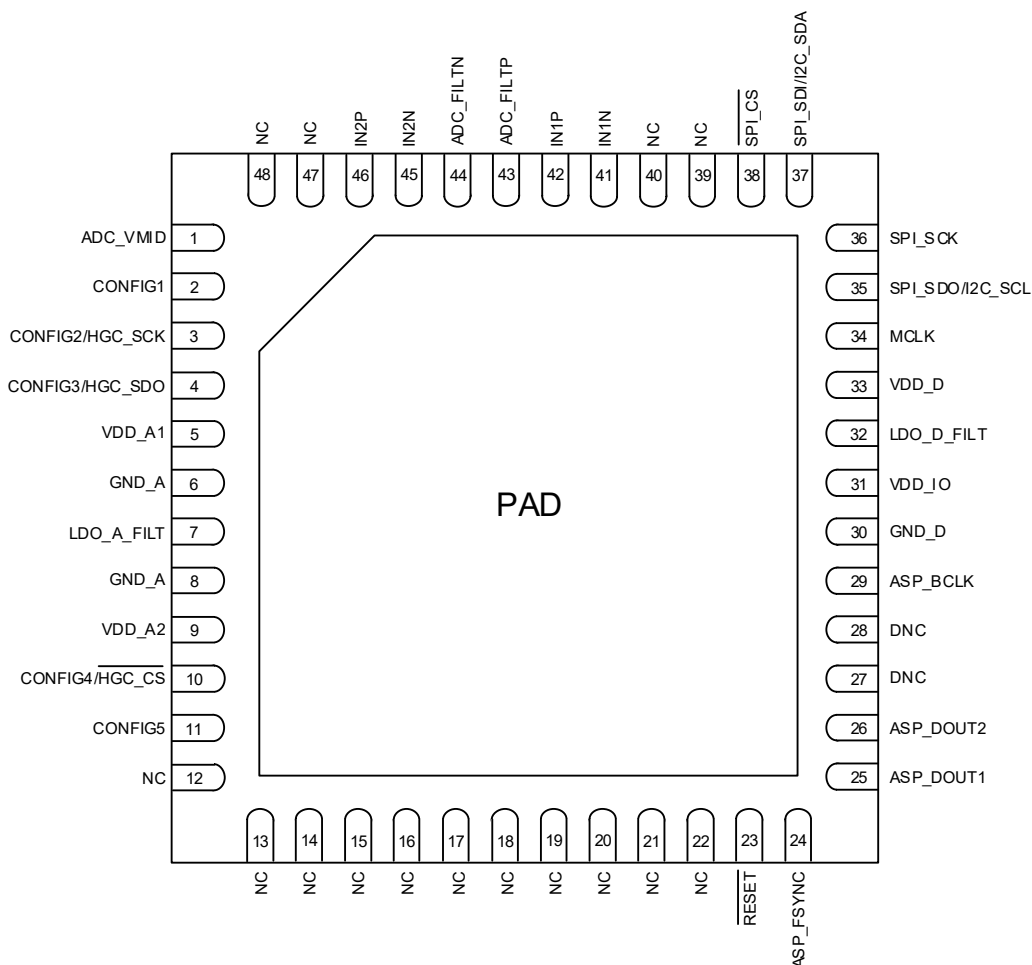


Figure 1-1. QFN 48-pin diagram (Top View, Through Package)

### 1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

| Pin Name           | Pin # | Power Supply | I/O | Description                           |
|--------------------|-------|--------------|-----|---------------------------------------|
| <b>Digital I/O</b> |       |              |     |                                       |
| ASP_BCLK           | 29    | VDD_IO       | I/O | Audio serial port bit clock.          |
| ASP_FSYNC          | 24    | VDD_IO       | I/O | Audio serial port frame sync.         |
| ASP_DOUT1          | 25    | VDD_IO       | O   | Audio serial port data output.        |
| ASP_DOUT2          | 26    |              |     |                                       |
| MCLK               | 34    | VDD_IO       | I   | Master clock input.                   |
| RESET              | 23    | VDD_IO       | I   | Hardware reset control (active low).  |
| SPI_SDO/I2C_SCL    | 35    | VDD_IO       | I/O | SPI data output/I2C clock input.      |
| SPI_SCK            | 36    | VDD_IO       | I   | SPI clock.                            |
| SPI_SDI/I2C_SDA    | 37    | VDD_IO       | I/O | SPI data input/I2C data input/output. |

**Table 1-1. QFN Pin Descriptions (Cont.)**

| Pin Name              | Pin #                                                                  | Power Supply | I/O | Description                                                                    |
|-----------------------|------------------------------------------------------------------------|--------------|-----|--------------------------------------------------------------------------------|
| SPI_CS                | 38                                                                     | VDD_IO       | I   | SPI chip select (active low).                                                  |
| <b>Analog I/O</b>     |                                                                        |              |     |                                                                                |
| ADC_FILT <sub>N</sub> | 44                                                                     | VDD_A        | O   | ADC external capacitor connection.                                             |
| ADC_FILT <sub>P</sub> | 43                                                                     |              |     | ADC_FILT <sub>P</sub> should be connected to VDD_A via a 1 Ω resistor.         |
| ADC_VMID              | 1                                                                      | VDD_A        | O   | Mid-rail voltage reference output.                                             |
| CONFIG1               | 2                                                                      | VDD_A        | I/O | Hardware control pins.                                                         |
| CONFIG2/HGC_SCK       | 3                                                                      |              |     | In software control mode, CONFIG2–4 support the hybrid gain control (HGC)      |
| CONFIG3/HGC_SDO       | 4                                                                      |              |     | SPI controller interface.                                                      |
| CONFIG4/HGC_CS        | 10                                                                     |              |     | In software control mode, CONFIG5 selects the I <sup>2</sup> C target address. |
| CONFIG5               | 11                                                                     |              |     |                                                                                |
| IN1 <sub>N</sub>      | 41                                                                     | VDD_A        | I   | Analog Input 1.                                                                |
| IN1 <sub>P</sub>      | 42                                                                     |              |     |                                                                                |
| IN2 <sub>N</sub>      | 45                                                                     | VDD_A        | I   | Analog Input 2.                                                                |
| IN2 <sub>P</sub>      | 46                                                                     |              |     |                                                                                |
| LDO_A_FILT            | 7                                                                      | VDD_A        | O   | LDO_A regulator external capacitor connection.                                 |
| LDO_D_FILT            | 32                                                                     | VDD_A        | O   | LDO_D regulator external capacitor connection.                                 |
| <b>Power Supplies</b> |                                                                        |              |     |                                                                                |
| VDD_D                 | 33                                                                     | —            | —   | Digital supply (powered from internal LDO)                                     |
| VDD_A1                | 5                                                                      | —            | —   | Analog supply                                                                  |
| VDD_A2                | 9                                                                      | —            | —   | Analog supply                                                                  |
| VDD_IO                | 31                                                                     | —            | —   | Digital I/O supply                                                             |
| GND_D                 | 30                                                                     | —            | —   | Digital ground <sup>1</sup>                                                    |
| GND_A                 | 6, 8, PAD                                                              | —            | —   | Analog ground <sup>1</sup>                                                     |
| <b>No Connect</b>     |                                                                        |              |     |                                                                                |
| DNC                   | 27, 28                                                                 | —            | —   | Do not connect.                                                                |
| NC                    | 12, 13, 14,<br>15, 16, 17,<br>18, 19, 20,<br>21, 22, 39,<br>40, 47, 48 | —            | —   | No connect                                                                     |

1. All ground pins, including the ground paddle, must be tied to a common ground plane directly underneath the CS5302P.

## 1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

**Table 1-2. Termination of Unused Pins**

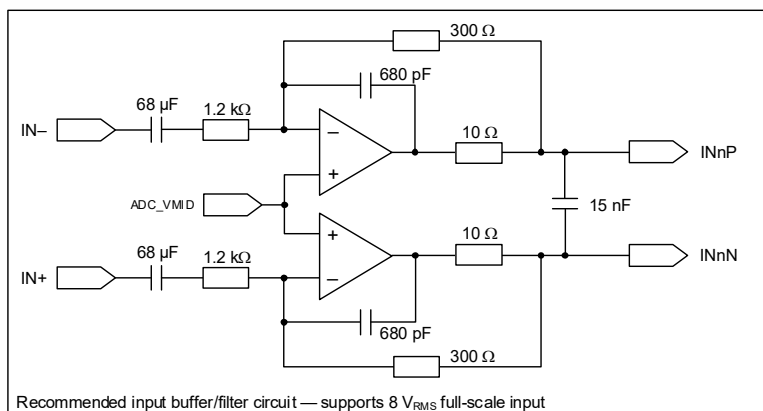
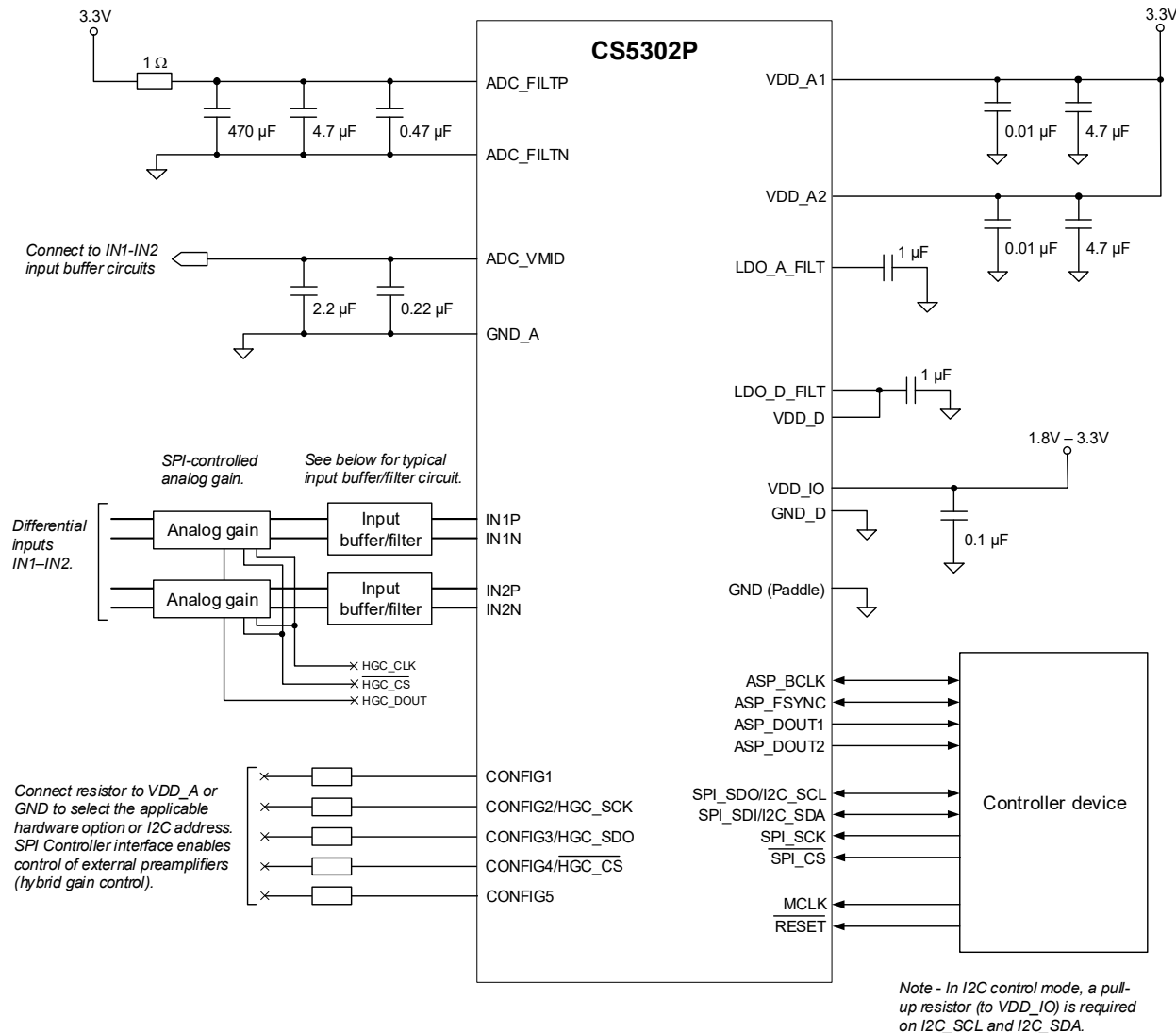
| Name                         | Termination if unused |
|------------------------------|-----------------------|
| ASP_DOUT <sub>x</sub>        | Float                 |
| RESET                        |                       |
| SPI_SDO/I <sup>2</sup> C_SCL | Grounded              |
| SPI_SCK                      |                       |
| SPI_SDI/I <sup>2</sup> C_SDA |                       |
| MCLK                         |                       |
| CONFIG <sub>x</sub>          |                       |
| IN <sub>n</sub> <sub>x</sub> |                       |
| SPI_CS                       | Connect to VDD_IO     |

## 1.4 Electrostatic Discharge (ESD) Protection



ESD-sensitive device. The CS5302P is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

## 2 Typical Connection Diagram



**Figure 2-1. Typical Connections**

## 3 Characteristics and Specifications

**Table 3-1** defines parameters as they are characterized in this section. Note that default register field configurations are used unless specified otherwise in the test conditions.

**Table 3-1. Parameter Definitions**

| Parameter                                    | Definition                                                                                                                                                                                                                                                                                                                                               |
|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Channel separation                           | The difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel. |
| Common-mode rejection ratio (CMRR)           | The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.                                                                                                                                                                                                               |
| Dynamic range                                | The difference in level between the maximum full scale output signal and the sum of all harmonic distortion products plus noise with a low-level input signal applied. Typically, an input signal level 60 dB below full scale is used.                                                                                                                  |
| Power-supply rejection ratio (PSRR)          | The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.                                                                                                                                                                                             |
| Total harmonic distortion plus noise (THD+N) | The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth relative to the RMS amplitude of the fundamental (i.e., test frequency) output.                                                                                                                                                                       |

**Note:** Unless specified otherwise, all performance measurements are for a 10 Hz to 20 kHz bandwidth.

**Table 3-2. Recommended Operating Conditions**

Test conditions (unless specified otherwise): Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground.

| Parameter                          |                                                         | Symbol              | Minimum | Maximum | Unit |
|------------------------------------|---------------------------------------------------------|---------------------|---------|---------|------|
| DC power supply                    | Analog supply <sup>1</sup>                              | VDD_A1, VDD_A2      | 3.13    | 3.47    | V    |
|                                    | Digital supply (powered from internal LDO) <sup>2</sup> | VDD_D               | 1.14    | 1.26    | V    |
|                                    | Digital I/O supply                                      | VDD_IO              | 1.71    | 3.63    | V    |
| Supply ramp up/down (all supplies) |                                                         | t <sub>PWR-UD</sub> | 0.01    | 10      | ms   |
| Ambient temperature                |                                                         | T <sub>A</sub>      | –40     | +85     | °C   |

**Note:** The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. The VDD\_A1 and VDD\_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD\_A.
2. The digital supply is powered from an internal LDO regulator. The VDD\_D pin must be connected to the LDO output pin, LDO\_D\_FILT.

**Table 3-3. Absolute Maximum Ratings**

Test conditions (unless specified otherwise): Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground.

| Parameter                                        |                            | Symbol            | Minimum | Maximum      | Unit |
|--------------------------------------------------|----------------------------|-------------------|---------|--------------|------|
| DC power supply                                  | Analog supply <sup>1</sup> | VDD_A1, VDD_A2    | –0.3    | 4.32         | V    |
|                                                  | Digital supply             | VDD_D             | –0.3    | 1.52         | V    |
|                                                  | Digital I/O supply         | VDD_IO            | –0.3    | 4.32         | V    |
| External voltage applied to digital input/output |                            | V <sub>INDI</sub> | –0.3    | VDD_IO + 0.3 | V    |
| External voltage applied to analog inputs        |                            | V <sub>INAI</sub> | –0.3    | VDD_A + 0.3  | V    |
| Input current                                    | digital input/output       | I <sub>in</sub>   | —       | ±10          | mA   |
|                                                  | analog inputs              |                   | —       | ±10          | mA   |
| Ambient operating temperature                    |                            | T <sub>A</sub>    | –40     | +115         | °C   |
| Junction operating temperature                   |                            | T <sub>J</sub>    | –40     | +125         | °C   |
| Storage temperature                              |                            | T <sub>STG</sub>  | –65     | +150         | °C   |

**Caution:** Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Table 3-2](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The VDD\_A1 and VDD\_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD\_A.

**Table 3-4. ADC Path Characteristics**

Test conditions (unless specified otherwise): External components as shown in [Fig. 2-1](#); VDD\_A = VDD\_IO = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; T<sub>A</sub> = +25°C; 1 kHz sine wave test signal; F<sub>s</sub> = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz (PLL bypass).

| Parameter                                  |                                    | Min | Typ  | Max  | Units            |
|--------------------------------------------|------------------------------------|-----|------|------|------------------|
| Input resistance (INnP to INnN)            |                                    | —   | 50   | —    | kΩ               |
| Full-scale input signal level <sup>1</sup> | 0 dBFS output                      | —   | 2.0  | —    | V <sub>RMS</sub> |
| Dynamic range                              | A-weighted                         | 123 | 126  | —    | dB               |
|                                            | unweighted                         | 120 | 123  | —    | dB               |
| THD+N                                      | –1 dBFS output                     | —   | –110 | –104 | dB               |
|                                            | –20 dBFS output                    | —   | –100 | —    | dB               |
|                                            | –60 dBFS output                    | —   | –60  | —    | dB               |
| CMRR                                       | 100 mV (peak-peak) 1 kHz           | —   | 80   | —    | dB               |
| Channel separation                         |                                    | —   | 110  | —    | dB               |
| Interchannel phase deviation               |                                    | —   | 0.03 | —    | degree           |
| Interchannel gain deviation                |                                    | —   | 0.1  | —    | dB               |
| Gain drift                                 |                                    | —   | ±100 | —    | ppm/°C           |
| PSRR (VDD_A)                               | 100 mV (peak-peak) 1 kHz sine wave | —   | 65   | —    | dB               |

1. The full-scale input signal level is also the maximum analog input level, before clipping occurs. A sinusoidal input signal is assumed.  
Full-scale input signal level scales with VDD\_A.

**Table 3-5. ADC Filter Characteristics**

Test conditions (unless specified otherwise): VDD\_A = VDD\_IO = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; T<sub>A</sub> = +25°C; 1 kHz sine wave test signal, 32-bit audio data.

|                       |               | Parameter                | Min               | Typ     | Max   | Units |
|-----------------------|---------------|--------------------------|-------------------|---------|-------|-------|
| Fs = 32 kHz           | Fast roll-off | Passband                 | to -3 dB corner   | —       | —     | Fs    |
|                       |               | Passband ripple          | $f \leq 0.45 F_s$ | -0.092  | 0.092 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.55 F_s$ | 98      | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 20.5/Fs | —     | s     |
|                       |               |                          | minimum phase     | 4.1/Fs  | —     | s     |
| Fs = 44.1 or 48 kHz   | Fast roll-off | Passband                 | to -3 dB corner   | —       | 0.48  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.46 F_s$ | -0.011  | 0.011 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.54 F_s$ | 98      | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 27.6/Fs | —     | s     |
|                       |               |                          | minimum phase     | 4.0/Fs  | —     | s     |
|                       | Slow roll-off | Passband                 | to -3 dB corner   | —       | 0.46  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.42 F_s$ | -0.099  | 0.099 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.58 F_s$ | 96      | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 13.3/Fs | —     | s     |
|                       |               |                          | minimum phase     | 3.9/Fs  | —     | s     |
| Fs = 88.2 or 96 kHz   | Fast roll-off | Passband                 | to -3 dB corner   | —       | 0.48  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.45 F_s$ | -0.006  | 0.006 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.55 F_s$ | 111     | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 32.3/Fs | —     | s     |
|                       |               |                          | minimum phase     | 6.3/Fs  | —     | s     |
|                       | Slow roll-off | Passband                 | to -3 dB corner   | —       | 0.43  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.27 F_s$ | -0.011  | 0.011 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.77 F_s$ | 103     | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 7.0/Fs  | —     | s     |
|                       |               |                          | minimum phase     | 4.1/Fs  | —     | s     |
| Fs = 176.4 or 192 kHz | Fast roll-off | Passband                 | to -3 dB corner   | —       | 0.47  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.43 F_s$ | -0.009  | 0.009 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.57 F_s$ | 99      | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 19.1/Fs | —     | s     |
|                       |               |                          | minimum phase     | 5.2/Fs  | —     | s     |
|                       | Slow roll-off | Passband                 | to -3 dB corner   | —       | 0.29  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.12 F_s$ | -0.010  | 0.010 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.67 F_s$ | 99      | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 6.4/Fs  | —     | s     |
|                       |               |                          | minimum phase     | 4.2/Fs  | —     | s     |
| Fs = 352.8 or 384 kHz | Fast roll-off | Passband                 | to -3 dB corner   | —       | 0.48  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.43 F_s$ | -0.010  | 0.010 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.57 F_s$ | 100     | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 23.8/Fs | —     | s     |
|                       |               |                          | minimum phase     | 7.5/Fs  | —     | s     |
|                       | Slow roll-off | Passband                 | to -3 dB corner   | —       | 0.34  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.06 F_s$ | -0.001  | 0.001 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.94 F_s$ | 129     | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 5.8/Fs  | —     | s     |
|                       |               |                          | minimum phase     | 4.7/Fs  | —     | s     |
| Fs = 705.6 or 768 kHz | Fast roll-off | Passband                 | to -3 dB corner   | —       | 0.38  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.22 F_s$ | -0.009  | 0.009 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.78 F_s$ | 118     | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 9.1/Fs  | —     | s     |
|                       |               |                          | minimum phase     | 6.4/Fs  | —     | s     |
|                       | Slow roll-off | Passband                 | to -3 dB corner   | —       | 0.30  | Fs    |
|                       |               | Passband ripple          | $f \leq 0.03 F_s$ | -0.008  | 0.008 | dB    |
|                       |               | Stopband attenuation     | $f \geq 0.97 F_s$ | 119     | —     | dB    |
|                       |               | Group delay <sup>1</sup> | linear phase      | 7.1/Fs  | —     | s     |
|                       |               |                          | minimum phase     | 6.2/Fs  | —     | s     |

1. Group delay is measured from the time at which a signal is presented on the input pins (INnP/INnN) to the time of the first data bit of the corresponding FSYNC frame being output on the ASP\_DOUTn pin.

**Table 3-6. ADC High-Pass Filter (HPF)**

Test conditions (unless specified otherwise): VDD\_A = VDD\_IO = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; T<sub>A</sub> = +25°C; 1 kHz sine wave test signal; F<sub>s</sub> = 48 kHz, 32-bit audio data.

| Parameter            |                 | Min | Typ   | Max | Units  |
|----------------------|-----------------|-----|-------|-----|--------|
| Passband             | −0.01 dB corner | —   | 19    | —   | Hz     |
|                      | −3 dB corner    | —   | 1     | —   | Hz     |
| Phase deviation      | f = 20 Hz       | —   | 0.001 | —   | degree |
| Filter settling time |                 | —   | 0.4   | —   | s      |

**Table 3-7. Device Power Consumption**

Test conditions (unless specified otherwise): VDD\_A = VDD\_IO = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; T<sub>A</sub> = +25°C; 1 kHz sine wave test signal; ASP secondary mode, load capacitance (ASP\_DOUTn) = 20 pF, F<sub>s</sub> = 48 kHz, 32-bit audio data.

| Use Configuration      |                               | Typical Current (mA) |                     | Total Power (mW) |
|------------------------|-------------------------------|----------------------|---------------------|------------------|
|                        |                               | I <sub>VDD_A</sub>   | I <sub>VDD_IO</sub> |                  |
| Reset                  | RESET = Logic 0               | 0.36                 | 0.04                | 1.32             |
| Two channels enabled   |                               | 58.4                 | 1.1                 | 196              |
| Four channels enabled  | Mid impedance (INxx_HIZ = 0)  | 31.6                 | 1.1                 | 108              |
|                        | High impedance (INxx_HIZ = 1) | 58.4                 | 1.1                 | 196              |
| Eight channels enabled | Mid impedance (INxx_HIZ = 0)  | 58.6                 | 1.9                 | 200              |
|                        | High impedance (INxx_HIZ = 1) | 112.2                | 1.9                 | 377              |

**Table 3-8. Digital Interface Specifications and Characteristics**

Test conditions (unless specified otherwise): Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; T<sub>A</sub> = +25°C.

| Parameter                                             |                   | Symbol          | Minimum    | Maximum    | Unit |
|-------------------------------------------------------|-------------------|-----------------|------------|------------|------|
| Input leakage current (per pin)                       |                   | I <sub>IN</sub> | —          | ±10        | μA   |
| Input capacitance (per pin)                           |                   | —               | —          | 5          | pF   |
| Digital I/O<br>(VDD_IO logic—all pins except CONFIGx) | High-level output | V <sub>OH</sub> | 0.9×VDD_IO | —          | V    |
|                                                       | Low-level output  | V <sub>OL</sub> | —          | 0.1×VDD_IO | V    |
|                                                       | High-level input  | V <sub>IH</sub> | 0.7×VDD_IO | —          | V    |
|                                                       | Low-level input   | V <sub>IL</sub> | —          | 0.3×VDD_IO | V    |
| Digital I/O<br>(VDD_A logic—CONFIGx pins 1)           | High-level output | V <sub>OH</sub> | 0.9×VDD_A  | —          | V    |
|                                                       | Low-level output  | V <sub>OL</sub> | —          | 0.1×VDD_A  | V    |

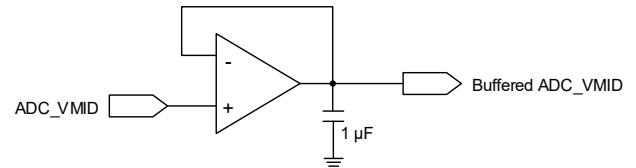
1. The CONFIGx pins are configured as digital output if HGC\_SPI\_EN is set; this is used to support the hybrid gain control (see Section 4.5.4). The CONFIGx pins also support digital output if configured as GP output (see Section 4.9).

**Table 3-9. DC Characteristics**

Test conditions (unless specified otherwise): VDD\_A = VDD\_IO = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; T<sub>A</sub> = +25°C.

| Parameter                                                |                        | Minimum | Typical | Maximum | Unit |
|----------------------------------------------------------|------------------------|---------|---------|---------|------|
| ADC_FILT <sup>1</sup>                                    | Nominal voltage        | —       | 3.3     | —       | V    |
|                                                          | Maximum output current | —       | 0.01    | —       | mA   |
| ADC_VMID <sup>2</sup>                                    | Nominal voltage        | —       | 1.65    | —       | V    |
|                                                          | Maximum output current | —       | 0.01    | —       | mA   |
| VDD_A power-on reset (POR) threshold (V <sub>POR</sub> ) | VDD_A rising           | 1.9     | —       | 2.7     | V    |
|                                                          | VDD_A falling          | 1.8     | —       | 2.6     | V    |
| VDD_D power-on reset (POR) threshold (V <sub>POR</sub> ) | VDD_D rising           | 0.90    | —       | 1.05    | V    |
|                                                          | VDD_D falling          | 0.75    | —       | 0.90    | V    |

1. ADC\_FILT characteristics are measured between ADC\_FILTP and ADC\_FILT<sub>N</sub>, and are provided as a guide for external component selection. The output current (arising from capacitor leakage) must be less than the maximum output current of the ADC\_FILT pin.
2. The output current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current of the ADC\_VMID pin. If a larger current is required, an external VMID buffer should be used. A buffer can be provided using a standard op-amp (noise voltage < 5 nV/√Hz, input current < 10 μA). An example circuit is as follows:


**Table 3-10. Switching Specifications—Reset and Clock References**

Test conditions (unless specified otherwise): VDD\_A = VDD\_IO = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; T<sub>A</sub> = +25°C.

| Parameter               |                                                                                                                                | Symbol                   | Minimum | Typical                                                                      | Maximum | Unit                                                 |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------|--------------------------|---------|------------------------------------------------------------------------------|---------|------------------------------------------------------|
| Reset                   | RESET low (logic 0) pulse width                                                                                                | t <sub>RLPW</sub>        | 1       | —                                                                            | —       | ms                                                   |
|                         | RESET rising edge to control port active                                                                                       | t <sub>IRS</sub>         | —       | —                                                                            | 5       | ms                                                   |
| MCLK input              | MCLK frequency (MCLK as clock source, PLL not used)                                                                            | f <sub>MCLK</sub>        | —       | 22.5792<br>24.576                                                            | —       | MHz<br>MHz                                           |
|                         | MCLK duty cycle (MCLK as clock source, PLL not used)                                                                           | D <sub>MCLK</sub>        | 40      | —                                                                            | 60      | %                                                    |
|                         | MCLK frequency tolerance (MCLK as clock source, PLL not used)                                                                  | —                        | −1      | —                                                                            | 1       | %                                                    |
|                         | REFCLK input frequency (BCLK or MCLK reference) <sup>1</sup>                                                                   | f <sub>REFCLK</sub>      | —       | 2.8224<br>5.6448<br>11.2896<br>22.5792<br>3.072<br>6.144<br>12.288<br>24.576 | —       | MHz<br>MHz<br>MHz<br>MHz<br>MHz<br>MHz<br>MHz<br>MHz |
| Phase-locked loop (PLL) | REFCLK input duty cycle                                                                                                        | D <sub>REFCLK</sub>      | 45      | —                                                                            | 55      | %                                                    |
|                         | REFCLK frequency tolerance                                                                                                     | —                        | −1      | —                                                                            | 1       | %                                                    |
|                         | PLL output frequency<br>F <sub>s</sub> = 32, 48, 96, 192, 384, 768 kHz<br>F <sub>s</sub> = 44.1, 88.2, 176.4, 352.8, 705.6 kHz | f <sub>PLL_OUT</sub>     | —       | 24.576<br>22.5792                                                            | —       | MHz<br>MHz                                           |
|                         | PLL output jitter                                                                                                              | j <sub>PLL_OUT</sub>     | —       | 500                                                                          | —       | ps <sub>RMS</sub>                                    |
|                         | PLL output period jitter                                                                                                       | j <sub>PLL_OUT-PER</sub> | —       | —                                                                            | 500     | ps                                                   |
|                         | PLL lock time                                                                                                                  | t <sub>PLL_LOCK</sub>    | —       | 0.3                                                                          | 1       | ms                                                   |

1. Note the REFCLK input frequency must be integer-related to the sample rate. See [Section 4.4](#) for further details.

**Table 3-11. Switching Specifications—Audio Serial Port (ASP)**

Test conditions (unless specified otherwise): VDD\_A = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; input timings are measured at V<sub>IL</sub> and V<sub>IH</sub> thresholds, output timings are measured at V<sub>OL</sub> and V<sub>OH</sub> thresholds for VDD\_IO logic (as specified in Table 3-8); T<sub>A</sub> = 25°C.

| Parameter 1,2,3,4,5                                    |                                                        | Symbol                                                                                                                                                                           | Minimum                  | Maximum                 | Unit                 |                  |
|--------------------------------------------------------|--------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------------------------|----------------------|------------------|
| Secondary Mode,<br>VDD_IO = 3.3 V                      | ASP_FSYNC input sample/frame rate                      | Fs                                                                                                                                                                               | 32                       | 768                     | kHz                  |                  |
|                                                        | ASP_FSYNC pulse width                                  | t <sub>HI:FSYNC</sub>                                                                                                                                                            | 1/f <sub>ASP_BCLK</sub>  | —                       | ns                   |                  |
|                                                        | ASP_BCLK frequency                                     | f <sub>BCLK</sub>                                                                                                                                                                | 2.048                    | 24.576                  | MHz                  |                  |
|                                                        | ASP_BCLK high period                                   | t <sub>HI:BCLK</sub>                                                                                                                                                             | 18                       | —                       | ns                   |                  |
|                                                        | ASP_BCLK low period                                    | t <sub>LO:BCLK</sub>                                                                                                                                                             | 18                       | —                       | ns                   |                  |
|                                                        | ASP_FSYNC setup time before ASP_BCLK latching edge     | t <sub>SU:FSYNC</sub>                                                                                                                                                            | 5                        | —                       | ns                   |                  |
|                                                        | ASP_FSYNC hold time after ASP_BCLK latching edge       | t <sub>H:FSYNC</sub>                                                                                                                                                             | 5                        | —                       | ns                   |                  |
|                                                        | ASP_DOUT delay after ASP_BCLK launching edge           | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>D:BCLK-DOUT</sub> | 0<br>0                  | 10<br>12             | ns<br>ns         |
|                                                        | ASP_DOUT Hi-Z delay after ASP_BCLK latching edge       | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>DLY:HiZ</sub>     | 0<br>0                  | 9<br>9               | ns<br>ns         |
|                                                        | ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>DLY:EN</sub>      | 0<br>10                 | 10<br>28             | ns<br>ns         |
|                                                        | ASP_x load capacitance                                 | ASP_DOUTx                                                                                                                                                                        | —                        | 0                       | 150                  | pF               |
|                                                        | Primary Mode,<br>VDD_IO = 3.3 V                        | ASP_FSYNC output sample/frame rate                                                                                                                                               | Fs                       | 32                      | 768                  | kHz              |
| ASP_BCLK frequency                                     |                                                        | f <sub>BCLK</sub>                                                                                                                                                                | 2.8224                   | 24.576                  | MHz                  |                  |
| ASP_BCLK duty cycle                                    |                                                        | PLL enabled, MCLK duty cycle 40–60%<br>PLL bypass, BCLK < 22.5792 MHz, MCLK 40–60%<br>PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 45–55%<br>PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 40–60% | D <sub>BCLK</sub>        | 45<br>45<br>42<br>37    | 55<br>55<br>58<br>63 | %<br>%<br>%<br>% |
| ASP_FSYNC delay time after ASP_BCLK launching edge     |                                                        | t <sub>D:BCLK-FSYNC</sub>                                                                                                                                                        | 0                        | 20                      | ns                   |                  |
| ASP_DOUT delay after ASP_BCLK launching edge           |                                                        | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>D:BCLK-DOUT</sub> | 0<br>0                  | 11<br>13             | ns<br>ns         |
| ASP_DOUT Hi-Z delay after ASP_BCLK latching edge       |                                                        | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>DLY:HiZ</sub>     | 0<br>0                  | 10<br>10             | ns<br>ns         |
| ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge |                                                        | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>DLY:EN</sub>      | 0<br>7                  | 15<br>28             | ns<br>ns         |
| ASP_x load capacitance                                 |                                                        | ASP_BCLK<br>ASP_FSYNC<br>ASP_DOUTx                                                                                                                                               | —                        | 0<br>0<br>0             | 50<br>50<br>150      | pF<br>pF<br>pF   |
| Secondary Mode,<br>VDD_IO = 1.8 V                      |                                                        | ASP_FSYNC input sample/frame rate                                                                                                                                                | Fs                       | 32                      | 768                  | kHz              |
|                                                        |                                                        | ASP_FSYNC pulse width                                                                                                                                                            | t <sub>HI:FSYNC</sub>    | 1/f <sub>ASP_BCLK</sub> | —                    | ns               |
|                                                        |                                                        | ASP_BCLK frequency                                                                                                                                                               | f <sub>BCLK</sub>        | 2.048                   | 24.576               | MHz              |
|                                                        |                                                        | ASP_BCLK high period                                                                                                                                                             | t <sub>HI:BCLK</sub>     | 18                      | —                    | ns               |
|                                                        | ASP_BCLK low period                                    | t <sub>LO:BCLK</sub>                                                                                                                                                             | 18                       | —                       | ns                   |                  |
|                                                        | ASP_FSYNC setup time before ASP_BCLK latching edge     | t <sub>SU:FSYNC</sub>                                                                                                                                                            | 5                        | —                       | ns                   |                  |
|                                                        | ASP_FSYNC hold time after ASP_BCLK latching edge       | t <sub>H:FSYNC</sub>                                                                                                                                                             | 5                        | —                       | ns                   |                  |
|                                                        | ASP_DOUT delay after ASP_BCLK launching edge           | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>D:BCLK-DOUT</sub> | 0<br>0                  | 15<br>17             | ns<br>ns         |
|                                                        | ASP_DOUT Hi-Z delay after ASP_BCLK latching edge       | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>DLY:HiZ</sub>     | 0<br>0                  | 12<br>12             | ns<br>ns         |
|                                                        | ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                                                  | t <sub>DLY:EN</sub>      | 0<br>11                 | 15<br>33             | ns<br>ns         |
|                                                        | ASP_x load capacitance                                 | ASP_DOUTx                                                                                                                                                                        | —                        | 0                       | 150                  | pF               |

**Table 3-11. Switching Specifications—Audio Serial Port (ASP) (Cont.)**

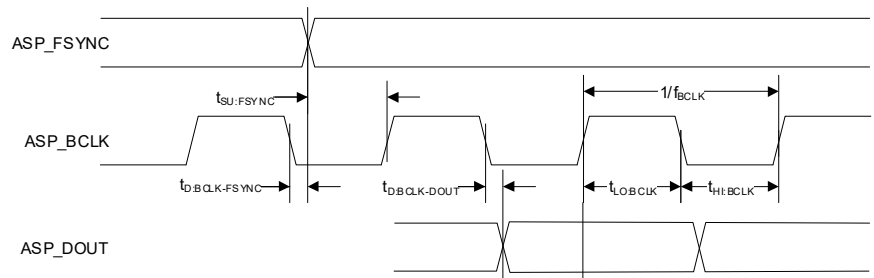
Test conditions (unless specified otherwise): VDD\_A = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; input timings are measured at V<sub>IL</sub> and V<sub>IH</sub> thresholds, output timings are measured at V<sub>OL</sub> and V<sub>OH</sub> thresholds for VDD\_IO logic (as specified in Table 3-8); T<sub>A</sub> = 25°C.

| Parameter 1,2,3,4,5             |                                                                                                                                                                                                         | Symbol                    | Minimum | Maximum | Unit |
|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|---------|---------|------|
| Primary Mode,<br>VDD_IO = 1.8 V | ASP_FSYNC output sample/frame rate                                                                                                                                                                      | F <sub>s</sub>            | 32      | 768     | kHz  |
|                                 | ASP_BCLK frequency                                                                                                                                                                                      | f <sub>BCLK</sub>         | 2.8224  | 24.576  | MHz  |
|                                 | ASP_BCLK duty cycle<br>PLL enabled, MCLK duty cycle 40–60%<br>PLL bypass, BCLK < 22.5792 MHz, MCLK 40–60%<br>PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 45–55%<br>PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 40–60% | D <sub>BCLK</sub>         | 45      | 55      | %    |
|                                 |                                                                                                                                                                                                         |                           | 45      | 55      | %    |
|                                 |                                                                                                                                                                                                         |                           | 40      | 60      | %    |
|                                 |                                                                                                                                                                                                         |                           | 35      | 65      | %    |
|                                 | ASP_FSYNC delay time after ASP_BCLK launching edge                                                                                                                                                      | t <sub>D:BCLK-FSYNC</sub> | 0       | 20      | ns   |
|                                 | ASP_DOUT delay after ASP_BCLK launching edge<br>half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                         | t <sub>D:BCLK-DOUT</sub>  | 0       | 16      | ns   |
|                                 |                                                                                                                                                                                                         |                           | 0       | 18      | ns   |
|                                 | ASP_DOUT Hi-Z delay after ASP_BCLK latching edge<br>half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                                     | t <sub>DLY:HiZ</sub>      | 0       | 13      | ns   |
|                                 |                                                                                                                                                                                                         |                           | 0       | 13      | ns   |
|                                 | ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge<br>half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF                                                                               | t <sub>DLY:EN</sub>       | 0       | 15      | ns   |
|                                 |                                                                                                                                                                                                         |                           | 7       | 34      | ns   |
|                                 |                                                                                                                                                                                                         |                           | 0       | 50      | pF   |
|                                 |                                                                                                                                                                                                         |                           | 0       | 50      | pF   |
|                                 | ASP_x load capacitance                                                                                                                                                                                  | —                         | 0       | 50      | pF   |
|                                 |                                                                                                                                                                                                         |                           | 0       | 50      | pF   |
|                                 |                                                                                                                                                                                                         |                           | 0       | 150     | pF   |

1. The ASP\_BCLK launching edge is selectable. Half-cycle mode = ASP\_BCLK launching edge is opposite to latching edge. Full-cycle mode = ASP\_BCLK launching edge is same as latching edge.

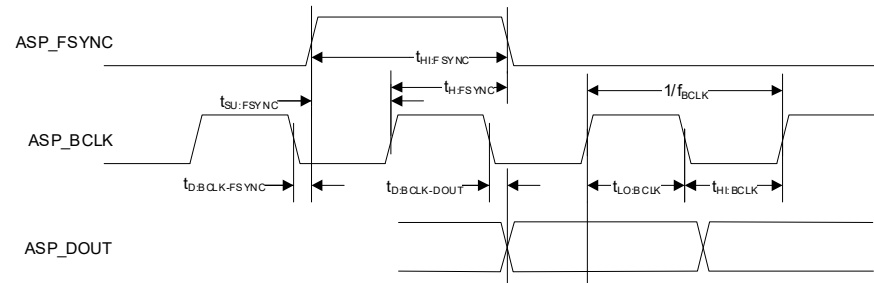
#### 2. ASP timing in I<sup>2</sup>S and Left-Justified Modes

Note that ASP\_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.

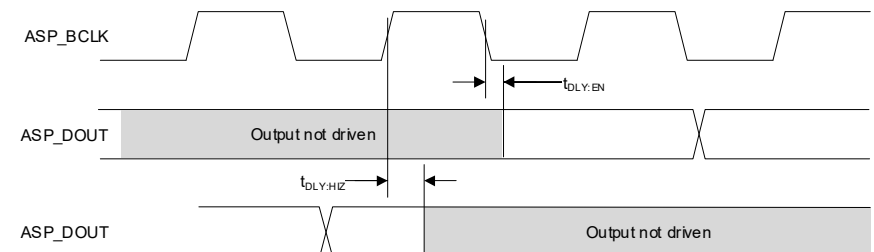


#### 3. ASP timing in TDM Mode

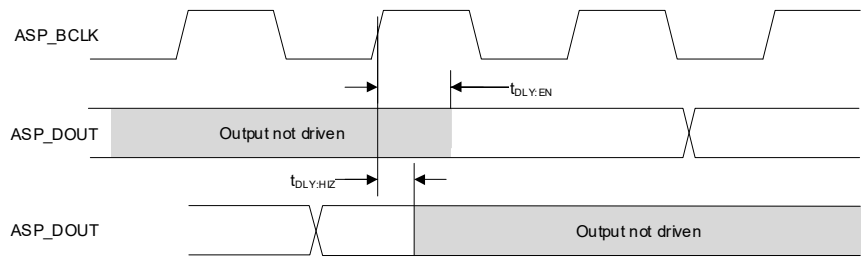
Note that ASP\_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.



#### 4. ASP\_DOUT timing for multiple devices sharing the audio serial port bus—half-cycle mode.



5. ASP\_DOUT timing for multiple devices sharing the audio serial port bus—full-cycle mode.



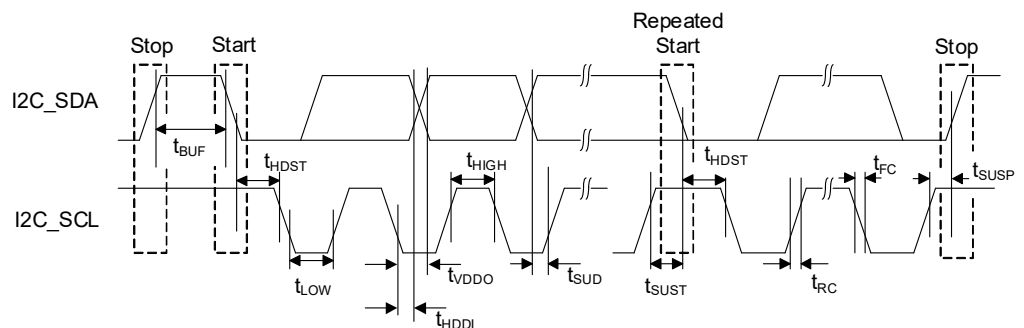
**Table 3-12. Switching Specifications—I<sup>2</sup>C Control Port**

Test conditions (unless specified otherwise): VDD\_A = 3.3 V; VDD\_IO = 1.71–3.63 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; input timings are measured at V<sub>IL</sub> and V<sub>IH</sub> thresholds, output timings are measured at V<sub>OL</sub> and V<sub>OH</sub> thresholds for VDD\_IO logic (as specified in Table 3-8); T<sub>A</sub> = 25°C.

| Parameter 1,2                                        | Symbol            | Minimum                               | Maximum | Unit |    |
|------------------------------------------------------|-------------------|---------------------------------------|---------|------|----|
| SCL clock frequency                                  | f <sub>SCL</sub>  | —                                     | 1000    | kHz  |    |
| Clock low time                                       | t <sub>LOW</sub>  | 500                                   | —       | ns   |    |
| Clock high time                                      | t <sub>HIGH</sub> | 260                                   | —       | ns   |    |
| Start condition hold time (before first clock pulse) | t <sub>HDST</sub> | 260                                   | —       | ns   |    |
| Setup time for repeated start                        | t <sub>SUST</sub> | 260                                   | —       | ns   |    |
| Rise time of SCL and SDA                             | t <sub>RC</sub>   | f <sub>SCL</sub> ≤ 100 kHz            | 600     | 1000 | ns |
|                                                      |                   | 100 kHz < f <sub>SCL</sub> ≤ 400 kHz  | 180     | 300  | ns |
|                                                      |                   | 400 kHz < f <sub>SCL</sub> ≤ 1000 kHz | 72      | 120  | ns |
| Fall time of SCL and SDA                             | t <sub>FC</sub>   | f <sub>SCL</sub> ≤ 100 kHz            | 6.5     | 300  | ns |
|                                                      |                   | 100 kHz < f <sub>SCL</sub> ≤ 400 kHz  | 6.5     | 300  | ns |
|                                                      |                   | 400 kHz < f <sub>SCL</sub> ≤ 1000 kHz | 6.5     | 120  | ns |
| Rise time variation between SDA and SCL              | —                 | —                                     | 1.67    | x    |    |
| Fall time variation between SDA and SCL              | —                 | f <sub>SCL</sub> ≤ 100 kHz            | —       | 100  | ns |
|                                                      |                   | 100 kHz < f <sub>SCL</sub> ≤ 400 kHz  | —       | 100  | ns |
|                                                      |                   | 400 kHz < f <sub>SCL</sub> ≤ 1000 kHz | —       | 75   | ns |
| Setup time for stop condition                        | t <sub>SUSP</sub> | 260                                   | —       | ns   |    |
| SDA setup time to SCL rising                         | t <sub>SUD</sub>  | 50                                    | —       | ns   |    |
| SDA input hold time from SCL falling <sup>3</sup>    | t <sub>HDDI</sub> | 0                                     | —       | ns   |    |
| Output data valid (Data/ACK) <sup>4</sup>            | t <sub>VDDO</sub> | f <sub>SCL</sub> ≤ 100 kHz            | —       | 3450 | ns |
|                                                      |                   | 100 kHz < f <sub>SCL</sub> ≤ 400 kHz  | —       | 900  | ns |
|                                                      |                   | 400 kHz < f <sub>SCL</sub> ≤ 1000 kHz | —       | 450  | ns |
| Bus free time between transmissions                  | t <sub>BUF</sub>  | 500                                   | —       | ns   |    |
| SDA bus capacitance                                  | C <sub>B</sub>    | —                                     | 550     | pF   |    |
| SCL/SDA pull-up resistance                           | R <sub>P</sub>    | 500                                   | —       | Ω    |    |
| Pulse width of spikes to be suppressed               | t <sub>ps</sub>   | 0                                     | 50      | ns   |    |

1. All timing is relative to thresholds specified in Table 3-8, V<sub>IL</sub> and V<sub>IH</sub> for input signals, and V<sub>OL</sub> and V<sub>OH</sub> for output signals.

2. I<sup>2</sup>C control-port timing.



3. Data must be held long enough to bridge the transition time, t<sub>FC</sub>, of SCL.

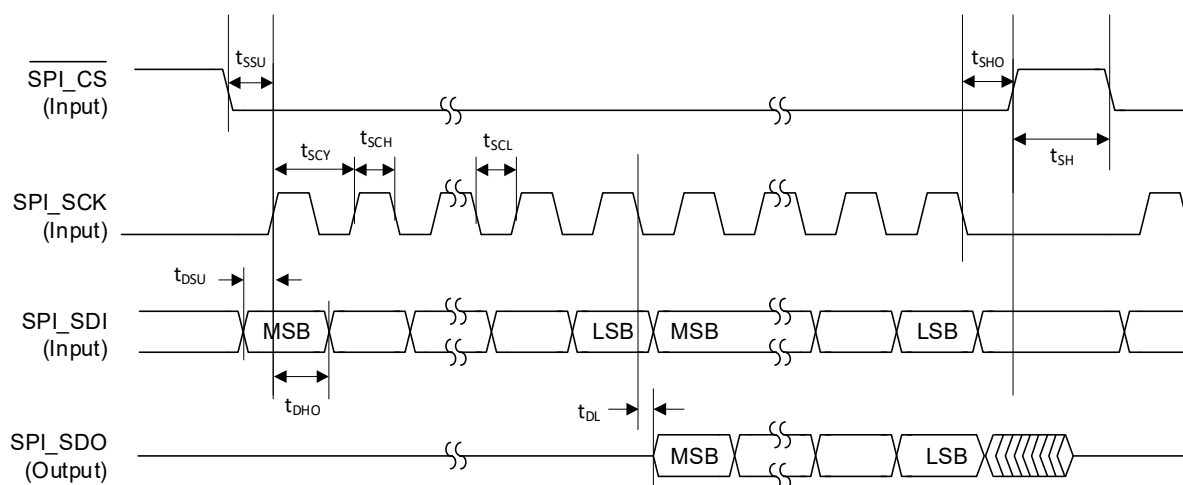
4. Time from falling edge of SCL until data output is valid.

**Table 3-13. Switching Specifications—SPI Control Port**

Test conditions (unless specified otherwise): VDD\_A = 3.3 V; VDD\_IO = 1.71–3.63 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; input timings are measured at V<sub>IL</sub> and V<sub>IH</sub> thresholds, output timings are measured at V<sub>OL</sub> and V<sub>OH</sub> thresholds for VDD\_IO logic (as specified in Table 3-8); T<sub>A</sub> = 25°C.

| Parameter <sup>1</sup>                      | Symbol           | Minimum | Maximum | Unit |
|---------------------------------------------|------------------|---------|---------|------|
| SPI_SCK frequency                           | f <sub>SCY</sub> | —       | 24      | MHz  |
| SPI_CS falling edge to SPI_SCK rising edge  | t <sub>SSU</sub> | 5       | —       | ns   |
| SPI_SCK falling edge to SPI_CS rising edge  | t <sub>SHO</sub> | 0.5     | —       | ns   |
| SPI_SCK pulse width low                     | t <sub>SCL</sub> | 18.5    | —       | ns   |
| SPI_SCK pulse width high                    | t <sub>SCH</sub> | 18.5    | —       | ns   |
| SPI_SDI to SPI_SCK setup time               | t <sub>DSU</sub> | 5       | —       | ns   |
| SPI_SDI to SPI_SCK hold time                | t <sub>DHO</sub> | 2.5     | —       | ns   |
| SPI_SCK falling edge to SPI_SDO transition  | t <sub>DL</sub>  | 0       | 15      | ns   |
| SPI_CS rising edge to SPI_SDO output high-Z | —                | 0       | 15      | ns   |
| Bus free time between active SPI_CS         | t <sub>SH</sub>  | 20      | —       | ns   |

1. SPI control-port timing.

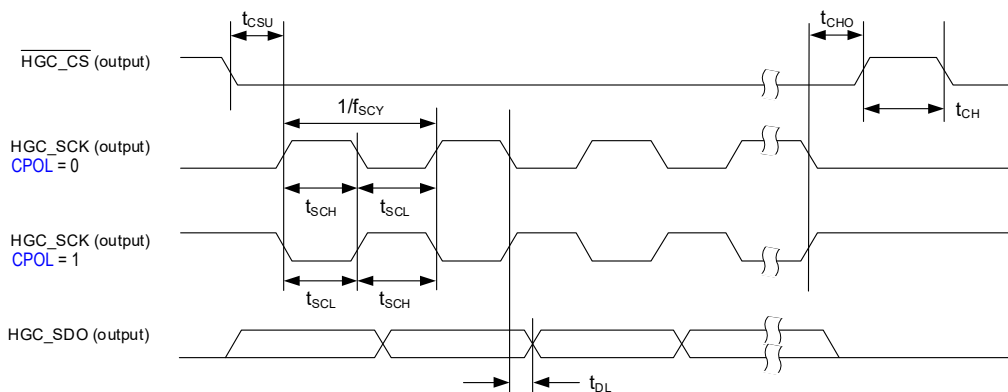


**Table 3-14. Switching Specifications—SPI Controller (Hybrid Gain Control)**

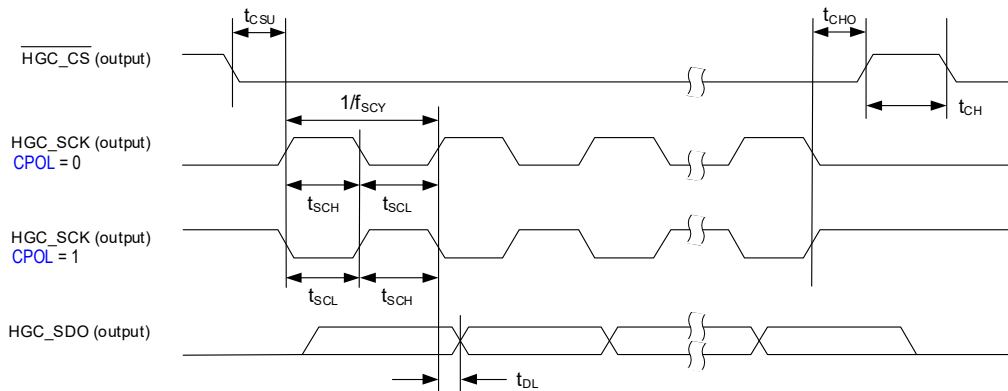
Test conditions (unless specified otherwise): VDD\_A = VDD\_IO = 3.3 V; VDD\_D = 1.2 V (powered from internal LDO); Ground = GND = GND\_A = GND\_D = 0 V; voltages are with respect to ground; output timings are measured at VOL and VOH thresholds for VDD\_A logic (as specified in Table 3-8); TA = 25°C.

| Parameter <sup>1,2</sup>                   | Symbol    | Minimum                                       | Maximum | Unit |
|--------------------------------------------|-----------|-----------------------------------------------|---------|------|
| HGC_SCK frequency                          | $f_{SCY}$ | —                                             | 12.288  | MHz  |
| HGC_CS falling edge to HGC_SCK rising edge | $t_{CSU}$ | 30                                            | —       | ns   |
| HGC_SCK falling edge to HGC_CS rising edge | $t_{CHO}$ | 30                                            | —       | ns   |
| HGC_SCK pulse width low                    | $t_{SCL}$ | 40                                            | —       | ns   |
| HGC_SCK pulse width high                   | $t_{SCH}$ | 40                                            | —       | ns   |
| HGC_SCK falling edge to HGC_SDO transition | $t_{DL}$  | $C_{LOAD} \text{ (HGC\_SDO)} = 30 \text{ pF}$ |         | 15   |
|                                            |           | $C_{LOAD} \text{ (HGC\_SDO)} = 60 \text{ pF}$ |         | 20   |
|                                            |           | –15                                           |         | ns   |
|                                            |           | –20                                           |         | ns   |

1. SPI Controller timing,  $CPHA = 0$ .



2. SPI Controller timing,  $CPHA = 1$ .



## 4 Functional Description

### 4.1 Device Power and Reset

The CS5302P is powered using VDD\_A1, VDD\_A2, VDD\_D, and VDD\_IO external supplies.

**Notes:** The VDD\_A1 and VDD\_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD\_A.

The digital supply, VDD\_D, is powered from an internal LDO regulator. The output of the LDO regulator is provided on the LDO\_D\_FILT pin—the VDD\_D pin should be connected to LDO\_D\_FILT.

There are no power-sequencing requirements—supplies can be enabled in any order.

The CS5302P is in reset if the  $\overline{\text{RESET}}$  pin is asserted (Logic 0), or if the VDD\_A or VDD\_D supply is below the respective reset threshold defined in [Table 3-9](#).

All ground pins, including the ground paddle, must be tied to a common ground plane directly underneath the CS5302P.

### 4.2 Hardware Configuration

The CS5302P supports hardware and software control modes. In hardware mode, the device configuration is determined entirely by external resistors connected to the hardware-control pins. In software mode, the I<sup>2</sup>C/SPI control port is used to configure the device.

In hardware mode, the audio serial port (ASP) configuration is selected using the CONFIG1 and CONFIG2 pins as described in [Table 4-1](#). See [Section 4.4](#) for more details of the sample-rate selection. See [Section 4.7](#) for more details of the ASP operation.

**Table 4-1. Hardware Control—ASP Configuration**

| Pin Name | Pin Configuration  |                | Description                                                                                                    |
|----------|--------------------|----------------|----------------------------------------------------------------------------------------------------------------|
| CONFIG1  | Pull-up to VDD_A   | 0 $\Omega$     | Software control mode (I <sup>2</sup> C/SPI)                                                                   |
|          |                    | 4.7 k $\Omega$ | ASP Primary Mode, 44.1 kHz, 48 kHz sample rate                                                                 |
|          |                    | 22 k $\Omega$  | ASP Primary Mode, 88.2 kHz, 96 kHz sample rate                                                                 |
|          |                    | 100 k $\Omega$ | ASP Primary Mode, 176.4 kHz, 192 kHz sample rate                                                               |
|          | Pull-down to GND_A | 100 k $\Omega$ | ASP Secondary Mode, 176.4 kHz, 192 kHz sample rate                                                             |
|          |                    | 22 k $\Omega$  | ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate                                                               |
|          |                    | 4.7 k $\Omega$ | ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate                                                               |
|          |                    | 0 $\Omega$     | ASP Secondary Mode, autodetect sample rate <sup>1,2</sup>                                                      |
| CONFIG2  | Pull-up to VDD_A   | 0 $\Omega$     | ASP TDM Mode—minimum time slots <sup>3</sup>                                                                   |
|          |                    | 4.7 k $\Omega$ | ASP TDM Mode—maximum time slots <sup>4</sup> , data output on BCLK falling edge (half-cycle mode) <sup>5</sup> |
|          |                    | 22 k $\Omega$  | ASP TDM Mode—maximum time slots <sup>4</sup> , data output on BCLK rising edge (full-cycle mode) <sup>6</sup>  |
|          |                    | 100 k $\Omega$ | —                                                                                                              |
|          | Pull-down to GND_A | 100 k $\Omega$ | —                                                                                                              |
|          |                    | 22 k $\Omega$  | —                                                                                                              |
|          |                    | 4.7 k $\Omega$ | ASP Left-Justified Mode                                                                                        |
|          |                    | 0 $\Omega$     | ASP I <sup>2</sup> S Mode                                                                                      |

1. Valid sample rates for autodetect are 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz.

2. Autodetect sample rate is only supported in MCLK = 256 fs(base) or MCLK = 512 fs(base) clocking configurations (see [Table 4-3](#)).

3. The ASP data format is configured to support the minimum number of time slots necessary for the 2-channel CS5302P output.

4. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate.

5. Half-cycle mode = ASP\_DOUT launching edge (BCLK falling) is opposite to the receiving-device latching edge (BCLK rising).

6. Full-cycle mode = ASP\_DOUT launching edge (BCLK rising) is same as the receiving-device latching edge.

If the ASP is configured for TDM data format with maximum time slots, the TDM slot selection is determined using the CONFIG3 pin as described in [Table 4-2](#). See [Section 4.7](#) for more details of the ASP TDM modes.

**Table 4-2. Hardware Control—TDM Slot Selection**

| Pin Name | Pin Configuration  |                | Description     |
|----------|--------------------|----------------|-----------------|
| CONFIG3  | Pull-up to VDD_A   | 0 $\Omega$     | Slots 14–15 [1] |
|          |                    | 4.7 k $\Omega$ | Slots 12–13 [1] |
|          |                    | 22 k $\Omega$  | Slots 10–11 [1] |
|          |                    | 100 k $\Omega$ | Slots 8–9 [1]   |
|          | Pull-down to GND_A | 100 k $\Omega$ | Slots 6–7 [2]   |
|          |                    | 22 k $\Omega$  | Slots 4–5 [2]   |
|          |                    | 4.7 k $\Omega$ | Slots 2–3       |
|          |                    | 0 $\Omega$     | Slots 0–1       |

1. Slots 8–15 are only valid in 16-slot TDM Mode.

2. Slots 4–7 are only valid in 8-slot or 16-slot TDM Mode.

The clock-reference and ASP channel-ordering configuration is determined using the CONFIG4 pin as described in [Table 4-3](#). See [Section 4.4](#) for more details of the CS5302P clocking architecture. See [Section 4.7.4](#) for more details of the ASP reverse channel-order option.

**Table 4-3. Hardware Control—Clocking Configuration**

| Pin Name | Pin Configuration  |                | Clock Reference 1,2,3,4 | PLL     | Channel Order |
|----------|--------------------|----------------|-------------------------|---------|---------------|
| CONFIG4  | Pull-up to VDD_A   | 0 $\Omega$     | BCLK = 64 fs            | Enabled | Default       |
|          |                    | 4.7 k $\Omega$ | MCLK = 512 fs(base)     | Bypass  | Default       |
|          |                    | 22 k $\Omega$  | MCLK = 256 fs(base)     | Enabled | Default       |
|          |                    | 100 k $\Omega$ | MCLK = 512 fs(base)     | Enabled | Default       |
|          | Pull-down to GND_A | 100 k $\Omega$ | MCLK = 512 fs(base)     | Enabled | Reversed      |
|          |                    | 22 k $\Omega$  | MCLK = 256 fs(base)     | Enabled | Reversed      |
|          |                    | 4.7 k $\Omega$ | MCLK = 512 fs(base)     | Bypass  | Reversed      |
|          |                    | 0 $\Omega$     | BCLK = 64 fs            | Enabled | Reversed      |

1. fs = sample rate, 44.1, 48, 88.2, 96, 176.4, or 192 kHz.

2. fs(base) is the base sample rate. fs(base) = 48 kHz for 48 kHz-related sample rates; fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.

3. BCLK 64 fs configuration is only supported in ASP Secondary Mode.

4. Autodetect sample rate (see [Table 4-1](#)) is only supported in MCLK = 256 fs(base) or MCLK = 512 fs(base) clocking configurations.

In hardware mode, the digital filter selection is determined using the CONFIG5 pin as described in [Table 4-4](#). See [Section 4.6](#) for more details of the digital filters.

**Table 4-4. Hardware Control—Digital Filter Selection**

| Pin Name | Pin Configuration  |                | Description                               |
|----------|--------------------|----------------|-------------------------------------------|
| CONFIG5  | Pull-up to VDD_A   | 0 $\Omega$     | Minimum phase, slow roll-off, HPF bypass  |
|          |                    | 4.7 k $\Omega$ | Minimum phase, fast roll-off, HPF bypass  |
|          |                    | 22 k $\Omega$  | Linear phase, slow roll-off, HPF bypass   |
|          |                    | 100 k $\Omega$ | Linear phase, fast roll-off, HPF bypass   |
|          | Pull-down to GND_A | 100 k $\Omega$ | Linear phase, fast roll-off, HPF enabled  |
|          |                    | 22 k $\Omega$  | Linear phase, slow roll-off, HPF enabled  |
|          |                    | 4.7 k $\Omega$ | Minimum phase, fast roll-off, HPF enabled |
|          |                    | 0 $\Omega$     | Minimum phase, slow roll-off, HPF enabled |

In hardware mode, the device configuration is latched when reset is released (either power-on reset or deassertion of the RESET pin). In hardware mode, the configuration cannot be changed while the device is operational. To update the device configuration, the RESET pin must be asserted (Logic 0), or the device power cycled, in order to read new settings on the CONFIGx pins.

If software mode is selected (i.e., CONFIG1 is connected to VDD\_A), the ASP configuration and digital-filter selection are controlled by register writes via the applicable control interface. Unused CONFIGx pins should be terminated as described in [Section 1.3](#).

**Notes:** In software mode, the CONFIG2, CONFIG3, and CONFIG4 pins can optionally be used to support the hybrid gain control function (see [Section 4.5.4](#)).

In software mode, the CONFIG5 pin is used to select the I<sup>2</sup>C target address (see [Section 4.8](#)). If the SPI control interface is used, it is recommended to connect the CONFIG5 pin to GND.

### 4.3 Software Configuration

Software control mode is enabled if the CONFIG1 pin is connected to VDD\_A. In software control mode, the CS5302P is configured by writing to control registers using the control port.

The control port supports I<sup>2</sup>C and SPI modes of operation; the applicable mode is detected automatically on the respective interface pins. In I<sup>2</sup>C mode, the target address is selectable using the CONFIG5 pin. See [Section 4.8](#) for further details of the I<sup>2</sup>C/SPI control port.

In software control mode, **GLOBAL\_EN** is used as the global control field for enabling/disabling the CS5302P functions. The device should be configured using the applicable control registers before setting **GLOBAL\_EN**.

**Note:** The clocking ([Section 4.4](#)) and ASP ([Section 4.7](#)) control registers are only valid on the rising edge of **GLOBAL\_EN**. Writing to these registers has no effect at any other time. It is recommended to select the disabled state (**GLOBAL\_EN** = 0) before writing to these registers.

A reset of the CS5302P can be triggered by writing 0x5A to the **SW\_RESET** field. A software reset disables all functions and sets the control registers to their default states.

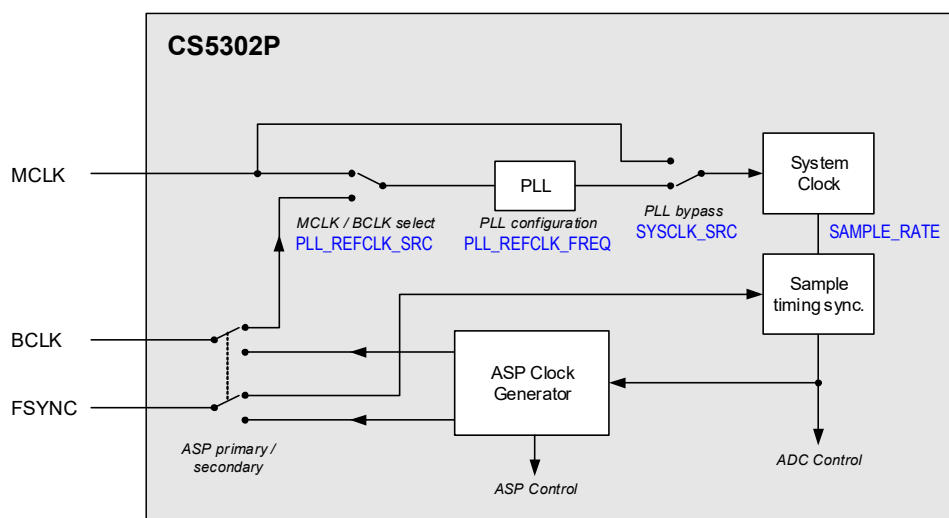
### 4.4 System Clocking

Clocking for the CS5302P is provided from the ASP interface (BCLK) or else using the dedicated MCLK input.

The integrated PLL can be used to generate the internal system clock from the external reference. The MCLK signal can be used as a direct clock reference, bypassing the PLL. If BCLK is selected as the clock reference, the PLL is always used and cannot be bypassed.

In ASP Secondary Mode, the FSYNC input is used to control the ADC sample timing, enabling multiple CS5302P devices to operate synchronously in a system. See [Section 4.7](#) for more details of the ASP.

The clocking architecture is illustrated in [Fig. 4-1](#).



**Figure 4-1. System Clocking**

### 4.4.1 Hardware Control Mode

In hardware control mode, the clocking configuration is determined by the CONFIG4 pin (see [Section 4.2](#)). Four possible clocking configurations are supported as follows:

- BCLK reference—64 fs, PLL enabled
- MCLK reference—512 fs(base), PLL bypass
- MCLK reference—256 fs(base), PLL enabled
- MCLK reference—512 fs(base), PLL enabled

The clocking configuration is defined with reference to the sample rate (fs). Note that fs(base) is the *base sample rate*; fs(base) = 48 kHz for 48 kHz-related sample rates, fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.

The sample rate is selected using the CONFIG1 pin as described in [Section 4.2](#). Sample rates 44.1 kHz–192 kHz can be configured, or else the autodetect option (32 kHz–192 kHz) automatically configures the device according to the ASP interface clock signals. Note the autodetect sample-rate option is only valid if the clock reference source is MCLK (with or without PLL) and the ASP is operating in Secondary Mode (see [Section 4.7](#)).

The BCLK 64 fs configuration enables the CS5302P to be clocked from the audio serial port (ASP) operating in Secondary Mode, with no requirement for any other clock reference. Note that, in the BCLK 64 fs clocking configuration, the ASP data format must be either I<sup>2</sup>S, left-justified, or TDM (minimum time slots); the TDM (maximum time slots) format is not supported.

The MCLK-referenced configurations use a fixed clock frequency of 12.288 / 24.576 MHz (for 48 kHz-related sample rates), or 11.2896 / 22.5792 MHz (for 44.1 kHz-related sample rates).

The supported clocking configurations are summarized in [Table 4-5](#).

**Table 4-5. System Clock Configuration**

| Description         | PLL Select | Reference Source | Reference Frequency       | ASP Operating Conditions <sup>1</sup>                                                                                                               |
|---------------------|------------|------------------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| BCLK = 64 fs        | Enabled    | BCLK             | 64 × sample rate          | Secondary Mode only, I <sup>2</sup> S, left-justified, or TDM (min slots) formats, sample rates 44.1–192 kHz, sample-rate autodetect not supported. |
| MCLK = 512 fs(base) | Bypass     | MCLK             | 24.576 MHz or 22.5792 MHz | Primary or Secondary Mode, I <sup>2</sup> S, left-justified, or TDM data formats, sample rates 32–192 kHz, sample-rate autodetect supported.        |
| MCLK = 256 fs(base) | Enabled    | MCLK             | 12.288 MHz or 11.2896 MHz |                                                                                                                                                     |
| MCLK = 512 fs(base) | Enabled    | MCLK             | 24.576 MHz or 22.5792 MHz |                                                                                                                                                     |

1. See [Section 4.7](#) for details of the audio serial port (ASP).

The sample rate must be related to the system clock reference as described in [Table 4-6](#).

**Table 4-6. Sample Rate Options**

| Reference Source | Clocking Configuration | Reference Frequency (MHz) | Sample Rate (kHz) |
|------------------|------------------------|---------------------------|-------------------|
| BCLK             | BCLK = 64 fs           | 2.8224                    | 44.1              |
|                  |                        | 5.6448                    | 88.2              |
|                  |                        | 11.2896                   | 176.4             |
|                  |                        | 3.072                     | 48                |
|                  |                        | 6.144                     | 96                |
|                  |                        | 12.288                    | 192               |
| MCLK             | MCLK = 256 fs(base)    | 11.2896                   | 44.1, 88.2, 176.4 |
|                  |                        | 12.288                    | 32, 48, 96, 192   |
|                  | MCLK = 512 fs(base)    | 22.5792                   | 44.1, 88.2, 176.4 |
|                  |                        | 24.576                    | 32, 48, 96, 192   |

Note that, if MCLK is configured as the clock source (with or without PLL) and the ASP is configured in Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

## 4.4.2 Software Control Mode

In software (I<sup>2</sup>C/SPI) control mode, the clocking configuration is selected using the following control fields:

- The sample rate is configured using [SAMPLE\\_RATE](#). Sample rates 32 kHz–768 kHz can be configured, or else the autodetect option automatically configures the device according to the ASP interface clock signals. The sample rate must be related to the system clock reference as described in [Table 4-8](#).

Note that the sample-rate autodetect option is only valid if all the following conditions are met:

- Sample rate is 32 kHz–192 kHz
- The clock reference source is MCLK (with or without PLL)
- ASP is operating in Secondary Mode (see [Section 4.7](#))
- The system clock source is selected using [SYSCLK\\_SRC](#). The clock source can be either MCLK or the output from the PLL. If MCLK is selected (i.e., PLL bypass), the MCLK frequency must be 24.576 MHz (for 48 kHz-related sample rates) or 22.5792 MHz (for 44.1 kHz-related sample rates).
- The input reference to the PLL is selected using [PLL\\_REFCLK\\_SRC](#). The reference can be either MCLK or BCLK. Note the BCLK reference is only valid if the ASP is operating in Secondary Mode.
- The frequency of the PLL input reference is configured using [PLL\\_REFCLK\\_FREQ](#).

The supported clocking configurations are summarized in [Table 4-7](#).

**Table 4-7. System Clock Configuration**

| <a href="#">SYSCLK_SRC</a> | <a href="#">PLL_REFCLK_SRC</a> | Description                 | Reference Frequency                           | Sample Rate Autodetect Supported |
|----------------------------|--------------------------------|-----------------------------|-----------------------------------------------|----------------------------------|
| 0                          | X                              | MCLK reference, PLL bypass  | 24.576 MHz or 22.5792 MHz                     | Yes                              |
| 1                          | 1                              | MCLK reference, PLL enabled | Configured by <a href="#">PLL_REFCLK_FREQ</a> | Yes                              |
| 1                          | 0                              | BCLK reference, PLL enabled |                                               | No                               |

The sample rate must be related to the system clock reference as described in [Table 4-8](#).

**Table 4-8. Sample Rate Options**

| Reference Frequency (MHz) | <a href="#">PLL_REFCLK_FREQ</a> | Sample Rate (kHz) <sup>1</sup>  |
|---------------------------|---------------------------------|---------------------------------|
| 2.8224                    | 00                              | 44.1, 88.2, 176.4, 352.8, 705.6 |
| 5.6448                    | 01                              |                                 |
| 11.2896                   | 10                              |                                 |
| 22.5792                   | 11                              |                                 |
| 3.072                     | 00                              | 32, 48, 96, 192, 384, 768       |
| 6.144                     | 01                              |                                 |
| 12.288                    | 10                              |                                 |
| 24.576                    | 11                              |                                 |

1. Sample rate is configured using [SAMPLE\\_RATE](#).

Note that, if MCLK is configured as the clock source (with or without PLL) and the ASP is configured in Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

## 4.5 ADC and Analog Input

The CS5302P supports two analog input channels, each incorporating a high-performance sigma-delta analog-to-digital converter (ADC). Digital volume and mute control is provided on each input channel.

Note that the digital volume and mute controls are supported in software (I<sup>2</sup>C/SPI) control mode only. In hardware control mode, all channels are enabled with 0 dB gain.

### 4.5.1 ADC Path Enable

The analog input and ADC paths are enabled using [INx\\_ADC\\_EN](#) (where x indicates the channel number 1–2).

The polarity of the ADC output can be inverted using [INx\\_INV](#) for the respective channel.

## 4.5.2 Digital Volume and Mute

The ADC signal path incorporates a digital volume control, supporting a gain range of –127.5 dB to 0 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using [INx\\_VOL](#) for the respective input channel. The digital mute is enabled by setting [INx\\_MUTE](#).

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to [IN\\_VU](#). Writing 1 to [IN\\_VU](#) causes the volume and mute settings to be updated on all input paths simultaneously.

When the volume or mute is changed, the gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by [IN\\_RAMP\\_RATE\\_INC](#); for decreasing gain, the rate is controlled by [IN\\_RAMP\\_RATE\\_DEC](#).

**Note:** The [IN\\_RAMP\\_RATE\\_INC](#) and [IN\\_RAMP\\_RATE\\_DEC](#) fields should not be changed while a volume ramp is in progress.

## 4.5.3 Input Clip Warning

The CS5302P provides a clip-warning function on the ADC input paths; this can be used to provide a warning of large or clipped signal levels. The clip warning is indicated using latching status bits, and can also be configured as a logic output on a hardware pin.

The clip-warning threshold level is configured using [IN\\_CLIP\\_THRESH](#). The selected level applies to all input paths.

If an input signal exceeds the clip-warning threshold, the [INx\\_CLIP\\_WARN](#) bit is set (where x indicates the channel number 1–2). These bits are latching fields which, once set, remain set until a 1 is written to the respective bits. These bits can be polled at any time or in response to the logic output signal being asserted.

The clip-warning status can be configured as a logic output on a hardware pin. This is supported on different pins by setting the applicable control bit shown in [Table 4-9](#).

The logic output is active low, i.e., Logic 0 if the clip-warning threshold is exceeded on any input path. The logic output can be either CMOS driven or open drain; this is selected using [CLIP\\_OP\\_CFG](#).

**Table 4-9. Clip Warning Output**

| Pin Name  | Power Supply 1 | Output Enable                     | Notes                                                                                                                                  |
|-----------|----------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| CONFIG4   | VDD_A          | <a href="#">CONFIG4_CLIP_EN</a>   | Clip-warning output is not supported if hybrid gain control (see <a href="#">Section 4.5.4</a> ) is used.                              |
| CONFIG3   | VDD_IO         | <a href="#">CONFIG3_CLIP_EN</a>   |                                                                                                                                        |
| CONFIG2   | VDD_IO         | <a href="#">CONFIG2_CLIP_EN</a>   |                                                                                                                                        |
| SPI_CS    | VDD_IO         | <a href="#">SPI_CS_CLIP_EN</a>    | Clip-warning output is not supported if the SPI control port (see <a href="#">Section 4.8.2</a> ) is used.                             |
| ASP_DOUT2 | VDD_IO         | <a href="#">ASP_DOUT2_CLIP_EN</a> | Clip-warning output is not supported if the ASP (see <a href="#">Section 4.7</a> ) is configured for 705.6 kHz or 768 kHz sample rate. |

1. The digital I/O logic levels for each pin are defined with respect to the applicable power supply. See [Table 3-8](#) for details.

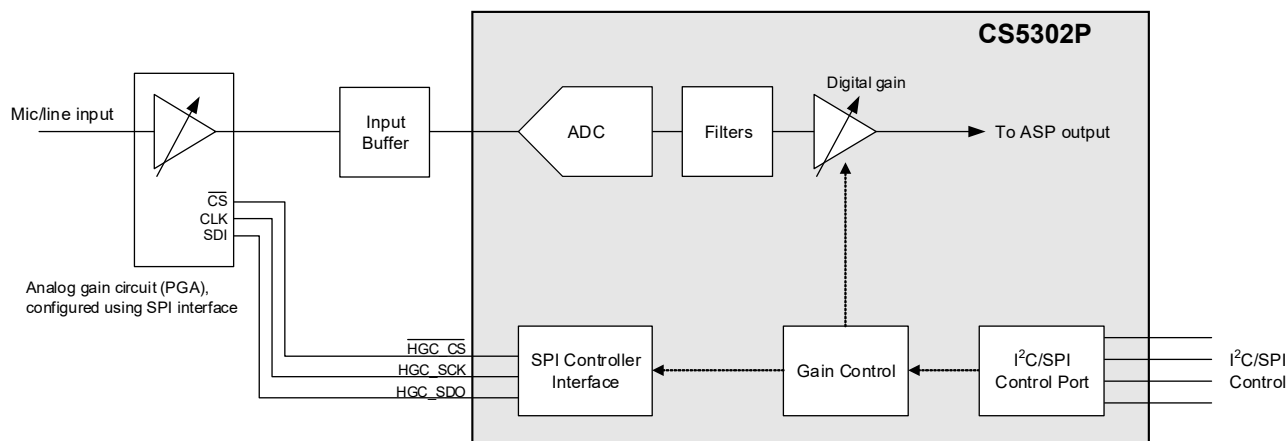
## 4.5.4 Hybrid Gain Control (HGC)

The CS5302P provides the capability to control an external preamplifier (or PGA) associated with the ADC input path. The combination of internal and external gain can be used to optimize the dynamic range of the signal path across a wide range of signal levels.

In typical applications, separate gain stages are provided for analog and digital control of the signal path. The analog stage provides a coarse gain control; the digital stage enables fine adjustment. The CS5302P enables external (analog) and internal (digital) gain adjustments to be fully synchronized across the combined gain range.

A configurable transient-masking function is integrated with the gain-control circuits; this enables seamless gain adjustment by actively suppressing the switching transients often associated with the analog gain selection.

The external PGA is controlled by the CS5302P using a serial interface implemented on the CONFIG pins as shown in Fig. 4-2. Multiple PGAs can be independently controlled in a daisy-chain configuration.



**Figure 4-2. Hybrid Gain Control**

To configure the signal path, the host processor writes control data to the CS5302P, which then forwards the data to the external PGAs using the serial interface. Zero-cross detection is used to synchronize the PGA configuration with the input signal and with the CS5302P digital volume control, ensuring seamless operation across the combined gain range.

Volume ramping is supported on the internal digital volume (see Section 4.5.2); the volume ramp is coordinated with the external PGA control, enabling smooth transitions across the full range of the internal and external gain selections.

The SPI controller interface can also be used to control auxiliary functions associated with the analog input path (e.g., high-pass filter, pad, or phantom power) using a port expander or similar external IC.

#### 4.5.4.1 SPI Controller Interface Configuration

The SPI controller interface is supported using the CONFIG2, CONFIG3, and CONFIG4 pins, which must be configured for the SPI function if required. The SPI function is enabled using `HGC_SPI_EN`. The interface comprises three connections as follows:

- CONFIG2/HGC\_SCK = Clock output
- CONFIG3/HGC\_SDO = Data output
- CONFIG4/HGC\_CS = Chip select ( $\overline{CS}$ ), active low

**Note:** The SPI interface connections are powered by VDD\_A. The digital I/O levels for these pins are referenced to nominal 3.3 V logic (see Table 3-8).

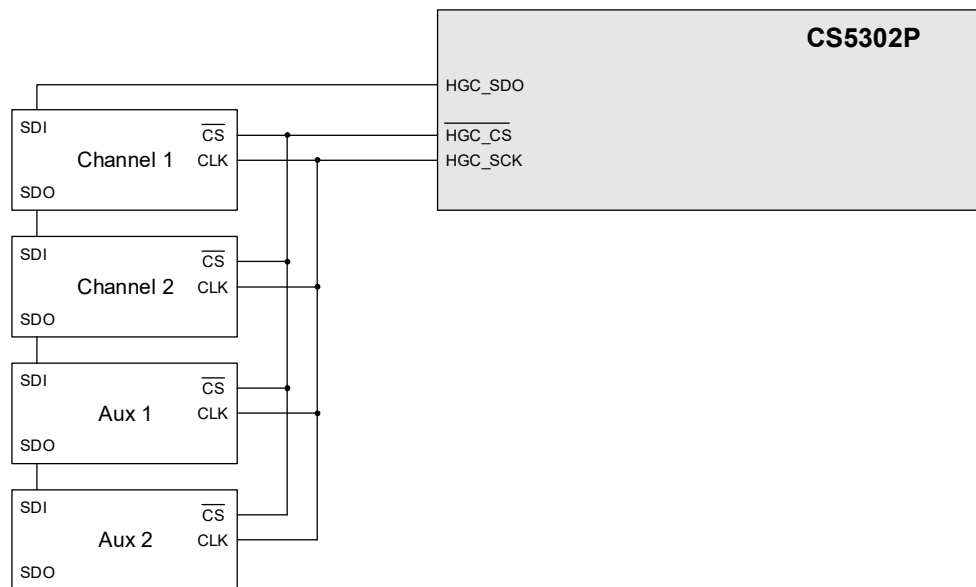
The CS5302P configures the analog gain circuits using a bit pattern which is transmitted to each of the connected devices in a daisy-chain manner. The bit pattern is shifted through each of the connected devices, allowing each device to be individually controlled via a shared data interface.

The SPI interface is fully configurable and flexible to support a wide variety of external gain-control implementations. The SPI data definition is not fixed on the CS5302P; the SPI data can be configured to support whatever bit patterns are required in the specific application.

The number of bits associated with each connected device is configured using the `CHx_BIT_PATT_LENGTH` field for the respective audio channel. This field should be set to 0 for any audio channel where there is no associated device to be controlled.

A maximum of two auxiliary devices can also be controlled (e.g., for high-pass filter, pad, or phantom-power selection). The number of bits associated with the auxiliary devices is configured using the respective `AUXx_BIT_PATT_LENGTH` field. This field should be set to 0 if there is no associated device to be controlled.

Typical connections are shown in Fig. 4-3. Note the CS5302P transmits the bit patterns in the sequence AUX2, AUX1, CH2, CH1. The daisy-chain wiring of the external devices must be in the order shown in Fig. 4-3, to ensure each device is configured with its corresponding bit pattern.



**Figure 4-3. Hybrid Gain Interface Connections**

The SPI controller is configurable to support different timing and signal-polarity options. The **CPOL** bit controls the polarity of the clock output; the **CPHA** bit controls which phase of the clock cycle the data output is valid. See Table 3-14 for timing specifications.

The SPI clock rate is derived as an integer division of the system clock frequency (24.576 MHz for 48 kHz-related sample rates, or 22.5792 MHz for 44.1 kHz-related sample rates). The SPI clock rate is configured using **SCK\_DIV**. The fastest SPI clock rate is 12.288 MHz or 11.2896 MHz, depending on sample rate. Slower clock rates can be used to ensure correct timing of the bus signals in applications where a large load capacitance is connected to the SPI outputs.

The minimum idle period between SPI transactions is configured using **CS\_IDLE\_DUR**. The delay between the falling  $\overline{\text{CS}}$  edge and the first SCK edge is configured using **CS\_FALL\_DELAY**. The minimum delay between the last SCK edge and the rising  $\overline{\text{CS}}$  edge is configured using **CS\_RISE\_DELAY**.

Note that, in normal operation, the timing of the rising  $\overline{\text{CS}}$  edge is controlled by the zero-cross detection; the **CS\_RISE\_DELAY** field determines the minimum delay.

The  $\overline{\text{CS}}$  output is asserted low at the start of each SPI transaction; the SPI controller then transmits the bit patterns for as many audio/aux channels as are configured with a non-zero bit-pattern length. After all the bit patterns have been transmitted,  $\overline{\text{CS}}$  is set high to complete the transaction (see Section 4.5.4.2 for further details on timing).

#### 4.5.4.2 Gain Control Optimization

The CS5302P provides tunable parameters to minimize any audible artifacts when changing the gain configuration.

After a bit pattern has been clocked out to configure the analog gain circuits, the CS5302P waits for a zero-cross detection in the affected audio channel before completing the SPI transaction by deasserting the  $\overline{\text{CS}}$  signal. This ensures the gain change is aligned with the zero crossing, on the assumption that deasserting the  $\overline{\text{CS}}$  (Logic 1) causes the new gain setting to be applied immediately in the external circuit. A timeout for zero-cross detection is configured using **ZC\_TIMEOUT**.

The digital gain for each signal path is controlled internally to the CS5302P. After the analog gain is updated, a delay is applied before updating the digital gain. The delay is used to account for the time difference between the analog gain being updated and the change in signal level reaching the gain-control block. The delay, configured using **DIG\_VOL\_DELAY**, is used to align the analog and digital gain updates in the audio stream.

The [DIG\\_VOL\\_DELAY](#) field should be set equal to the sum of the external path delay (analog gain circuit + input buffer) and the ADC filter group delay. The ADC filter characteristics are specified in [Table 3-5](#). The combined delay should be rounded down for the purposes of selecting the nearest [DIG\\_VOL\\_DELAY](#) option.

A transient-masking function is also available; this is enabled using [TM\\_EN](#). If enabled, the CS5302P repeats one audio sample for the duration of the transient period, masking the artifact arising from the gain change.

The [TM\\_DELAY](#) field defines the time from the analog gain update to the onset of the transient masking. The duration of the masking is configured using [TM\\_HOLD\\_TIME](#).

Transient masking is most effective on low-amplitude signals and is not recommended for larger signals. The CS5302P incorporates a level detector to selectively determine whether the masking should be applied. The transient-masking level detector is enabled on each audio channel using the respective [CHx\\_TM\\_LD\\_EN](#) bit. The level detector calculates the signal level using an exponential moving average (EMA) function; the time constant is configurable using [TM\\_LD\\_TIME](#).

If the level detector is enabled, the threshold for transient masking is configured using [TM\\_LD\\_THRESH](#)—masking is applied if the signal level is below the threshold. If the level detector is disabled, transient masking is applied regardless of the signal level.

#### 4.5.4.3 Audio Channel Gain Control

The host processor configures the analog and digital gain for each audio channel by writing to the respective [CHx\\_ANA\\_VOL](#) and [CHx\\_DIG\\_VOL](#) fields. The host also writes the [CHx\\_BIT\\_PATT](#) fields to provide the bit pattern to configure the external device for the required analog gain.

**Note:** The bit pattern is a maximum of 32 bits (the size is configured using [CHx\\_BIT\\_PATT\\_LENGTH](#)). If the bit pattern is 16 bits or less, it is stored in the [CHx\\_BIT\\_PATT\\_1](#) field. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in [CHx\\_BIT\\_PATT\\_0](#).

The analog and digital gain settings do not become effective immediately on updating the control fields. Writing 1 to [CHx\\_UPDATE](#) indicates the settings for the respective audio channel have been updated and are ready to be applied; the CS5302P services each updated channel in turn and applies the respective gain settings at the earliest opportunity. Note that the exact timing varies, dependent on the zero-cross detection for each affected channel.

The [BUSY\\_STS](#) bit, if set, indicates that gain updates are pending for one or more audio channels (i.e., gain settings have been written to the CS5302P, but not yet applied to the respective audio paths). The bit is cleared automatically when all updates have been applied to the respective channels.

Note that the gain settings and bit patterns for each audio channel can be written at any time, regardless of whether an earlier update is currently pending for that channel.

If an audio channel is enabled, but does not have any associated SPI-controlled external gain circuit, the analog gain and digital gain for the respective channel must be maintained at 0 dB (default).

For efficiency of the host-processor interactions, the [CHx\\_BIT\\_PATT](#), [CHx\\_ANA\\_VOL](#), and [CHx\\_DIG\\_VOL](#) fields can be written as a contiguous block (i.e., one auto-incrementing I<sup>2</sup>C/SPI write operation). The [CHx\\_UPDATE](#) bit can be set in the same I<sup>2</sup>C/SPI operation as writing to the corresponding [CHx\\_DIG\\_VOL](#).

**Note:** If [CHx\\_UPDATE](#) is written 0 when updating the volume/bit-pattern fields, the settings are latched internally but the updates are not applied to the audio path and do not cause the [BUSY\\_STS](#) bit to be set. Writing 0 to [CHx\\_UPDATE](#) is used in the initialization steps described in [Section 4.5.4.6](#). The hybrid gain control must be initialized as described in [Section 4.5.4.6](#) before writing 1 to any of the [CHx\\_UPDATE](#) bits.

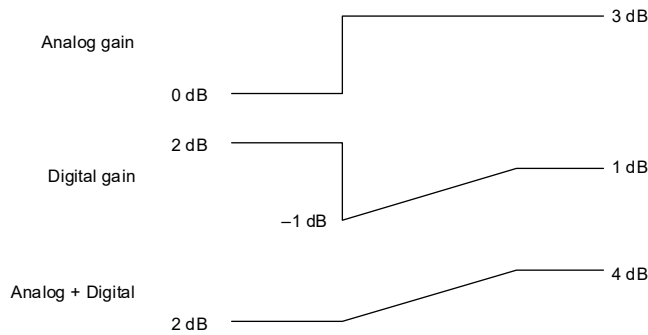
#### 4.5.4.4 Gain Ramping Control

The CS5302P supports independent control of the analog (coarse) and digital (fine) gain stages of the input path. When the digital gain is updated, the gain is ramped up or down to the new value; the ramp rate is configurable as described in [Section 4.5.2](#). When the analog gain is updated, the CS5302P uses the digital gain to provide a ramped response, masking the larger step size of the analog gain.

For example, if the analog gain is increased by 3 dB, the gain step is initially canceled out by decreasing the digital gain by  $-3$  dB. Following this, the digital gain is smoothly ramped up by 3 dB to give the desired overall gain.

Note there is no restriction on whether the analog, digital, or both gains are updated in the same operation—the gain ramping is supported for all combinations.

The gain ramping is illustrated in [Fig. 4-4](#). In the example shown, the analog gain is updated from 0 dB to 3 dB. The digital gain is updated from 2 dB to 1 dB. The digital gain is initially set to  $-1$  dB and then ramped to give a smooth transition from 2 dB to 4 dB in the overall (analog + digital) response.



**Figure 4-4. Gain Ramping**

The gain ramping is configurable using [STEP\\_RAMP\\_EN](#). If this bit is set (default), the CS5302P uses a step change in the digital gain to mask the analog gain steps. If this bit is clear, there is no masking of the analog gain steps.

**Note:** If gain ramping is enabled ([STEP\\_RAMP\\_EN](#) = 1), the volume increasing/decreasing ramp rates must be set to nonzero values. See [Section 4.5.2](#) to configure the volume ramp rates.

#### 4.5.4.5 Auxiliary Device Control

The host processor configures the auxiliary devices by writing to the respective [AUXx\\_BIT\\_PATT](#) fields. Each field contains the bit pattern to configure the respective external device as required.

**Note:** The bit pattern is a maximum of 32 bits (the size is configured using [AUXx\\_BIT\\_PATT\\_LENGTH](#)). If the bit pattern is 16 bits or less, it is stored in the [AUXx\\_BIT\\_PATT\\_1](#) field. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in [AUXx\\_BIT\\_PATT\\_0](#).

If the auxiliary bit patterns are updated, the new settings are latched internally and are not reflected in the SPI data output until a 1 is written to [INIT\\_UPDATE](#). Note that the host processor must confirm that the gain controller is idle ([BUSY\\_STS](#) = 0) before writing to [INIT\\_UPDATE](#).

#### 4.5.4.6 Initialization

The hybrid gain controller must be initialized to ensure correct gain-ramping behavior. The host processor should configure the bit patterns, analog gain, and digital gain fields for all channels—writing [CHx\\_UPDATE](#) = 0 for each audio channel—and then write 1 to [INIT\\_UPDATE](#) to transmit the bit patterns and initialize the internal gain-control algorithms. Note that the host processor must confirm that the gain controller is idle ([BUSY\\_STS](#) = 0) before writing to [INIT\\_UPDATE](#).

**Note:** There is no zero-cross detection or transient masking when using [INIT\\_UPDATE](#), so audible artifacts may occur. It is recommended to mute all audio channels (using [INx\\_MUTE](#)) to suppress any unintended transients.

Writing to [INIT\\_UPDATE](#) has no effect if [BUSY\\_STS](#) = 1, indicating that gain updates are pending for one or more audio channels. The host processor can cancel any pending gain updates by writing 1 to [ABORT](#)—this can be used to return the controller to the idle state as quickly as possible, in readiness for initializing the system with a new configuration.

If the [ABORT](#) bit is written, the CS5302P does not become idle until it has finished applying the updates to the audio channel currently being processed. The host processor must always check the controller is idle ([BUSY\\_STS](#) = 0) before writing to [INIT\\_UPDATE](#).

**Note:** Any gain updates that are canceled using the [ABORT](#) bit may result in an inconsistency between the register map and the respective internal/external gain settings. The [ABORT](#) bit should only be used as part of a control sequence that also uses [INIT\\_UPDATE](#) to apply a new configuration to all channels.

### 4.5.5 External Components

The analog input channels are supported using external buffer circuits, also incorporating anti-alias filters. A typical buffer circuit is shown in [Fig. 2-1](#); the typical buffer circuit shown produces a full-scale (0 dBFS) output from a 8 V<sub>RMS</sub> differential input.

Note that other input-buffer circuit topologies are possible, including support for single-ended input signals and the use of single-ended op-amps.

## 4.6 Digital Filter Selection

The ADC input path incorporates a decimation filter and a high-pass filter. Four types of decimation filter are supported:

- Fast roll-off, minimum phase
- Fast roll-off, linear phase
- Slow roll-off, minimum phase
- Slow roll-off, linear phase

The minimum-phase filters offer the lowest latency and an impulse response with no pre-ringing, at the expense of potential in-band phase distortion. The linear-phase filters have no phase distortion, but also higher latency and a symmetric impulse response.

The slow roll-off filters offer the best impulse response and signal clarity across the audio bandwidth, minimizing latency and phase distortion up to 20 kHz. The fast roll-off filters maximize the signal bandwidth (as a function of the selected sample rate), and widen the stop band to a lower minimum frequency.

In hardware control mode, the filter selection is determined by the CONFIG5 pin (see [Section 4.2](#)). In software (I<sup>2</sup>C/SPI) control mode, the decimation filter is selected using [IN\\_FILTER\\_SEL](#); the high-pass filter is enabled using [IN\\_HPF\\_EN](#).

Performance plots showing the characteristics of the different filters are shown in [Section 7](#).

## 4.7 Audio Serial Port (ASP)

The multichannel ASP supports the output of digital audio samples from the CS5302P. The ASP can be configured as a primary or secondary interface, and supports I<sup>2</sup>S, left-justified, and TDM data formats. The audio samples can be distributed across two data lines, enabling additional bandwidth and flexibility.

Timing specifications for the ASP are described in [Table 3-11](#). An option is supported to drive the output data (DOUT) on the rising or falling BCLK edge; driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS5302P and the sampling edge at the receiving device.

In hardware control mode, the ASP data format is determined by the CONFIGx pins (see [Section 4.2](#)). In software (I<sup>2</sup>C/SPI) control mode, the ASP data format is configured using register fields.

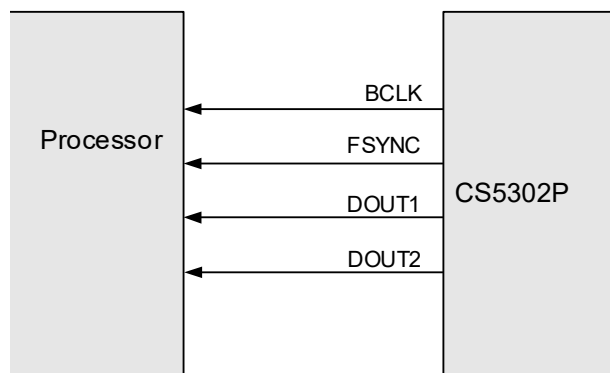
In hardware mode, sample rates 32 kHz–192 kHz are supported. In software mode, the CS5302P supports sample rates 32 kHz–768 kHz.

### 4.7.1 Primary and Secondary Operation

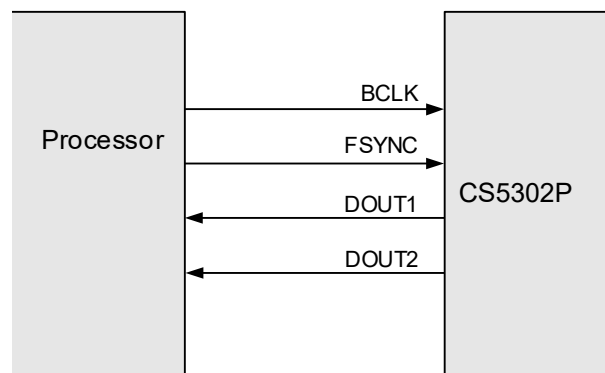
The ASP interface can operate as a primary or secondary interface. In the primary configuration, the BCLK and FSYNC signals are generated by the CS5302P. In the secondary configuration, the BCLK and FSYNC pins are inputs, allowing another device to drive the respective signals.

In hardware control mode, the ASP is configured as a primary or secondary interface using the CONFIG1 pin (see [Section 4.2](#)). In software control mode, the ASP primary/secondary configuration is selected using `ASP_PRIMARY`.

The ASP operation as a primary or secondary interface is illustrated in [Fig. 4-5](#) and [Fig. 4-6](#).



**Figure 4-5. Primary Mode**



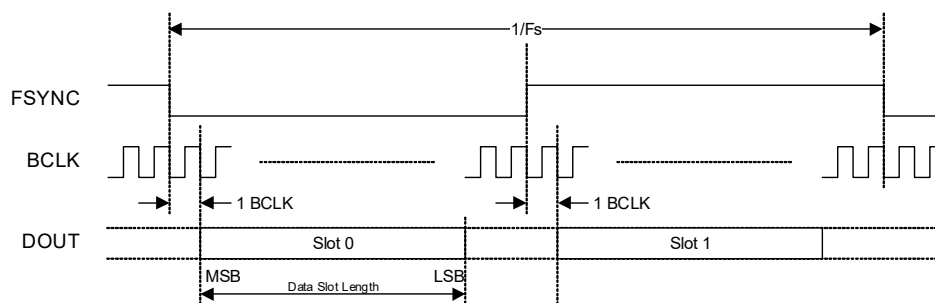
**Figure 4-6. Secondary Mode**

## 4.7.2 ASP Data Formats

The ASP interface can be configured to operate in I<sup>2</sup>S, left-justified, or TDM data formats as illustrated in [Fig. 4-7](#) through [Fig. 4-9](#). The data-bit order is MSB first in each case; data words are encoded in 2's complement (signed, fixed-point) format. Each audio sample is allocated a time slot within the FSYNC frame. Multiple data lines provide capacity to support different audio channels concurrently on different data pins.

- In I<sup>2</sup>S Mode, the MSB is valid on the second BCLK rising edge following a FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

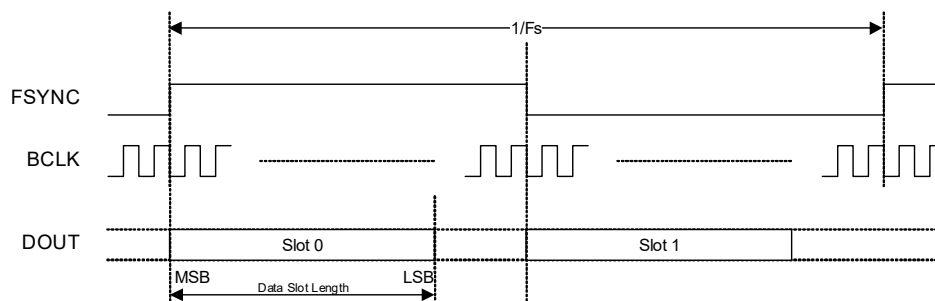
I<sup>2</sup>S Mode data format is shown in [Fig. 4-7](#).



**Figure 4-7. I<sup>2</sup>S Data Format**

- In Left-Justified Mode, the MSB is valid on the first BCLK rising edge following a FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

Left-Justified Mode data format is shown in [Fig. 4-8](#).

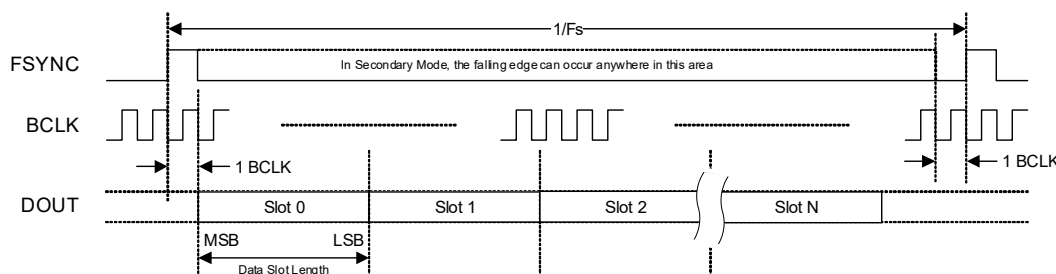


**Figure 4-8. Left-Justified Data Format**

- In TDM modes, the MSB of the first channel is valid on the second BCLK rising edge following the rising FSYNC edge. Subsequent channels follow immediately after the previous one. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of the last channel data and the start of the next FSYNC frame.

In Primary Mode, the FSYNC output resembles the frame pulse shown in [Fig. 4-9](#). In Secondary Mode, the FSYNC pulse duration can be anything less than  $1/F_s$ , provided the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse.

TDM Mode data format is shown in [Fig. 4-9](#).



**Figure 4-9. TDM Data Format**

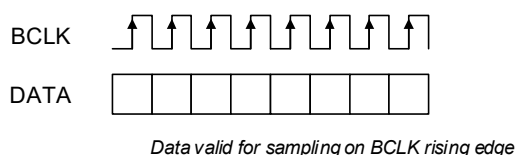
### 4.7.3 ASP Configuration

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see [Section 4.2](#)).

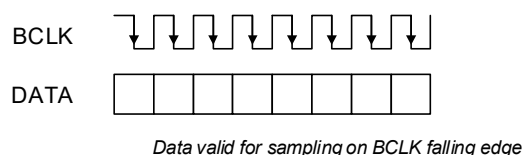
In software control mode, the ASP data format is configured using [SAMPLE\\_RATE](#) and [ASP\\_FORMAT](#). If ASP Primary Mode is selected (see [Section 4.7.1](#)), the BCLK frequency is configured using [ASP\\_BCLK\\_FREQ](#).

In software control mode, the BCLK polarity is selected using [ASP\\_BCLK\\_INV](#). The polarity selection is valid in primary and secondary modes, and determines whether the data is valid for sampling on the rising edge or the falling edge.

The BCLK polarity is illustrated in [Fig. 4-10](#) and [Fig. 4-11](#). Note that, in hardware control mode, the BCLK polarity is assumed to be noninverted.



**Figure 4-10. Noninverted BCLK**



**Figure 4-11. Inverted BCLK**

In TDM Mode, the two data-format options are supported as follows:

- TDM Mode—minimum time slots. The ASP data format is configured to support the minimum number of time slots necessary for the 2-channel CS5302P output. This mode allows the BCLK rate to be as low as possible, equating to a minimum of 32 BCLK cycles per audio sample.
- TDM Mode—maximum time slots. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate. The mode is designed for the maximum BCLK rate (22.5792 MHz for 44.1 kHz-related sample rates, or 24.576 MHz for 48 kHz-related sample rates), enabling the maximum possible bandwidth on the ASP data bus to be shared with other devices.

Note that, for sample rates >192 kHz, the TDM data format is the same regardless of the minimum/maximum time-slot option.

If the ASP is configured for TDM Mode with maximum time slots, the output data (DOUT) can be driven either on the rising or falling BCLK edge. Driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS5302P and the sampling edge at the receiving device.

Note that the ASP timing options are dependent on the behavior of the receiving device. It is assumed, for noninverted BCLK, the data is sampled on the rising BCLK edge. Similarly, for inverted BCLK, it is assumed the data is sampled on the falling BCLK edge.

The DOUT drive options for half-cycle and full-cycle mode are described in [Table 4-10](#). In full-cycle mode, the output data is driven on the same BCLK edge as it is sampled (i.e., one full BCLK cycle before the sampling edge).

**Table 4-10. TDM Mode (Maximum Time Slots)—DOUT Drive Timing**

| TDM Mode <sup>1</sup> | BCLK Polarity <sup>2</sup> | DOUT launching (drive) edge | DOUT latching (sampling) edge |
|-----------------------|----------------------------|-----------------------------|-------------------------------|
| Half-cycle            | Noninverted                | BCLK falling                | BCLK rising                   |
|                       | Inverted                   | BCLK rising                 | BCLK falling                  |
| Full-cycle            | Noninverted                | BCLK rising                 | BCLK rising                   |
|                       | Inverted                   | BCLK falling                | BCLK falling                  |

1. The TDM variant is selected using the CONFIG2 pin (in hardware control mode) or [ASP\\_FORMAT](#) (in software control mode).

2. The BCLK polarity is selected using [ASP\\_BCLK\\_INV](#) in software control mode. In hardware control mode, the polarity is assumed noninverted.

The ASP configuration depends on the sample rate and the selected data format as described in [Table 4-11](#). The output data is provided on ASP\_DOUT1 in most cases; the ASP\_DOUT2 pin is used for 705.6 kHz/768 kHz operation only.

**Table 4-11. ASP Data Format**

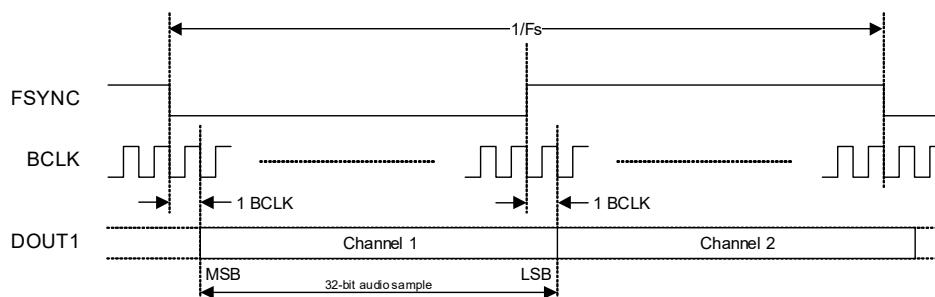
| ASP Format <sup>1</sup>          | ASP Sample Rate <sup>2,3</sup> | DOUT pins used | Time slots per frame <sup>4</sup> | BCLK <sup>5,6</sup>          |
|----------------------------------|--------------------------------|----------------|-----------------------------------|------------------------------|
| I <sup>2</sup> S, Left-Justified | 32 kHz                         | 1              | 2                                 | BCLK ≥ 64 fs <sup>[7]</sup>  |
|                                  | 44.1 kHz, 48 kHz               | 1              | 2                                 | BCLK ≥ 64 fs                 |
|                                  | 88.2 kHz, 96 kHz               | 1              | 2                                 | BCLK ≥ 64 fs                 |
|                                  | 176.4 kHz, 192 kHz             | 1              | 2                                 | BCLK ≥ 64 fs                 |
|                                  | 352.8 kHz, 384 kHz             | 1              | 2                                 | BCLK = 64 fs                 |
|                                  | 705.6 kHz, 768 kHz             | —              | —                                 | —                            |
|                                  | Autodetect (32 kHz–192 kHz)    | 1              | 2                                 | BCLK ≥ 64 fs                 |
| TDM—minimum time slots           | 32 kHz                         | 1              | 2                                 | BCLK ≥ 64 fs <sup>[7]</sup>  |
|                                  | 44.1 kHz, 48 kHz               | 1              | 2                                 | BCLK ≥ 64 fs                 |
|                                  | 88.2 kHz, 96 kHz               | 1              | 2                                 | BCLK ≥ 64 fs                 |
|                                  | 176.4 kHz, 192 kHz             | 1              | 2                                 | BCLK ≥ 64 fs                 |
|                                  | 352.8 kHz, 384 kHz             | 1              | 2                                 | BCLK = 64 fs                 |
|                                  | 705.6 kHz, 768 kHz             | 2              | 1                                 | BCLK = 32 fs                 |
|                                  | Autodetect (32 kHz–192 kHz)    | 1              | 2                                 | BCLK ≥ 64 fs                 |
| TDM—maximum time slots           | 32 kHz                         | 1              | 16                                | BCLK ≥ 512 fs <sup>[7]</sup> |
|                                  | 44.1 kHz, 48 kHz               | 1              | 16                                | BCLK = 512 fs                |
|                                  | 88.2 kHz, 96 kHz               | 1              | 8                                 | BCLK = 256 fs                |
|                                  | 176.4 kHz, 192 kHz             | 1              | 4                                 | BCLK = 128 fs                |
|                                  | 352.8 kHz, 384 kHz             | 1              | 2                                 | BCLK = 64 fs                 |
|                                  | 705.6 kHz, 768 kHz             | 2              | 1                                 | BCLK = 32 fs                 |
|                                  | Autodetect (32 kHz–192 kHz)    | 1              | 4                                 | BCLK ≥ 128 fs                |

1. The ASP format is selected using the CONFIG2 pin (in hardware control mode) or [ASP\\_FORMAT](#) (in software control mode).
2. The sample rate is selected using the CONFIG1 pin (in hardware control mode) or [SAMPLE\\_RATE](#) (in software control mode).
3. Sample rates 32 kHz–768 kHz supported in software control mode, 32 kHz–192 kHz in hardware control mode.
4. Time slots per frame is the number of data-sample time slots supported on each of the active DOUT pins.
5. The BCLK rate must be a constant integer multiple of the sample rate (fs).
6. In ASP primary mode (hardware control), the BCLK frequency is the minimum specified rate. In ASP primary mode (software control), the BCLK frequency is configured using [ASP\\_BCLK\\_FREQ](#).
7. In ASP primary mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96 fs, 192 fs, 384 fs, or 768 fs.

The ASP data format in I<sup>2</sup>S, Left-Justified, and TDM interface modes as illustrated in [Fig. 4-12](#) through [Fig. 4-15](#). Refer to [Table 4-11](#) for the applicable definition.

- If I<sup>2</sup>S data format is selected, the ASP supports audio channels 1–2 as shown in [Fig. 4-12](#). The minimum BCLK rate is 64 fs (where fs is the sample rate). A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

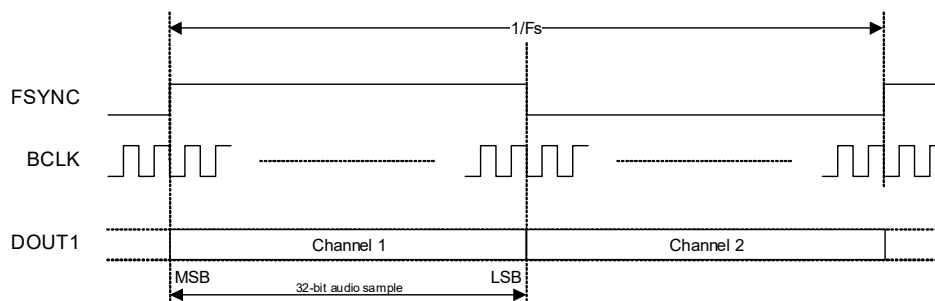
Note that the output data is provided on ASP\_DOUT1; the ASP\_DOUT2 pin is not used.



**Figure 4-12. I<sup>2</sup>S Data Format**

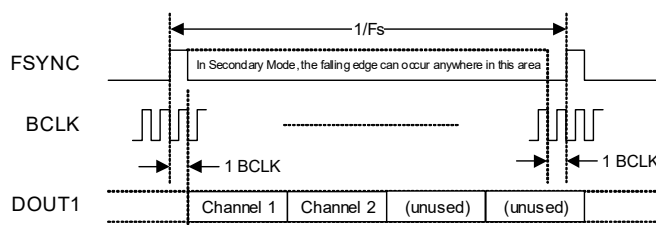
- If Left-Justified data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-13. The minimum BCLK rate is 64 fs (where fs is the sample rate). A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

Note that the output data is provided on ASP\_DOUT1; the ASP\_DOUT2 pin is not used.



**Figure 4-13. Left-Justified Data Format**

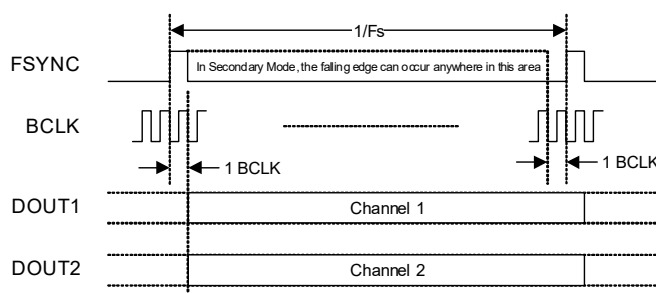
- In TDM Mode, the FSYNC frame is configured for 1, 2, 4, 8, or 16 slots as specified in Table 4-11. In 4-, 8-, and 16-slot modes, the slot assignment for audio channels 1–2 is selected using the CONFIG3 pin (in hardware control mode—see Section 4.2) or else using ASP\_TDM\_SLOT (in software control mode). In 2-slot modes, the default slot assignment (slots 0–1) should be selected. The BCLK rate is related to the sample rate (fs) as described in Table 4-11. Where applicable, the BCLK rate can be higher than the stated minimum, resulting in additional unused BCLK cycles between the last slot in the frame and the start of the next frame. The ASP\_DOUTn pins are high impedance if the CS5302P is not transmitting data, allowing other devices on the bus to transmit data during any unused time slots. In 2-, 4-, 8-, and 16-slot modes, the output data is provided on ASP\_DOUT1; the ASP\_DOUT2 pin is not used. The 4-slot TDM format is shown in Fig. 4-14. In the example shown, audio channels 1–2 occupy TDM slots 0–1 respectively.



**Figure 4-14. TDM Data Format—1 x DOUT**

In 1-slot mode, the output data is provided on ASP\_DOUT1 and ASP\_DOUT2. Note the 1-slot format is used to support 705.6 kHz and 768 kHz sample rates only.

The 1-slot TDM format is shown in Fig. 4-15.



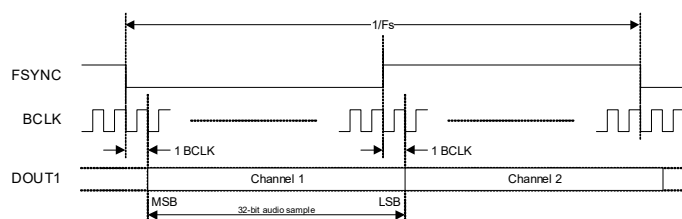
**Figure 4-15. TDM Data Format—2 x DOUT**

### 4.7.4 ASP Channel Reverse Order

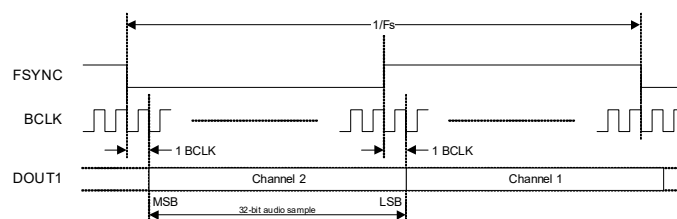
The CS5302P supports an option to reverse the ASP channel order. If the reverse channel order is selected, the ASP data format is reconfigured to output the channels in the opposite order to the default order shown in [Section 4.7.3](#).

The reverse channel-order option can be used to ease PCB layout constraints, enabling the ASP data ordering to be aligned with the external pin connections, regardless of the orientation of the device on the PCB.

The reverse channel order is illustrated in [Fig. 4-16](#) and [Fig. 4-17](#). The I<sup>2</sup>S data format is shown as an example; the equivalent channel substitutions are supported in left-justified and TDM format also.



**Figure 4-16. Default Channel Order**



**Figure 4-17. Reverse Channel Order**

In hardware control mode, the ASP channel order is selected using the CONFIG4 hardware control pin, as described in [Section 4.2](#). In software (I<sup>2</sup>C/SPI) control mode, the ASP channel order is selected using [ASP\\_CH\\_REVERSE](#).

## 4.8 I<sup>2</sup>C/SPI Control Port

The CS5302P incorporates a control port, supporting I<sup>2</sup>C or SPI modes of operation. In software control mode, the CS5302P is configured by writing to control registers using the control port.

The control port is automatically configured in I<sup>2</sup>C mode or SPI mode following the first valid I<sup>2</sup>C/SPI activity detected after power-on or hardware reset.

### 4.8.1 I<sup>2</sup>C Control Port

The I<sup>2</sup>C control port is supported using the I2C\_SCL and I2C\_SDA pins.

The CS5302P is a target device on the I<sup>2</sup>C bus—SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS5302P transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device address (this is not the same as the address of each register in the CS5302P). Note that the LSB of the device address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I<sup>2</sup>C device address is configured using the CONFIG5 pin as described in [Table 4-12](#).

**Table 4-12. I<sup>2</sup>C Address Selection—CONFIG5 pin**

| Pin Configuration  |        | I <sup>2</sup> C Address  |
|--------------------|--------|---------------------------|
| Pull-up to VDD_A   | 0 Ω    | 0x9E (write), 0x9F (read) |
|                    | 4.7 kΩ | 0x9C (write), 0x9D (read) |
|                    | 22 kΩ  | 0x9A (write), 0x9B (read) |
|                    | 100 kΩ | 0x98 (write), 0x99 (read) |
| Pull-down to GND_A | 100 kΩ | 0x96 (write), 0x97 (read) |
|                    | 22 kΩ  | 0x94 (write), 0x95 (read) |
|                    | 4.7 kΩ | 0x92 (write), 0x93 (read) |
|                    | 0 Ω    | 0x90 (write), 0x91 (read) |

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS5302P responds to the start condition and shifts in the next 8 bits on SDA (8-bit device address, including read/write bit, MSB first). If the device address received matches the device address of the CS5302P, the CS5302P responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognized or the R/W bit is set incorrectly, the CS5302P returns to the idle condition and waits for a new start condition.

If the device address matches the device address of the CS5302P, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence the CS5302P returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

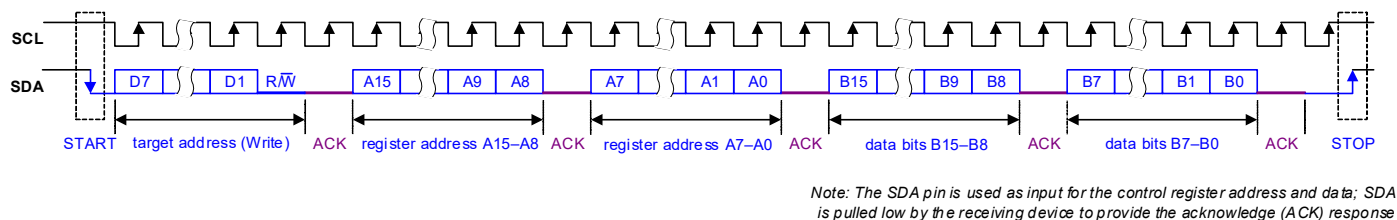
The I<sup>2</sup>C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). Note that the full I<sup>2</sup>C message protocol also includes a device address, a read/write bit, and other signaling bits (see Fig. 4-18 and Fig. 4-19).

The CS5302P supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

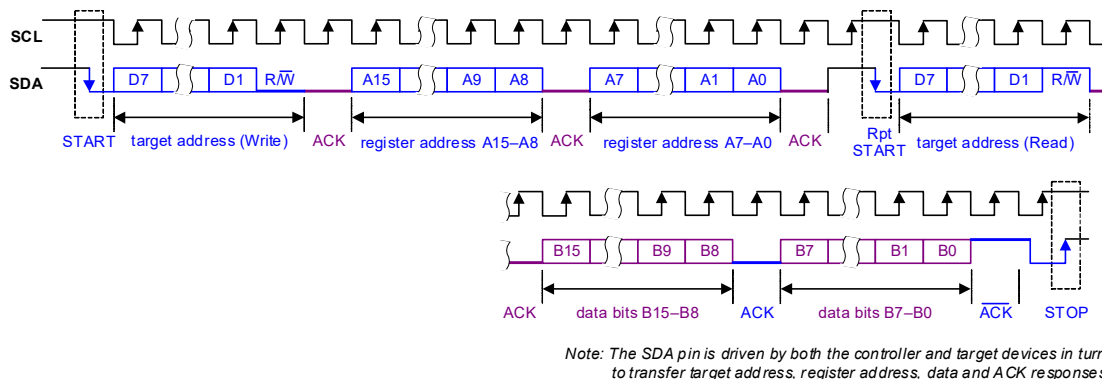
Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS5302P automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

The I<sup>2</sup>C protocol for a single, 16-bit register write operation is shown in Fig. 4-18.



**Figure 4-18. Control Interface I<sup>2</sup>C Register Write**

The I<sup>2</sup>C protocol for a single, 16-bit register read operation is shown in Fig. 4-19.



**Figure 4-19. Control Interface I<sup>2</sup>C Register Read**

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-20 through Fig. 4-23. The terminology used in the following figures is detailed in Table 4-13.

**Table 4-13. Control Interface (I<sup>2</sup>C) Terminology**

| Terminology   | Description                              |
|---------------|------------------------------------------|
| S             | Start condition                          |
| Sr            | Repeated start                           |
| A             | Acknowledge (SDA low)                    |
| $\bar{A}$     | No Acknowledge (SDA high)                |
| P             | Stop condition                           |
| $R/\bar{W}$   | Read/not Write: 0 = Write, 1 = Read      |
| [White field] | Data flow from bus controller to CS5302P |
| [Gray field]  | Data from CS5302P to bus controller      |

Fig. 4-20 shows a single register write to a specified address.

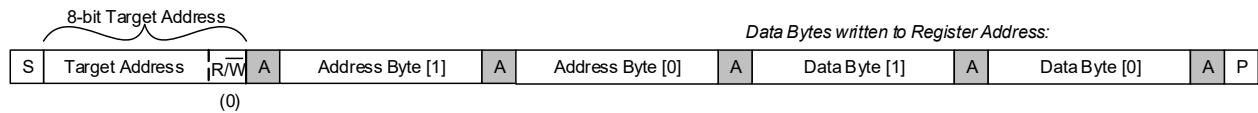

**Figure 4-20. Single-Register Write to Specified Address**

Fig. 4-21 shows a single register read from a specified address.

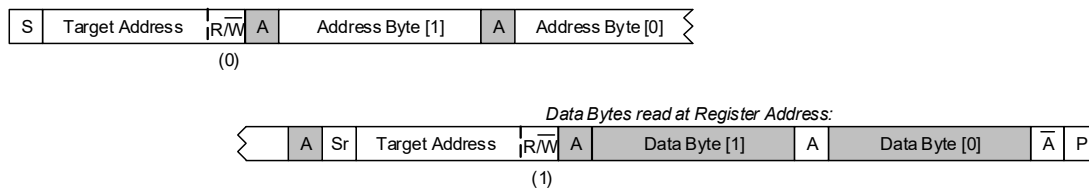

**Figure 4-21. Single-Register Read from Specified Address**

Fig. 4-22 shows a multiple register write to a specified address.

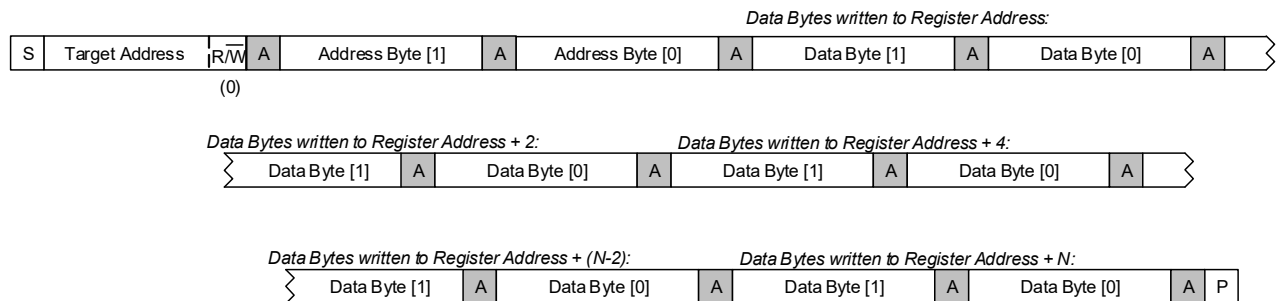
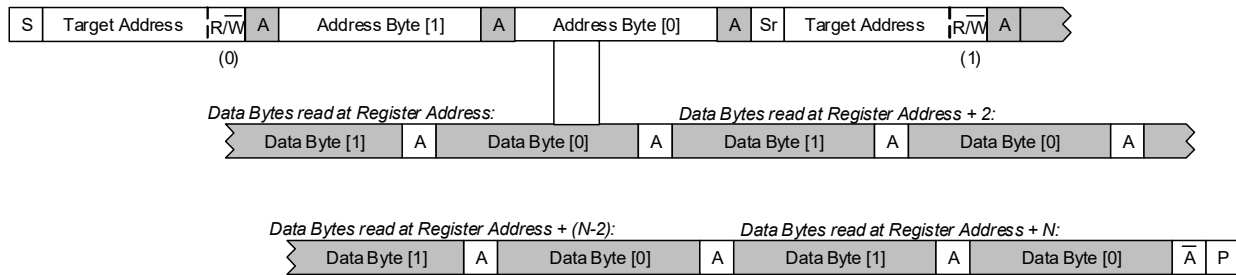

**Figure 4-22. Multiple-Register Write to Specified Address**

Fig. 4-23 shows a multiple register read from a specified address.



**Figure 4-23. Multiple-Register Read from Specified Address**

## 4.8.2 SPI Interface

The SPI interface is supported using the  $\overline{\text{SPI\_CS}}$ , SPI\_SCK, SPI\_SDI, and SPI\_SDO pins.

The SDI (data-input) pin supports the following behavior:

- In write operations ( $\overline{\text{R/W}} = 0$ ), the SDI pin input is driven by the controlling device.
- In read operations ( $\overline{\text{R/W}} = 1$ ), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

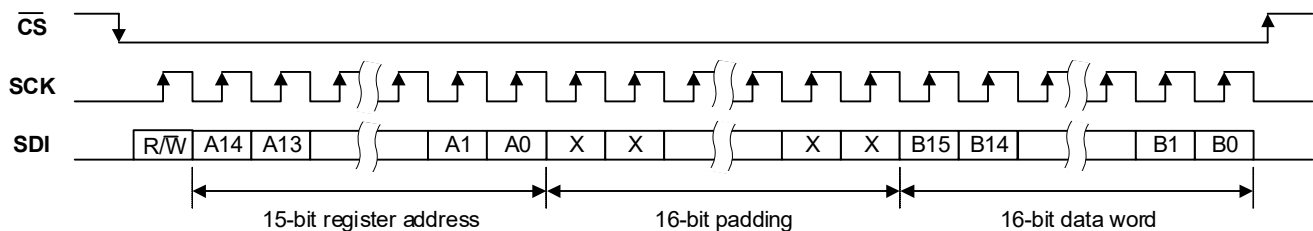
- If  $\overline{\text{CS}}$  is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If  $\overline{\text{CS}}$  is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-13 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. Note that the full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-24 and Fig. 4-25).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS5302P automatically increments the register address at the end of each data word, for as long as  $\overline{\text{CS}}$  is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

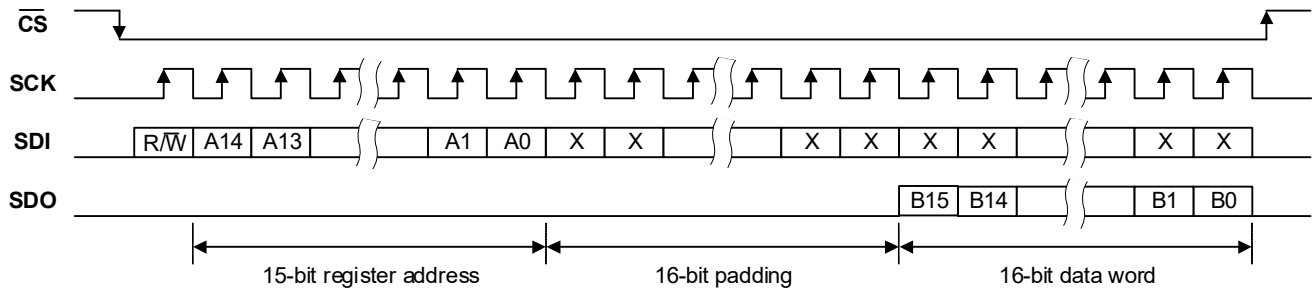
The SPI protocol is shown in Fig. 4-24 and Fig. 4-25.

Fig. 4-24 shows a single register write to a specified address.



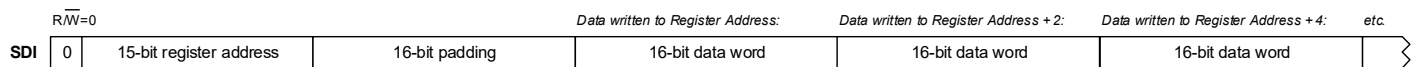
**Figure 4-24. Control Interface SPI Register Write**

Fig. 4-25 shows a single register read from a specified address.



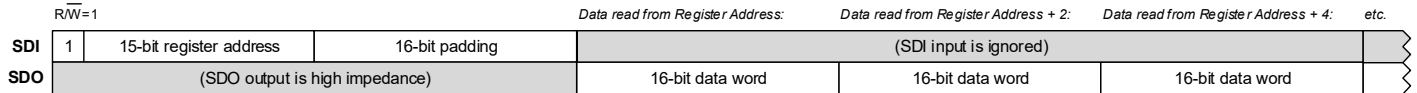
**Figure 4-25. Control Interface SPI Register Read**

Fig. 4-26 shows a multiple register write to a specified address.



**Figure 4-26. Multiple-Register Write to Specified Address**

Fig. 4-27 shows a multiple register read from a specified address.



**Figure 4-27. Multiple-Register Read from Specified Address**

## 4.9 General-Purpose Output

The CS5302P supports general-purpose outputs on selected digital I/O pins. General-purpose (GP) outputs can be used to provide hardware control signals to other devices.

The general-purpose outputs are multiplexed with other pin functions (e.g., hybrid gain control, I<sup>2</sup>C/SPI control port, or the audio serial port). Note that care must be taken not to configure a pin for GP output if the shared pin function is required.

Each pin is configured for GP output by setting the respective `_FN` bit as noted in [Table 4-14](#). If a pin is configured for GP output, the logic output level is selected using the respective `_LVL` bit.

**Table 4-14. General Purpose Output**

| Pin Name        | Power Supply <sup>1</sup> | Pin Function Select          | Output Level Select           | Notes                                                                                                                        |
|-----------------|---------------------------|------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| CONFIG5         | VDD_A                     | <a href="#">CONFIG5_FN</a>   | <a href="#">CONFIG5_LVL</a>   | GP output is not supported if the I2C control port (see <a href="#">Section 4.8.1</a> ) is used.                             |
| CONFIG4/HGC_CS  | VDD_A                     | <a href="#">CONFIG4_FN</a>   | <a href="#">CONFIG4_LVL</a>   | GP output is not supported if hybrid gain control (see <a href="#">Section 4.5.4</a> ) is used.                              |
| CONFIG3/HGC_SDO | VDD_A                     | <a href="#">CONFIG3_FN</a>   | <a href="#">CONFIG3_LVL</a>   |                                                                                                                              |
| CONFIG2/HGC_SCK | VDD_A                     | <a href="#">CONFIG2_FN</a>   | <a href="#">CONFIG2_LVL</a>   |                                                                                                                              |
| SPI_SCK         | VDD_IO                    | <a href="#">SPI_SCK_FN</a>   | <a href="#">SPI_SCK_LVL</a>   | GP output is not supported if the SPI control port (see <a href="#">Section 4.8.2</a> ) is used.                             |
| SPI_CS          | VDD_IO                    | <a href="#">SPI_CS_FN</a>    | <a href="#">SPI_CS_LVL</a>    |                                                                                                                              |
| ASP_DOUT2       | VDD_IO                    | <a href="#">ASP_DOUT2_FN</a> | <a href="#">ASP_DOUT2_LVL</a> | GP output is not supported if the ASP (see <a href="#">Section 4.7</a> ) is configured for 705.6 kHz or 768 kHz sample rate. |

1. The digital I/O logic levels for each pin are defined with respect to the applicable power supply. See [Table 3-8](#) for details.

## 4.10 Device ID

The device ID, and other associated data, can be read from the control fields listed in [Table 4-15](#).

**Table 4-15. Device ID**

| Label    | Description                 |
|----------|-----------------------------|
| DEVID    | Device ID                   |
| AREVID   | All-layer device revision   |
| MTLREVID | Metal-layer device revision |

## 5 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS5302P.

- The register field default values are established upon the deassertion of the **RESET** pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access
  Read-only access
  Write-only access

**Table 5-1. Block Base Addresses**

| Base Address | Block Name         | Register Quick Reference    | Register Description Reference |
|--------------|--------------------|-----------------------------|--------------------------------|
| 0x0000 0000  | <b>DEVID</b>       | <a href="#">Section 5.1</a> | <a href="#">Section 6.1</a>    |
| 0x0000 0040  | <b>CONFIG</b>      | <a href="#">Section 5.2</a> | <a href="#">Section 6.2</a>    |
| 0x0000 0080  | <b>INPUT_PATH</b>  | <a href="#">Section 5.3</a> | <a href="#">Section 6.3</a>    |
| 0x0000 2000  | <b>HGC</b>         | <a href="#">Section 5.4</a> | <a href="#">Section 6.4</a>    |
| 0x0000 3D00  | <b>PIN_CONFIG</b>  | <a href="#">Section 5.5</a> | <a href="#">Section 6.5</a>    |
| 0x0000 3E00  | <b>CLIP_DETECT</b> | <a href="#">Section 5.6</a> | <a href="#">Section 6.6</a>    |

### 5.1 DEVID

| Address                              | Register | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
|--------------------------------------|----------|----------|----|----|----|----|----|---|---|--------|---|---|---|----------|---|---|---|
| 0x0000 0000<br><a href="#">p. 44</a> | DEVID    | DEVID    |    |    |    |    |    |   |   |        |   |   |   |          |   |   |   |
|                                      |          | 0        | 1  | 0  | 1  | 0  | 0  | 1 | 1 | 0      | 0 | 0 | 0 | 0        | 0 | 1 | 0 |
| 0x0000 0004<br><a href="#">p. 44</a> | REVID    | —        |    |    |    |    |    |   |   | AREVID |   |   |   | MTLREVID |   |   |   |
|                                      |          | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 1      | 0 | 1 | 1 | 0        | 0 | 0 | 0 |
| 0x0000 0022<br><a href="#">p. 44</a> | SW_RESET | SW_RESET |    |    |    |    |    |   |   | —      |   |   |   |          |   |   |   |
|                                      |          | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0      | 0 | 0 | 0 | 0        | 0 | 0 | 0 |

### 5.2 CONFIG

| Address                              | Register        | 15 | 14 | 13 | 12         | 11 | 10 | 9              | 8 | 7            | 6               | 5            | 4 | 3           | 2          | 1              | 0 |
|--------------------------------------|-----------------|----|----|----|------------|----|----|----------------|---|--------------|-----------------|--------------|---|-------------|------------|----------------|---|
| 0x0000 0040<br><a href="#">p. 45</a> | CLK_CFG_0       | —  |    |    | SYSCLK_SRC | —  |    |                |   |              | PLL_REFCLK_FREQ |              | — |             |            | PLL_REFCLK_SRC |   |
|                                      |                 | 0  | 0  | 0  | 0          | 0  | 0  | 0              | 0 | 0            | 0               | 1            | 1 | 0           | 0          | 0              | 0 |
| 0x0000 0042<br><a href="#">p. 45</a> | CLK_CFG_1       | —  |    |    |            |    |    |                |   |              |                 |              |   | SAMPLE_RATE |            |                |   |
|                                      |                 | 0  | 0  | 0  | 0          | 0  | 0  | 0              | 0 | 0            | 0               | 0            | 0 | 0           | 0          | 1              | 0 |
| 0x0000 0044<br><a href="#">p. 45</a> | CHIP_ENABLE     | —  |    |    |            |    |    |                |   |              |                 |              |   |             |            |                |   |
|                                      |                 | 0  | 0  | 0  | 0          | 0  | 0  | 0              | 0 | 0            | 0               | 0            | 0 | 0           | 0          | 0              | 0 |
| 0x0000 0048<br><a href="#">p. 46</a> | ASP_CFG         | —  |    |    |            |    |    |                |   | ASP_BCLK_INV |                 | ASP_PRIMARY  | — |             |            | ASP_BCLK_FREQ  |   |
|                                      |                 | 0  | 0  | 0  | 0          | 0  | 0  | 0              | 0 | 0            | 0               | 0            | 0 | 0           | 0          | 0              | 0 |
| 0x0000 0050<br><a href="#">p. 46</a> | SIGNAL_PATH_CFG | —  |    |    |            |    |    | ASP_CH_REVERSE | — |              |                 | ASP_TDM_SLOT |   |             | ASP_FORMAT |                |   |
|                                      |                 | 0  | 0  | 0  | 0          | 0  | 0  | 0              | 0 | 0            | 0               | 0            | 0 | 0           | 0          | 0              | 0 |

## 5.3 INPUT\_PATH

| Address                              | Register       | 15       | 14 | 13 | 12        | 11             | 10 | 9             | 8 | 7       | 6                | 5 | 4 | 3 | 2                | 1          | 0          |
|--------------------------------------|----------------|----------|----|----|-----------|----------------|----|---------------|---|---------|------------------|---|---|---|------------------|------------|------------|
| 0x0000 0080<br><a href="#">p. 47</a> | IN_ENABLES     | —        |    |    |           |                |    |               |   |         |                  |   |   |   |                  | IN2_ADC_EN | IN1_ADC_EN |
|                                      |                | 0        | 0  | 0  | 0         | 0              | 0  | 0             | 0 | 0       | 0                | 0 | 0 | 0 | 0                | 0          | 0          |
| 0x0000 0082<br><a href="#">p. 47</a> | IN_RAMP_SUM    | —        |    |    |           | IN_CLIP_THRESH |    |               |   | —       | IN_RAMP_RATE_DEC |   |   | — | IN_RAMP_RATE_INC |            |            |
|                                      |                | 0        | 0  | 0  | 0         | 0              | 0  | 0             | 0 | 0       | 0                | 1 | 0 | 0 | 0                | 1          | 0          |
| 0x0000 0086<br><a href="#">p. 47</a> | IN_FILTER      | —        |    |    | IN_HPF_EN | —              |    | IN_FILTER_SEL |   | —       |                  |   |   |   |                  |            |            |
|                                      |                | 0        | 0  | 0  | 0         | 0              | 0  | 0             | 0 | 0       | 0                | 0 | 0 | 0 | 0                | 0          | 0          |
| 0x0000 008A<br><a href="#">p. 48</a> | IN_INV         | —        |    |    |           |                |    |               |   |         |                  |   |   |   |                  | IN2_INV    | IN1_INV    |
|                                      |                | 0        | 0  | 0  | 0         | 0              | 0  | 0             | 0 | 0       | 0                | 0 | 0 | 0 | 0                | 0          | 0          |
| 0x0000 0090<br><a href="#">p. 48</a> | IN_VOL_CTRL1_0 | IN1_MUTE | —  |    |           |                |    |               |   | IN1_VOL |                  |   |   |   |                  |            |            |
|                                      |                | 1        | 0  | 0  | 0         | 0              | 0  | 0             | 0 | 0       | 0                | 0 | 0 | 0 | 0                | 0          | 0          |
| 0x0000 0092<br><a href="#">p. 48</a> | IN_VOL_CTRL1_1 | IN2_MUTE | —  |    |           |                |    |               |   | IN2_VOL |                  |   |   |   |                  |            |            |
|                                      |                | 1        | 0  | 0  | 0         | 0              | 0  | 0             | 0 | 0       | 0                | 0 | 0 | 0 | 0                | 0          | 0          |
| 0x0000 00A0<br><a href="#">p. 49</a> | IN_VOL_CTRL5   | —        |    |    |           |                |    |               |   |         |                  |   |   |   |                  | IN_VU      |            |
|                                      |                | 0        | 0  | 0  | 0         | 0              | 0  | 0             | 0 | 0       | 0                | 0 | 0 | 0 | 0                | 0          | 0          |

## 5.4 HGC

| Address                              | Register   | 15           | 14 | 13 | 12           | 11          | 10 | 9 | 8 | 7             | 6 | 5 | 4                   | 3             | 2          | 1            | 0            |  |
|--------------------------------------|------------|--------------|----|----|--------------|-------------|----|---|---|---------------|---|---|---------------------|---------------|------------|--------------|--------------|--|
| 0x0000 2000<br><a href="#">p. 49</a> | CONTROL    | —            |    |    |              |             |    |   |   |               |   |   | ABORT               | —             |            |              | INIT_UPDATE  |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 0 | 0 | 0             | 0 | 0 | 0                   | 0             | 0          | 0            | 0            |  |
| 0x0000 2004<br><a href="#">p. 49</a> | STATUS     | —            |    |    |              |             |    |   |   |               |   |   |                     |               |            |              | BUSY_STS     |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 0 | 0 | 0             | 0 | 0 | 0                   | 0             | 0          | 0            | 0            |  |
| 0x0000 2010<br><a href="#">p. 49</a> | GEN_CONFIG | —            |    |    |              |             |    |   |   |               |   |   | STEP_RAMP_EN        | —             | ZC_TIMEOUT |              |              |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 0 | 0 | 0             | 0 | 0 | 1                   | 0             | 1          | 1            | 1            |  |
| 0x0000 2014<br><a href="#">p. 50</a> | PATH_DELAY | TM_DELAY     |    |    |              |             |    |   |   | DIG_VOL_DELAY |   |   |                     |               |            |              |              |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 1 | 1 | 0             | 0 | 0 | 0                   | 0             | 1          | 0            | 0            |  |
| 0x0000 2018<br><a href="#">p. 50</a> | TM         | TM_HOLD_TIME |    |    |              |             |    |   |   | —             |   |   |                     |               |            |              | TM_EN        |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 1  | 1 | 1 | 0             | 0 | 0 | 0                   | 0             | 0          | 0            | 0            |  |
| 0x0000 201C<br><a href="#">p. 50</a> | TM_LD_0    | —            |    |    |              |             |    |   |   |               |   |   |                     |               |            | CH2_TM_LD_EN | CH1_TM_LD_EN |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 0 | 0 | 1             | 1 | 1 | 1                   | 1             | 1          | 1            | 1            |  |
| 0x0000 201E<br><a href="#">p. 51</a> | TM_LD_1    | —            |    |    | TM_LD_THRESH |             |    |   |   | —             |   |   | TM_LD_TIME          |               |            |              |              |  |
|                                      |            | 0            | 0  | 0  | 0            | 1           | 0  | 0 | 1 | 0             | 0 | 0 | 0                   | 1             | 1          | 0            | 0            |  |
| 0x0000 2020<br><a href="#">p. 51</a> | SPI_0      | —            |    |    |              |             |    |   |   | SCK_DIV       |   |   |                     | —             |            | CPHA         | CPOL         |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 0 | 0 | 0             | 0 | 0 | 0                   | 0             | 0          | 0            | 0            |  |
| 0x0000 2022<br><a href="#">p. 52</a> | SPI_1      | —            |    |    |              | CS_IDLE_DUR |    |   |   | CS_RISE_DELAY |   |   |                     | CS_FALL_DELAY |            |              |              |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 0 | 0 | 0             | 0 | 0 | 0                   | 0             | 0          | 0            | 0            |  |
| 0x0000 2030<br><a href="#">p. 52</a> | CH1_CONFIG | —            |    |    |              |             |    |   |   |               |   |   | CH1_BIT_PATT_LENGTH |               |            |              |              |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 0 | 0 | 0             | 0 | 0 | 0                   | 0             | 0          | 0            | 0            |  |
| 0x0000 2034<br><a href="#">p. 53</a> | CH2_CONFIG | —            |    |    |              |             |    |   |   |               |   |   | CH2_BIT_PATT_LENGTH |               |            |              |              |  |
|                                      |            | 0            | 0  | 0  | 0            | 0           | 0  | 0 | 0 | 0             | 0 | 0 | 0                   | 0             | 0          | 0            | 0            |  |

| Address                              | Register        | 15              | 14 | 13 | 12 | 11 | 10          | 9 | 8 | 7           | 6 | 5                    | 4 | 3 | 2 | 1 | 0 |
|--------------------------------------|-----------------|-----------------|----|----|----|----|-------------|---|---|-------------|---|----------------------|---|---|---|---|---|
| 0x0000 2050<br><a href="#">p. 53</a> | AUX1_CONFIG     | —               |    |    |    |    |             |   |   |             |   | AUX1_BIT_PATT_LENGTH |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2054<br><a href="#">p. 53</a> | AUX2_CONFIG     | —               |    |    |    |    |             |   |   |             |   | AUX2_BIT_PATT_LENGTH |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2060<br><a href="#">p. 53</a> | CH1_BIT_PATT_0  | CH1_BIT_PATT_0  |    |    |    |    |             |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2062<br><a href="#">p. 53</a> | CH1_BIT_PATT_1  | CH1_BIT_PATT_1  |    |    |    |    |             |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2064<br><a href="#">p. 54</a> | CH1_VOL_0       | —               |    |    |    |    | CH1_ANA_VOL |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2066<br><a href="#">p. 54</a> | CH1_VOL_1       | CH1<br>UPDATE   | —  |    |    |    |             |   |   | CH1_DIG_VOL |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2068<br><a href="#">p. 54</a> | CH2_BIT_PATT_0  | CH2_BIT_PATT_0  |    |    |    |    |             |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 206A<br><a href="#">p. 54</a> | CH2_BIT_PATT_1  | CH2_BIT_PATT_1  |    |    |    |    |             |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 206C<br><a href="#">p. 55</a> | CH2_VOL_0       | —               |    |    |    |    | CH2_ANA_VOL |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 206E<br><a href="#">p. 55</a> | CH2_VOL_1       | CH2<br>UPDATE   | —  |    |    |    |             |   |   | CH2_DIG_VOL |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 20A0<br><a href="#">p. 55</a> | AUX1_BIT_PATT_0 | AUX1_BIT_PATT_0 |    |    |    |    |             |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 20A2<br><a href="#">p. 55</a> | AUX1_BIT_PATT_1 | AUX1_BIT_PATT_1 |    |    |    |    |             |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 20A4<br><a href="#">p. 56</a> | AUX2_BIT_PATT_0 | AUX2_BIT_PATT_0 |    |    |    |    |             |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |
| 0x0000 20A6<br><a href="#">p. 56</a> | AUX2_BIT_PATT_1 | AUX2_BIT_PATT_1 |    |    |    |    |             |   |   |             |   |                      |   |   |   |   |   |
|                                      |                 | 0               | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0           | 0 | 0                    | 0 | 0 | 0 | 0 | 0 |

## 5.5 PIN\_CONFIG

| Address                  | Register    | 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8           | 7           | 6               | 5               | 4               | 3          | 2              | 1 | 0             |                   |
|--------------------------|-------------|-------------|----|----|----|----|----|-------------|-------------|-------------|-----------------|-----------------|-----------------|------------|----------------|---|---------------|-------------------|
| 0x0000 3D1C<br><br>p. 56 | PAD_CLIP    | CLIP_OP_CFG | —  |    |    |    |    |             |             |             | CONFIG4_CLIP_EN | CONFIG3_CLIP_EN | CONFIG2_CLIP_EN | —          | SPI_CS_CLIP_EN | — |               | ASP_DOUT2_CLIP_EN |
|                          |             | 0           | 0  | 0  | 0  | 0  | 0  | 0           | 0           | 0           | 0               | 0               | 0               | 0          | 0              | 0 | 0             |                   |
| 0x0000 3D20<br><br>p. 57 | PAD_HGC_SPI | —           |    |    |    |    |    |             |             |             |                 |                 |                 |            |                |   | HGC_SPI_EN    |                   |
|                          |             | 0           | 0  | 0  | 0  | 0  | 0  | 0           | 0           | 0           | 0               | 0               | 0               | 0          | 0              | 0 | 0             |                   |
| 0x0000 3D24<br><br>p. 57 | PAD_FN      | —           |    |    |    |    |    | CONFIG5_FN  | CONFIG4_FN  | CONFIG3_FN  | CONFIG2_FN      | —               | SPI_SCK_FN      | SPI_CS_FN  | —              |   | ASP_DOUT2_FN  |                   |
|                          |             | 0           | 0  | 0  | 0  | 0  | 0  | 0           | 0           | 0           | 0               | 0               | 0               | 0          | 0              | 0 | 0             |                   |
| 0x0000 3D28<br><br>p. 57 | PAD_LVL     | —           |    |    |    |    |    | CONFIG5_LVL | CONFIG4_LVL | CONFIG3_LVL | CONFIG2_LVL     | —               | SPI_SCK_LVL     | SPI_CS_LVL | —              |   | ASP_DOUT2_LVL |                   |
|                          |             | 0           | 0  | 0  | 0  | 0  | 0  | 0           | 0           | 0           | 0               | 0               | 0               | 0          | 0              | 0 | 0             |                   |

## 5.6 CLIP\_DETECT

| Address               | Register  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2                   | 1                   | 0 |
|-----------------------|-----------|----|----|----|----|----|----|---|---|---|---|---|---|---|---------------------|---------------------|---|
| 0x0000 3E1C           | CLIP_WARN | —  |    |    |    |    |    |   |   |   |   |   |   |   | IN2<br>CLIP<br>WARN | IN1<br>CLIP<br>WARN | — |
| <a href="#">p. 58</a> |           | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0                   | 0 |

## 6 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS5302P.

- The register field default values are established upon the deassertion of the  $\overline{\text{RESET}}$  pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

☐ Read/write access     
 ☐ Read-only access     
 ☐ Write-only access

### 6.1 DEVID

#### 6.1.1 DEVID

Address: 0x0000 0000

|         |       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|-------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RO      | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | DEVID |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0     | 1  | 0  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Bits | Name  | Description                                                                                                                |
|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DEVID | This register indicates the Device ID CS5302P.<br>0x0000–0x5301 = Reserved<br>0x5302 = CS5302P<br>0x5303–0xFFFF = Reserved |

#### 6.1.2 REVID

Address: 0x0000 0004

|         |        |        |   |   |   |          |   |   |   |
|---------|--------|--------|---|---|---|----------|---|---|---|
| RO      | 15...8 | 7      | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
|         | —      | AREVID |   |   |   | MTLREVID |   |   |   |
| Default | 0x00   | 1      | 0 | 1 | 1 | 0        | 0 | 0 | 0 |

| Bits | Name     | Description                                                                                                                                         |
|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | —        | Reserved                                                                                                                                            |
| 7:4  | AREVID   | This field indicates the all-layer device revision.<br>0x0–0x9 = Reserved<br>0xA = Revision Ax<br>0xB = (Default) Revision Bx<br>0xC–0xF = Reserved |
| 3:0  | MTLREVID | This field indicates the metal-layer device revision.<br>0x0 = (Default) Revision x0<br>0x1–0xF = Reserved                                          |

#### 6.1.3 SW\_RESET

Address: 0x0000 0022

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| WO      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | SW_RESET |    |    |    |    |    |   |   | — |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description                                                                                                                                           |
|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | SW_RESET | Software Reset. Writing 0x5A triggers a reset.<br>0x00 = (Default) No action<br>0x01–0x59 = Reserved<br>0x5A = Software reset<br>0x5B–0xFF = Reserved |
| 7:0  | —        | Reserved                                                                                                                                              |

## 6.2 CONFIG

### 6.2.1 CLK\_CFG\_0

**Address: 0x0000 0040**

| RW      | 15 | 14 | 13 | 12         | 11 | 10 | 9 | 8 | 7 | 6 | 5               | 4 | 3 | 2 | 1 | 0              |
|---------|----|----|----|------------|----|----|---|---|---|---|-----------------|---|---|---|---|----------------|
|         | —  |    |    | SYSCLK_SRC | —  |    |   |   |   |   | PLL_REFCLK_FREQ |   | — |   |   | PLL_REFCLK_SRC |
| Default | 0  | 0  | 0  | 0          | 0  | 0  | 0 | 0 | 0 | 0 | 1               | 1 | 0 | 0 | 0 | 0              |

| Bits  | Name            | Description                                                                                                                                                                                                              |
|-------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | —               | Reserved                                                                                                                                                                                                                 |
| 12    | SYSCLK_SRC      | System clock source. If MCLK is selected, the PLL is bypassed.<br>0 = (Default) MCLK<br>1 = PLL                                                                                                                          |
| 11:6  | —               | Reserved                                                                                                                                                                                                                 |
| 5:4   | PLL_REFCLK_FREQ | PLL reference clock frequency. The selection must match the frequency of the selected input reference.<br>00 = 3.072/2.8224 MHz<br>01 = 6.144/5.6448 MHz<br>10 = 12.288/11.2896 MHz<br>11 = (Default) 24.576/22.5792 MHz |
| 3:1   | —               | Reserved                                                                                                                                                                                                                 |
| 0     | PLL_REFCLK_SRC  | PLL reference clock source. Note the BCLK reference is only valid in ASP Secondary Mode.<br>0 = (Default) BCLK<br>1 = MCLK                                                                                               |

### 6.2.2 CLK\_CFG\_1

**Address: 0x0000 0042**

| RW      | 15...8 | 7 | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
|---------|--------|---|---|---|---|-------------|---|---|---|
|         | —      | — |   |   |   | SAMPLE_RATE |   |   |   |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0           | 0 | 0 | 1 |

| Bits | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | —           | Reserved                                                                                                                                                                                                                                                                                                                                                                                            |
| 2:0  | SAMPLE_RATE | Audio sample frequency. Note the sample rate must be integer-related to the system clock frequency. Auto-detect is only valid if sample rate = 32-192kHz, clock reference = MCLK, and the ASP is in Secondary Mode.<br>000 = 32 kHz<br>001 = (Default) 48/44.1 kHz<br>010 = 96/88.2 kHz<br>011 = 192/176.4 kHz<br>100 = 384/356.8 kHz<br>101 = 768/705.6 kHz<br>110 = Auto-detect<br>111 = Reserved |

### 6.2.3 CHIP\_ENABLE

**Address: 0x0000 0044**

| RW      | 15...8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
|---------|--------|---|---|---|---|---|---|---|-----------|
|         | —      | — |   |   |   |   |   |   | GLOBAL_EN |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         |

| Bits | Name      | Description                                                                                                                                                                                                                                                                       |
|------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:1 | —         | Reserved                                                                                                                                                                                                                                                                          |
| 0    | GLOBAL_EN | Global enable. Set to 1 to configure and enable all functions. Clear to 0 to disable. Note the clocking and ASP control registers are only valid on the rising edge of GLOBAL_EN. It is recommended to select the disabled state (GLOBAL_EN=0) before writing to these registers. |

## 6.2.4 ASP\_CFG

**Address: 0x0000 0048**

|         |        |   |              |             |   |   |   |               |   |
|---------|--------|---|--------------|-------------|---|---|---|---------------|---|
| RW      | 15...8 | 7 | 6            | 5           | 4 | 3 | 2 | 1             | 0 |
|         | —      | — | ASP_BCLK_INV | ASP_PRIMARY | — | — | — | ASP_BCLK_FREQ | — |
| Default | 0x00   | 0 | 0            | 0           | 0 | 0 | 0 | 0             | 0 |

| Bits | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | —             | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 6    | ASP_BCLK_INV  | ASP BCLK polarity. Selects the valid BCLK edge for data sampling.<br>In non-inverted mode, data is valid on BCLK rising edge. Data is driven on BCLK falling edge (half-cycle mode) or rising edge (full-cycle mode).<br>In inverted mode, data is valid on BCLK falling edge. Data is driven on BCLK rising edge (half-cycle mode) or falling edge (full-cycle mode).<br>0 = (Default) Non-inverted<br>1 = Inverted                                                                                    |
| 5    | ASP_PRIMARY   | ASP Primary/Secondary Mode select. In ASP Primary Mode, BCLK and FSYNC are outputs. In ASP Secondary Mode, BCLK and FSYNC are inputs.<br>0 = (Default) Secondary Mode<br>1 = Primary Mode                                                                                                                                                                                                                                                                                                               |
| 4:2  | —             | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 1:0  | ASP_BCLK_FREQ | ASP BCLK frequency. The BCLK frequency must be high enough to support the required number of data bits at the selected sample rate. Only valid in ASP Primary Mode.<br>Note the BCLK frequency is integer-related to the system clock frequency i.e., multiples of 3.072 MHz for 12.288 / 24.576 MHz system clock, or multiples of 2.8224 MHz for 11.2896 / 22.5792 MHz system clock.<br>00 = (Default) 3.072/2.8224 MHz<br>01 = 6.144/5.6448 MHz<br>10 = 12.288/11.2896 MHz<br>11 = 24.576/22.5792 MHz |

## 6.2.5 SIGNAL\_PATH\_CFG

**Address: 0x0000 0050**

|         |    |    |    |    |    |    |                |   |   |   |   |              |   |   |            |   |
|---------|----|----|----|----|----|----|----------------|---|---|---|---|--------------|---|---|------------|---|
| RW      | 15 | 14 | 13 | 12 | 11 | 10 | 9              | 8 | 7 | 6 | 5 | 4            | 3 | 2 | 1          | 0 |
|         | —  | —  | —  | —  | —  | —  | ASP_CH_REVERSE | — | — | — | — | ASP_TDM_SLOT | — | — | ASP_FORMAT | — |
| Default | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0 | 0 | 0 | 0 | 0            | 0 | 0 | 0          | 0 |

| Bits  | Name           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | —              | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 9     | ASP_CH_REVERSE | ASP channel-ordering reversal. Selects normal- or reverse-order ASP data format.<br>0 = (Default) Normal<br>1 = Reverse                                                                                                                                                                                                                                                                                                                                                                             |
| 8:6   | —              | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 5:3   | ASP_TDM_SLOT   | TDM slot select. Configures which TDM slots are used in TDM maximum-time-slots mode.<br>000 = (Default) Slots 0-1<br>001 = Slots 2-3<br>010 = Slots 4-5<br>011 = Slots 6-7<br>100 = Slots 8-9<br>101 = Slots 10-11<br>110 = Slots 12-13<br>111 = Slots 14-15                                                                                                                                                                                                                                        |
| 2:0   | ASP_FORMAT     | ASP data format. Selects how the audio samples are arranged within the FSYNC frame.<br>In TDM Maximum Time Slots Full-Cycle Mode, data is driven on same edge as sampling edge.<br>In TDM Maximum Time Slots Half-Cycle Mode, data is driven on opposite edge to sampling edge.<br>000 = (Default) I2S Mode<br>001 = Left-Justified Mode<br>010–100 = Reserved<br>101 = TDM Maximum Time Slots Full-Cycle Mode<br>110 = TDM Maximum Time Slots Half-Cycle Mode<br>111 = TDM Minimum Time Slots Mode |

## 6.3 INPUT\_PATH

### 6.3.1 IN\_ENABLES

**Address: 0x0000 0080**

|         |        |   |   |   |   |   |   |            |            |
|---------|--------|---|---|---|---|---|---|------------|------------|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3 | 2 | 1          | 0          |
|         | —      |   |   |   | — |   |   | IN2_ADC_EN | IN1_ADC_EN |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0          |

| Bits | Name       | Description                                                |
|------|------------|------------------------------------------------------------|
| 15:2 | —          | Reserved                                                   |
| 1    | IN2_ADC_EN | Channel 2 enable.<br>0 = (Default) Disabled<br>1 = Enabled |
| 0    | IN1_ADC_EN | Channel 1 enable.<br>0 = (Default) Disabled<br>1 = Enabled |

### 6.3.2 IN\_RAMP\_SUM

**Address: 0x0000 0082**

|         |    |    |    |    |    |    |   |                |   |   |   |                  |   |   |   |                  |
|---------|----|----|----|----|----|----|---|----------------|---|---|---|------------------|---|---|---|------------------|
| RW      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8              | 7 | 6 | 5 | 4                | 3 | 2 | 1 | 0                |
|         |    | —  |    |    |    |    |   | IN_CLIP_THRESH | — |   |   | IN_RAMP_RATE_DEC | — |   |   | IN_RAMP_RATE_INC |
| Default | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0              | 0 | 0 | 1 | 0                | 0 | 0 | 1 | 0                |

| Bits  | Name             | Description                                                                                                                                                                                                                                                                             |
|-------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | —                | Reserved                                                                                                                                                                                                                                                                                |
| 11:8  | IN_CLIP_THRESH   | Input clip-warning threshold<br>0x0 = (Default) 0.0 dBFS<br>0x1 = -0.125 dBFS<br>0x2 = -0.25 dBFS<br>0x3 = -0.5 dBFS<br>0x4 = -1.0 dBFS<br>0x5 = -3.0 dBFS<br>0x6 = -6.0 dBFS<br>0x7–0xF = Reserved                                                                                     |
| 7     | —                | Reserved                                                                                                                                                                                                                                                                                |
| 6:4   | IN_RAMP_RATE_DEC | Volume Decrease Ramp Rate (ms/6 dB), used for gain changes including HGC operations. This field should not be changed while a volume ramp is in progress.<br>000 = 0 ms<br>001 = 0.5 ms<br>010 = (Default) 1 ms<br>011 = 2 ms<br>100 = 4 ms<br>101 = 8 ms<br>110 = 15 ms<br>111 = 30 ms |
| 3     | —                | Reserved                                                                                                                                                                                                                                                                                |
| 2:0   | IN_RAMP_RATE_INC | Volume Increase Ramp Rate (ms/6 dB), used for gain changes including HGC operations. This field should not be changed while a volume ramp is in progress.<br>000 = 0 ms<br>001 = 0.5 ms<br>010 = (Default) 1 ms<br>011 = 2 ms<br>100 = 4 ms<br>101 = 8 ms<br>110 = 15 ms<br>111 = 30 ms |

### 6.3.3 IN\_FILTER

**Address: 0x0000 0086**

|         |    |    |    |           |    |    |   |               |   |   |   |   |   |   |   |   |
|---------|----|----|----|-----------|----|----|---|---------------|---|---|---|---|---|---|---|---|
| RW      | 15 | 14 | 13 | 12        | 11 | 10 | 9 | 8             | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         |    | —  |    | IN_HPF_EN |    | —  |   | IN_FILTER_SEL |   |   |   |   | — |   |   |   |
| Default | 0  | 0  | 0  | 0         | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits  | Name      | Description                                                               |
|-------|-----------|---------------------------------------------------------------------------|
| 15:13 | —         | Reserved                                                                  |
| 12    | IN_HPF_EN | High-pass filter enable.<br>0 = (Default) HPF disabled<br>1 = HPF enabled |
| 11:10 | —         | Reserved                                                                  |

| Bits | Name          | Description                                                                                                                                                                                                                                                                                  |
|------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8  | IN_FILTER_SEL | Digital filter select. Configures the decimation filter.<br>00 = (Default) Minimum phase, slow roll-off decimation filter<br>01 = Minimum phase, fast roll-off decimation filter<br>10 = Linear phase, slow roll-off decimation filter<br>11 = Linear phase, fast roll-off decimation filter |
| 7:0  | —             | Reserved                                                                                                                                                                                                                                                                                     |

### 6.3.4 IN\_INV

**Address: 0x0000 008A**

|         |        |   |   |   |   |   |   |         |         |
|---------|--------|---|---|---|---|---|---|---------|---------|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3 | 2 | 1       | 0       |
|         | —      |   |   |   | — |   |   | IN2_INV | IN1_INV |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0 | 0 | 0       | 0       |

| Bits | Name    | Description                                                                |
|------|---------|----------------------------------------------------------------------------|
| 15:2 | —       | Reserved                                                                   |
| 1    | IN2_INV | Channel 2 ADC invert.<br>0 = (Default) No inversion<br>1 = ADC data invert |
| 0    | IN1_INV | Channel 1 ADC invert.<br>0 = (Default) No inversion<br>1 = ADC data invert |

### 6.3.5 IN\_VOL\_CTRL1\_0

**Address: 0x0000 0090**

|         |          |    |    |    |    |    |   |   |   |   |   |   |         |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---------|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3       | 2 | 1 | 0 |
|         | IN1_MUTE |    |    |    | —  |    |   |   |   |   |   |   | IN1_VOL |   |   |   |
| Default | 1        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0       | 0 | 0 | 0 |

| Bits | Name     | Description                                                                                                                       |
|------|----------|-----------------------------------------------------------------------------------------------------------------------------------|
| 15   | IN1_MUTE | Channel 1 mute.<br>0 = Unmute<br>1 = (Default) Mute                                                                               |
| 14:8 | —        | Reserved                                                                                                                          |
| 7:0  | IN1_VOL  | Channel 1 digital volume, –127.5dB to 0dB in 0.5dB steps.<br>0x00 = (Default) 0.0 dB<br>0x01 = –0.5 dB<br>...<br>0xFF = –127.5 dB |

### 6.3.6 IN\_VOL\_CTRL1\_1

**Address: 0x0000 0092**

|         |          |    |    |    |    |    |   |   |   |   |   |   |         |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---------|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3       | 2 | 1 | 0 |
|         | IN2_MUTE |    |    |    | —  |    |   |   |   |   |   |   | IN2_VOL |   |   |   |
| Default | 1        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0       | 0 | 0 | 0 |

| Bits | Name     | Description                                                                                                                       |
|------|----------|-----------------------------------------------------------------------------------------------------------------------------------|
| 15   | IN2_MUTE | Channel 2 mute.<br>0 = Unmute<br>1 = (Default) Mute                                                                               |
| 14:8 | —        | Reserved                                                                                                                          |
| 7:0  | IN2_VOL  | Channel 2 digital volume, –127.5dB to 0dB in 0.5dB steps.<br>0x00 = (Default) 0.0 dB<br>0x01 = –0.5 dB<br>...<br>0xFF = –127.5 dB |

Address: 0x0000 00A0

| Bits | Name  | Description                                                                                                                    |
|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 15:1 | —     | Reserved                                                                                                                       |
| 0    | IN_VU | Global volume update trigger<br>0 = (Default) No action<br>1 = Write 1 to trigger an update of all input volume/mute registers |

**Address: 0x0000 2000**

| Bits | Name        | Description                                                                                                                                                                                                                                              |
|------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | —           | Reserved                                                                                                                                                                                                                                                 |
| 4    | ABORT       | Abort gain updates. Write 1 to abort any pending gain updates. Note that any updates already in progress will complete as normal and are not aborted.<br>0 = (Default) No action<br>1 = Write 1 to abort gain updates                                    |
| 3:1  | —           | Reserved                                                                                                                                                                                                                                                 |
| 0    | INIT_UPDATE | Initialize gain settings. Write 1 to transmit the SPI bit patterns and initialize all gain settings. Note the zero-cross detection is not applied when initializing gain settings.<br>0 = (Default) No action<br>1 = Write 1 to initialize gain settings |

**Address: 0x0000 2004**

| Bits | Name     | Description                                                                                                       |
|------|----------|-------------------------------------------------------------------------------------------------------------------|
| 15:1 | —        | Reserved                                                                                                          |
| 0    | BUSY_STS | Busy status. Indicates gain updates are pending for one or more audio channels.<br>0 = (Default) Idle<br>1 = Busy |

**Address: 0x0000 2010**

| <b>Bits</b> | <b>Name</b>  | <b>Description</b>                                                                                                                                                 |
|-------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5        | —            | Reserved                                                                                                                                                           |
| 4           | STEP_RAMP_EN | Step ramp enable. Enables the digital gain to be used to compensate for step changes in the analog gain.<br>0 = Disabled<br>1 = (Default) Enabled                  |
| 3           | —            | Reserved                                                                                                                                                           |
| 2:0         | ZC_TIMEOUT   | Timeout for zero-cross detection.<br><br>000 = 0 (OFF)<br>001–010 = Reserved<br>011 = 1 ms<br>100 = 2 ms<br><br>101 = 5 ms<br>110 = 10 ms<br>111 = (Default) 20 ms |

#### 6.4.4 PATH\_DELAY

**Address: 0x0000 2014**

|         |          |    |    |    |    |    |   |   |               |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---------------|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | TM_DELAY |    |    |    |    |    |   |   | DIG_VOL_DELAY |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 1 | 1 | 0             | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bits | Name          | Description                                                                                                                                                                                                                                     |
|------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | TM_DELAY      | Transient masking delay. Configures the delay from the analog-gain update to the start of the transient-masking period. The delay is defined in audio sample (1/fs) units.<br>0x00 = 0 samples<br>0x01 = 1 samples<br>...<br>0xFF = 255 samples |
| 7:0  | DIG_VOL_DELAY | Digital volume update delay. Configures the delay from the analog-gain update to the digital-volume update. The delay is defined in audio sample (1/fs) units.<br>0x00 = 3 samples<br>0x01 = 4 samples<br>...<br>0xFF = 258 samples             |

#### 6.4.5 TM

**Address: 0x0000 2018**

|         |              |    |    |    |    |    |   |   |   |   |   |   |       |   |   |   |
|---------|--------------|----|----|----|----|----|---|---|---|---|---|---|-------|---|---|---|
| RW      | 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3     | 2 | 1 | 0 |
|         | TM_HOLD_TIME |    |    |    |    |    |   |   | — |   |   |   | TM_EN |   |   |   |
| Default | 0            | 0  | 0  | 0  | 0  | 1  | 1 | 1 | 0 | 0 | 0 | 0 | 0     | 0 | 0 | 0 |

| Bits | Name         | Description                                                                                                                                                                                            |
|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | TM_HOLD_TIME | Transient masking hold time. Configures the duration of the transient masking. The delay is defined in audio sample (1/fs) units.<br>0x00 = 0 samples<br>0x01 = 1 samples<br>...<br>0xFF = 255 samples |
| 7:1  | —            | Reserved                                                                                                                                                                                               |
| 0    | TM_EN        | Transient masking enable.<br>0 = (Default) Disabled<br>1 = Enabled                                                                                                                                     |

#### 6.4.6 TM\_LD\_0

**Address: 0x0000 201C**

|         |        |   |   |   |   |   |   |              |              |
|---------|--------|---|---|---|---|---|---|--------------|--------------|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3 | 2 | 1            | 0            |
|         | —      | — |   |   |   |   |   | CH2_TM_LD_EN | CH1_TM_LD_EN |
| Default | 0x00   | 1 | 1 | 1 | 1 | 1 | 1 | 1            | 1            |

| Bits | Name         | Description                                                                               |
|------|--------------|-------------------------------------------------------------------------------------------|
| 15:2 | —            | Reserved                                                                                  |
| 1    | CH2_TM_LD_EN | Channel 2 transient masking level-detect enable.<br>0 = Disabled<br>1 = (Default) Enabled |
| 0    | CH1_TM_LD_EN | Channel 1 transient masking level-detect enable.<br>0 = Disabled<br>1 = (Default) Enabled |

### 6.4.7 TM\_LD\_1

**Address: 0x0000 201E**

|         |    |    |    |              |    |    |   |   |   |   |   |            |   |   |   |   |
|---------|----|----|----|--------------|----|----|---|---|---|---|---|------------|---|---|---|---|
| RW      | 15 | 14 | 13 | 12           | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4          | 3 | 2 | 1 | 0 |
|         | —  |    |    | TM_LD_THRESH |    |    |   |   | — |   |   | TM_LD_TIME |   |   |   |   |
| Default | 0  | 0  | 0  | 0            | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 0          | 1 | 1 | 0 | 0 |

| Bits  | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | —            | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 12:8  | TM_LD_THRESH | Transient masking level-detect threshold. Transient masking is applied if the signal level is below the threshold. Signal levels listed are the approximate RMS level of a sine wave that would be detected as just above the threshold.<br><div><div>0x00–0x02 = Reserved</div><div>0x03 = –20 dBFS</div><div>0x04 = –26 dBFS</div><div>0x05 = –32 dBFS</div><div>0x06 = –38 dBFS</div><div>...</div><div>0x09 = (Default) –56 dBFS</div><div>...</div></div> <div><div>0x0E = –86 dBFS</div><div>0x0F = –92 dBFS</div><div>0x10 = –98 dBFS</div><div>0x11 = –104 dBFS</div><div>0x12 = –110 dBFS</div><div>0x13 = –116 dBFS</div><div>0x14–0x1F = Reserved</div></div> |
| 7:5   | —            | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 4:0   | TM_LD_TIME   | Transient masking level-detect time constant. The time constant is defined in audio sample (1/fs) units.<br><div><div>0x00–0x09 = Reserved</div><div>0x0A = 1024 samples</div><div>0x0B = 2048 samples</div><div>0x0C = (Default) 4096 samples</div><div>0x0D = 8192 samples</div></div> <div><div>0x0E = 16384 samples</div><div>0x0F = 32768 samples</div><div>0x10 = 65536 samples</div><div>0x11–0x1F = Reserved</div></div>                                                                                                                                                                                                                                         |

### 6.4.8 SPI\_0

**Address: 0x0000 2020**

|         |        |   |   |   |         |   |   |      |      |
|---------|--------|---|---|---|---------|---|---|------|------|
| RW      | 15...8 | 7 | 6 | 5 | 4       | 3 | 2 | 1    | 0    |
|         | —      |   |   |   | SCK_DIV |   | — | CPHA | CPOL |
| Default | 0x00   | 0 | 0 | 0 | 0       | 0 | 0 | 0    | 0    |

| Bits | Name    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | —       | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7:4  | SCK_DIV | SPI clock divider. Configures the SPI clock frequency as a division of the system clock frequency.<br>For 48 kHz-related sample rates, the system-clock frequency is 24.576 MHz. For 44.1 kHz-related sample rates, the system-clock frequency is 22.5792 MHz.<br><div><div>0x0 = (Default) Divide by 2<br/>0x1 = Divide by 4<br/>0x2 = Divide by 6<br/>0x3 = Divide by 8<br/>0x4 = Divide by 10<br/>0x5 = Divide by 12<br/>0x6 = Divide by 14<br/>0x7 = Divide by 16</div><div>0x8 = Divide by 18<br/>0x9 = Divide by 20<br/>0xA = Divide by 22<br/>0xB = Divide by 24<br/>0xC = Divide by 26<br/>0xD = Divide by 28<br/>0xE = Divide by 30<br/>0xF = Divide by 32</div></div> |
| 3:2  | —       | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 1    | CPHA    | SPI clock phase select (CPHA)<br>0 = (Default) Negative SPI clock phase<br>1 = Positive SPI clock phase                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 0    | CPOL    | SPI clock polarity select (CPOL)<br>0 = (Default) Negative SPI clock polarity<br>1 = Positive SPI clock polarity                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 6.4.9 SPI\_1

**Address: 0x0000 2022**

|         |    |    |    |    |             |    |   |   |               |   |   |   |               |   |   |   |
|---------|----|----|----|----|-------------|----|---|---|---------------|---|---|---|---------------|---|---|---|
| RW      | 15 | 14 | 13 | 12 | 11          | 10 | 9 | 8 | 7             | 6 | 5 | 4 | 3             | 2 | 1 | 0 |
|         | —  |    |    |    | CS_IDLE_DUR |    |   |   | CS_RISE_DELAY |   |   |   | CS_FALL_DELAY |   |   |   |
| Default | 0  | 0  | 0  | 0  | 0           | 0  | 0 | 0 | 0             | 0 | 0 | 0 | 0             | 0 | 0 | 0 |

| Bits                             | Name                    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
|----------------------------------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|-------------------------|------------------------|-------------------------|------------------------|-------------------------|------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 15:12                            | —                       | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 11:8                             | CS_IDLE_DUR             | <p>Minimum idle duration between SPI transactions (from CS rising edge to CS falling edge). The duration is defined in system-clock cycles.</p> <p>For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz.</p> <table><tr><td>0x0 = (Default) 32 clock cycles</td><td>0x8 = 96 clock cycles</td></tr><tr><td>0x1 = 36 clock cycles</td><td>0x9 = 128 clock cycles</td></tr><tr><td>0x2 = 40 clock cycles</td><td>0xA = 160 clock cycles</td></tr><tr><td>0x3 = 44 clock cycles</td><td>0xB = 224 clock cycles</td></tr><tr><td>0x4 = 48 clock cycles</td><td>0xC = 288 clock cycles</td></tr><tr><td>0x5 = 56 clock cycles</td><td>0xD = 416 clock cycles</td></tr><tr><td>0x6 = 64 clock cycles</td><td>0xE = 544 clock cycles</td></tr><tr><td>0x7 = 80 clock cycles</td><td>0xF = 800 clock cycles</td></tr></table>                                                                                                                                                                                                                       | 0x0 = (Default) 32 clock cycles  | 0x8 = 96 clock cycles   | 0x1 = 36 clock cycles  | 0x9 = 128 clock cycles  | 0x2 = 40 clock cycles  | 0xA = 160 clock cycles  | 0x3 = 44 clock cycles  | 0xB = 224 clock cycles  | 0x4 = 48 clock cycles   | 0xC = 288 clock cycles  | 0x5 = 56 clock cycles   | 0xD = 416 clock cycles  | 0x6 = 64 clock cycles   | 0xE = 544 clock cycles  | 0x7 = 80 clock cycles   | 0xF = 800 clock cycles  |
| 0x0 = (Default) 32 clock cycles  | 0x8 = 96 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x1 = 36 clock cycles            | 0x9 = 128 clock cycles  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x2 = 40 clock cycles            | 0xA = 160 clock cycles  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x3 = 44 clock cycles            | 0xB = 224 clock cycles  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x4 = 48 clock cycles            | 0xC = 288 clock cycles  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x5 = 56 clock cycles            | 0xD = 416 clock cycles  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x6 = 64 clock cycles            | 0xE = 544 clock cycles  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x7 = 80 clock cycles            | 0xF = 800 clock cycles  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 7:4                              | CS_RISE_DELAY           | <p>Chip Select (CS) rise delay. Configures the minimum time from SCLK active edge to CS rising edge (end of SPI transaction). The delay is defined in system-clock cycles.</p> <p>For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz.</p> <table><tr><td>0x0 = (Default) 2 clock cycles</td><td>0x8 = 18 clock cycles</td></tr><tr><td>0x1 = 4 clock cycles</td><td>0x9 = 20 clock cycles</td></tr><tr><td>0x2 = 6 clock cycles</td><td>0xA = 22 clock cycles</td></tr><tr><td>0x3 = 8 clock cycles</td><td>0xB = 24 clock cycles</td></tr><tr><td>0x4 = 10 clock cycles</td><td>0xC = 26 clock cycles</td></tr><tr><td>0x5 = 12 clock cycles</td><td>0xD = 28 clock cycles</td></tr><tr><td>0x6 = 14 clock cycles</td><td>0xE = 30 clock cycles</td></tr><tr><td>0x7 = 16 clock cycles</td><td>0xF = 32 clock cycles</td></tr></table>                                                                                                                                                                                                   | 0x0 = (Default) 2 clock cycles   | 0x8 = 18 clock cycles   | 0x1 = 4 clock cycles   | 0x9 = 20 clock cycles   | 0x2 = 6 clock cycles   | 0xA = 22 clock cycles   | 0x3 = 8 clock cycles   | 0xB = 24 clock cycles   | 0x4 = 10 clock cycles   | 0xC = 26 clock cycles   | 0x5 = 12 clock cycles   | 0xD = 28 clock cycles   | 0x6 = 14 clock cycles   | 0xE = 30 clock cycles   | 0x7 = 16 clock cycles   | 0xF = 32 clock cycles   |
| 0x0 = (Default) 2 clock cycles   | 0x8 = 18 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x1 = 4 clock cycles             | 0x9 = 20 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x2 = 6 clock cycles             | 0xA = 22 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x3 = 8 clock cycles             | 0xB = 24 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x4 = 10 clock cycles            | 0xC = 26 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x5 = 12 clock cycles            | 0xD = 28 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x6 = 14 clock cycles            | 0xE = 30 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x7 = 16 clock cycles            | 0xF = 32 clock cycles   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 3:0                              | CS_FALL_DELAY           | <p>Chip Select (CS) fall delay. Configures the minimum time from CS falling edge (start of SPI transaction) to the first SCK edge. The delay is defined in system-clock cycles.</p> <p>For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz.</p> <p>The delay is dependent on the SPI clock divider (SCK_DIV) setting – the 'N' variable in the enumeration represents the value of SCK_DIV field (0-15).</p> <table><tr><td>0x0 = (Default) 3+N clock cycles</td><td>0x8 = 19+N clock cycles</td></tr><tr><td>0x1 = 5+N clock cycles</td><td>0x9 = 21+N clock cycles</td></tr><tr><td>0x2 = 7+N clock cycles</td><td>0xA = 23+N clock cycles</td></tr><tr><td>0x3 = 9+N clock cycles</td><td>0xB = 25+N clock cycles</td></tr><tr><td>0x4 = 11+N clock cycles</td><td>0xC = 27+N clock cycles</td></tr><tr><td>0x5 = 13+N clock cycles</td><td>0xD = 29+N clock cycles</td></tr><tr><td>0x6 = 15+N clock cycles</td><td>0xE = 31+N clock cycles</td></tr><tr><td>0x7 = 17+N clock cycles</td><td>0xF = 33+N clock cycles</td></tr></table> | 0x0 = (Default) 3+N clock cycles | 0x8 = 19+N clock cycles | 0x1 = 5+N clock cycles | 0x9 = 21+N clock cycles | 0x2 = 7+N clock cycles | 0xA = 23+N clock cycles | 0x3 = 9+N clock cycles | 0xB = 25+N clock cycles | 0x4 = 11+N clock cycles | 0xC = 27+N clock cycles | 0x5 = 13+N clock cycles | 0xD = 29+N clock cycles | 0x6 = 15+N clock cycles | 0xE = 31+N clock cycles | 0x7 = 17+N clock cycles | 0xF = 33+N clock cycles |
| 0x0 = (Default) 3+N clock cycles | 0x8 = 19+N clock cycles |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x1 = 5+N clock cycles           | 0x9 = 21+N clock cycles |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x2 = 7+N clock cycles           | 0xA = 23+N clock cycles |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x3 = 9+N clock cycles           | 0xB = 25+N clock cycles |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x4 = 11+N clock cycles          | 0xC = 27+N clock cycles |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x5 = 13+N clock cycles          | 0xD = 29+N clock cycles |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x6 = 15+N clock cycles          | 0xE = 31+N clock cycles |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |
| 0x7 = 17+N clock cycles          | 0xF = 33+N clock cycles |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                  |                         |                        |                         |                        |                         |                        |                         |                         |                         |                         |                         |                         |                         |                         |                         |

### 6.4.10 CH1\_CONFIG

**Address: 0x0000 2030**

|         |        |   |                     |   |   |   |   |   |   |
|---------|--------|---|---------------------|---|---|---|---|---|---|
| RW      | 15...8 | 7 | 6                   | 5 | 4 | 3 | 2 | 1 | 0 |
|         | —      | — | CH1_BIT_PATT_LENGTH |   |   |   |   |   |   |
| Default | 0x00   | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name                | Description                                                                                                                                                                          |
|------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:6 | —                   | Reserved                                                                                                                                                                             |
| 5:0  | CH1_BIT_PATT_LENGTH | Channel 1 bit-pattern length for SPI gain control<br>0x00 = (Default) 0 bits (device not present)<br>0x01 = 1 bits<br>0x02 = 2 bits<br>...<br>0x20 = 32 bits<br>0x21–0x3F = Reserved |

### 6.4.11 CH2\_CONFIG

**Address: 0x0000 2034**

|         |        |   |   |   |   |                     |   |   |   |
|---------|--------|---|---|---|---|---------------------|---|---|---|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3                   | 2 | 1 | 0 |
|         | —      | — |   |   |   | CH2_BIT_PATT_LENGTH |   |   |   |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 |

| Bits | Name                | Description                                                                                                                                                                          |
|------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:6 | —                   | Reserved                                                                                                                                                                             |
| 5:0  | CH2_BIT_PATT_LENGTH | Channel 2 bit-pattern length for SPI gain control<br>0x00 = (Default) 0 bits (device not present)<br>0x01 = 1 bits<br>0x02 = 2 bits<br>...<br>0x20 = 32 bits<br>0x21–0x3F = Reserved |

### 6.4.12 AUX1\_CONFIG

**Address: 0x0000 2050**

|         |        |   |   |   |   |                      |   |   |   |
|---------|--------|---|---|---|---|----------------------|---|---|---|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3                    | 2 | 1 | 0 |
|         | —      | — |   |   |   | AUX1_BIT_PATT_LENGTH |   |   |   |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0                    | 0 | 0 | 0 |

| Bits | Name                 | Description                                                                                                                                                                           |
|------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:6 | —                    | Reserved                                                                                                                                                                              |
| 5:0  | AUX1_BIT_PATT_LENGTH | Auxiliary 1 bit-pattern length for SPI aux control<br>0x00 = (Default) 0 bits (device not present)<br>0x01 = 1 bits<br>0x02 = 2 bits<br>...<br>0x20 = 32 bits<br>0x21–0x3F = Reserved |

### 6.4.13 AUX2\_CONFIG

**Address: 0x0000 2054**

|         |        |   |   |   |   |                      |   |   |   |
|---------|--------|---|---|---|---|----------------------|---|---|---|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3                    | 2 | 1 | 0 |
|         | —      | — |   |   |   | AUX2_BIT_PATT_LENGTH |   |   |   |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0                    | 0 | 0 | 0 |

| Bits | Name                 | Description                                                                                                                                                                           |
|------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:6 | —                    | Reserved                                                                                                                                                                              |
| 5:0  | AUX2_BIT_PATT_LENGTH | Auxiliary 2 bit-pattern length for SPI aux control<br>0x00 = (Default) 0 bits (device not present)<br>0x01 = 1 bits<br>0x02 = 2 bits<br>...<br>0x20 = 32 bits<br>0x21–0x3F = Reserved |

### 6.4.14 CH1\_BIT\_PATT\_0

**Address: 0x0000 2060**

|         |                |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | CH1_BIT_PATT_0 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0              | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name           | Description                                                                                                                                                                                                                                                                                                       |
|------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | CH1_BIT_PATT_0 | Channel 1 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

### 6.4.15 CH1\_BIT\_PATT\_1

**Address: 0x0000 2062**

|         |                |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | CH1_BIT_PATT_1 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0              | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name           | Description                                                                                                                                                                                                                                                 |
|------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | CH1_BIT_PATT_1 | Channel 1 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused. |

### 6.4.16 CH1\_VOL\_0

**Address: 0x0000 2064**

|         |    |    |    |    |             |    |   |   |   |   |   |   |   |   |   |   |
|---------|----|----|----|----|-------------|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15 | 14 | 13 | 12 | 11          | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | —  |    |    |    | CH1_ANA_VOL |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0  | 0  | 0  | 0  | 0           | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits  | Name        | Description                                                                                                                                                                                                                                                                           |
|-------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | —           | Reserved                                                                                                                                                                                                                                                                              |
| 10:0  | CH1_ANA_VOL | Channel 1 analog gain. The selected value must match the analog gain of the associated SPI bit pattern.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>0x002 = 0.250 dB<br>...<br>0x23F = 71.875 dB<br>0x240–0x5BF = Reserved<br>0x5C0 = –72.000 dB<br>...<br>0x7FF = –0.125 dB |

### 6.4.17 CH1\_VOL\_1

**Address: 0x0000 2066**

|         |            |    |    |    |    |             |   |   |   |   |   |   |   |   |   |   |
|---------|------------|----|----|----|----|-------------|---|---|---|---|---|---|---|---|---|---|
|         | 15         | 14 | 13 | 12 | 11 | 10          | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | CH1_UPDATE | —  |    |    |    | CH1_DIG_VOL |   |   |   |   |   |   |   |   |   |   |
| Access  | WO         | —  |    |    |    | RW          |   |   |   |   |   |   |   |   |   |   |
| Default | 0          | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name        | Description                                                                                                                                                                                   |
|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | CH1_UPDATE  | Channel 1 gain update. Write 1 to apply the Channel 1 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned.                  |
| 14:8 | —           | Reserved                                                                                                                                                                                      |
| 7:0  | CH1_DIG_VOL | Channel 1 digital gain.<br>0x00 = (Default) 0.000 dB<br>0x01 = 0.125 dB<br>0x02 = 0.250 dB<br>...<br>0x5F = 11.875 dB<br>0x60–0x9F = Reserved<br>0xA0 = –12.000 dB<br>...<br>0xFF = –0.125 dB |

### 6.4.18 CH2\_BIT\_PATT\_0

**Address: 0x0000 2068**

|         |                |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | CH2_BIT_PATT_0 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0              | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name           | Description                                                                                                                                                                                                                                                                                                       |
|------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | CH2_BIT_PATT_0 | Channel 2 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

### 6.4.19 CH2\_BIT\_PATT\_1

**Address: 0x0000 206A**

|         |                |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | CH2_BIT_PATT_1 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0              | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name           | Description                                                                                                                                                                                                                                                 |
|------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | CH2_BIT_PATT_1 | Channel 2 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused. |

### 6.4.20 CH2\_VOL\_0

**Address: 0x0000 206C**

|         |    |    |    |    |             |    |   |   |   |   |   |   |   |   |   |   |
|---------|----|----|----|----|-------------|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15 | 14 | 13 | 12 | 11          | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | —  |    |    |    | CH2_ANA_VOL |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0  | 0  | 0  | 0  | 0           | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits  | Name        | Description                                                                                                                                                                                                                                                                           |
|-------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | —           | Reserved                                                                                                                                                                                                                                                                              |
| 10:0  | CH2_ANA_VOL | Channel 2 analog gain. The selected value must match the analog gain of the associated SPI bit pattern.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>0x002 = 0.250 dB<br>...<br>0x23F = 71.875 dB<br>0x240–0x5BF = Reserved<br>0x5C0 = –72.000 dB<br>...<br>0x7FF = –0.125 dB |

### 6.4.21 CH2\_VOL\_1

**Address: 0x0000 206E**

|         |            |    |    |    |    |             |   |   |   |   |   |   |   |   |   |   |
|---------|------------|----|----|----|----|-------------|---|---|---|---|---|---|---|---|---|---|
|         | 15         | 14 | 13 | 12 | 11 | 10          | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | CH2_UPDATE | —  |    |    |    | CH2_DIG_VOL |   |   |   |   |   |   |   |   |   |   |
| Access  | WO         | —  |    |    |    | RW          |   |   |   |   |   |   |   |   |   |   |
| Default | 0          | 0  | 0  | 0  | 0  | 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name        | Description                                                                                                                                                                                   |
|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | CH2_UPDATE  | Channel 2 gain update. Write 1 to apply the Channel 2 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned.                  |
| 14:8 | —           | Reserved                                                                                                                                                                                      |
| 7:0  | CH2_DIG_VOL | Channel 2 digital gain.<br>0x00 = (Default) 0.000 dB<br>0x01 = 0.125 dB<br>0x02 = 0.250 dB<br>...<br>0x5F = 11.875 dB<br>0x60–0x9F = Reserved<br>0xA0 = –12.000 dB<br>...<br>0xFF = –0.125 dB |

### 6.4.22 AUX1\_BIT\_PATT\_0

**Address: 0x0000 20A0**

|         |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | AUX1_BIT_PATT_0 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name            | Description                                                                                                                                                                                                                                                                                                         |
|------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | AUX1_BIT_PATT_0 | Auxiliary 1 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

### 6.4.23 AUX1\_BIT\_PATT\_1

**Address: 0x0000 20A2**

|         |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | AUX1_BIT_PATT_1 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name            | Description                                                                                                                                                                                                                                                      |
|------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | AUX1_BIT_PATT_1 | Auxiliary 1 SPI bit pattern for external gain control, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused. |

**6.4.24 AUX2\_BIT\_PATT\_0**
**Address: 0x0000 20A4**

|         |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | AUX2_BIT_PATT_0 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name            | Description                                                                                                                                                                                                                                                                                                         |
|------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | AUX2_BIT_PATT_0 | Auxiliary 2 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

**6.4.25 AUX2\_BIT\_PATT\_1**
**Address: 0x0000 20A6**

|         |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | AUX2_BIT_PATT_1 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name            | Description                                                                                                                                                                                                                                                   |
|------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | AUX2_BIT_PATT_1 | Auxiliary 2 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused. |

**6.5 PIN\_CONFIG**
**6.5.1 PAD\_CLIP**
**Address: 0x0000 3D1C**

|         |             |    |    |    |    |    |   |   |                 |                 |                 |   |                |   |                   |   |
|---------|-------------|----|----|----|----|----|---|---|-----------------|-----------------|-----------------|---|----------------|---|-------------------|---|
| RW      | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6               | 5               | 4 | 3              | 2 | 1                 | 0 |
|         | CLIP_OP_CFG | —  |    |    |    |    |   |   | CONFIG4_CLIP_EN | CONFIG3_CLIP_EN | CONFIG2_CLIP_EN | — | SPI_CS_CLIP_EN | — | ASP_DOUT2_CLIP_EN |   |
| Default | 0           | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0               | 0               | 0               | 0 | 0              | 0 | 0                 | 0 |

| Bits | Name              | Description                                                                        |
|------|-------------------|------------------------------------------------------------------------------------|
| 15   | CLIP_OP_CFG       | Clip-detect output configuration<br>0 = (Default) CMOS<br>1 = Open drain           |
| 14:8 | —                 | Reserved                                                                           |
| 7    | CONFIG4_CLIP_EN   | CONFIG4 pin function select<br>0 = (Default) HW config<br>1 = Clip-detect output   |
| 6    | CONFIG3_CLIP_EN   | CONFIG3 pin function select<br>0 = (Default) HW config<br>1 = Clip-detect output   |
| 5    | CONFIG2_CLIP_EN   | CONFIG2 pin function select<br>0 = (Default) HW config<br>1 = Clip-detect output   |
| 4    | —                 | Reserved                                                                           |
| 3    | SPI_CS_CLIP_EN    | SPI_CS pin function select<br>0 = (Default) SPI_CS<br>1 = Clip-detect output       |
| 2:1  | —                 | Reserved                                                                           |
| 0    | ASP_DOUT2_CLIP_EN | ASP_DOUT2 pin function select<br>0 = (Default) ASP_DOUT2<br>1 = Clip-detect output |

### 6.5.2 PAD\_HGC\_SPI

**Address: 0x0000 3D20**

|         |        |   |   |   |   |   |   |   |            |
|---------|--------|---|---|---|---|---|---|---|------------|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0          |
|         | —      |   |   |   | — |   |   |   | HGC_SPI_EN |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          |

| Bits | Name       | Description                                                                                                |
|------|------------|------------------------------------------------------------------------------------------------------------|
| 15:1 | —          | Reserved                                                                                                   |
| 0    | HGC_SPI_EN | HGC pin function select. Set this bit to enable the HGC function on the CONFIG2, CONFIG3, and CONFIG4 pins |

### 6.5.3 PAD\_FN

**Address: 0x0000 3D24**

|         |    |    |    |    |    |    |            |            |            |            |   |            |           |   |   |              |
|---------|----|----|----|----|----|----|------------|------------|------------|------------|---|------------|-----------|---|---|--------------|
| RW      | 15 | 14 | 13 | 12 | 11 | 10 | 9          | 8          | 7          | 6          | 5 | 4          | 3         | 2 | 1 | 0            |
|         |    |    |    | —  |    |    | CONFIG5_FN | CONFIG4_FN | CONFIG3_FN | CONFIG2_FN | — | SPI_SCK_FN | SPI_CS_FN | — |   | ASP_DOUT2_FN |
| Default | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0          | 0          | 0          | 0 | 0          | 0         | 0 | 0 | 0            |

| Bits  | Name         | Description                                                                     |
|-------|--------------|---------------------------------------------------------------------------------|
| 15:10 | —            | Reserved                                                                        |
| 9     | CONFIG5_FN   | CONFIG5 pin function select<br>0 = (Default) HW config<br>1 = GP output         |
| 8     | CONFIG4_FN   | CONFIG4 pin function select<br>0 = (Default) HW config/HGC_CS<br>1 = GP output  |
| 7     | CONFIG3_FN   | CONFIG3 pin function select<br>0 = (Default) HW config/HGC_SDO<br>1 = GP output |
| 6     | CONFIG2_FN   | CONFIG2 pin function select<br>0 = (Default) HW config/HGC_SCK<br>1 = GP output |
| 5     | —            | Reserved                                                                        |
| 4     | SPI_SCK_FN   | SPI_SCK pin function select<br>0 = (Default) SPI_SCK<br>1 = GP output           |
| 3     | SPI_CS_FN    | SPI_CS pin function select<br>0 = (Default) SPI_CS<br>1 = GP output             |
| 2:1   | —            | Reserved                                                                        |
| 0     | ASP_DOUT2_FN | ASP_DOUT2 pin function select<br>0 = (Default) ASP_DOUT2<br>1 = GP output       |

### 6.5.4 PAD\_LVL

**Address: 0x0000 3D28**

|         |    |    |    |    |    |    |             |             |             |             |   |             |            |   |   |               |
|---------|----|----|----|----|----|----|-------------|-------------|-------------|-------------|---|-------------|------------|---|---|---------------|
| RW      | 15 | 14 | 13 | 12 | 11 | 10 | 9           | 8           | 7           | 6           | 5 | 4           | 3          | 2 | 1 | 0             |
|         |    |    |    | —  |    |    | CONFIG5_LVL | CONFIG4_LVL | CONFIG3_LVL | CONFIG2_LVL | — | SPI_SCK_LVL | SPI_CS_LVL | — |   | ASP_DOUT2_LVL |
| Default | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0           | 0           | 0           | 0 | 0           | 0          | 0 | 0 | 0             |

| Bits  | Name        | Description                                                                                                                |
|-------|-------------|----------------------------------------------------------------------------------------------------------------------------|
| 15:10 | —           | Reserved                                                                                                                   |
| 9     | CONFIG5_LVL | CONFIG5 output level. Sets the output level if CONFIG5 is configured as GP output.<br>0 = (Default) Logic 0<br>1 = Logic 1 |
| 8     | CONFIG4_LVL | CONFIG4 output level. Sets the output level if CONFIG4 is configured as GP output.<br>0 = (Default) Logic 0<br>1 = Logic 1 |

| Bits | Name          | Description                                                                                                                    |
|------|---------------|--------------------------------------------------------------------------------------------------------------------------------|
| 7    | CONFIG3_LVL   | CONFIG3 output level. Sets the output level if CONFIG3 is configured as GP output.<br>0 = (Default) Logic 0<br>1 = Logic 1     |
| 6    | CONFIG2_LVL   | CONFIG2 output level. Sets the output level if CONFIG2 is configured as GP output.<br>0 = (Default) Logic 0<br>1 = Logic 1     |
| 5    | —             | Reserved                                                                                                                       |
| 4    | SPI_SCK_LVL   | SPI_SCK output level. Sets the output level if SPI_SCK is configured as GP output.<br>0 = (Default) Logic 0<br>1 = Logic 1     |
| 3    | SPI_CS_LVL    | SPI_CS output level. Sets the output level if SPI_CS is configured as GP output.<br>0 = (Default) Logic 0<br>1 = Logic 1       |
| 2:1  | —             | Reserved                                                                                                                       |
| 0    | ASP_DOUT2_LVL | ASP_DOUT2 output level. Sets the output level if ASP_DOUT2 is configured as GP output.<br>0 = (Default) Logic 0<br>1 = Logic 1 |

## 6.6 CLIP\_DETECT

### 6.6.1 CLIP\_WARN

**Address: 0x0000 3E1C**

|         |        |   |   |   |   |   |               |               |   |
|---------|--------|---|---|---|---|---|---------------|---------------|---|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3 | 2             | 1             | 0 |
|         | —      |   |   | — |   |   | IN2_CLIP_WARN | IN1_CLIP_WARN | — |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0 | 0             | 0             | 0 |

| Bits | Name          | Description                                                                                                           |
|------|---------------|-----------------------------------------------------------------------------------------------------------------------|
| 15:3 | —             | Reserved                                                                                                              |
| 2    | IN2_CLIP_WARN | Channel 2 clip-detect indication. Rising edge triggered. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Clip detect |
| 1    | IN1_CLIP_WARN | Channel 1 clip-detect indication. Rising edge triggered. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Clip detect |
| 0    | —             | Reserved                                                                                                              |

## 7 Performance Plots

### 7.1 ADC Filter Response

The ADC filter performance is described in this section. Note the group-delay plots represent the filter only—see [Table 3-5](#) for full-path latency.

ADC Filter Response—Fast Roll-Off, 32 kHz Sample Rate

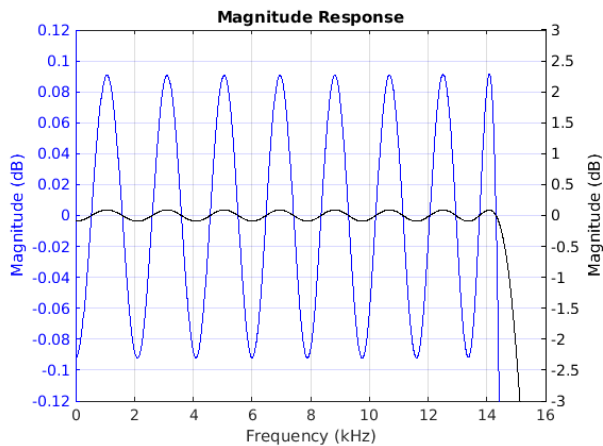


Figure 7-1. Passband Magnitude

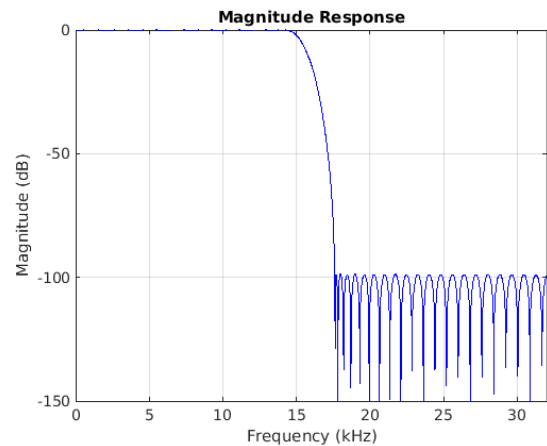


Figure 7-2. Stopband Magnitude

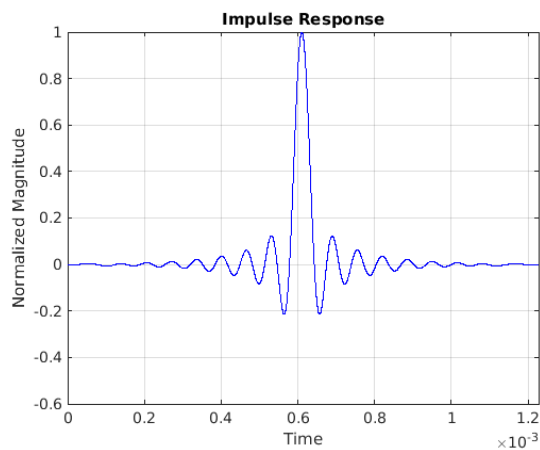


Figure 7-3. Impulse Response—Linear Phase

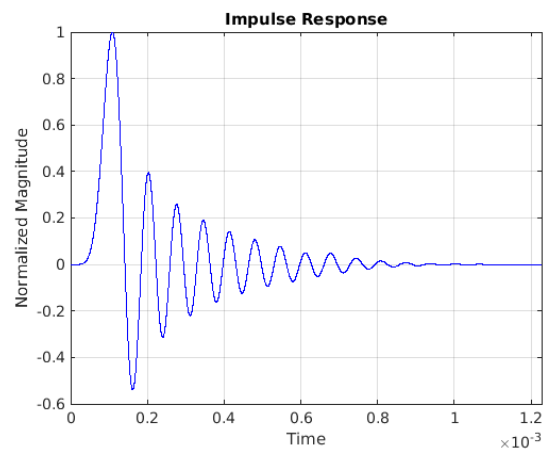


Figure 7-4. Impulse Response—Minimum Phase

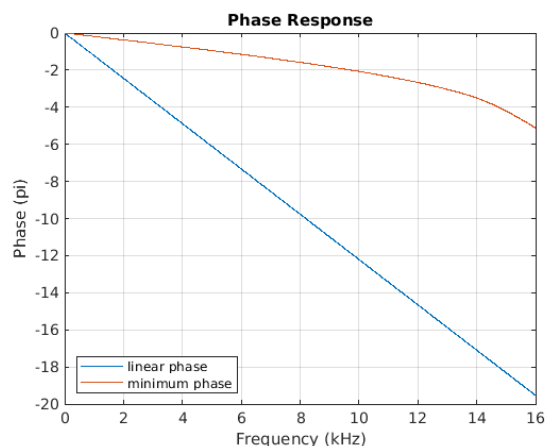


Figure 7-5. Phase vs. Frequency

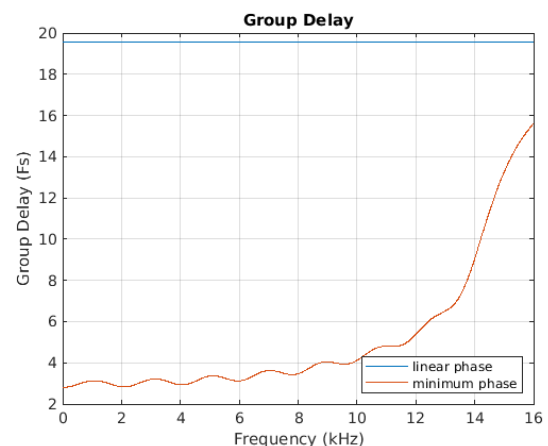
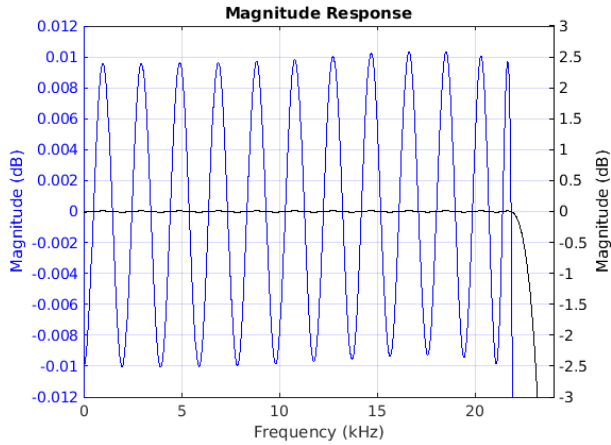
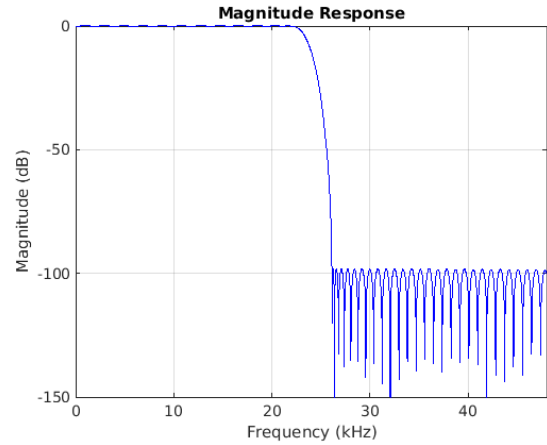
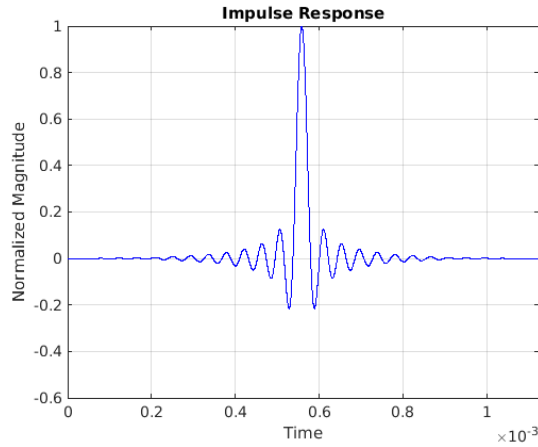
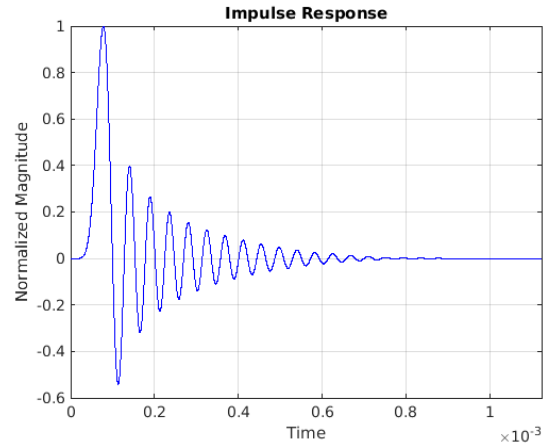
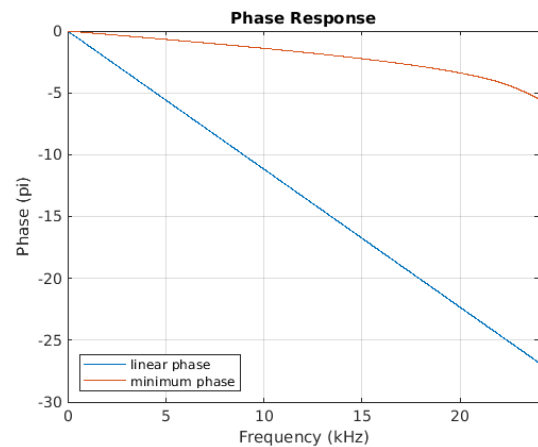
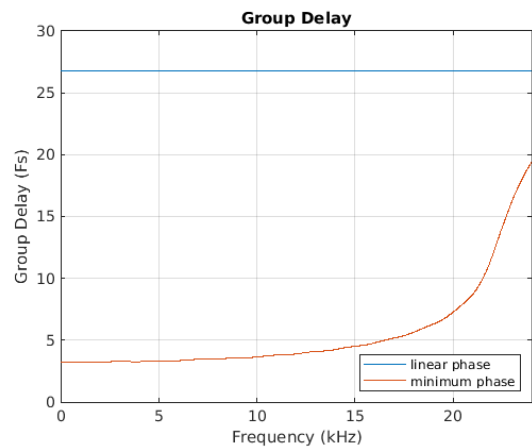
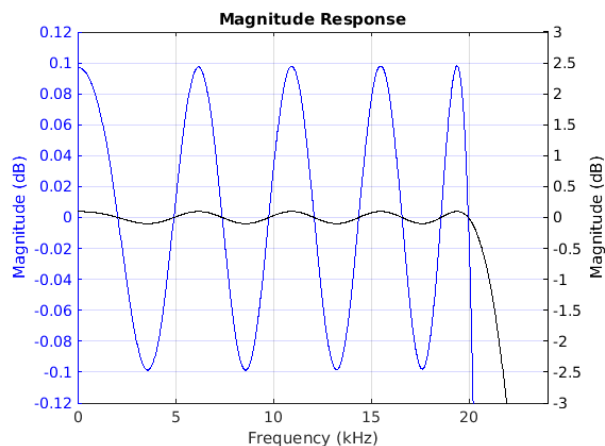
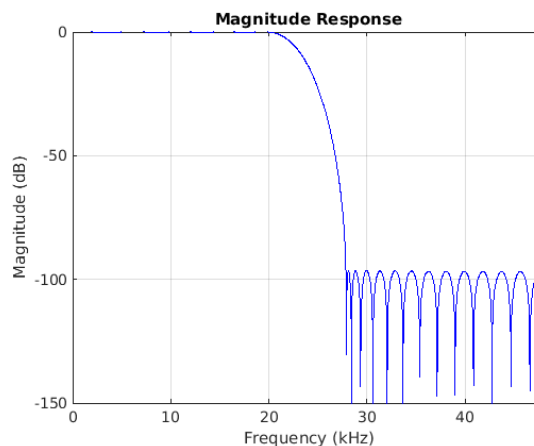
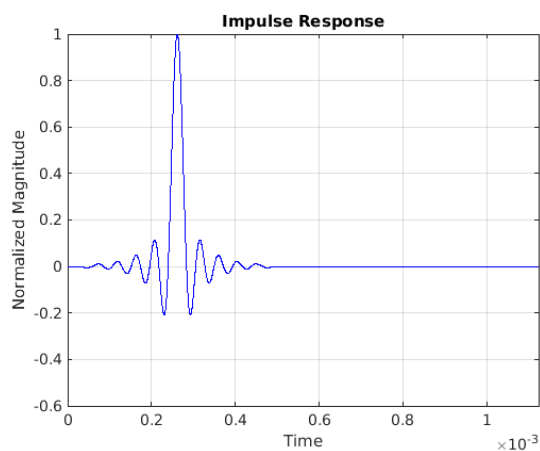
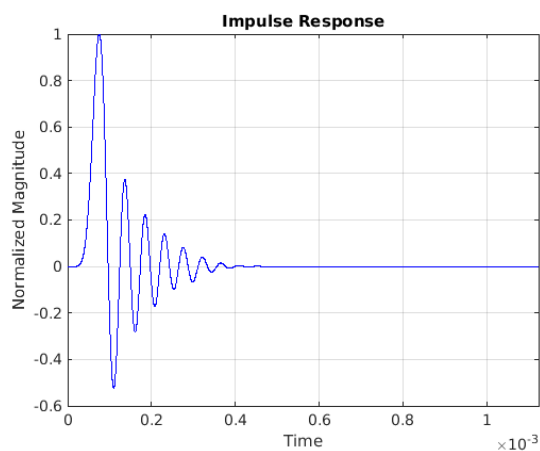
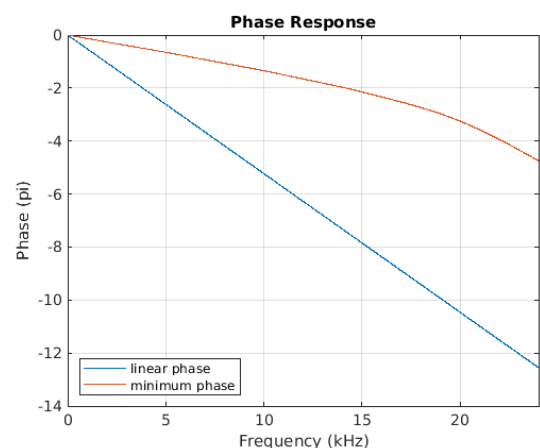
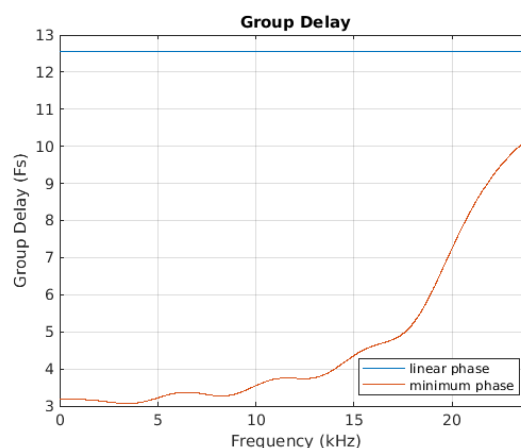
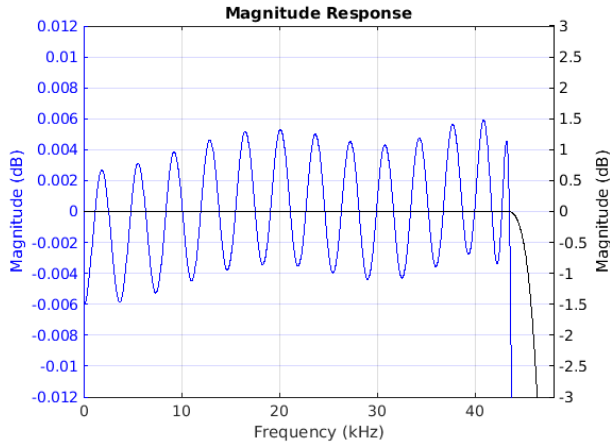
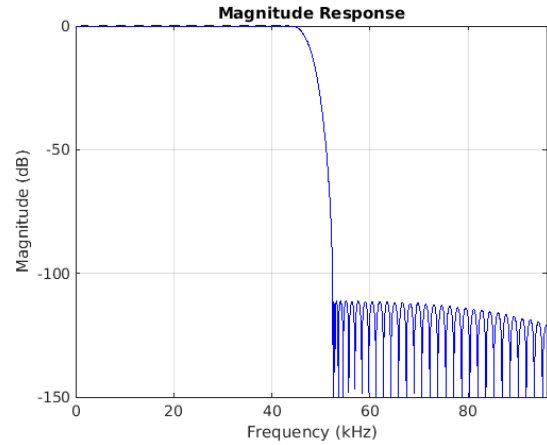
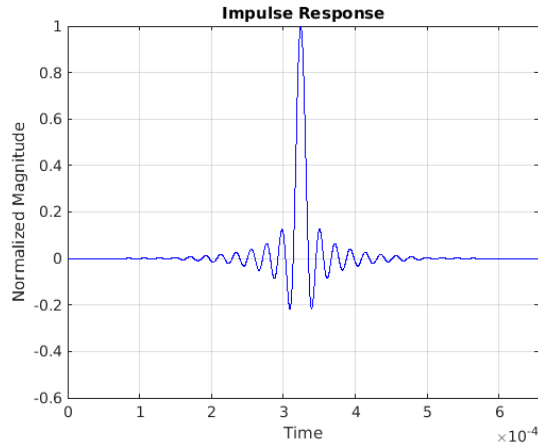
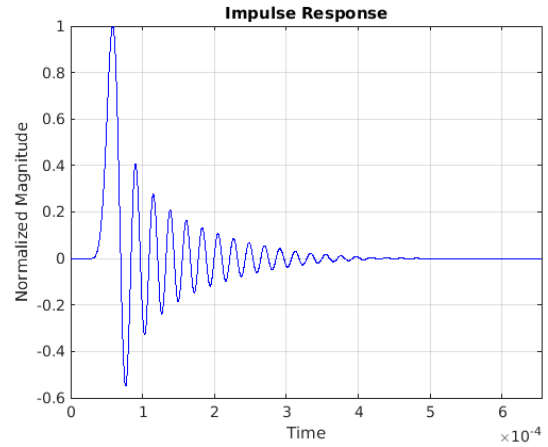
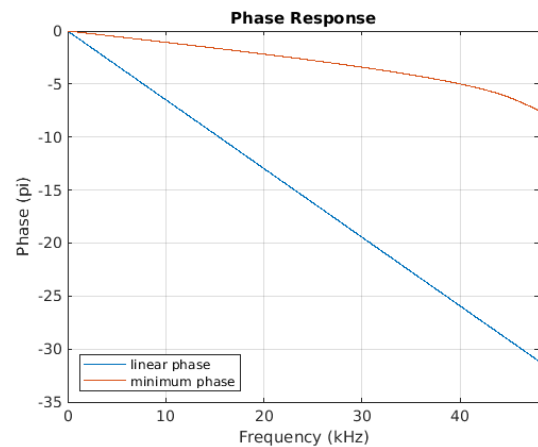
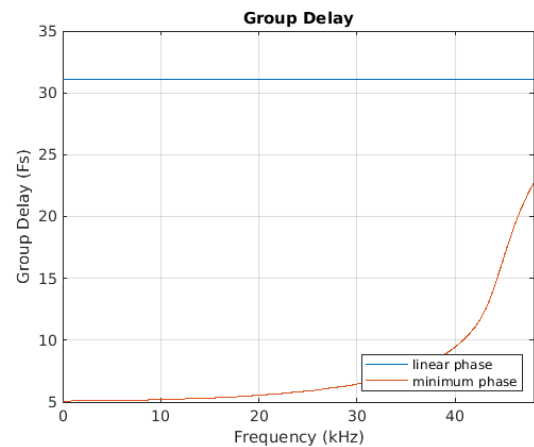
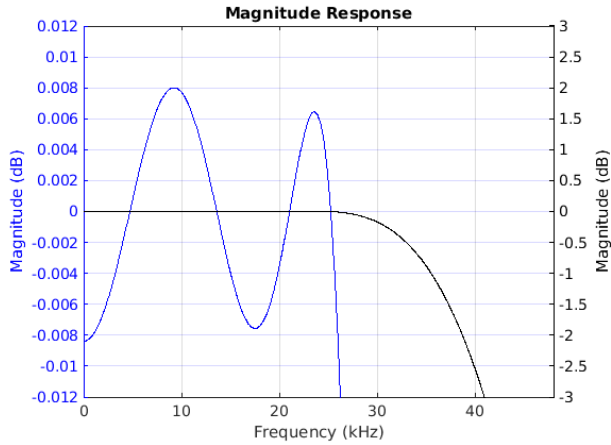
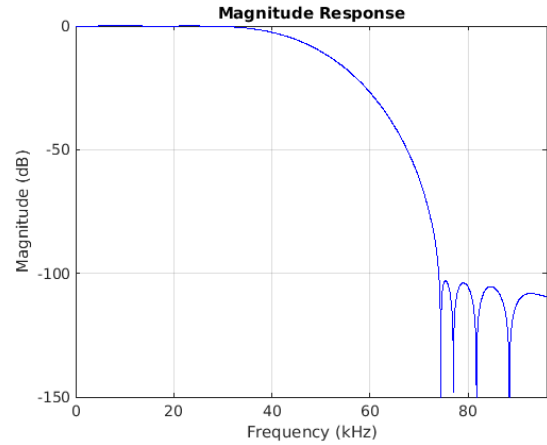
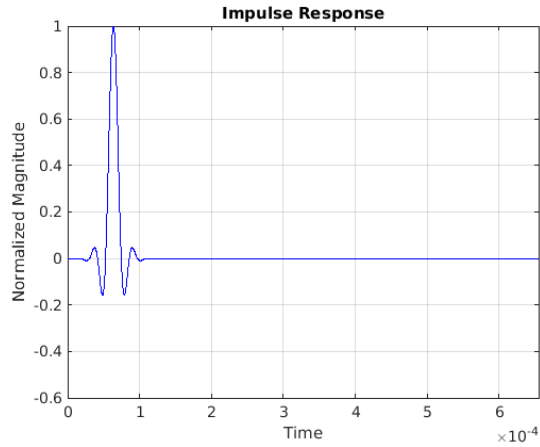
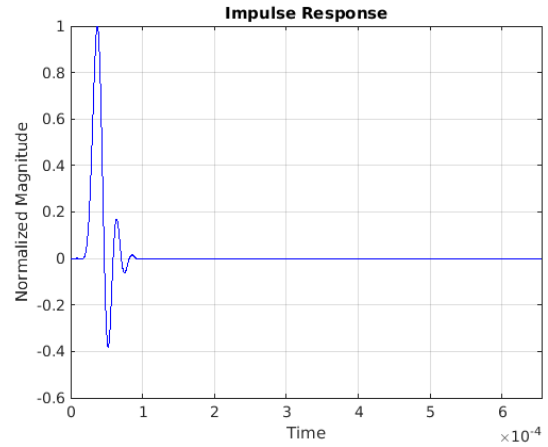
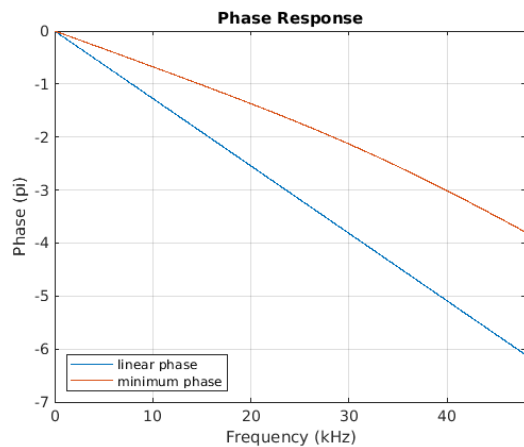
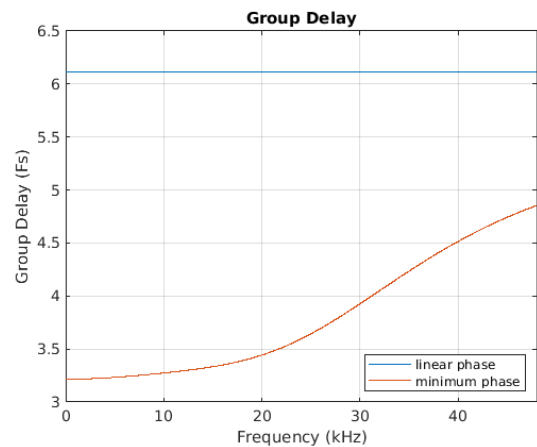


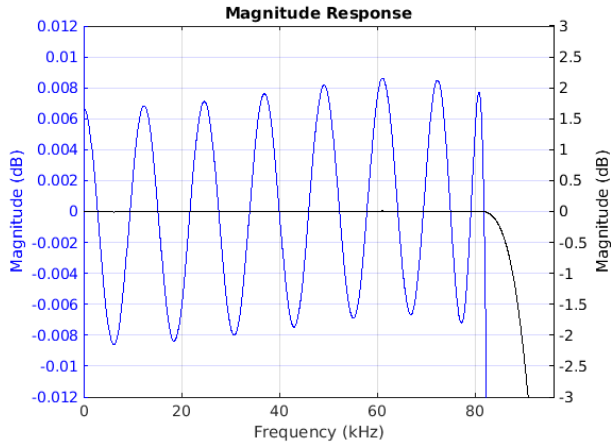
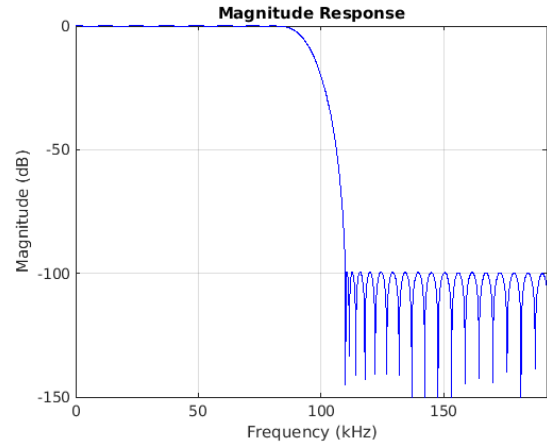
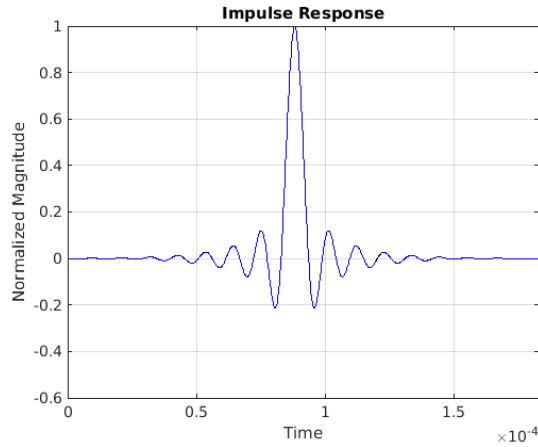
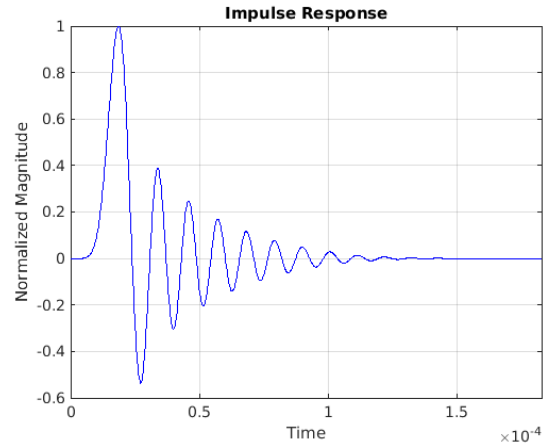
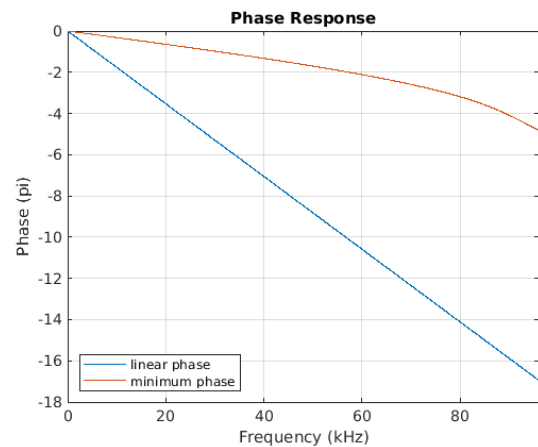
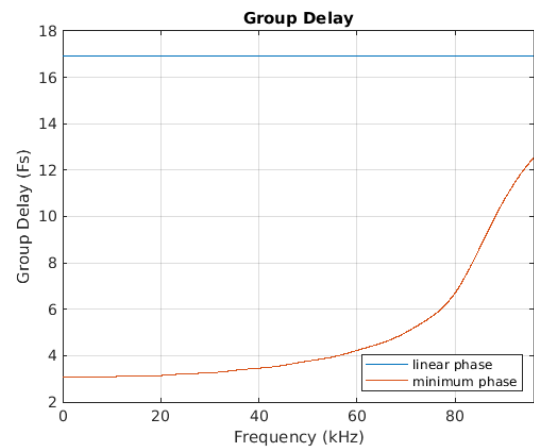
Figure 7-6. Group Delay vs. Frequency

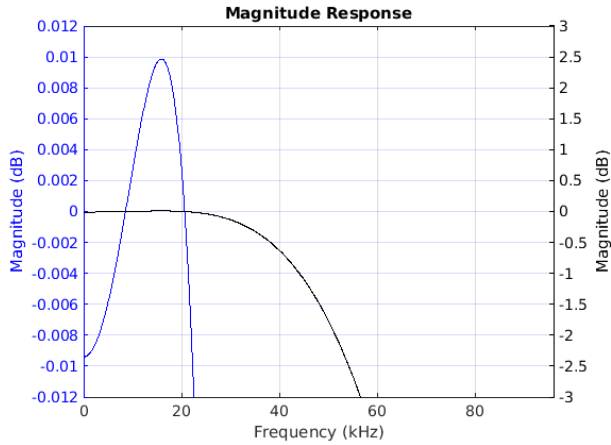
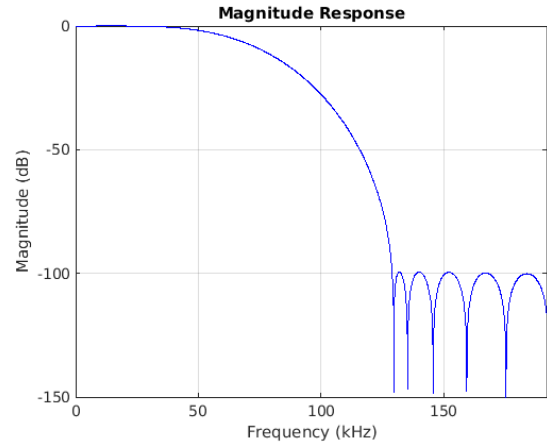
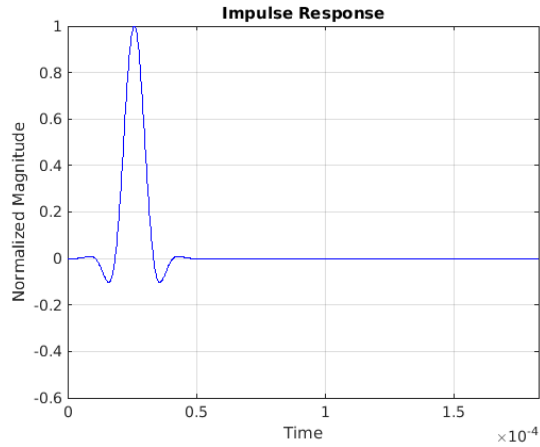
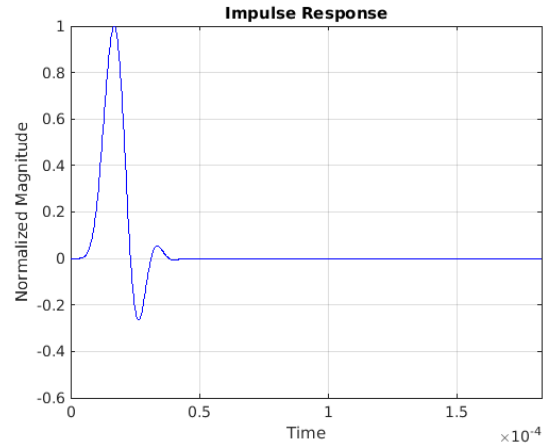
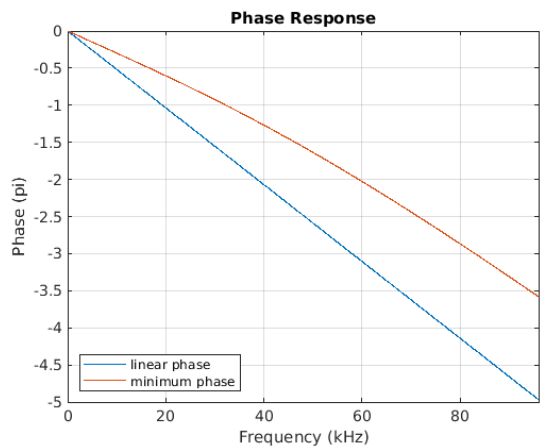
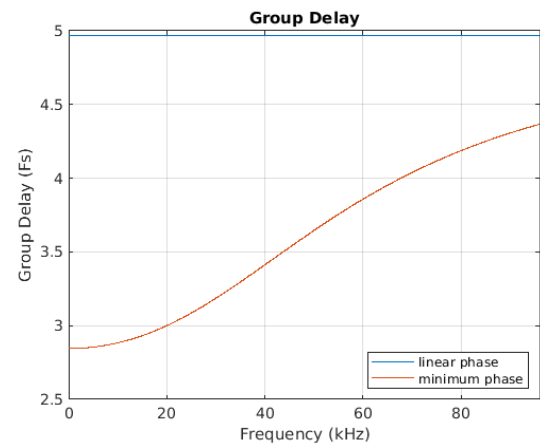
**ADC Filter Response—Fast Roll-Off, 48 kHz Sample Rate**

**Figure 7-7. Passband Magnitude**

**Figure 7-8. Stopband Magnitude**

**Figure 7-9. Impulse Response—Linear Phase**

**Figure 7-10. Impulse Response—Minimum Phase**

**Figure 7-11. Phase vs. Frequency**

**Figure 7-12. Group Delay vs. Frequency**

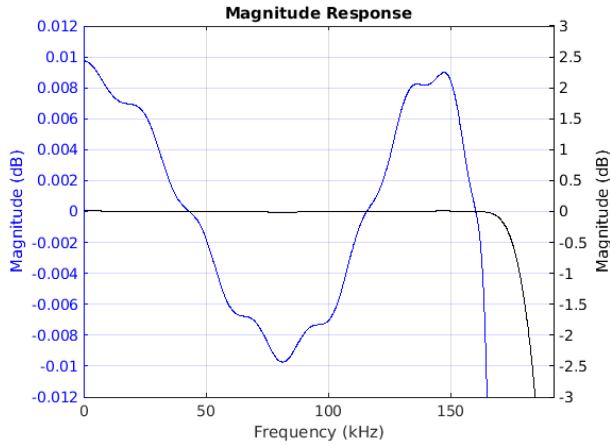
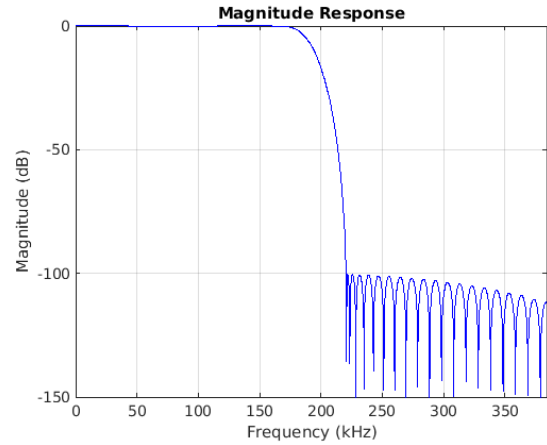
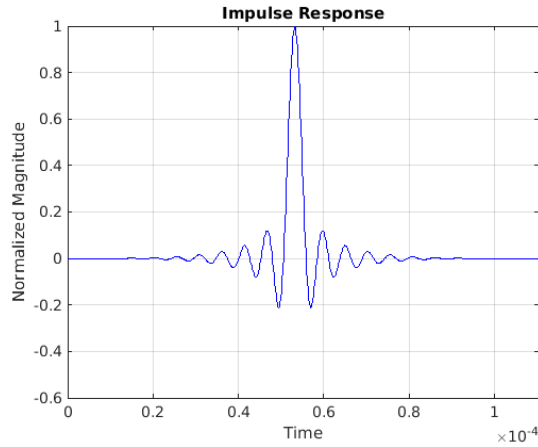
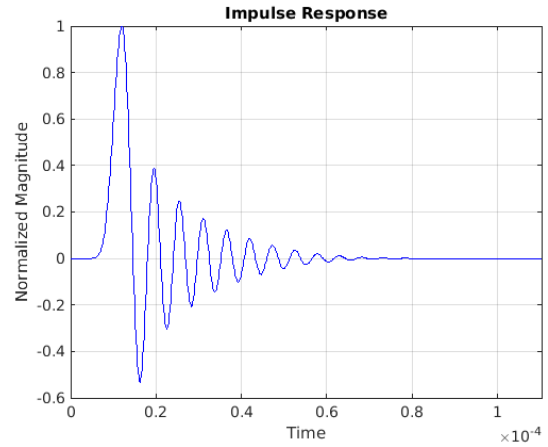
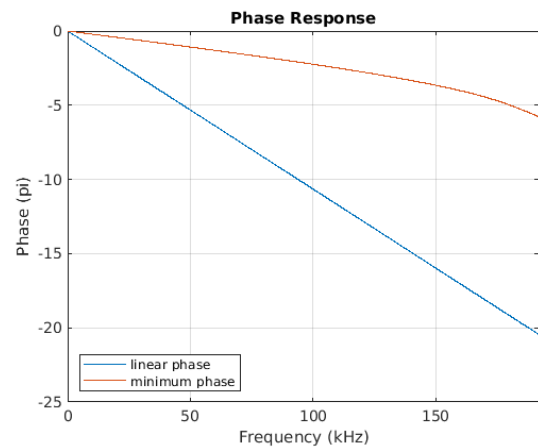
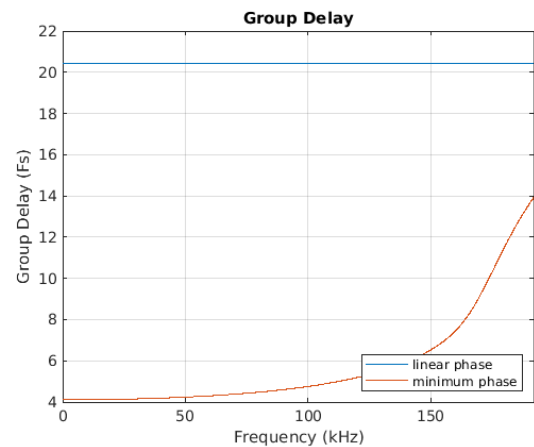
**ADC Filter Response—Slow Roll-Off, 48 kHz Sample Rate**

**Figure 7-13. Passband Magnitude**

**Figure 7-14. Stopband Magnitude**

**Figure 7-15. Impulse Response—Linear Phase**

**Figure 7-16. Impulse Response—Minimum Phase**

**Figure 7-17. Phase vs. Frequency**

**Figure 7-18. Group Delay vs. Frequency**

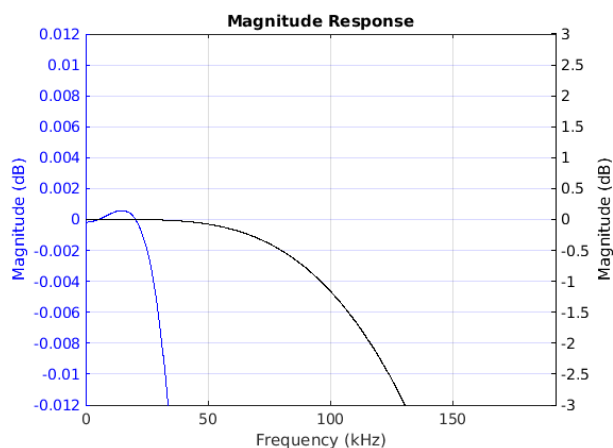
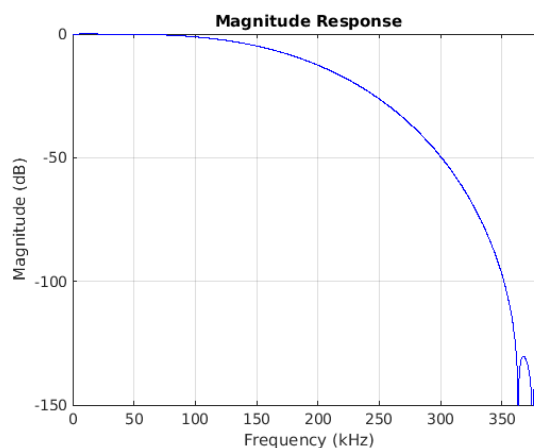
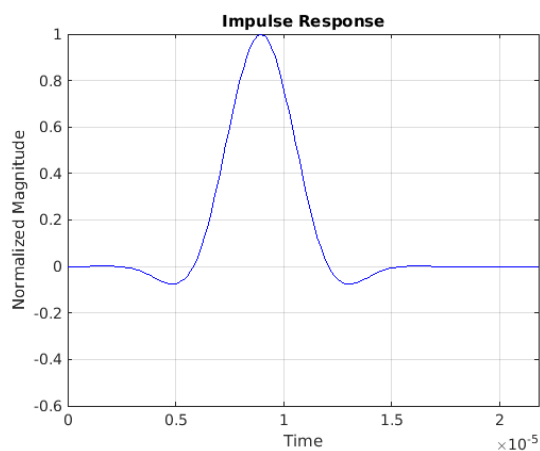
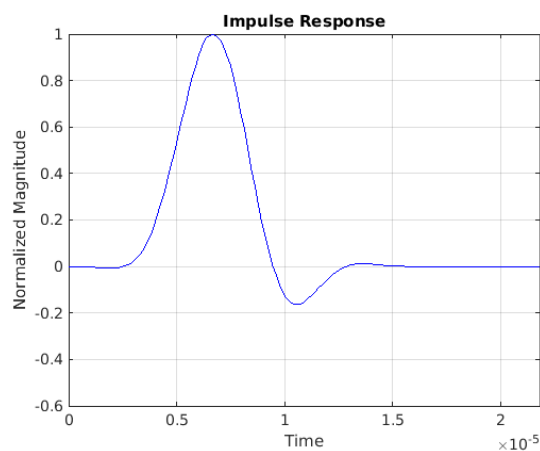
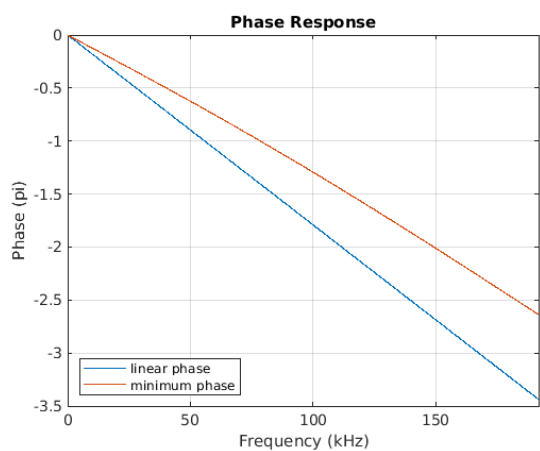
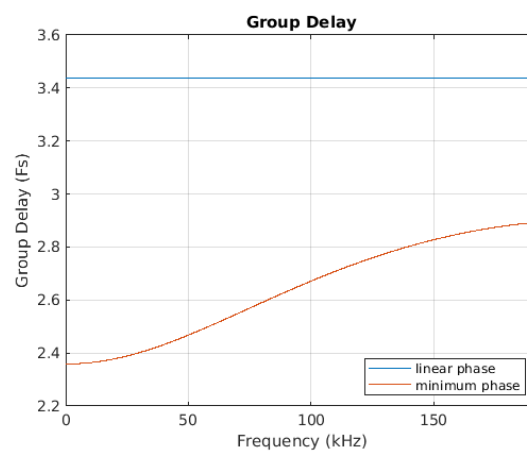
**ADC Filter Response—Fast Roll-Off, 96 kHz Sample Rate**

**Figure 7-19. Passband Magnitude**

**Figure 7-20. Stopband Magnitude**

**Figure 7-21. Impulse Response—Linear Phase**

**Figure 7-22. Impulse Response—Minimum Phase**

**Figure 7-23. Phase vs. Frequency**

**Figure 7-24. Group Delay vs. Frequency**

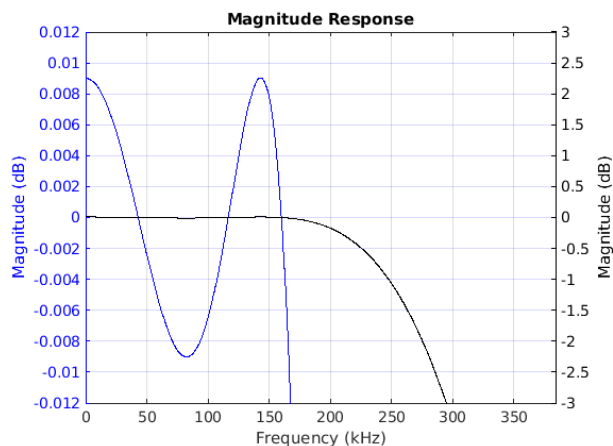
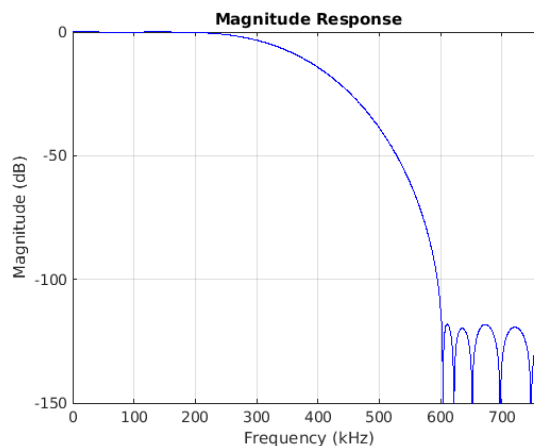
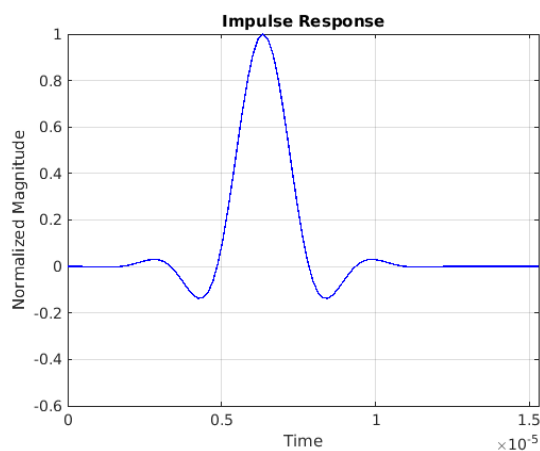
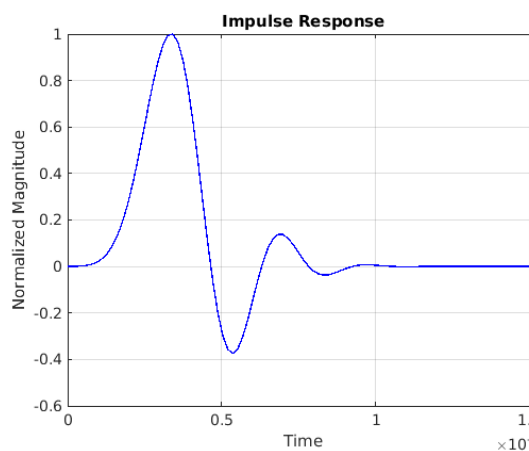
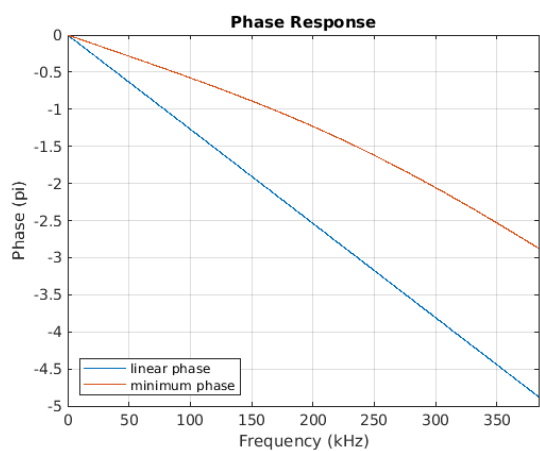
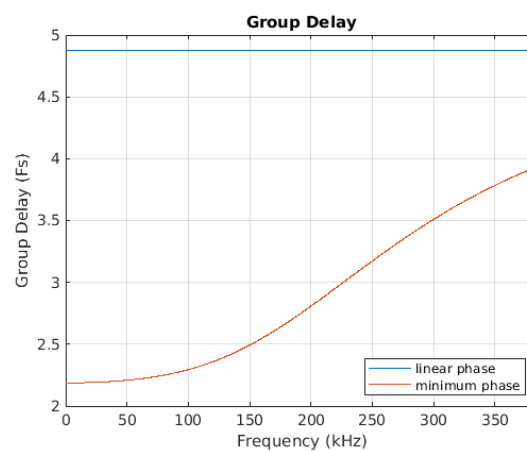
**ADC Filter Response—Slow Roll-Off, 96 kHz Sample Rate**

**Figure 7-25. Passband Magnitude**

**Figure 7-26. Stopband Magnitude**

**Figure 7-27. Impulse Response—Linear Phase**

**Figure 7-28. Impulse Response—Minimum Phase**

**Figure 7-29. Phase vs. Frequency**

**Figure 7-30. Group Delay vs. Frequency**

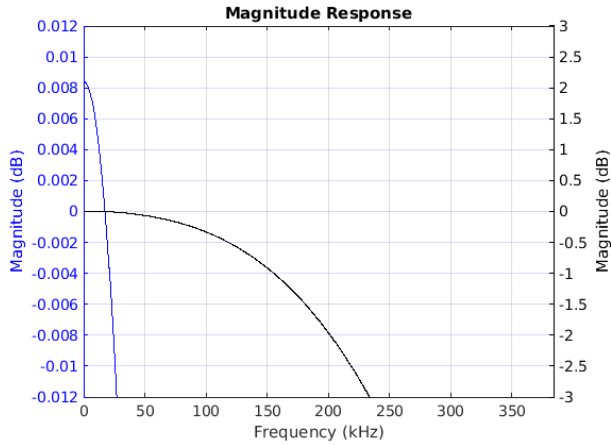
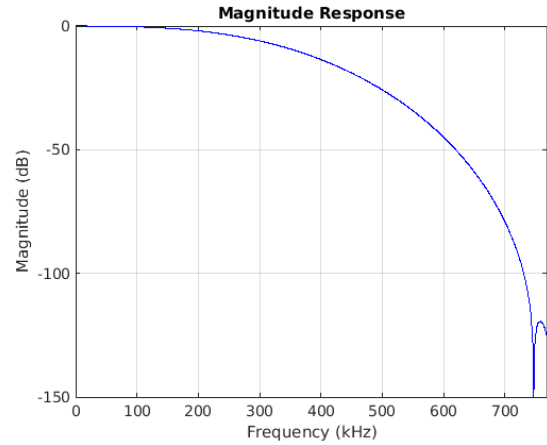
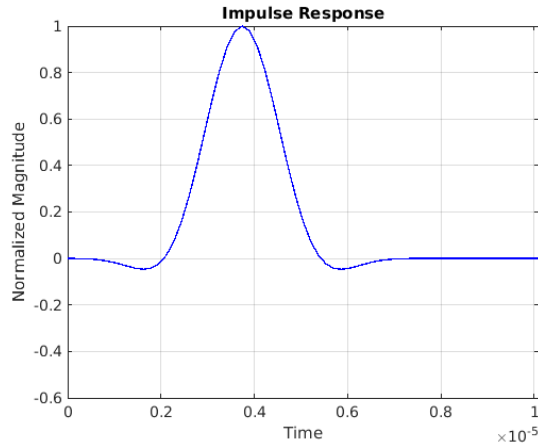
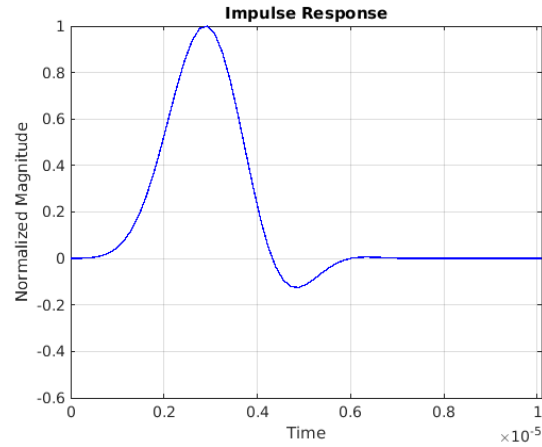
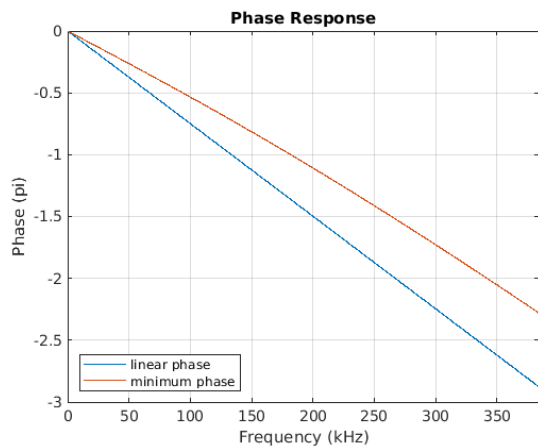
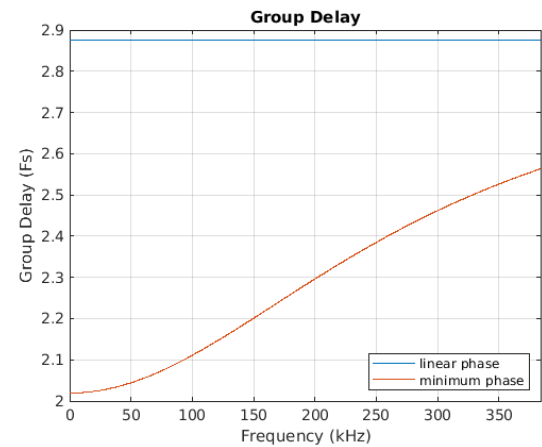
**ADC Filter Response—Fast Roll-Off, 192 kHz Sample Rate**

**Figure 7-31. Passband Magnitude**

**Figure 7-32. Stopband Magnitude**

**Figure 7-33. Impulse Response—Linear Phase**

**Figure 7-34. Impulse Response—Minimum Phase**

**Figure 7-35. Phase vs. Frequency**

**Figure 7-36. Group Delay vs. Frequency**

**ADC Filter Response—Slow Roll-Off, 192 kHz Sample Rate**

**Figure 7-37. Passband Magnitude**

**Figure 7-38. Stopband Magnitude**

**Figure 7-39. Impulse Response—Linear Phase**

**Figure 7-40. Impulse Response—Minimum Phase**

**Figure 7-41. Phase vs. Frequency**

**Figure 7-42. Group Delay vs. Frequency**

**ADC Filter Response—Fast Roll-Off, 384 kHz Sample Rate**

**Figure 7-43. Passband Magnitude**

**Figure 7-44. Stopband Magnitude**

**Figure 7-45. Impulse Response—Linear Phase**

**Figure 7-46. Impulse Response—Minimum Phase**

**Figure 7-47. Phase vs. Frequency**

**Figure 7-48. Group Delay vs. Frequency**

**ADC Filter Response—Slow Roll-Off, 384 kHz Sample Rate**

**Figure 7-49. Passband Magnitude**

**Figure 7-50. Stopband Magnitude**

**Figure 7-51. Impulse Response—Linear Phase**

**Figure 7-52. Impulse Response—Minimum Phase**

**Figure 7-53. Phase vs. Frequency**

**Figure 7-54. Group Delay vs. Frequency**

**ADC Filter Response—Fast Roll-Off, 768 kHz Sample Rate**

**Figure 7-55. Passband Magnitude**

**Figure 7-56. Stopband Magnitude**

**Figure 7-57. Impulse Response—Linear Phase**

**Figure 7-58. Impulse Response—Minimum Phase**

**Figure 7-59. Phase vs. Frequency**

**Figure 7-60. Group Delay vs. Frequency**

**ADC Filter Response—Slow Roll-Off, 768 kHz Sample Rate**

**Figure 7-61. Passband Magnitude**

**Figure 7-62. Stopband Magnitude**

**Figure 7-63. Impulse Response—Linear Phase**

**Figure 7-64. Impulse Response—Minimum Phase**

**Figure 7-65. Phase vs. Frequency**

**Figure 7-66. Group Delay vs. Frequency**

## 8 Thermal Characteristics

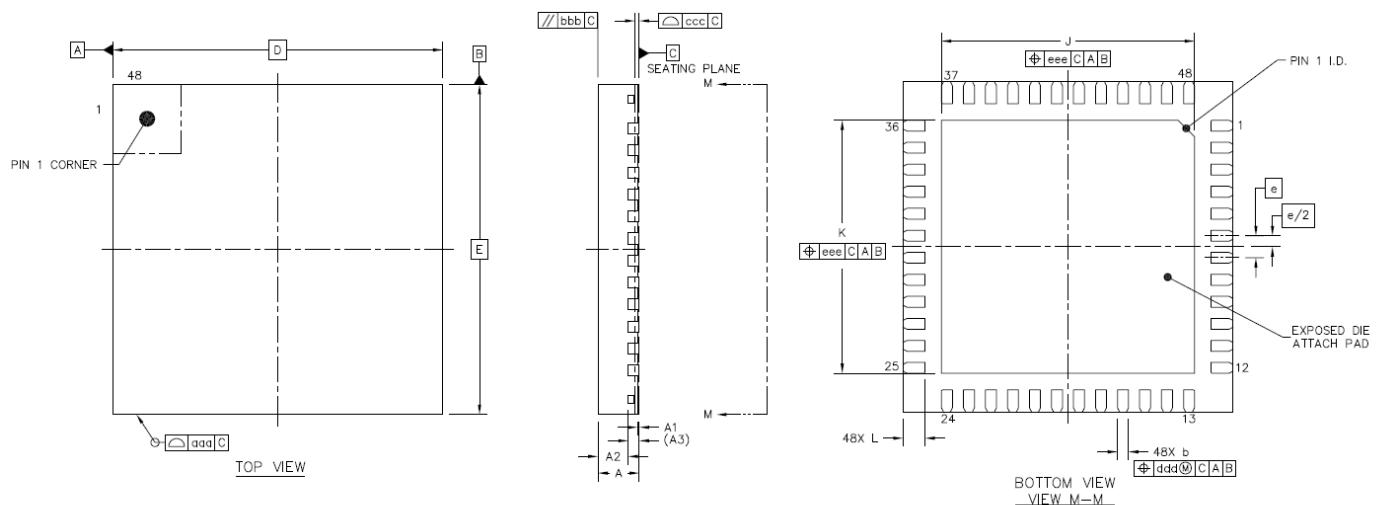
**Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics**

| Parameter                                                  | Symbol        | QFN   | Units |
|------------------------------------------------------------|---------------|-------|-------|
| Junction-to-ambient thermal resistance                     | $\theta_{JA}$ | 20.03 | °C/W  |
| Junction-to-board thermal resistance                       | $\theta_{JB}$ | 7.75  | °C/W  |
| Junction-to-case (top) thermal resistance                  | $\theta_{JC}$ | 45.5  | °C/W  |
| Junction-to-board thermal-characterization parameter       | $\Psi_{JB}$   | 7.38  | °C/W  |
| Junction-to-package-top thermal-characterization parameter | $\Psi_{JT}$   | 1.83  | °C/W  |

**Notes:**

- Natural convection at the maximum recommended operating temperature  $T_A$  (see [Table 3-2](#))
- Four-layer, 2s2p PCB as specified by JESD51-9 and JESD51-11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51-12

## 9 Package Dimensions



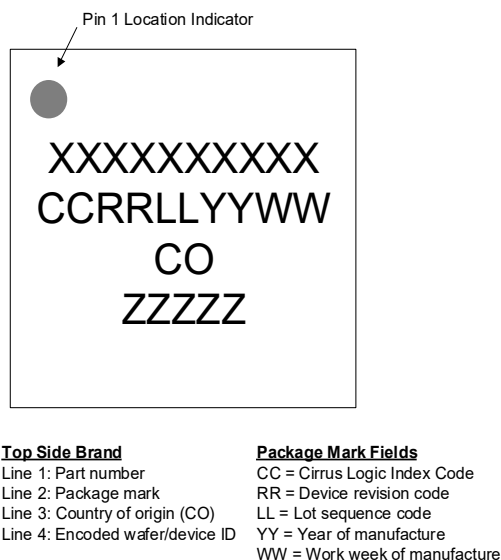
|                        |   | SYMBOL | MIN       | NOM   | MAX  |
|------------------------|---|--------|-----------|-------|------|
| TOTAL THICKNESS        |   | A      | 0.7       | 0.75  | 0.8  |
| STAND OFF              |   | A1     | 0         | 0.035 | 0.05 |
| MOLD THICKNESS         |   | A2     | ----      | 0.55  | ---- |
| L/F THICKNESS          |   | A3     | 0.203 REF |       |      |
| LEAD WIDTH             |   | b      | 0.15      | 0.2   | 0.25 |
| BODY SIZE              | X | D      | 6 BSC     |       |      |
|                        | Y | E      | 6 BSC     |       |      |
| LEAD PITCH             |   | e      | 0.4 BSC   |       |      |
| EP SIZE                | X | J      | 4.5       | 4.6   | 4.7  |
|                        | Y | K      | 4.5       | 4.6   | 4.7  |
| LEAD LENGTH            |   | L      | 0.35      | 0.4   | 0.45 |
| PACKAGE EDGE TOLERANCE |   | aaa    | 0.1       |       |      |
| MOLD FLATNESS          |   | bbb    | 0.1       |       |      |
| COPLANARITY            |   | ccc    | 0.08      |       |      |
| LEAD OFFSET            |   | ddd    | 0.1       |       |      |
| EXPOSED PAD OFFSET     |   | eee    | 0.1       |       |      |
|                        |   |        |           |       |      |
|                        |   |        |           |       |      |
|                        |   |        |           |       |      |
|                        |   |        |           |       |      |

**NOTES**

- 1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
- 2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.

**Figure 9-1. QFN Package Drawing**

## 10 Package Marking



**Figure 10-1. Package Marking**

## 11 Ordering Information

**Table 11-1. Ordering Information**

| Product | Description                       | Package    | RoHS Compliant | Grade      | Temperature Range | Container     | Orderable Part Number |
|---------|-----------------------------------|------------|----------------|------------|-------------------|---------------|-----------------------|
| CS5302P | High Performance Stereo Audio ADC | 48-pin QFN | Yes            | Commercial | –40 to +85°C      | Tray          | CS5302P–DN            |
| CS5302P | High Performance Stereo Audio ADC | 48-pin QFN | Yes            | Commercial | –40 to +85°C      | Tape and Reel | CS5302P–DNR           |

## 12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, <http://www.nxp.com>

## 13 Revision History

**Table 13-1. Revision History**

| Revision       | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A2<br>JUN 2023 | <ul style="list-style-type: none"> <li>Initial publication</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| A3<br>MAY 2024 | <ul style="list-style-type: none"> <li>Added ADC_FILT_N connection to GND (<a href="#">Fig. 2-1</a>)</li> <li>Removed specific component recommendation for input-buffer op-amp (<a href="#">Fig. 2-1</a>)</li> <li>Noted measurement bandwidth for all specifications (<a href="#">Table 3-1</a>)</li> <li>Input impedance updated (<a href="#">Table 3-4</a>)</li> <li>Updated minimum SPI idle duration (<a href="#">Table 3-13</a>)</li> <li>Ordering information updated for automotive-grade parts (<a href="#">Section 11</a>)</li> </ul> |

**Table 13-1. Revision History (Cont.)**

| Revision       | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A4<br>JUL 2024 | <ul style="list-style-type: none"> <li>Updated VDD_D reset threshold (<a href="#">Table 3-9</a>)</li> <li>Updated “fsb” references to “fs(base)” (<a href="#">Section 4.2</a>, <a href="#">Section 4.4.1</a>)</li> <li>Removed constraint on duration of MCLK interruption (<a href="#">Section 4.4.1</a>, <a href="#">Section 4.4.2</a>)</li> <li>Add clip-detect function (<a href="#">Section 4.5.3</a>)</li> <li>Fixed glitch behavior of HGC_CS if update all HGC bit patterns are zero length (<a href="#">Section 4.5.4.1</a>)</li> <li>Removed requirement to check HGC is idle before disabling ADCs (<a href="#">Section 4.5.1</a>)</li> <li>Removed restriction on updating HGC channels while ADCs are enabled (<a href="#">Section 4.5.4.3</a>)</li> <li>Clarification of <math>\theta_{JC}</math> definition (<a href="#">Section 8</a>)</li> <li>Orderable part numbers updated (<a href="#">Section 11</a>)</li> </ul> |
| A5<br>DEC 2024 | <ul style="list-style-type: none"> <li>Typical connections updated (<a href="#">Section 2</a>)</li> <li>Thermal characteristics updated (<a href="#">Section 8</a>)</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

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