CDB-CLOCKING

Hazelburn System (CDB-CLOCKING) User Guide

Introduction

The Hazelburn system (CDB-CLOCKING-MB with daughter cards) is the development platform for the Cirrus Logic high-performance clocking devices CS2500, CS2501 and CS2600. It supports clock inputs and clock outputs and allows configuration and programming for a variety of possible use cases. This document describes the features and usage of the Hazelburn system.

The CDB-CLOCKING-MB is the motherboard of the development platform; this board provides all clock I/O connectors, control switches, power supplies and control-interface hardware. This user guide also details how to connect the CDB2600-DC-SD and CDB250X-DC-SD daughter cards onto a Hazelburn system and how to get started. Real-time control of the devices is supported using the SoundClear Studio tool.

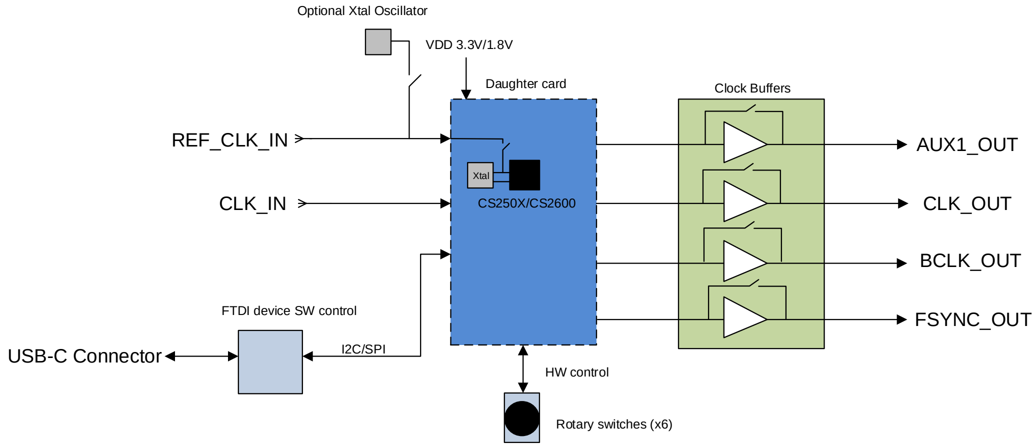

Figure 1: Hazelburn System - High Level Block Diagram

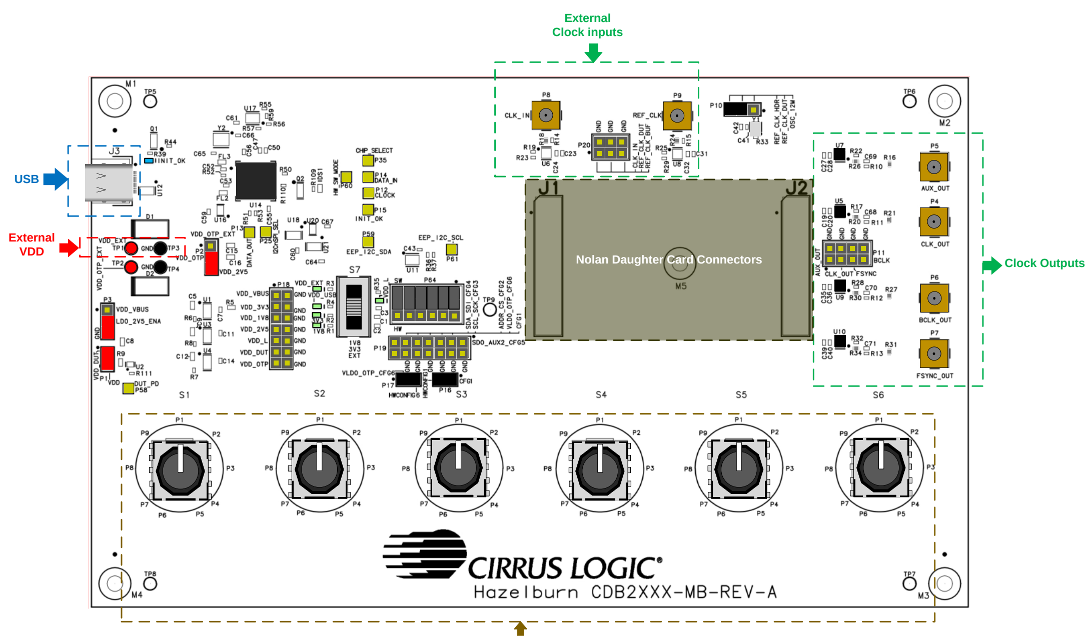

Figure 2: Hazelburn System - Board Overview

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1 Hardware Connections

1.1 USB & Power Connection

The Hazelburn system is powered and controlled via a single USB connection. An FTDI device supports the I2C/SPI communications to control device and board via the USB connection.

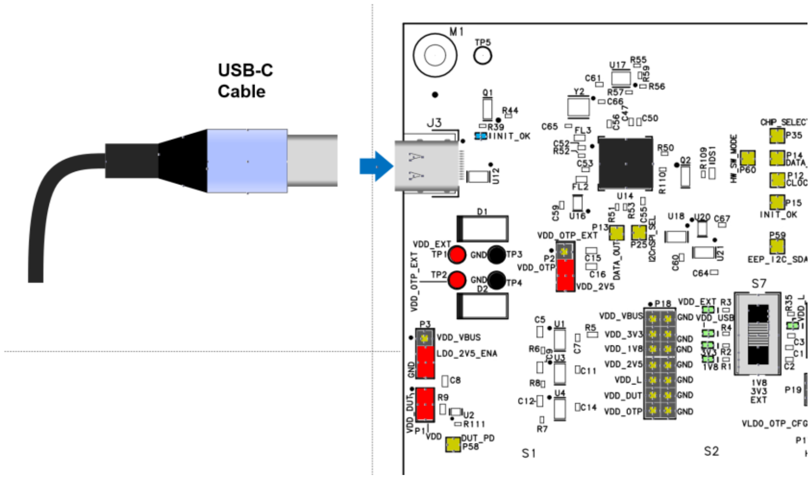


Figure 3: Hazelburn system with USB connection.

1.2 Power Options

The Hazelburn system generates all the required supplies from the USB 5 V supply rail. A VDD supply of 3.3 V or 1.8 V is provided to the daughter card on J1 and J2. Alternatively, the VDD power domain can be provided from an external supply via test points TP1 and TP3 (GND).

Caution:

When connecting external power supplies, ensure that the supplies are disabled before connecting to the Hazelburn system.

1.2.1 USB power supply with VDD 3.3V

If slider switch S7 selects “3V3”, the Hazelburn system provides a VDD supply of 3.3V to the daughter card on J1 and J2. This is the default setting of the Hazelburn system.

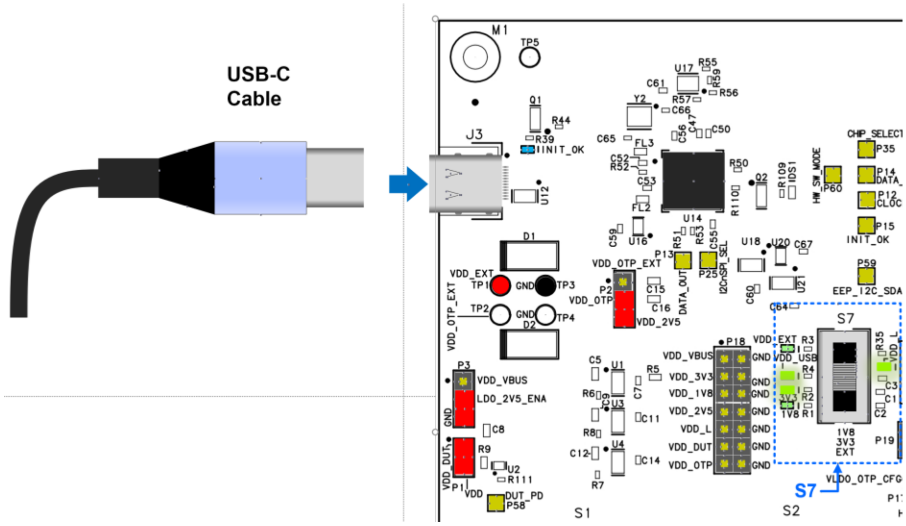


Figure 4: USB power supply with VDD 3.3V

1.2.2 USB power supply with VDD 1.8V

If slider switch S7 selects “1V8”, the Hazelburn system provides a VDD supply of 1.8V to the daughter card on J1 and J2. <u>Note the incorrect silk screen at S7.</u>

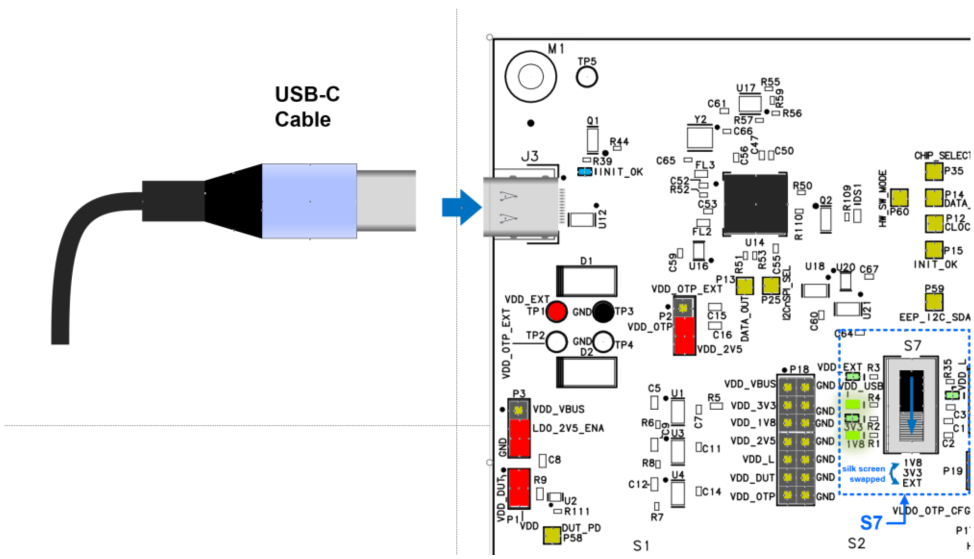


Figure 5: USB power supply with VDD 1.8V

1.2.3 External VDD (1.8–3.3 V) Supply

If slider switch S7 selects "VDD_EXT", an external source (1.8–3.3 V) can be used to provide power to the daughtercard using test points TP1 (VDD_EXT) and TP3 (GND). Note the incorrect silk screen at S7.

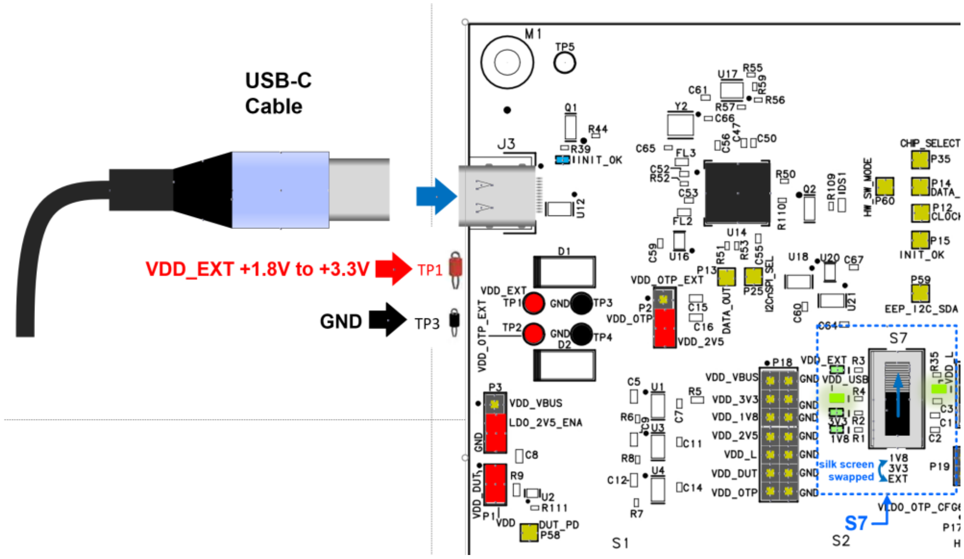


Figure 6: External VDD_EXT Supply

1.2.4 VDD current measurement

Jumper link P1 can be used to measure current of the VDD supply to the DUT on the daughter card.

Note that P1 measures the current supply of the DUT only.

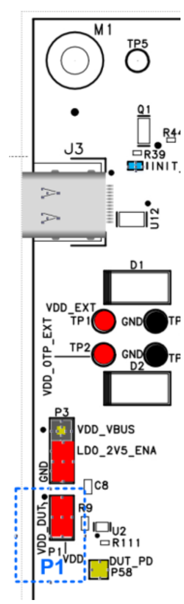


Figure 7: VDD Current Measurement

1.3 Clock Inputs/Outputs

1.3.1 Input Clocks

The DUT requires a clock input (CLK_IN) and a frequency reference (REF_CLK). The clock input (CLK_IN) is supported on SMB connector P8.

The frequency reference (REF_CLK) is provided by a 12 MHz crystal on the daughter card by default. Alternatively, an external reference can be provided via SMB connector P9, or a 12 MHz crystal oscillator on the motherboard can be used.

The selection of the REF_CLK source on the motherboard is described in Section 1.3.1.1. See also Section 2.4 for the associated configuration requirements on the daughtercard and for additional REF_CLK source options.

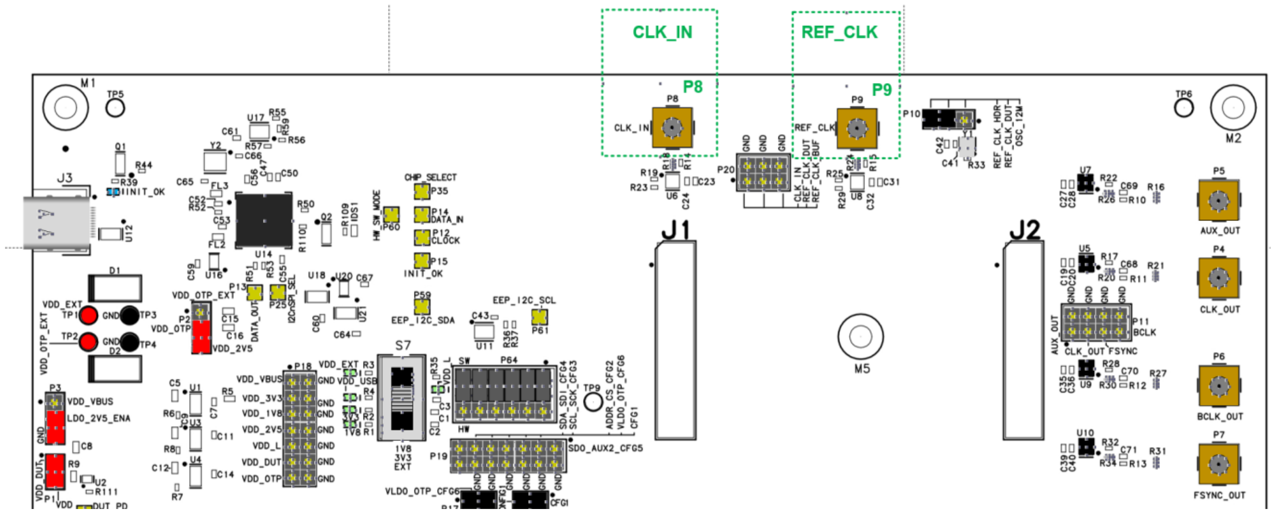


Figure 8: Input clocks CLK_IN and REF_CLK

1.3.1.1 REF_CLK Source – External Reference or 12 MHz Crystal Oscillator

The REF_CLK source is configured on the motherboard using link P10. In the “REF_CLK_HDR” position (default), the external reference is supported on SMB connector P9. In the “OSC_12M” position, the on-board crystal oscillator is selected. Note the daughtercard must also be configured as described in Section 2.4.

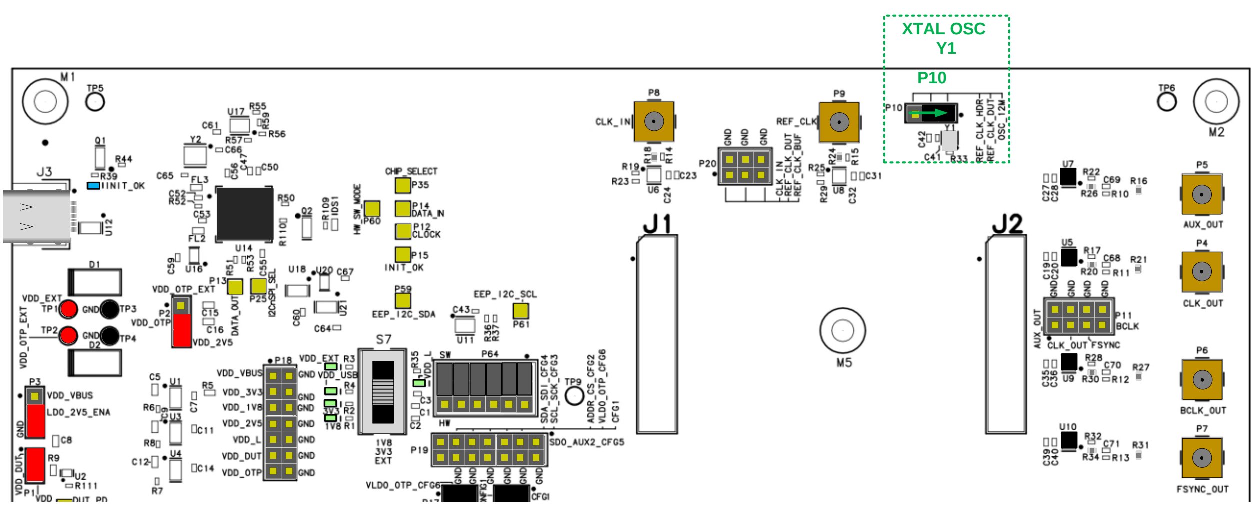


Figure 9: REF_CLK Source Selection

1.3.2 Output Clocks

The Hazelburn system supports output clocks on SMB connectors P4, P5, P6, and P7.

The main output clock (CLK_OUT) is provided on connector P4; an optional clock/signal output (AUX_OUT) is provided on P5; the optional BCLK output (BCLK_OUT) on P6, and the optional FSYNC output (FSYNC_OUT) on P7. Note that BCLK_OUT and FSYNC_OUT are only supported when using a CS2600 device.

Output buffers are incorporated for AUX_OUT, CLK_OUT, BCLK_OUT and FSYNC_OUT.

Test point (CLK_OUT) on P11 is connected directly to the DUT output and can be used to measure jitter or phase noise.

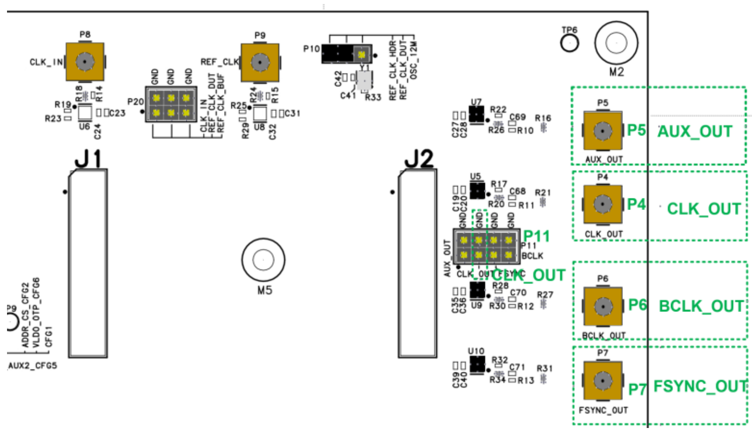


Figure 10: Output Clocks CLK_OUT, AUX_OUT, BCLK_OUT, FSYNC_OUT

1.3.2.1 Output Clock Buffers

Output buffers U7, U5, U9 and U10 are provided for AUX_OUT, CLK_OUT, BCLK_OUT and FSYNC_OUT on the Hazelburn system. The clock buffers are enabled by default but can be disabled if not required.

- To disable the AUX_OUT buffer, move the 33 Ω resistor R16 to position R10, and remove resistor R26.
- To disable the CLK_OUT buffer, move the 33 Ω resistor R21 to position R11, and remove resistor R20.
- To disable the BCLK_OUT buffer, move the 33 Ω resistor R27 to position R12, and remove resistor R30.
- To disable the FSYNC_OUT buffer, move the 33 Ω resistor R31 to position R13, and remove resistor R34.

The Hazelburn provides the same VDD supply for the clock buffers as for the DUT on the daughter card.

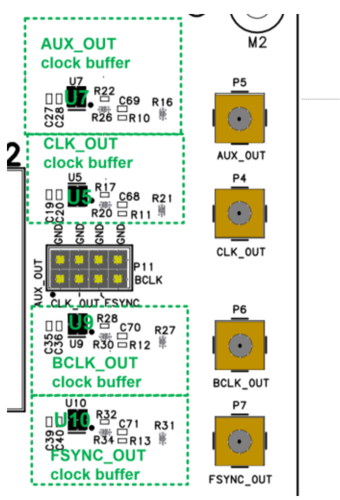


Figure 11: Output clocks buffers AUX_OUT, CLK_OUT, BCLK_OUT and FSYNC_OUT

1.4 LED Indicators

Status LEDs on the Hazelburn motherboard indicate the current state of operation.

Table 1: Hazelburn LED Indicators

Refdes	Color	Name	Normally Lit?	Description
1V8	Green	1V8	Yes	Indicates if the 1.8V supply is enabled
3V3	Green	3V3	Yes	Indicates if the 3.3V supply is enabled
VDD_EXT	Green	VDD_EXT	Yes	Indicates if the external VDD_EXT (3.3V) supply is enabled, when VDD_EXT is 1.8V, the LED is off due to a bug.
USB_VDD	Green	USB_VDD	Yes	Indicates if the USB_VDD 5V supply is enabled
VDD_L	Green	VDD_L	Yes	Indicates if the VDD supply (3.3V) to the daughtercard is enabled, when VDD_L is 1.8V, the LED is off due to a bug.
INIT_OK	Blue	INIT_OK	Yes	Indicates the FTDI device has initialized correctly

1.5 Jumper Links

Jumper links are provided on the Hazelburn motherboard; these are related to signal routing and power supply rails. The default jumper configuration is illustrated in Figure 12.

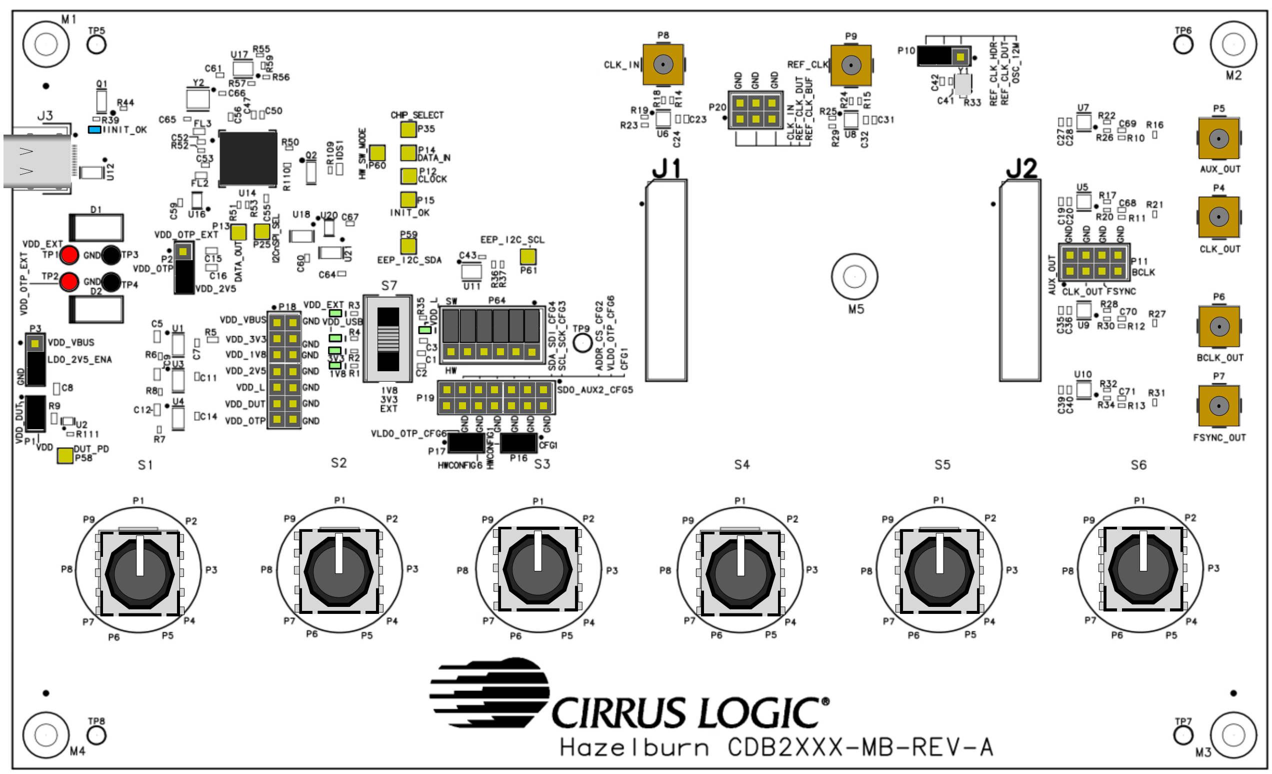


Figure 12: Hazelburn Jumper Links

2 Daughter Cards

The Hazelburn system works with interchangeable daughter cards to support a variety of clocking devices.

Caution:

Daughter cards should not be inserted or removed while the Hazelburn system is powered or with external clock generators enabled. Fully disconnect or power down external power supply and disable or remove external clock generators before changing daughter cards.

The daughter cards are connected to the Hazelburn board as shown below:

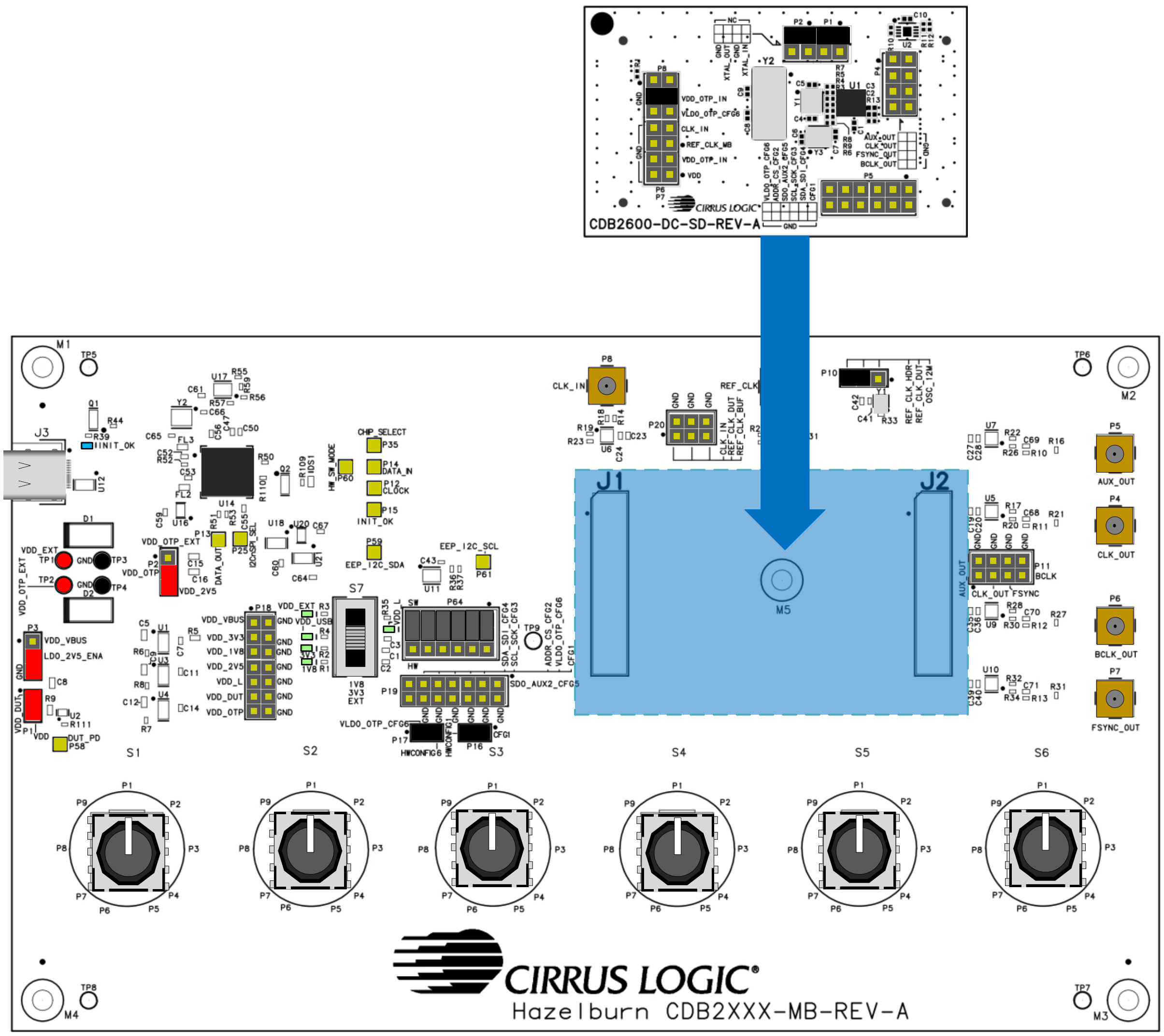


Figure 13: How to Connect Daughter Cards to Hazelburn System

The CDB2600-DC-SD is a 2-header daughter card and should be plugged onto J1 and J2. The daughter card connectors are keyed and can only plugged in one way.

2.1 CDB2600-DC-SD Daughter Card

The CDB2600-DC-SD is a daughter card for the Hazelburn system for high-performance clocking devices. This board incorporates a CS2600 device.

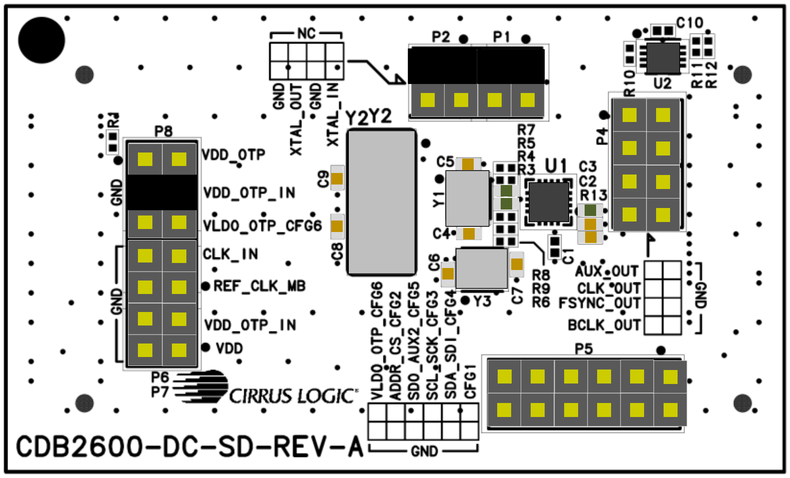


Figure 14: CDB2600-DC-SD Daughter Card

2.2 CDB2500-DC-SD Daughter Card

The CDB2500-DC-SD is a daughter card for the Hazelburn system for high-performance clocking devices. This board incorporates a CS2500 device.

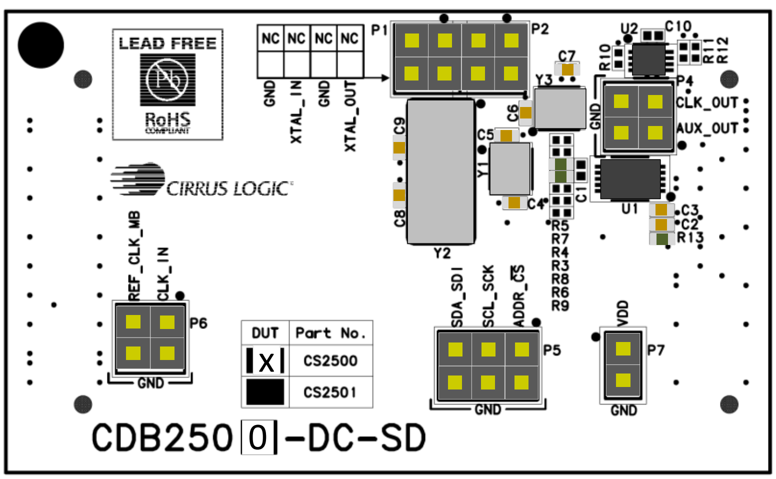


Figure 15: CDB2500-DC-SD Daughter Card

2.3 CDB2501-DC-SD Daughter Card

The CDB2501-DC-SD is a daughter card for the Hazelburn system for high-performance clocking devices. This board incorporates a CS2501 device.

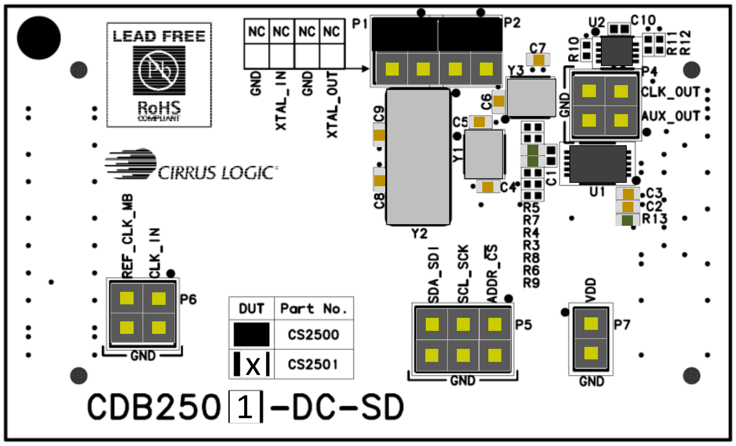


Figure 16: CDB2501-DC-SD Daughter Card

2.4 Reference Clock Selection – Crystal, External Reference, or Internal LCO

The frequency reference (REF_CLK) is provided by a 12 MHz crystal (Y1) on the daughter card by default. Alternative sources for REF_CLK are configured using 0 Ω resistor links and PCB jumper connections.

The daughter card configuration for each option is described as follows.

- The 12 MHz crystal Y1 on the daughter card is the default REF_CLK source. The part number of the crystal is *NX3225SA-12.000M-STD-CRS-2* (SMD/SMT crystal); further information can be found in the crystal datasheet.

  The daughter card configuration (default) is R3, R4 populated (0 Ω); R5, R6, R7, R8, R9 non-populated.

  The configuration is illustrated in Figure 17 for CDB2600-DC-SD; the same is applicable for CDB250X-DC-SD.

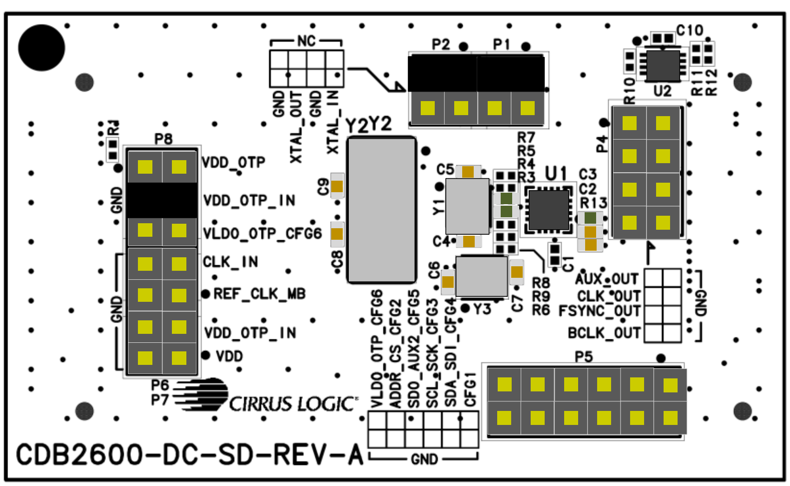


Figure 17: Daughter Card with Crystal Y1 Reference Clock Option (R3 and R4)

- The REF_CLK can be provided from the Hazelburn motherboard (CDB-CLOCKING-MB). This can be either an external signal via connector P9, or the 12 MHz crystal oscillator on the motherboard. See Section 1.3.1.1 to configure the motherboard for the required option.

  The daughter card configuration is R9 populated (0 Ω); R3, R4, R5, R6, R7, R8 non-populated.

  The configuration is illustrated in Figure 18 for CDB2600-DC-SD; the same is applicable for CDB250X-DC-SD.

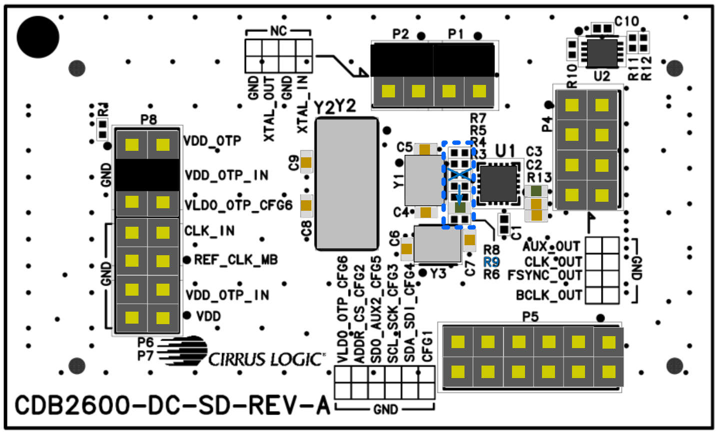


Figure 18: Daughter Card with External Reference Clock Option (R9)

- The REF_CLK can be provided from the internal LCO of the CS2600 or CS2501. This option is configured by moving jumpers P1 and P2 to positions 2 and 4.

  The configuration is illustrated in Figure 19 for CDB2600-DC-SD; the same is applicable for CDB2501-DC-SD.

  Note the internal LCO is not supported on the CS2500 device.

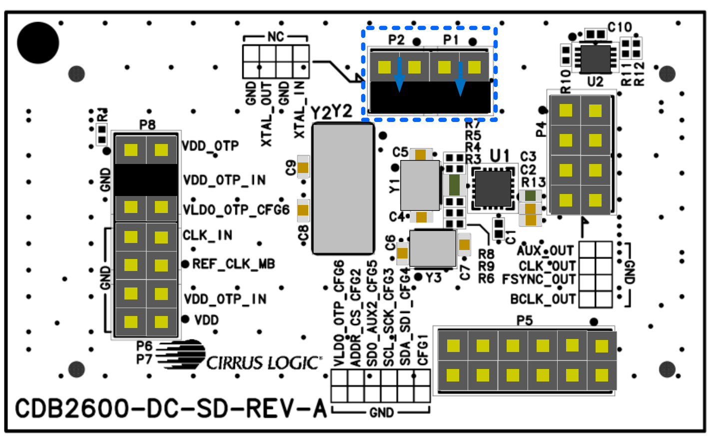


Figure 19: Daughter Card with Internal LCO Reference Clock Option

- The REF_CLK can be provided from the 12 MHz crystal Y2 on the daughter card. The part number of the crystal is *ECS-120-18-4X-CKM* (through-hole crystal); further information can be found in the crystal datasheet.

  Crystal Y2 is provided in a socketed connector; other pin-compatible through-hole crystals can also be substituted.

  The daughter card configuration is R7, R8 populated (0 Ω); R3, R4, R5, R6, R9 non-populated.

  The configuration is illustrated in Figure 20 for CDB2600-DC-SD; the same is applicable for CDB250X-DC-SD.

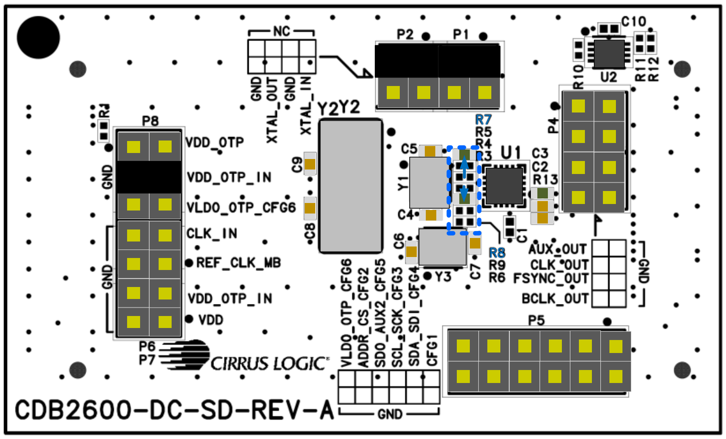


Figure 20: Daughter Card with Crystal Y2 Reference Clock Option (R7 and R8)

- The REF_CLK can be provided from the 12 MHz crystal Y3 on the daughter card. The part number of the crystal is *ECS-120-8-33Q-RES-TR* (SMD/SMT crystal); further information can be found in the crystal datasheet.

  The daughter card configuration is R5, R6 populated (0 Ω); R3, R4, R7, R8, R9 non-populated.

  The configuration is illustrated in Figure 21 for CDB2600-DC-SD; the same is applicable for CDB250X-DC-SD.

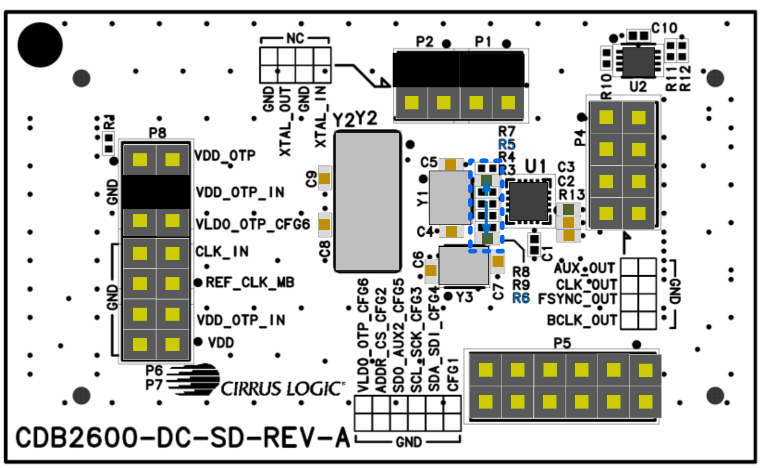


Figure 21: Daughter Card with crystal Y3 as reference clock option (R5 and R6)

3 Hardware Mode Control (with CDB2600-DC-SD only)

3.1 Hardware Mode Control

The CS2600 supports Hardware Control Mode, where the device configuration is determined by external resistors connected to the hardware-control pins CONFIG1 – CONFIG6. The external resistors are connected to GND or VDD; different resistor values allow the CS2600 to detect eight configuration options per pin.

The Hazelburn system supports the hardware control modes (stand-alone) for the CS2600 device. To enable Hardware Control Mode, the P64 jumpers must be moved to the “HW” position; this configuration connects the rotary switches on the motherboard to the hardware-control pins of the CS2600.

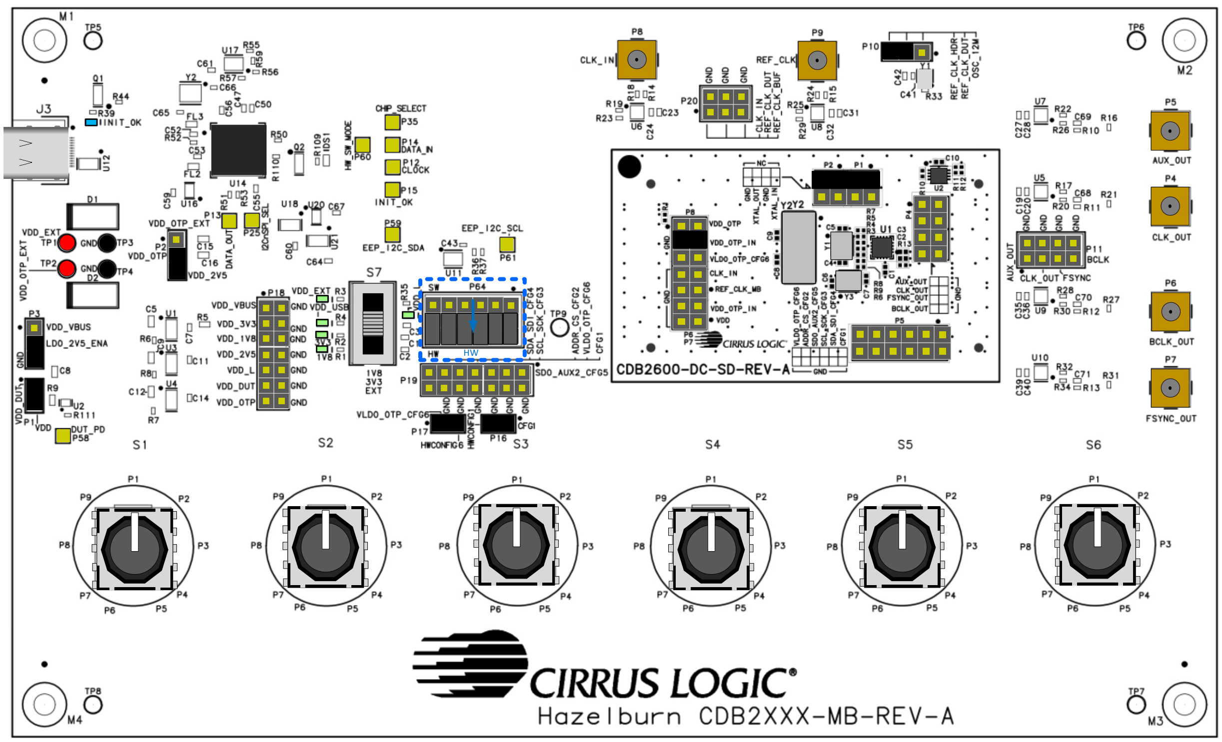
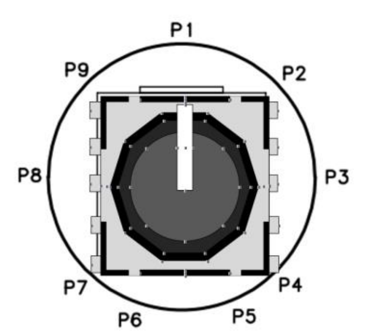


Figure 22: Jumper Configuration (P64) for Hardware Control Mode

The board silkscreen indicates the position of each switch. Each switch position enables a pull resistor on the respective CONFIG pin to VDD or GND. See Table 2 below:

Table 2: Rotary Switch Positions



Switch Position	CONFIG Pin Configuration	
P1	Pull-up to VDD	0 Ω
P2		4.7 kΩ
P3		22 kΩ
P4		100 kΩ
P5	Pull-Down to GND	100 kΩ
P6		22 kΩ
P7		4.7 kΩ
P8		0 Ω
P9	No Connection	—

3.2 Hardware Mode Rotary Switch Settings

The rotary switch functions are described in the following tables. Refer to the CS2600 datasheet for further details of the hardware-mode control options.

The CONFIG1 pin selects the PLL operating mode and the timing-reference clock frequency as shown in Table 3.

Table 3: CONFIG1 Hardware Configuration

Switch Position	Pin Configuration		Operation Mode	Timing Reference Clock (REF_CLK_IN)
P1	Pull-up to VDD	0 Ω	Synthesizer	10 MHz
P2		4.7 kΩ		25 MHz
P3		22 kΩ		24.576 MHz
P4		100 kΩ		49.152 MHz
P5	Pull-Down to GND	100 kΩ	Multiplier	8 – 18 MHz
P6		22 kΩ		16 – 37.5 MHz
P7		4.7 kΩ		32 – 75 MHz
P8		0 Ω	Software control mode (I2C/SPI)	
P9	No Connection	—		

In Multiplier Mode, the remaining CONFIGx pin functions are described in Section 3.2.1.

In Synthesizer Mode, the remaining CONFIGx pin functions are described in Section 3.2.2.

3.2.1 Multiplier Mode

The CONFIG2 pin selects Holdover Mode, PLL bandwidth, and the AUX1_OUT function as shown in Table 4.

Table 4: CONFIG2 Hardware Configuration—Multiplier Mode

Switch Position	Pin Configuration		Holdover Mode	PLL Bandwidth	AUX1 Output
P1	Pull-up to VDD	0 Ω	Enabled	1 Hz	Frequency Unlock Indicator
P2		4.7 kΩ			Phase Unlock Indicator
P3		22 kΩ		128 Hz	Frequency Unlock Indicator
P4		100 kΩ			Phase Unlock Indicator
P5	Pull-Down to GND	100 kΩ	Disabled	1 Hz	Frequency Unlock Indicator
P6		22 kΩ			Phase Unlock Indicator
P7		4.7 kΩ		128 Hz	Frequency Unlock Indicator
P8		0 Ω			Phase Unlock Indicator
P9	No Connection	—			

The CONFIG3 pin selects the clock output configuration as shown in Table 5. The supported configurations are designed for target applications using I2S, LJ/RJ, or TDM serial data interfaces.

Table 5: CONFIG3 Hardware Configuration—Multiplier Mode

Switch Position	Pin Configuration		Phase Alignment	Target Application	Input/Output Configuration		
					CLK_IN	BCLK_OUT	FSYNC_OUT [1]
P1	Pull-up to VDD	0 Ω	Enabled	I2S	Inverted	Inverted	
P2		4.7 kΩ		LJ/RJ	Not Inverted	Inverted	Not Inverted
P3		22 kΩ		TDM-A [2]			
P4		100 kΩ		TDM-B [2]			
P5	Pull-Down to GND	100 kΩ	Disabled	I2S		Inverted	
P6		22 kΩ		LJ/RJ		Inverted	Not Inverted
P7		4.7 kΩ		TDM-A [2]			
P8		0 Ω		TDM-B [2]			
P9	No Connection	—					

1.In TDM applications, the FSYNC duty cycle corresponds to 1 BCLK period. In other formats, the FSYNC duty cycle is 50%.

2.The TDM‑A and TDM‑B selections provide the same inverted/non-inverted behavior. The two options differ from each other in how the BCLK frequency is determined.

The CONFIG4 pin selects the BCLK output frequency as shown in Table 6. Note the pin function is dependent on the target application (see CONFIG3 pin configuration in Table 5).

Table 6. CONFIG4 Hardware Configuration—Multiplier Mode

Switch Position	Pin Configuration		BCLK Frequency			
			I2S	Left-Justified/ Right-Justified	TDM-A	TDM-B
P1	Pull-up to VDD	0 Ω	Invalid			
P2		4.7 kΩ				
P3		22 kΩ				
P4		100 kΩ	64 x FSYNC	64 x FSYNC	1024 x FSYNC	CLK_OUT
P5	Pull-Down to GND	100 kΩ			512 x FSYNC	CLK_OUT/2
P6		22 kΩ			256 x FSYNC	CLK_OUT/4
P7		4.7 kΩ			128 x FSYNC	CLK_OUT/8
P8		0 Ω			64 x FSYNC	CLK_OUT/16
P9	No Connection	—				

Note: Selecting a BCLK frequency referenced to FSYNC can result in an invalid BCLK divider value (depending on the FSYNC and MCLK_OUT frequencies). Refer to the BCLK_DIV field for the supported BCLK divider ratios. If an invalid selection is made, the clock outputs are disabled; normal operation resumes when a valid configuration is detected.

The CONFIG5 pin selects the ARC function and the FSYNC output frequency as shown in Table 7.

Table 7: CONFIG5 Hardware Configuration—Multiplier Mode

Switch Position	Pin Configuration		Automatic Rate Control (ARC)	FSYNC Frequency
P1	Pull-up to VDD	0 Ω	Enabled	CLK_IN
P2		4.7 kΩ	Disabled	CLK_OUT / 1024
P3		22 kΩ		CLK_OUT / 512
P4		100 kΩ		CLK_OUT / 256
P5	Pull-Down to GND	100 kΩ		CLK_OUT / 128
P6		22 kΩ		CLK_OUT / 64
P7		4.7 kΩ		CLK_OUT / 32
P8		0 Ω		CLK_OUT / 16
P9	No Connection	—		

The CONFIG6 pin selects the CLK_OUT frequency as shown in Table 8. Note the pin function is dependent on the ARC status (see CONFIG5 pin configuration in Table 5).

Table 8: CONFIG6 Hardware Configuration—Multiplier Mode

Switch Position	Pin Configuration		CLK_OUT Frequency	
			ARC Disabled	ARC Enabled
P1	Pull-up to VDD	0 Ω	128 x CLK_IN	12.288 or 11.2896 MHz [1]
P2		4.7 kΩ	256 x CLK_IN	24.576MHz or 22.5792 MHz [1]
P3		22 kΩ	512 x CLK_IN	49.152 or 45.1584 MHz [1]
P4		100 kΩ	768 x CLK_IN	Invalid
P5	Pull-Down to GND	100 kΩ	1024 x CLK_IN	
P6		22 kΩ	1536 x CLK_IN	
P7		4.7 kΩ	3072 x CLK_IN	
P8		0 Ω	6144 x CLK_IN	
P9	No Connection	—		

1.The applicable frequency is the same base as CLK_IN

3.2.2 Synthesizer Mode

The CONFIG2 pin selects the AUX1_OUT function as shown in Table 9.

Table 9: CONFIG2 Hardware Configuration—Synthesizer Mode

Switch Position	Config Pin Configuration		AUX1 Output
P1	Pull-up to VDD	0 Ω	Frequency Unlock Indicator
P2		4.7 kΩ	Disabled
P3		22 kΩ	
P4		100 kΩ	
P5	Pull-Down to GND	100 kΩ	
P6		22 kΩ	
P7		4.7 kΩ	
P8		0 Ω	CLK_OUT
P9	No Connection	—	

The CONFIG3 pin has no function in Synthesizer Mode; the pin should be connected to VDD or GND.

The CONFIG4 pin selects the BCLK output frequency as shown in Table 10.

Table 10: CONFIG4 Hardware Configuration—Synthesizer Mode

Switch Position	Config Pin Configuration		BCLK frequency
P1	Pull-up to VDD	0 Ω	CLK_OUT / 16
P2		4.7 kΩ	CLK_OUT / 8
P3		22 kΩ	CLK_OUT / 4
P4		100 kΩ	CLK_OUT / 2
P5	Pull-Down to GND	100 kΩ	CLK_OUT
P6		22 kΩ	Invalid
P7		4.7 kΩ	
P8		0 Ω	
P9	No Connection		—

The CONFIG5 pin selects the FSYNC output frequency as shown in Table 11.

Table 11: CONFIG5 Hardware Configuration—Synthesizer Mode

Switch Position	Config Pin Configuration		FSYNC frequency
P1	Pull-up to VDD	0 Ω	Invalid
P2		4.7 kΩ	CLK_OUT / 1024
P3		22 kΩ	CLK_OUT / 512
P4		100 kΩ	CLK_OUT / 256
P5	Pull-Down to GND	100 kΩ	CLK_OUT / 128
P6		22 kΩ	CLK_OUT / 64
P7		4.7 kΩ	CLK_OUT / 32
P8		0 Ω	CLK_OUT / 16
P9	No Connection		—

The CONFIG6 pin selects the CLK_OUT frequency as shown in Table 12.

Table 12: CONFIG6 Hardware Configuration—Synthesizer Mode

Switch Position	Config Pin Configuration		CLK_OUT frequency
P1	Pull-up to VDD	0 Ω	Invalid
P2		4.7 kΩ	
P3		22 kΩ	11.2896 MHz
P4		100 kΩ	12.288 MHz
P5	Pull-Down to GND	100 kΩ	22.5792 MHz
P6		22 kΩ	24.576 MHz
P7		4.7 kΩ	45.1584 MHz
P8		0 Ω	49.152 MHz
P9	No Connection		—

4 I2C/SPI Software Control

Software control of the Hazelburn system and the connected daughter card is supported via an FTDI device. The system supports I2C and SPI control modes.

5 SoundClear Studio Support

5.1 SoundClear Studio

SoundClear Studio (SCS) is a PC/Mac-based tool used to configure Cirrus Logic devices. The tools suite provides support for evaluation and development and can be used with Hazelburn system and associated daughter cards.

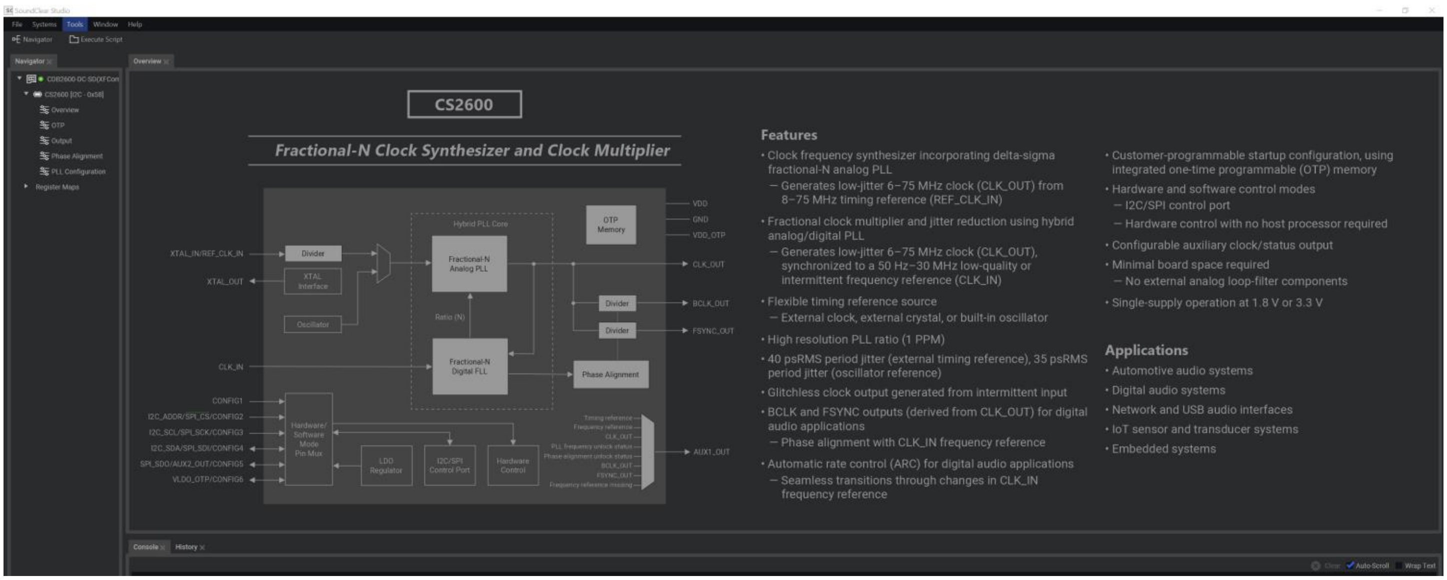


Figure 23: SoundClear Studio

5.1.1 Download SoundClear Studio Software

The latest release of SoundClear Studio software is available on the Cirrus Logic software portal. Please contact your Cirrus Logic representative for access.

Note that, by downloading software from the Cirrus Logic software portal, you agree to the terms of our license agreement; please read the terms before downloading.

5.2 SoundClear Studio Quick Start Guide

5.2.1 Installing Packages

Each daughter card has its own individual SoundClear Studio package that must be installed separately from the main SoundClear Studio Software. These are installed from the main menu using **"File → Install Package..."**. Multiple packages can be installed together by selecting more than one using the file dialog.

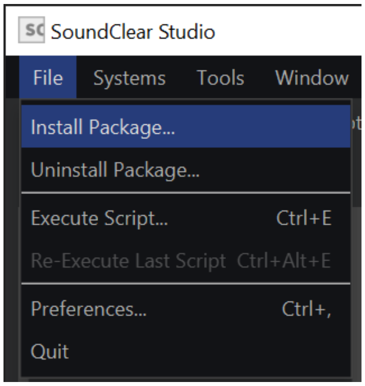


Figure 24: SoundClear Studio – Installing Board Packages

5.2.2 SoundClear Studio User Guide

The SoundClear Studio User Guide can be accessed from the main menu using **"Help → Open Help Contents..."**:

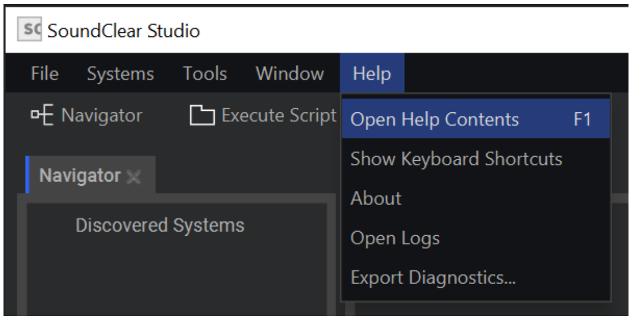


Figure 25: SoundClear Studio – User Guide

5.2.3 Creating a Virtual System

A virtual (non-hardware) version of the system can be created using **"Systems → Add Virtual System..."**. A virtual system enables the user to interact with virtual versions of the device register map and helper panels.

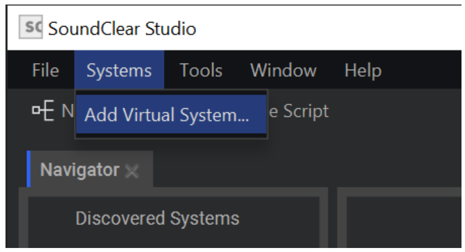


Figure 26: SoundClear Studio – Creating a Virtual System

This opens a dialog to select an installed system (shown here is the CDB2600-DC-SD):

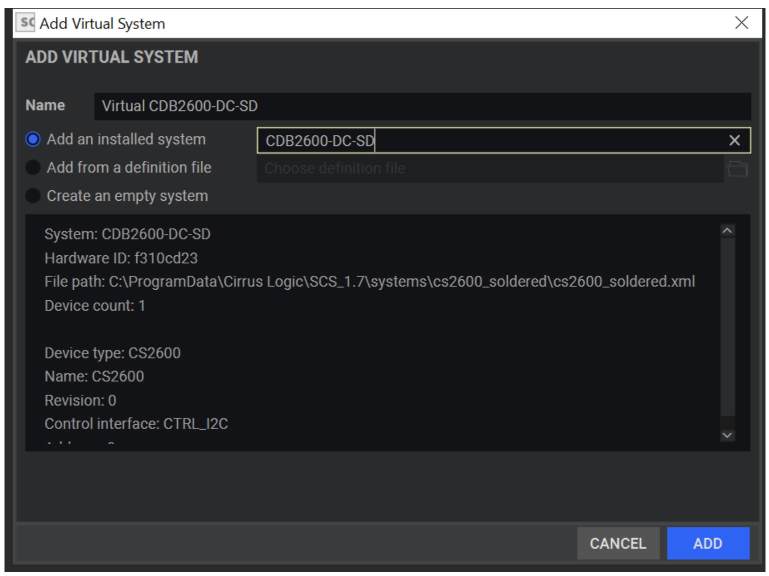


Figure 27: SoundClear Studio – Adding a Virtual System

5.2.4 Adding an Existing System

SoundClear Studio automatically detects board hardware with Cirrus Logic devices. In the event of devices not being detected automatically, a device can be added manually. Right click on the system and select **“Add Device…”**:

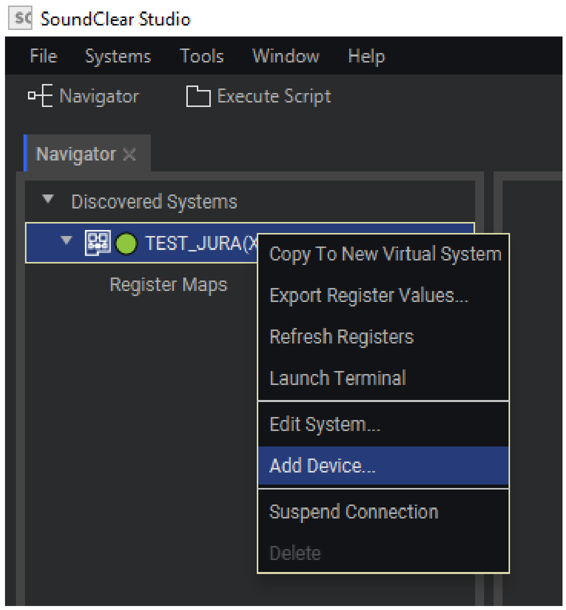


Figure 28: SoundClear Studio – Adding an Existing System

Select the device from those installed, along with the control-interface protocol and address of the part (this can be edited again by right clicking on the device and selected **"Edit Device..."**):

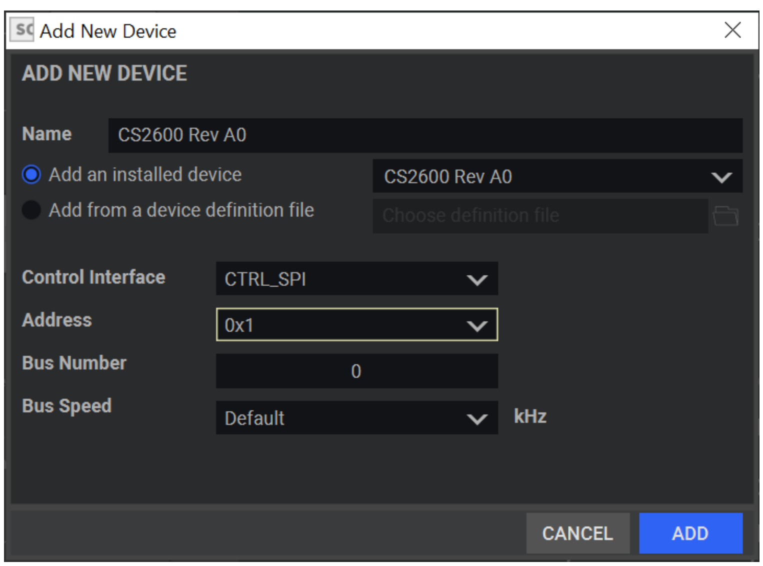


Figure 29: SoundClear Studio – Adding an Existing System

- *I2C address selection on the Hazelburn system with CS2600 is fixed at 0x58 (write), 0x59 (read).*
- *I2C address selection on the Hazelburn system with CS250X is fixed at 0x9E (write), 0x9F (read).*

5.2.5 Executing SoundClear Studio Scripts

SoundClear Studio provides the ability to interact with the device register map using Python scripts. These scripts can sequence register operations to configure the desire into desired states, which can then be executed from SoundClear Studio using **“File→Execute Script…”**:

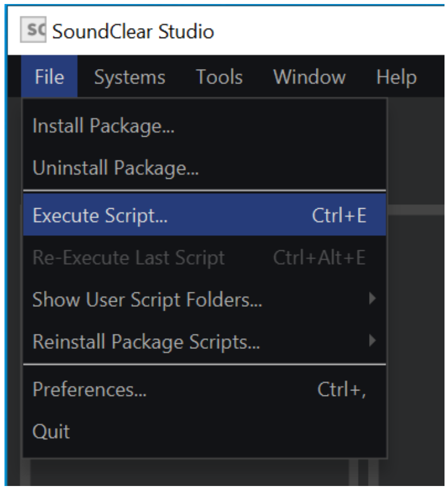


Figure 30: SoundClear Studio – Executing Script

The daughter-card SoundClear Studio package installs a set of scripts to configure the device for common use cases. The scripts are available at <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

The scripts can be accessed from SoundClear Studio using **“File→Show User Script Folder…→<Package Name>”**:

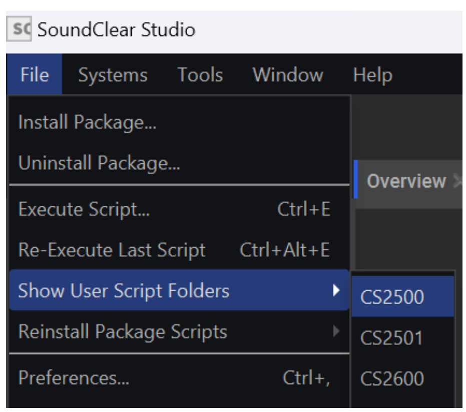


Figure 31: SoundClear Studio – Show User Script Folder

6 Quick Start Guide

This section describes how to get started with the Hazelburn system, using a simple setup in software control mode or hardware control mode. (Note the hardware control mode is supported on the CS2600 device; it is not supported on the CS2500 or CS2501.)

With the CDB2600-DC-SD daughter card, the quick start provides a basic check to get clock output signals on the Hazelburn system connectors P4 (CLK_OUT), P5 (AUX1_OUT), P6 (BCLK_OUT) and P7 (FSYNC_OUT).

With the CDB2500-DC-SD or CDB2501-DC-SD daughter cards, the quick start provides a clock output on P4 (CLK_OUT) and P5 (AUX1_OUT).

6.1 Software Mode Setup (in Synthesizer Mode)

1. Set the rotary switch S1 to position P8. This is the default position, selecting Software Control Mode.

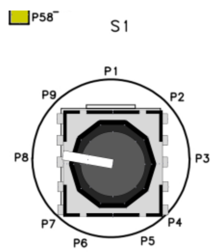


Figure 32: Set Rotary Switch S1 to Position P8

2. Connect USB-C cable to USB-connector J3 on the Hazelburn system.

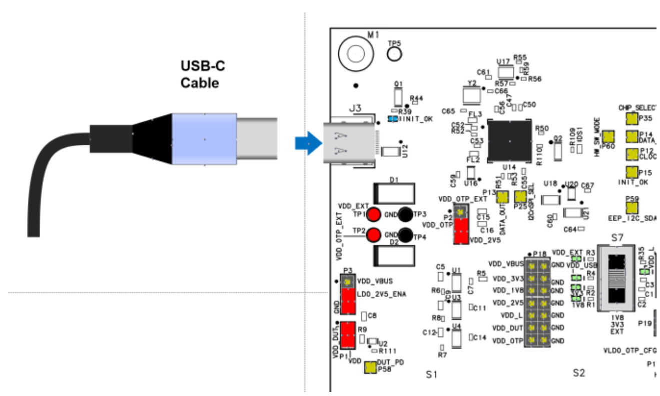


Figure 33: Connect USB-C Cable to J3

3. Connect a clock input (CLK_IN) signal of 48 kHz 3.3 V to connector P8 on the Hazelburn system.

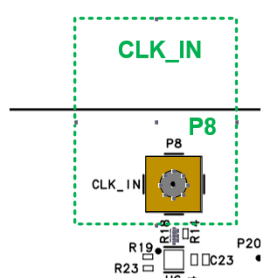


Figure 34: Connect Clocking Signal to P8

4. Start-up SoundClear Studio (SCS) software and load the SCS script using **“File→Execute Script…”:**

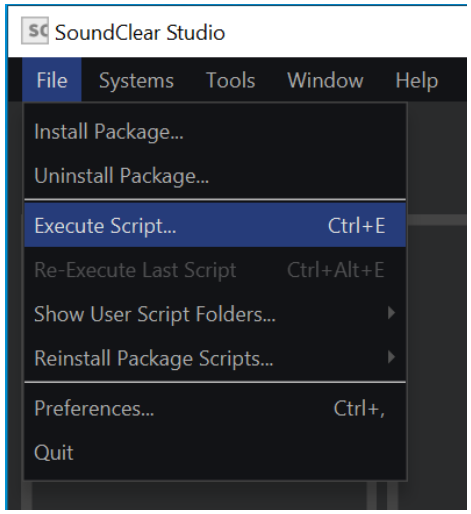


Figure 35: File -> Execute Script

5. Select the applicable SCS script from <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>:
   - For a CDB2600-DC-SD system, select the following script: *CS2600_Multiplier_Mode_CLK_IN_48kHz_CLK_OUT_24M576_REF_CLK_12M_High_Resolution.py*
   - For a CDB2500-DC-SD system, select the following script: *CS2500_Multiplier_Mode_CLK_IN_48kHz_CLK_OUT_24M576_REF_CLK_12M_High_Resolution.py*
   - For a CDB2501-DC-SD system, select the following script: *CS2501_Multiplier_Mode_CLK_IN_48kHz_CLK_OUT_24M576_REF_CLK_12M_High_Resolution.py*

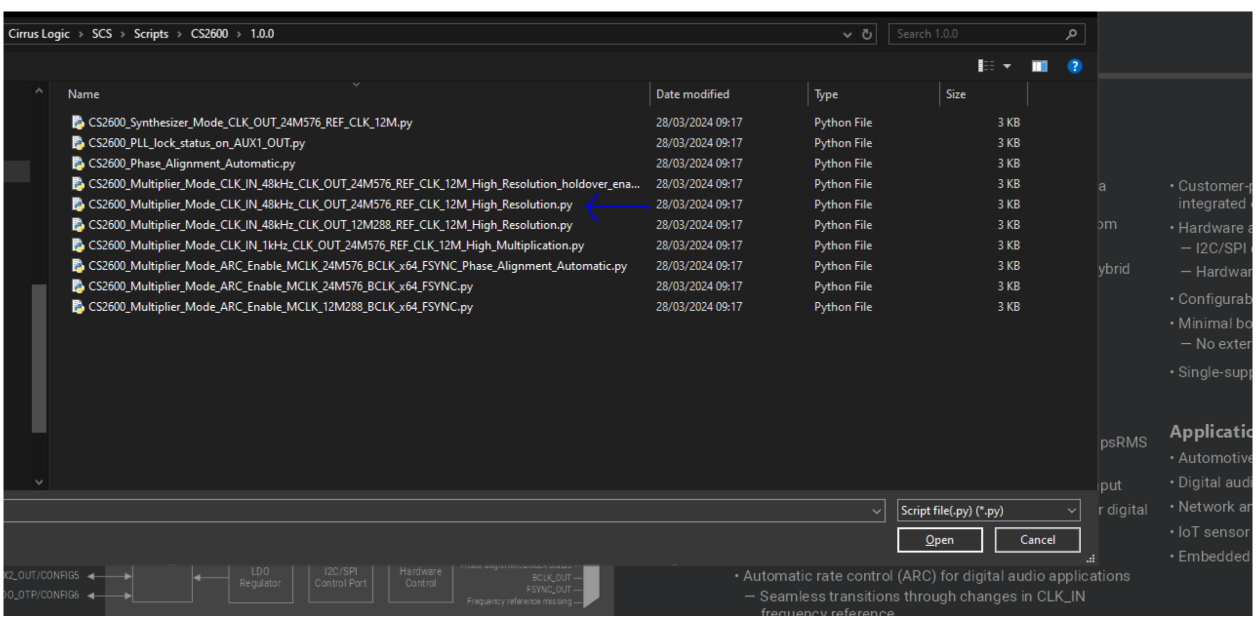


Figure 36: Select SCS Script

6. Clocks should be observed at the output connectors of the Hazelburn system as follows:
   - CLK_OUT = 24,576 MHz (Connector P4 on Hazelburn system)
   - AUX1_OUT = 12 MHz (Connector P5 on Hazelburn system)
   - BCLK_OUT = 24.576 MHz (Connector P6 on Hazelburn system)
   - FSYNC_OUT = 1.536 MHz (Connector P7 on Hazelburn system)

Note the BCLK_OUT and FSYNC_OUT clocks are only supported on the CS2600 device; these outputs are not supported on the CS2500 or CS2501.

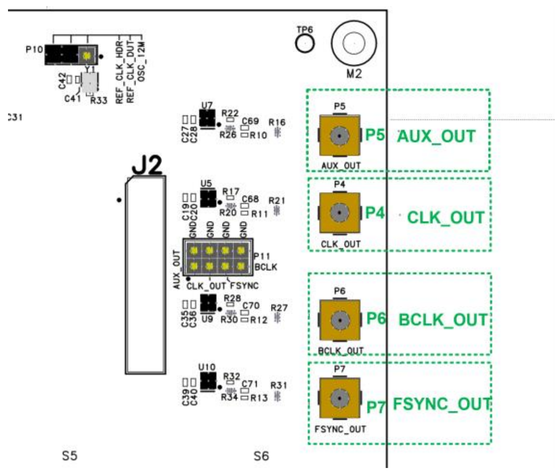


Figure 37: Output Connectors on Hazelburn System

6.2 Hardware Mode Setup (with CDB2600-DC-SD only)

1. Set the jumper P64 to “HW” on the Hazelburn system.

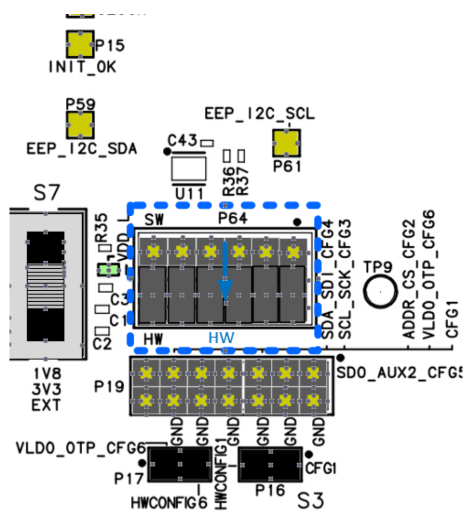


Figure 38: Set Jumper P64 to HW Position

2. Set rotary switches S1–S6 on the Hazelburn system to the following positions:
   - Set rotary switch S1 to position P5 (Multiplier Mode with 8–18 MHz REF_CLK input)
   - Set rotary switch S2 to position P1 (AUX1_OUT set to frequency-unlock indictor)
   - Set rotary switch S3 to position P1 (I2S target application)
   - Set rotary switch S4 to position P8 (BCLK = 64 × FSYNC)
   - Set rotary switch S5 to position P8 (FSYNC = CLK_OUT / 16)
   - Set rotary switch S6 to position P3 (CLK_OUT = 512 × CLK_IN)

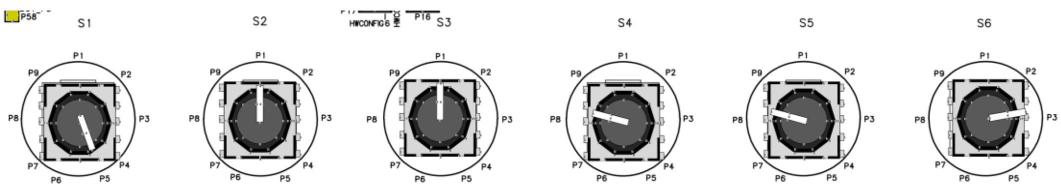


Figure 39: Set Rotary Switches S1-S6 on the Hazelburn System

3. Connect USB-C cable to USB-connector J3 on the Hazelburn system.

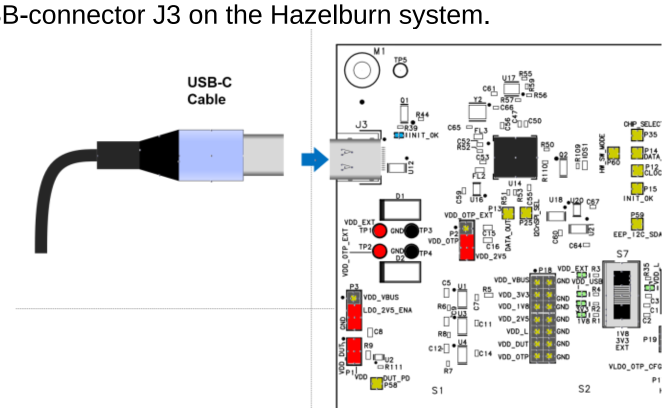


Figure 40: Connect USB-C Cable to J3

4. Connect a clock input (CLK_IN) signal of 48 kHz 3.3 V to connector P8 on the Hazelburn system.

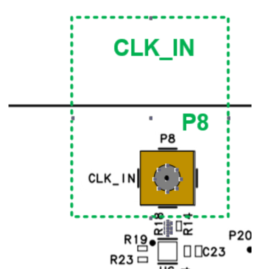


Figure 41: Connect Clocking Signal to P8

5. Clocks should be observed at the output connectors of the Hazelburn system as follows:
   - CLK_OUT = 24.576 MHz (Connector P4 on Hazelburn system)
   - AUX1_OUT = Logic 0 (Connector P5 on Hazelburn system); indicates the PLL is locked
   - BCLK_OUT = 24.576 MHz (Connector P6 on Hazelburn system)
   - FSYNC_OUT = 1.536 MHz (Connector P7 on Hazelburn system)

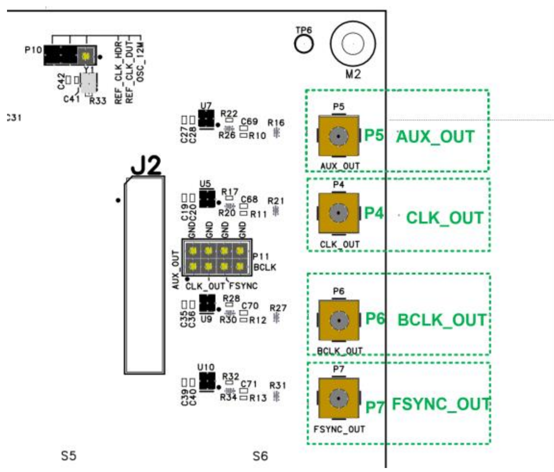


Figure 42: Output Connectors on Hazelburn System

7 Revision History

Revision History

Revision	Changes
R1 JUNE 2024	• Initial version.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.