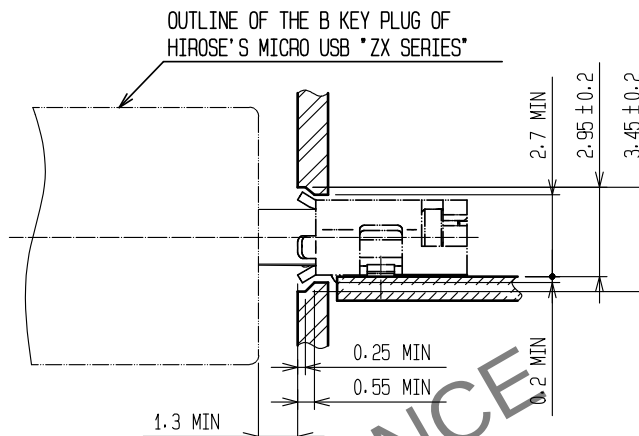
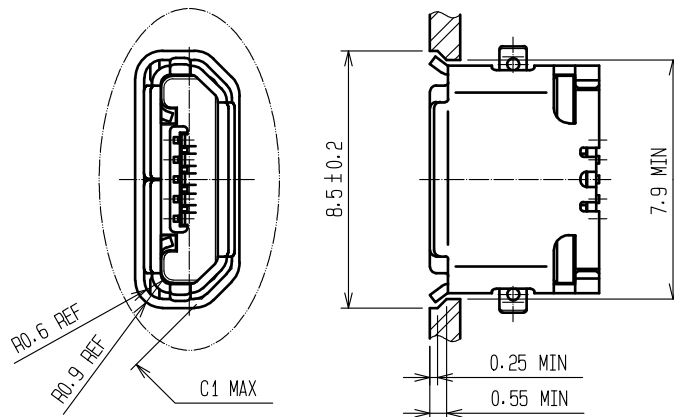
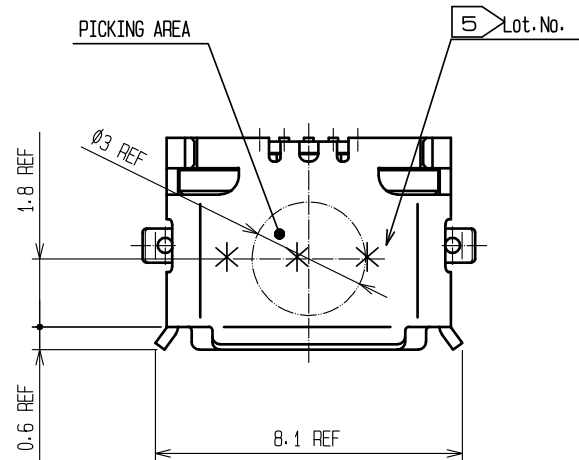
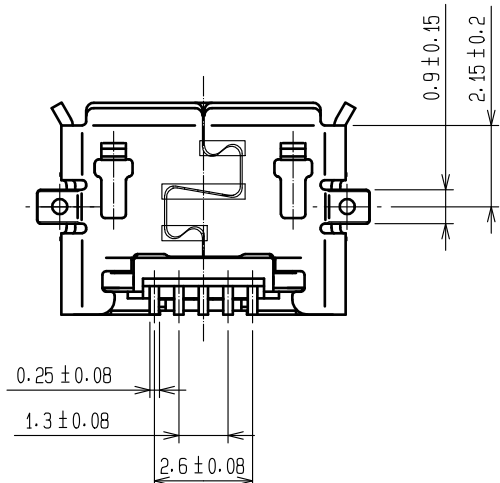
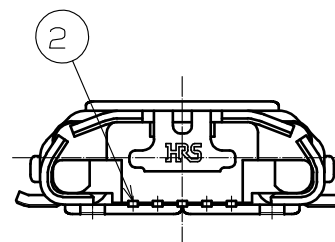
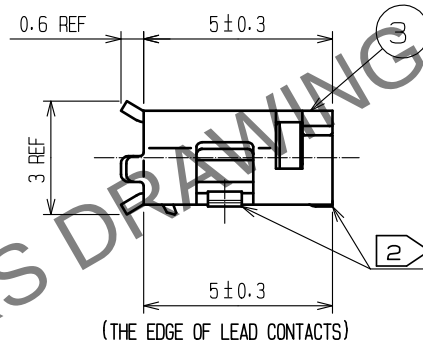
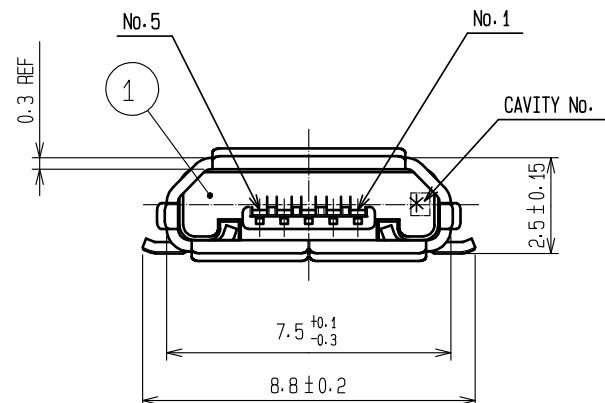
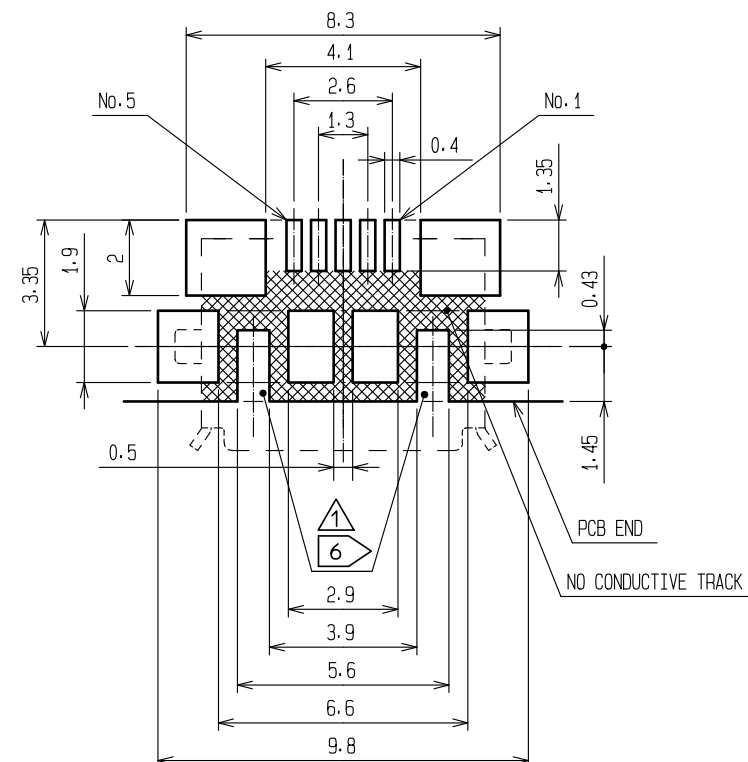




(GENERAL TOLERANCE IS $\pm 0.05\text{mm}$)

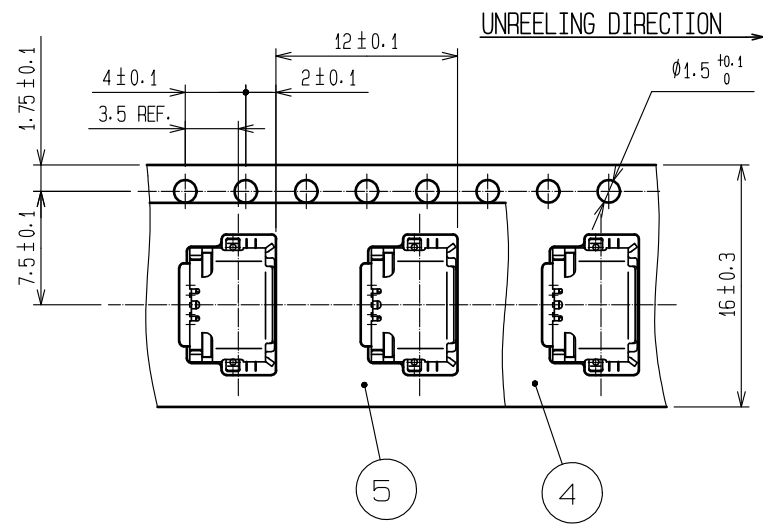


- NOTES
- 1 INTERFACE DIMENSIONS CONFORM TO USB2.0 SPECIFICATION.
 - 2 CO-PLANARITY IS WITHIN 0.08 mm.
 - 3 PLATING
CONTACT AREA : GOLD 0.75 μ m MIN.
LEAD AREA : GOLD 0.05 μ m MIN.
UNDER PLATING : NICKEL 2 μ m MIN.
 - 4 PER REEL : 2000 PCS.
 - 5 CODE CONFIGURATION IS SHOWN IN FIG.1
 - 6 PCB CUTOUTS ARE NECESSARY TO PREVENT THE LOCK FROM HITTING THE PCB WHEN MATING PLUG.

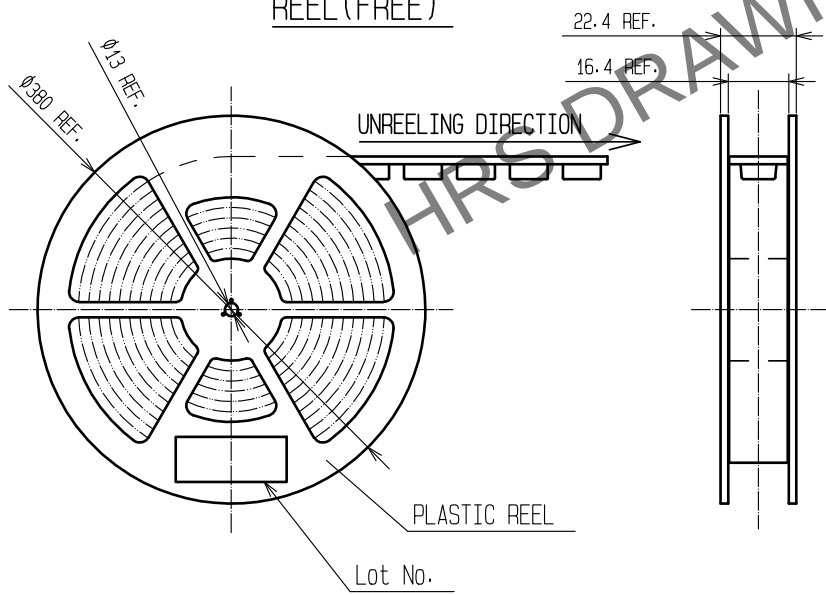
2	COPPER ALLOY	3	5	PE			
1	LCP	BLACK , UL94V-0	3	STAINLESS STEEL	TIN PLATING 1 μm MIN. LUBRICANT		
NO.	MATERIAL	FINISH , REMARKS	NO.	MATERIAL	FINISH , REMARKS		
UNITS mm		SCALE 5 : 1	COUNT 2	DESCRIPTION OF REVISIONS DIS-E-00011746	DESIGNED KIM JAEHYEON	CHECKED KG. OKITA	DATE 20221127
HRS HIROSE ELECTRIC CO., LTD.	APPROVED : NM. NISHIMATSU		20151027		DRAWING NO. EDC-126271-30-00		
	CHECKED : KN. ICHIKAWA		20151027		PART NO. ZX62R-B-5P(30)		
	DESIGNED : TS. ITO		20151027		CODE NO. CL0242-0028-8-30		
	DRAWN : AK. AKIYAMA		20151027		1/1		

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4> DRAWING FOR PACKING (2:1)



REEL (FREE)



5> Fig.1 LOT CODE CONFIGURATION FOR 3 DIGITS

YEAR		MONTH		DAY					
YEAR	CODE	MONTH	CODE	DAY	CODE	DAY	CODE	DAY	CODE
2007	7	Jan.	A	1	1	11	B	21	M
2008	8	Feb.	B	2	2	12	C	22	N
2009	9	Mar.	C	3	3	13	D	23	P
2010	0	Apr.	D	4	4	14	E	24	Q
2011	1	May.	E	5	5	15	F	25	R
		Jun.	F	6	6	16	G	26	S
		Jul.	G	7	7	17	H	27	T
		Aug.	H	8	8	18	J	28	U
		Sep.	I	9	9	19	K	29	V
		Oct.	J	10	A	20	L	30	W
		Nov.	K					31	X
		Dec.	L						

HR5

DRAWING NO.	EDC-126271-30-00		
PART NO.	ZX62R-B-5P(30)		
CODE NO.	CL0242-0028-8-30		

1/2