

## Features

- 32.768 kHz  $\pm 5$ ,  $\pm 10$ ,  $\pm 20$  ppm frequency stability options over temp
- World's smallest TCXO in a 1.5 x 0.8 mm CSP
- Operating temperature ranges:
  - 0°C to +70°C
  - -40°C to +85°C
- Ultra-low power: <1  $\mu$ A
- Vdd supply range: 1.5 V to 3.63 V
- Improved stability reduces system power with fewer network timekeeping updates
- Internal filtering eliminates external Vdd bypass cap and saves space
- Pb-free, RoHS and REACH compliant
- PFAS free option available with ordering code 'P'

## Applications

- Smart Meters (AMR)
- Health and Wellness Monitors
- Pulse-per-Second (pps) Timekeeping
- RTC Reference Clock

TempFlat<sup>®</sup>  
MEMS



Order  
samples



Buy at  
SiTimeDirect



Green  
solutions



Lifetime  
warranty

## Electrical Specifications

Table 1. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency and Stability</b>						
Output Frequency	F <sub>out</sub>	32.768			kHz	
Frequency Stability Over Temperature <sup>[1]</sup> (without Initial Offset <sup>[2]</sup> )	F <sub>stab</sub>	-5.0	–	5.0	ppm	Stability part number code = E
		-10	–	10		Stability part number code = F
		-20	–	20		Stability part number code = 1
Frequency Stability Over Temperature (with Initial Offset <sup>[2]</sup> )	F <sub>stab</sub>	-10	–	10	ppm	Stability part number code = E
		-13	–	13		Stability part number code = F
		-22	–	22		Stability part number code = 1
Frequency Stability vs Voltage	F <sub>vdd</sub>	-0.75	–	0.75	ppm	1.8 V $\pm$ 10%
		-1.5	–	1.5	ppm	1.5 V – 3.63 V
First Year Frequency Aging	F <sub>aging</sub>	-1.0	–	1.0	ppm	T <sub>A</sub> = 25°C, Vdd = 3.3 V
<b>Jitter Performance (T<sub>A</sub> = over temp)</b>						
Long Term Jitter		–	–	2.5	$\mu$ s <sub>pp</sub>	81920 cycles (2.5 sec), 100 samples
Period Jitter		–	35	–	ns <sub>RMS</sub>	Cycles = 10,000, T <sub>A</sub> = 25°C, Vdd = 1.5 V – 3.63 V
<b>Supply Voltage and Current Consumption</b>						
Operating Supply Voltage	Vdd	1.5	–	3.63	V	T <sub>A</sub> = -40°C to +85°C
Core Supply Current <sup>[3]</sup>	I <sub>dd</sub>	–	0.99	–	$\mu$ A	T <sub>A</sub> = 25°C, Vdd = 1.8 V, LVCMOS Output configuration, No Load
		–	–	1.52		T <sub>A</sub> = -40°C to +85°C, Vdd = 1.5 V – 3.63 V, No Load
Power-Supply Ramp	t <sub>Vdd_Ramp</sub>	–	–	100	ms	Vdd Ramp-Up 0 to 90% Vdd, T <sub>A</sub> = -40°C to +85°C
Start-up Time at Power-up	t <sub>start</sub>	–	180	300	ms	T <sub>A</sub> = -40°C +60°C, valid output
		–	–	350		T <sub>A</sub> = +60°C to +70°C, valid output
		–	–	380		T <sub>A</sub> = +70°C to +85°C, valid output

### Notes:

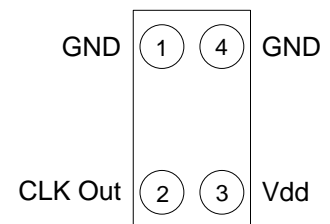
1. No board level underfill. Measured as peak-to-peak/2. Inclusive of 3x-reflow and  $\pm 20\%$  load variation. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be  $\geq 100$  ms to ensure an accurate frequency measurement.
2. Initial offset is defined as the frequency deviation from the ideal 32.768 kHz at room temperature, post reflow.
3. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + output driver operating current, which is a function of the output voltage swing. See the description titled [Calculating Load Current](#).

**Table 1. Electrical Characteristics (continued)**

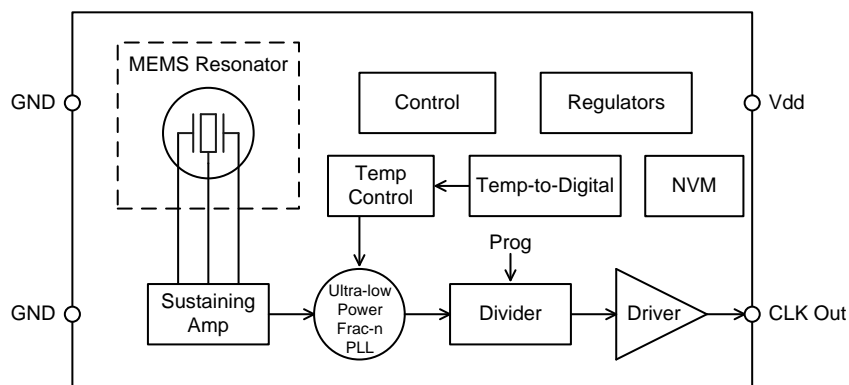
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Temperature Range						
Commercial Temperature	Op_Temp	0	–	70	°C	
Industrial Temperature		-40	–	85	°C	
LVCMOS Output						
Output Rise/Fall Time	tr, tf	–	100	200	ns	10-90% (Vdd), 15 pF Load
		–	–	50		10-90% (Vdd), 5 pF Load, Vdd ≥ 1.62 V
Output Clock Duty Cycle	DC	48	–	52	%	
Output Voltage High	VOH	90%	–		V	Vdd: 1.5 V – 3.63 V. IOH = -1 µA, 15 pF Load
Output Voltage Low	VOL		–	10%	V	Vdd: 1.5 V – 3.63 V. IOL = 1 µA, 15 pF Load
NanoDrive™ Programmable, Reduced Swing Output						
Output Rise/Fall Time	tf, tf	–	–	200	ns	30-70% (VOL/VOH), 10 pF Load
Output Clock Duty Cycle	DC	48	–	52	%	
AC-coupled Programmable Output Swing	V_sw	–	0.20 to 0.80	–	V	SiT1552 does not internally AC-couple. This output description is intended for a receiver that is AC-coupled. See Table 4 for acceptable NanoDrive swing options. Vdd: 1.5 V – 3.63 V, 10 pF Load, IOH / IOL = ±0.2 µA
DC-Biased Programmable Output Voltage High Range	VOH	–	0.60 to 1.225	–	V	Vdd: 1.5 V – 3.63 V. IOH = -0.2 µA, 10 pF Load. See Table 4 for acceptable VOH/VOL setting levels.
DC-Biased Programmable Output Voltage Low Range	VOL	–	0.35 to 0.80	–	V	Vdd: 1.5 V – 3.63 V. IOL = 0.2 µA, 10 pF Load. See Table 4 for acceptable VOH/VOL setting levels.
Programmable Output Voltage Swing Tolerance		-0.055	–	0.055	V	TA = -40°C to +85°C, Vdd = 1.5 V to 3.63 V

**Table 2. Pin Configuration**

CSP Pin	Symbol	I/O	Functionality
1, 4	GND	Power Supply Ground	Connect to ground. All GND pins must be connected to power supply ground. The GND pins can be connected together, as long as both GND pins are connected ground.
2	CLK Out	OUT	Oscillator clock output. When interfacing to an MCU's XTAL, the CLK Out is typically connected to the receiving IC's X IN pin. The SiT1552 oscillator output includes an internal driver. As a result, the output swing and operation is not dependent on capacitive loading. This makes the output much more flexible, layout independent, and robust under changing environmental and manufacturing conditions.
3	Vdd	Power Supply	Connect to power supply 1.5 V ≤ Vdd ≤ 3.63 V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). For more information about the internal power-supply filtering, see <a href="#">Power-Supply Noise Immunity</a> section in the detailed description. <a href="#">Contact SiTime</a> for applications that require a wider operating supply voltage range.

**CSP Package (Top View)**

**Figure 1. Pin Assignments**

## System Block Diagram



**Figure 2. SiT1552 Block Diagram**

**Table 3. Absolute Maximum Limits**

Attempted operation outside the absolute maximum ratings cause permanent damage to the part.

Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	≤30 minutes	4.0	V
Continuous Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V	105	°C
Short Duration Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V, ≤30 mins	125	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD22- C101	750	V
Machine Model (MM) ESD Protection	JESD22- A115	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65°C to 150°C	

## Description

The [SiT1552](#) is an ultra-small and ultra-low power 32.768 kHz TCXO optimized for battery-powered applications. SiTime's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical core supply current is only 1  $\mu$ A.

SiTime's MEMS oscillators consist of MEMS resonators and a programmable analog circuit. Our MEMS resonators are built with SiTime's unique MEMS First® process. A key manufacturing step is EpiSeal® during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

## TCXO Frequency Stability

The SiT1552 is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 ppm/C<sup>2</sup> temperature coefficient, the SiT1552 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range. [Contact SiTime](#) for applications that require a wider supply voltage range >3.63 V, or lower operating frequency below 32 kHz.

When measuring the SiT1552 output frequency with a frequency counter, it is important to make sure the counter's gate time is >100 ms. The slow frequency of a 32 kHz clock will give false readings with faster gate times.

## Power Supply Noise Immunity

In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor to keep the footprint as small as possible. Internal power supply filtering is designed to reject more than  $\pm 150$  mV noise and frequency components from low frequency to more than 10 MHz.

## Start-up and Steady-State Supply Current

The SiT1552 TCXO starts-up to a valid output frequency within 300 ms (180 mstyp). To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 – 20 ms (to within 90% of Vdd).

During initial power-up, the SiT1552 power-cycles internal blocks, as shown in the power-supply start-up and steady state plot in the [Typical Operating Curves](#) section. Power-up and initialization is typically 200 ms, and during that time, the peak supply current reaches 28  $\mu$ A as the internal capacitors are charged, then sequentially drops to its 990 nA steady-state current. During steady-state operation, the internal temperature compensation circuit turns on every 350 ms for a duration of approximately 10 ms.

## Output Voltage

The SiT1552 has two output voltage options. One option is a standard LVCMOS output swing. The second option is the NanoDrive reduced swing output. Output swing is customer specific and programmed between 200 mV and 800 mV. For DC-coupled applications, output V<sub>OH</sub> and V<sub>OL</sub> are individually factory programmed to the customers' requirement. V<sub>OH</sub> programming range is between 600 mV and 1.225 V in 100 mV increments. Similarly, V<sub>OL</sub> programming range is between 350 mV and 800 mV. For example; a PMIC or MCU is internally 1.8V logic compatible, and requires a 1.2 V V<sub>IH</sub> and a 0.6 V V<sub>IL</sub>. Simply select SiT1552 NanoDrive factory programming code to be "D14" and the correct output thresholds will match the downstream PMIC or MCU input requirements. Interface logic will vary by manufacturer and we recommend that you review the input voltage requirements for the input interface.

For DC-biased NanoDrive output configuration, the minimum V<sub>OL</sub> is limited to 350 mV and the maximum allowable swing (V<sub>OH</sub> - V<sub>OL</sub>) is 750 mV. For example, 1.1V V<sub>OH</sub> and 400 mV V<sub>OL</sub> is acceptable, but 1.2 V V<sub>OH</sub> and 400 mV V<sub>OL</sub> is not acceptable.

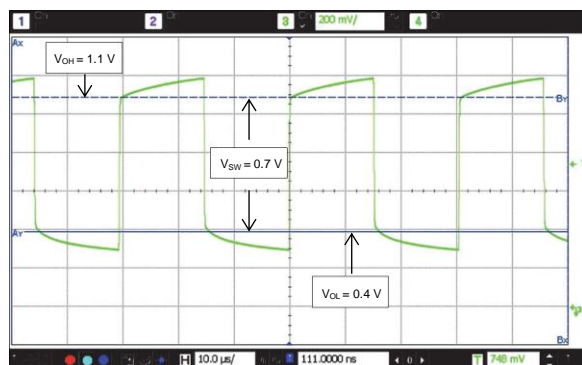
When the output is interfacing to an XTAL input that is internally AC-coupled, the SiT1552 output can be factory programmed to match the input swing requirements. For example, if a PMIC or MCU input is internally AC-coupled and requires an 800 mV swing, then simply choose the SiT1552 NanoDrive programming code "AA8" in the part number. It is important to note that the SiT1552 does not include internal AC-coupling capacitors. Please see the [Part Number Ordering](#) section at the end of the datasheet for more information about the part number ordering scheme.

## SiT1552 NanoDrive™

Figure 3 shows a typical output waveform of the SiT1552 (into a 10 pF load) when factory programmed for a 0.70 V swing and DC bias ( $V_{OH}/V_{OL}$ ) for 1.8 V logic:

### Example:

- NanoDrive™ part number coding: **D14**.  
Example part number: SiT1552AI-JE-**D14**-32.768
- $V_{OH} = 1.1$  V,  $V_{OL} = 0.4$  V ( $V_{SW} = 0.70$  V)



**Figure 3. SiT1552AI-JE-D14-32.768 Output Waveform (10 pF load)**

Table 4 shows the supported NanoDrive™  $V_{OH}$ ,  $V_{OL}$  factory programming options.

**Table 4. Acceptable  $V_{OH}/V_{OL}$  NanoDrive™ Levels**

NanoDrive	$V_{OH}$ (V)	$V_{OL}$ (V)	Swing (mV)	Comments
D26	1.2	0.6	600 ±55	1.8 V logic compatible
D14	1.1	0.4	700 ±55	1.8 V logic compatible
D74	0.7	0.4	300 ±55	XTAL compatible
AA3	n/a	n/a	300 ±55	XTAL compatible

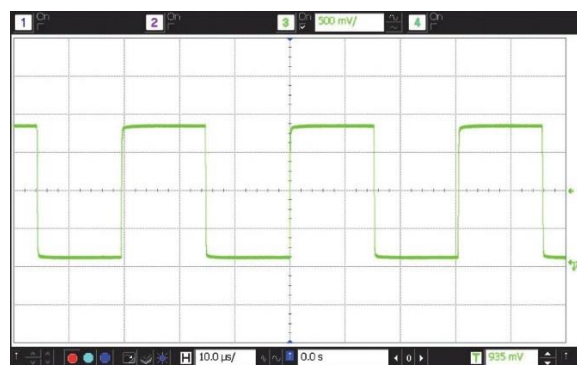
The values listed in Table 4 are nominal values at 25°C and will exhibit a tolerance of ±55 mV across  $V_{dd}$  and -40°C to 85°C operating temperature range.

## SiT1552 Full Swing LVCMOS Output

The SiT1552 can be factory programmed to generate full-swing LVCMOS levels. Figure 4 shows the typical waveform ( $V_{dd} = 1.8$  V) at room temperature into a 15 pF load.

### Example:

- LVCMOS output part number coding is always **DCC**
- Example part number: SiT1552AI-JE-**DCC**-32.768



**Figure 4. LVCMOS Waveform ( $V_{dd} = 1.8$  V) into 15 pF Load**

## Calculating Load Current

### No Load Supply Current

When calculating no-load power for the SiT1552, the core and output driver components need to be added. Since the output voltage swing can be programmed to minimize load current, the output driver current is variable. Therefore, no-load operating supply current is broken into two sections; core and output driver. The equation is as follows:

Total Supply Current (no load) = Idd Core + Idd Output Driver

#### Example 1: Full-swing LVCMOS

- Vdd = 1.8 V
- Idd Core = 990 nA (typ)
- Voutpp = 1.8 V
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5 pF)(1.8 V)(32768 Hz) = 206 nA

Supply Current = 990 nA + 206 nA = 1.2  $\mu$ A

#### Example 2: NanoDrive™ Reduced Swing

- Vdd = 1.8 V
- Idd Core = 990 nA (typ)
- Voutpp (D14) = V<sub>OH</sub> - V<sub>OL</sub> = 1.1 V - 0.4 V = 700 mV
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5 pF)(0.7 V)(32768 Hz) = 80 nA

Supply Current = 990 nA + 80 nA = 1.07  $\mu$ A

### Total Supply Current with Load

To calculate the total supply current, including the load, follow the equation listed below.

Total Current = Idd Core + Idd Output Driver + Load Current

#### Example 1: Full-swing LVCMOS

- Vdd = 1.8 V
- Idd Core = 990 nA
- Load Capacitance = 10 pF
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5 pF)(1.8 V)(32768 Hz) = 206 nA

Load Current: (10 pF)(1.8 V)(32768 Hz) = 590 nA

Total Current = 990 nA + 206 nA + 590 nA = 1.79  $\mu$ A

#### Example 2: NanoDrive™ Reduced Swing

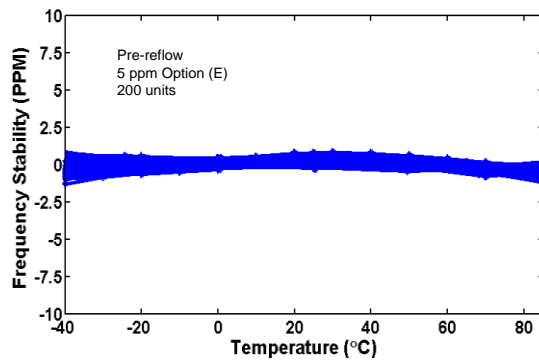
- Vdd = 1.8 V
- Idd Core = 990 nA
- Load Capacitance = 10 pF
- Voutpp (D14): V<sub>OH</sub> - V<sub>OL</sub> = 1.1 V - 0.4 V = 700 mV
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5 pF)(0.7 V)(32768 Hz) = 80 nA

Load Current: (10 pF)(0.7 V)(32.768 kHz) = 229 nA

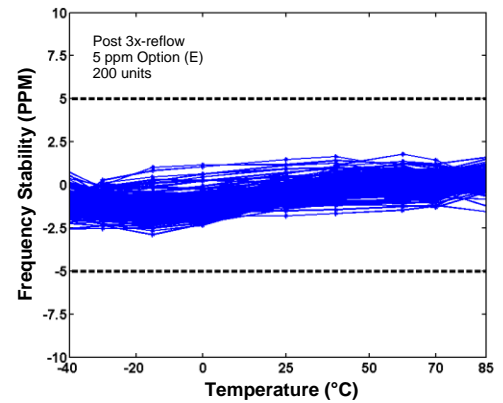
Total Current = 990 nA + 80 nA + 229 nA = 1.299  $\mu$ A

## Typical Operating Curves

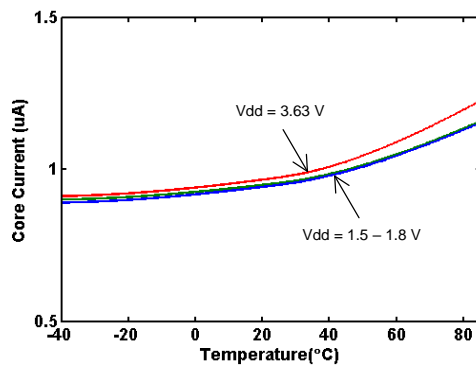
(T<sub>A</sub> = 25°C, V<sub>dd</sub> = 1.8 V, unless otherwise stated)



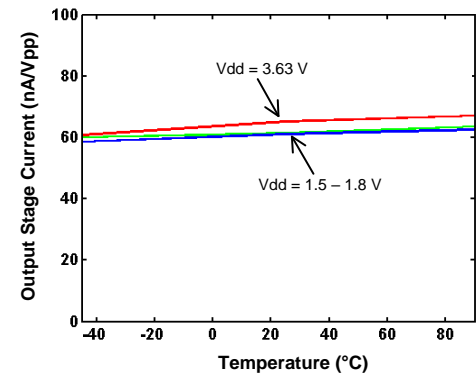
**Figure 5. Frequency Stability Over Temperature (Pre-Reflow)**



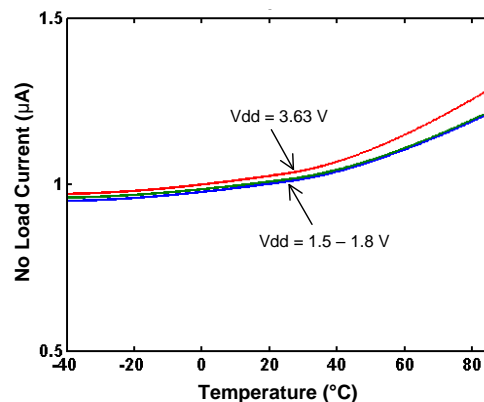
**Figure 6. Frequency Stability Over Temperature (Post-Reflow)**



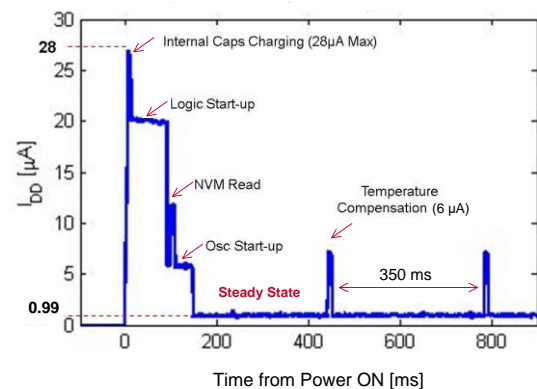
**Figure 7. Core Current Over Temperature**



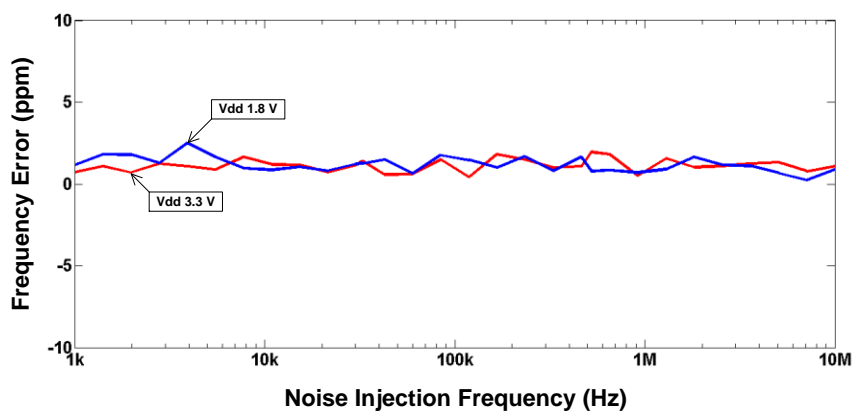
**Figure 8. Output Stage Current Over Temperature**



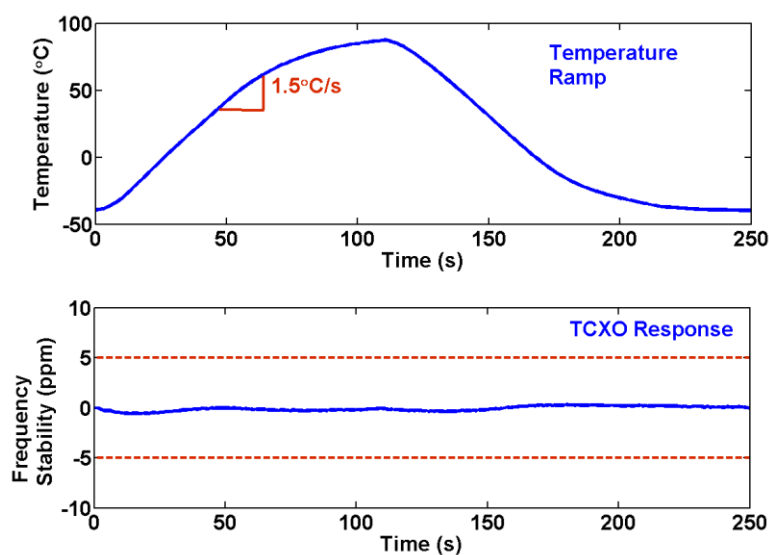
**Figure 9. Total Supply Current Over Temperature, LVCMOS (Core + LVCMOS Output Driver, No Load)**



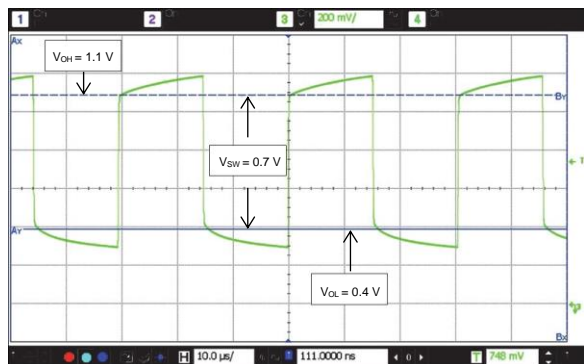
**Figure 10. Start-up and Steady-State Current Profile**



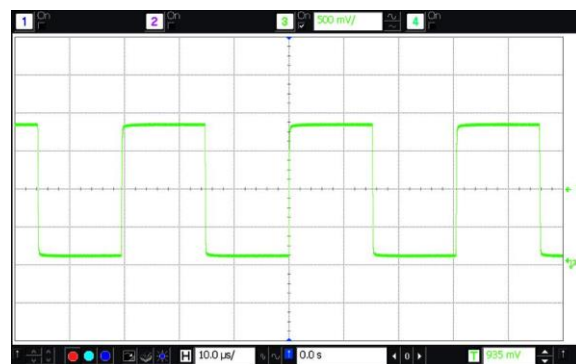
**Figure 11. Power Supply Noise Rejection ( $\pm 150$  mV Noise)**



**Figure 12. Temperature Ramp Response**



**Figure 13. NanoDrive™ Output Waveform**  
( $V_{OH} = 1.1$  V,  $V_{OL} = 0.4$  V; SiT1552AI-JE-D14-32.768)

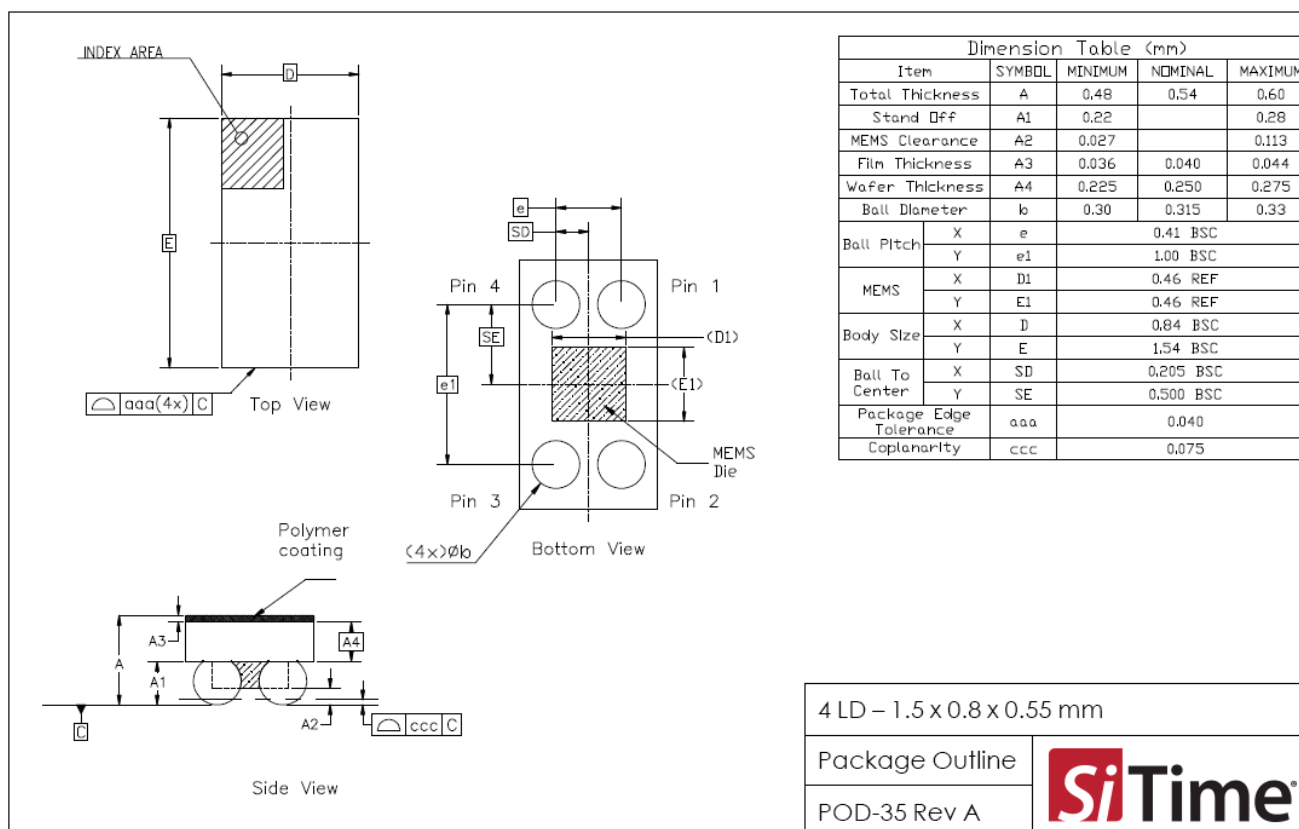


**Figure 14. LVCMOS Output Waveform**  
( $V_{swing} = 1.8$  V, SiT1552AI-JE-DCC-32.768, 10 pF Load)

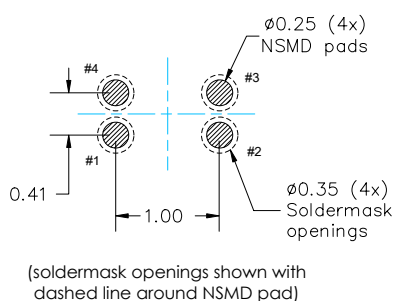


## Dimensions and Patterns

Package Size – Dimensions (Unit: mm)



Recommended Land Pattern (Unit: mm)



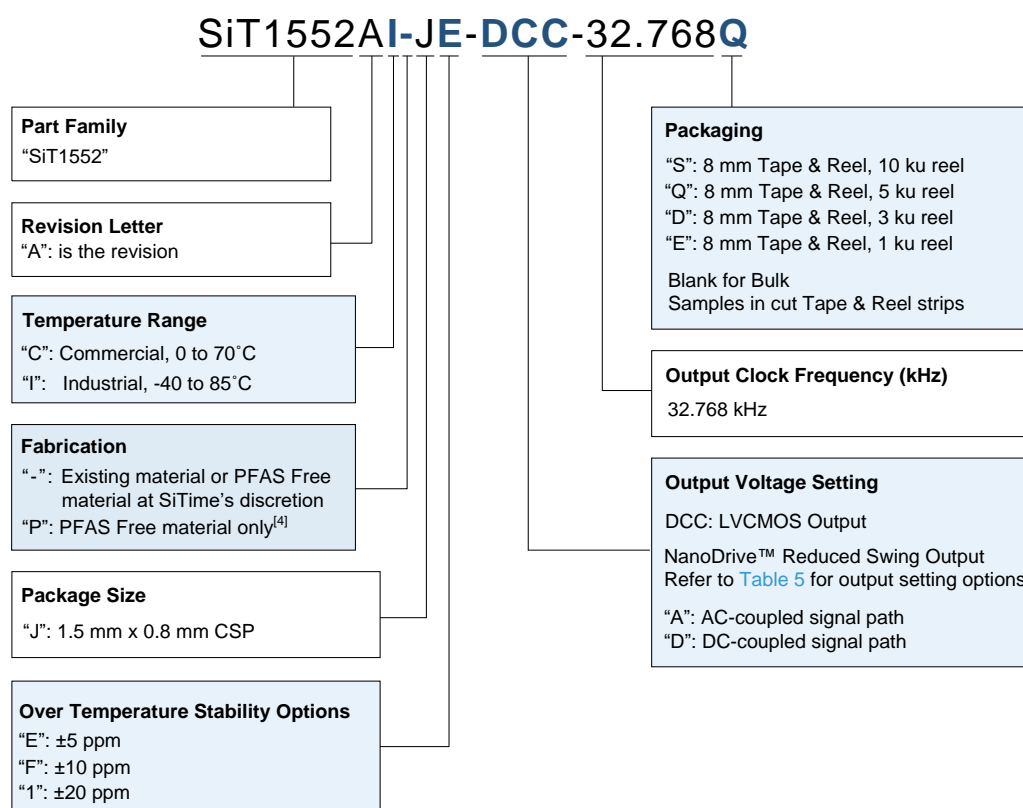
Recommended 4-mil (0.1mm) stencil thickness

## Manufacturing Guidelines

- 1) No Ultrasonic Cleaning: Do not subject the SiT1552 to an ultrasonic cleaning environment. Permanent damage or long term reliability issues to the MEMS structure may occur.
- 2) Do not apply underfill to the SiT1552. The device will not meet the frequency stability specification if underfill is applied.
- 3) Reflow profile, per JESD22-A113D.
- 4) The SiT1576 CSP includes a protective, opaque polymer top-coat. If the SiT1576 will see intense light, especially in the 1.0-1.2  $\mu\text{m}$  IR spectrum, we recommend a protective “glob-top” epoxy or other cover to keep the light from negatively impacting the frequency stability.
- 5) For additional manufacturing guidelines and marking /tape-reel instructions, refer to [SiTime Manufacturing Notes](#).

## Ordering Information

Part number characters in **blue** represent the customer specific options. The other characters in the part number are fixed.



**Note:**

4. "P" option is still preliminary, pending characterization completion.

The following examples illustrate how to select the appropriate temp range and output voltage requirements:

**Example 1: SiT1552AI-JE-DCC-32.768**

- Industrial temperature range
- CSP package
- 5 ppm frequency stability over temp
- Output swing requirements:
  - a) Output frequency = 32.769 kHz
  - b) "D" = DC-coupled receiver
  - c) "C" = LVCMOS output swing
  - d) "C" = LVCMOS output swing

**Example 2: SiT1552AC-JF-D14-32.768**

- Commercial temperature range
- CSP package
- 10 ppm frequency stability over temp
- Output swing requirements:
  - a) Output frequency = 32.769 kHz
  - b) "D" = DC-coupled receiver
  - c) "1" = V<sub>OH</sub> = 1.1 V
  - d) "4" = V<sub>OL</sub> = 400 mV

**Table 5. Acceptable V<sub>OH</sub>/V<sub>OL</sub> NanoDrive™ Levels<sup>[5]</sup>**

NanoDrive	V <sub>OH</sub> (V)	V <sub>OL</sub> (V)	Swing (mV)	Comments
D26	1.2	0.6	600 ±55	1.8 V logic compatible
D14	1.1	0.4	700 ±55	1.8 V logic compatible
D74	0.7	0.4	300 ±55	XTAL compatible
AA3	n/a	n/a	300 ±55	XTAL compatible

**Note:**

5. If these available options do not accommodate your application, [contact SiTime](#) for other NanoDrive options.

**Table 6. Revision History**

Version	Release Date	Change Summary
1.0	17-Sep-2014	Rev 0.9 Preliminary to Rev 1.0 Production Release Updated start-up time specification Added typical operating plots Removed SOT23 and 2012 SMD package options Added "no underfill" in frequency stability specification condition Added Manufacturing Guidelines section
1.1	14-Oct-2014	Improved Start-up Time at Power-up spec Added 5 pF LVCMOS rise/fall time spec
1.2	10-Nov-2014	Updated 5 pF LVCMOS rise/fall time spec
1.3	12-Nov-2015	Removed NanoDrive from EC Table and Ordering Info
1.31	18-Jan-2018	Updated SPL, page layout changes
1.32	15-Mar-2018	Updated POD (Package Outline Drawing) Updated logo and company address, other page layout changes
1.4	12-Apr-2018	Added the NanoDrive sections
1.41	23-Nov-2020	Formatting, rev table date format, TempFlat MEMS logo and trademarks update Added Q-suffix to the Ordering table options
1.42	8-Feb-2022	Revised Manufacturing Guidelines section Changed date format
1.43	17-Jun-2024	PFAS free Ordering Code update Updated icons links on page 1, updated disclaimer

**SiTime Corporation**, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439

© SiTime Corporation 2014-2024. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

**Disclaimer:** SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. This product is not suitable or intended to be used in a life support application or component or to operate nuclear facilities, in military or aerospace applications, or in other applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

#### CRITICAL USE EXCLUSION POLICY

BUYER AGREES NOT TO USE THIS PRODUCT FOR ANY APPLICATION OR IN ANY COMPONENTS: USED IN LIFE SUPPORT DEVICES, TO OPERATE NUCLEAR FACILITIES, FOR MILITARY OR AEROSPACE USE, OR IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

For military and aerospace applications, [contact SiTime](#).

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.