User guide to BGT24LTR11N16

XENSIV™ 24 GHz radar sensor

About this document

Scope and purpose

This user guide describes the key features of Infineon's XENSIV™ BGT24LTR11N16 24 GHz MMIC, and helps the user quickly get started with the sensor evaluation board. It provides:

- Description of all the different building blocks of the MMIC.
- Operation of the different blocks.
- Measurement data showing behavior over temperature.
- VCO control using different methodologies – PTAT, PLL, and a software-based open loop.

Intended audience

This document serves as a primer for firmware or software engineers who want to get started with hardware design for Infineon's XENSIV™ 24 GHz radar sensors.

Table of contents

1 Introduction

BGT24LTR11 is a Silicon Germanium radar MMIC for signal generation and reception, operating in the 24.0 GHz to 24.25 GHz industrial, scientific and medical (ISM) band. It is based on a 24 GHz fundamental voltage-controlled oscillator (VCO). The device was designed with Doppler-radar applications in mind—as it is capable of keeping the transmit signal inside the ISM band without any external phase-locked loop (PLL) — and may also be used in other types of radar such as frequency-modulated continuous wave (FMCW) or frequency shift keying (FSK).

A built-in voltage source delivers a VCO tuning voltage which is proportional to absolute temperature (PTAT). When connected to the VCO tuning pin, it compensates for the inherent frequency drift of the VCO over temperature, thus stabilizing the VCO within the ISM band, eliminating the need for a PLL/Microcontroller. An integrated 1:16 frequency divider also allows for external phase lock loop VCO frequency stabilization.

The receiver section uses a low noise amplifier (LNA) in front of a quadrature homodyne down-conversion mixer to provide excellent receiver sensitivity. Derived from the internal VCO signal, an RC-polyphase filter (PPF) generates quadrature LO signals for the quadrature mixer. I/Q IF outputs are available through single-ended terminals.

The device is manufactured in a 0.18 µm SiGe:C technology, offering a cutoff frequency of 200 GHz. It is packaged in a 16-pin leadless RoHS compliant TSNP package.

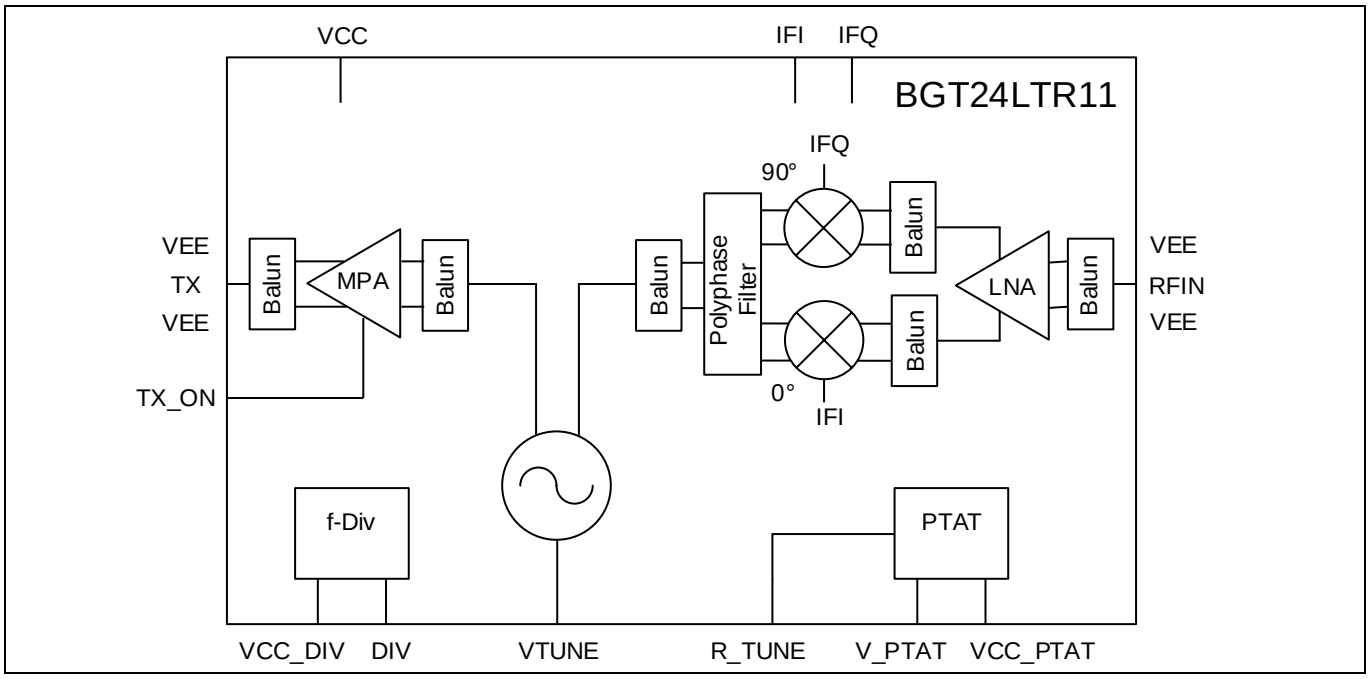

Figure 1 BGT24LTR11 block diagram

2 Building blocks

2.1 Transmitter

BGT24LTR11 has a single-ended transmitter output TX (pin 11) with a typical output power of 6 dBm. The transmitter's output may be enabled and disabled by applying appropriate voltages to TX_ON (pin 5) as shown in Table 1.

Disabling the TX output will not save power, as the output will be switched to an internal load while the rest of the chip is still running. This is necessary in case one wants to implement a software-controlled oscillator, as explained in section 4.

Table 1 Enabling/disabling TX output

Enable TX	Disable TX
Voltage at TX_ON > 2 V	Voltage at TX_ON < 0.8 V

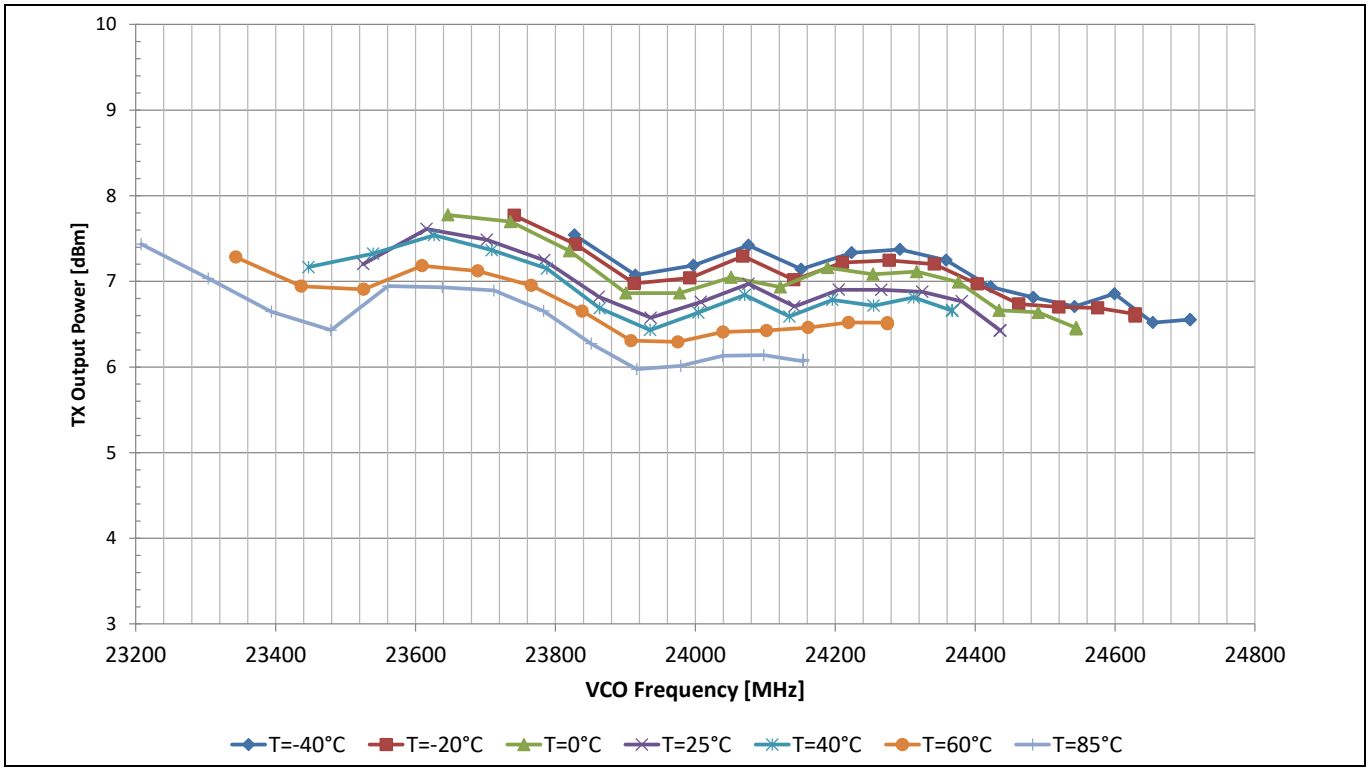

Figure 2 TX output power vs. VCO frequency and temperature

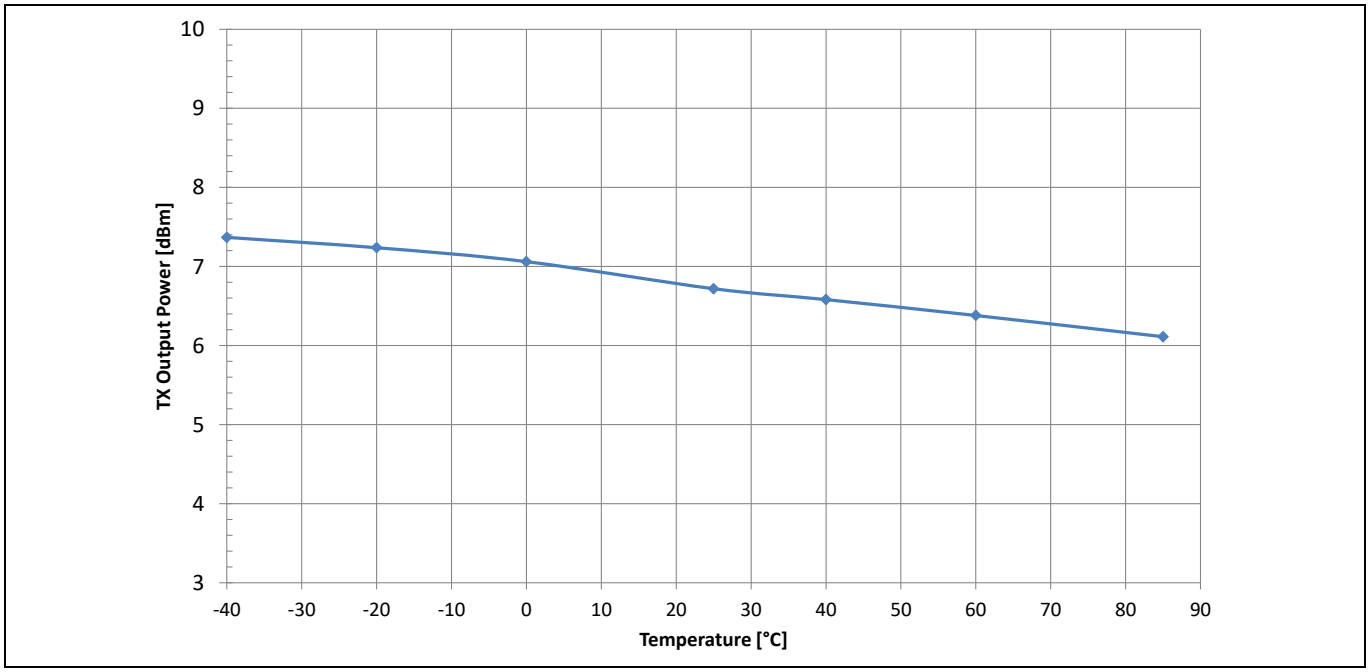

Figure 3 TX output power with VTUNE connected to V_PTAT vs. temperature

2.2 Receiver

The receiver consists of an LNA followed by a quadrature direct-conversion mixer. Its input (RX, pin 3) is single ended. The voltage conversion gain is typically 20 dB with a single side-band noise figure of 10 dB.

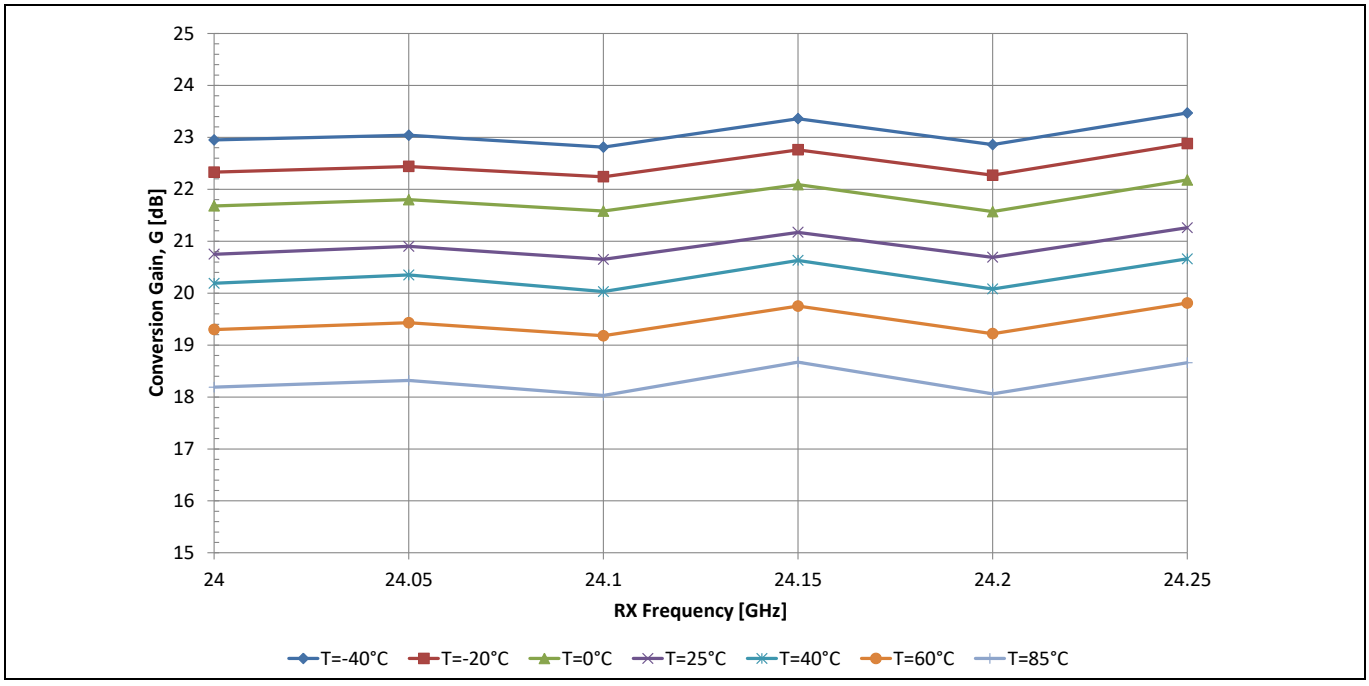

Figure 4 Conversion gain vs. RX frequency and temperature

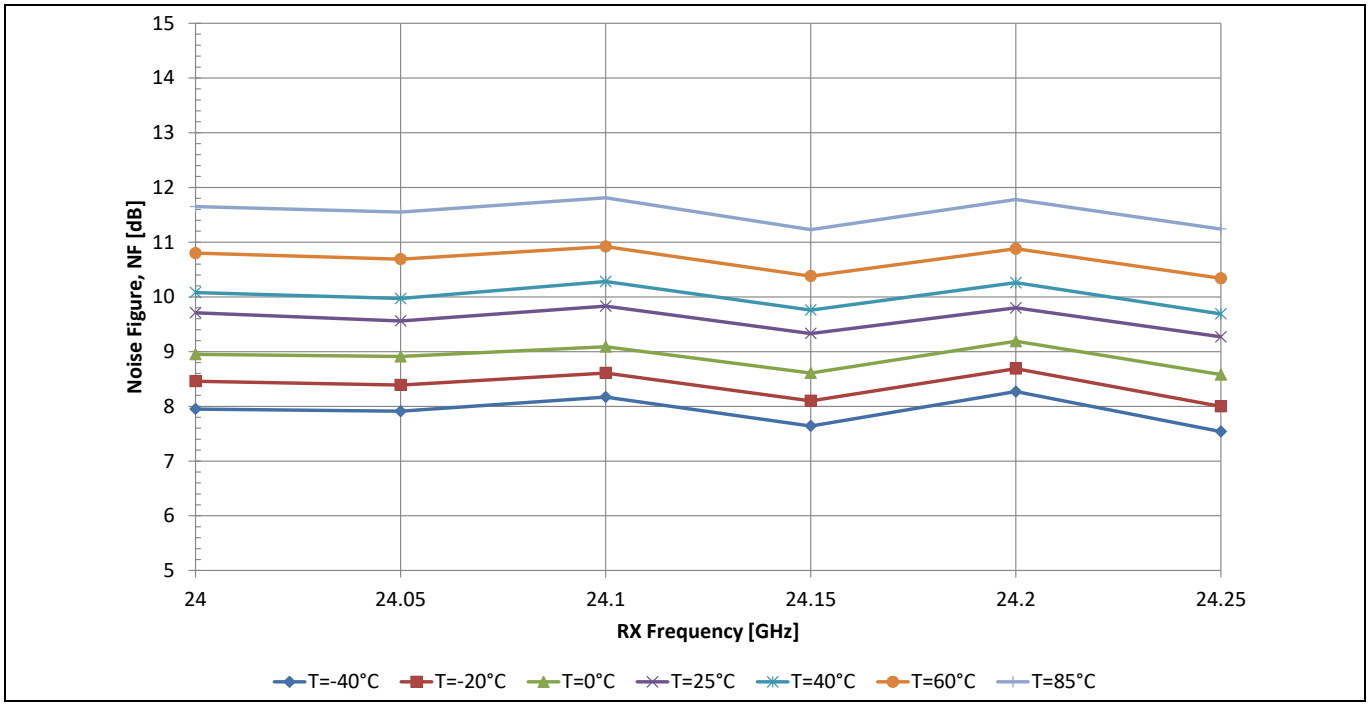

Figure 5 Noise figure vs. RX frequency and temperature

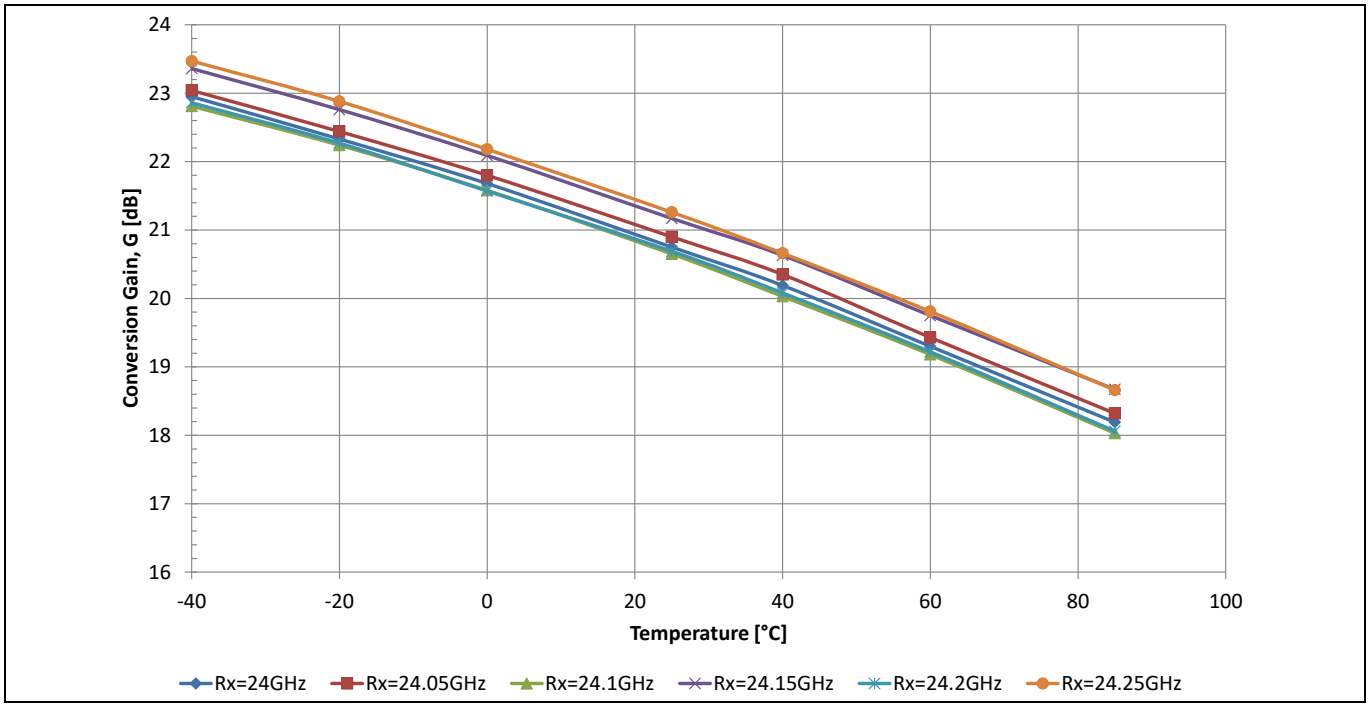

Figure 6 Conversion gain vs. temperature and RX frequency

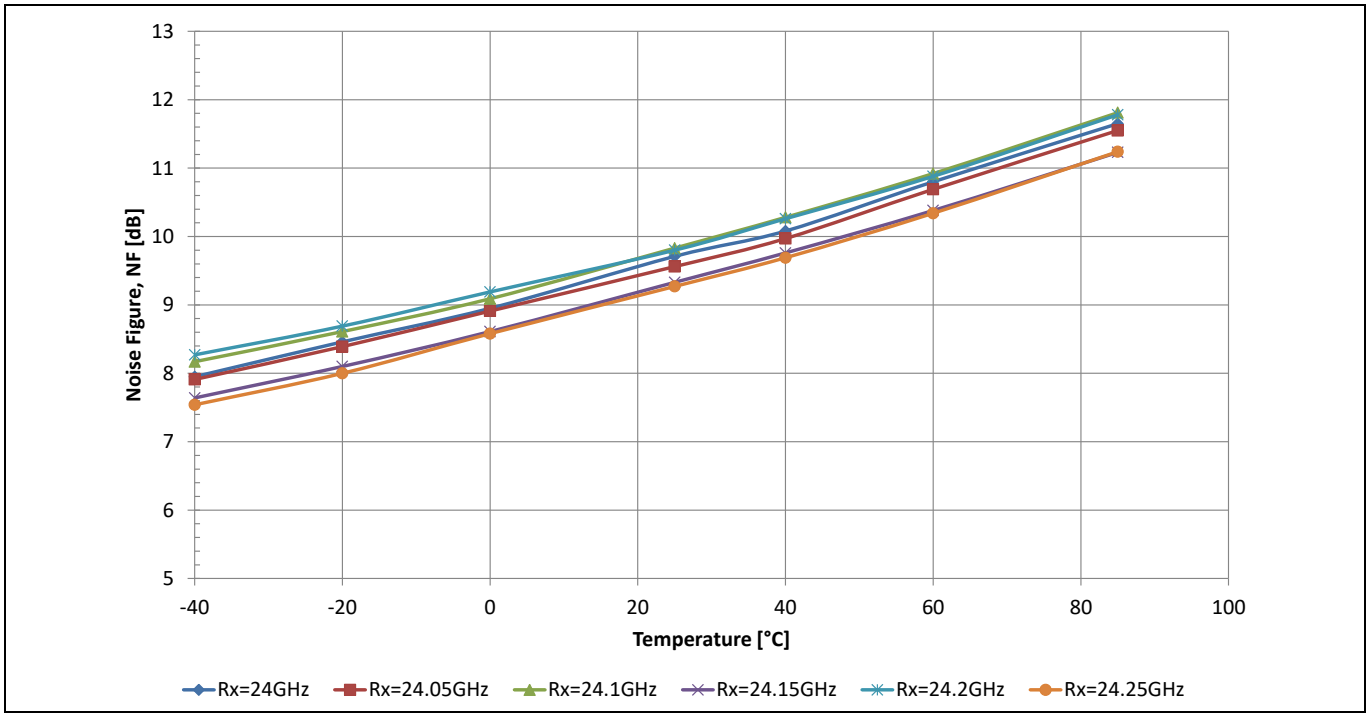

Figure 7 Noise figure vs. temperature and RX frequency

2.3 Voltage controller oscillator (VCO)

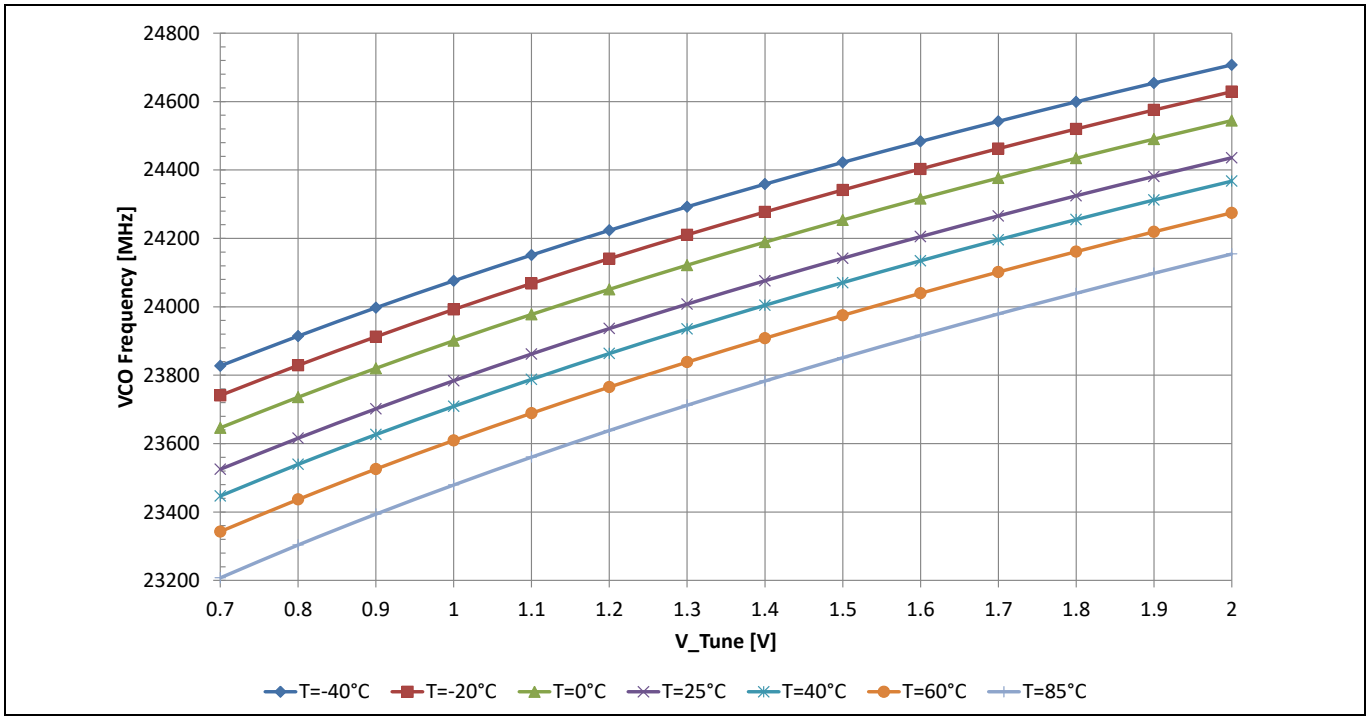

Figure 8 VCO frequency vs. tuning voltage and temperature

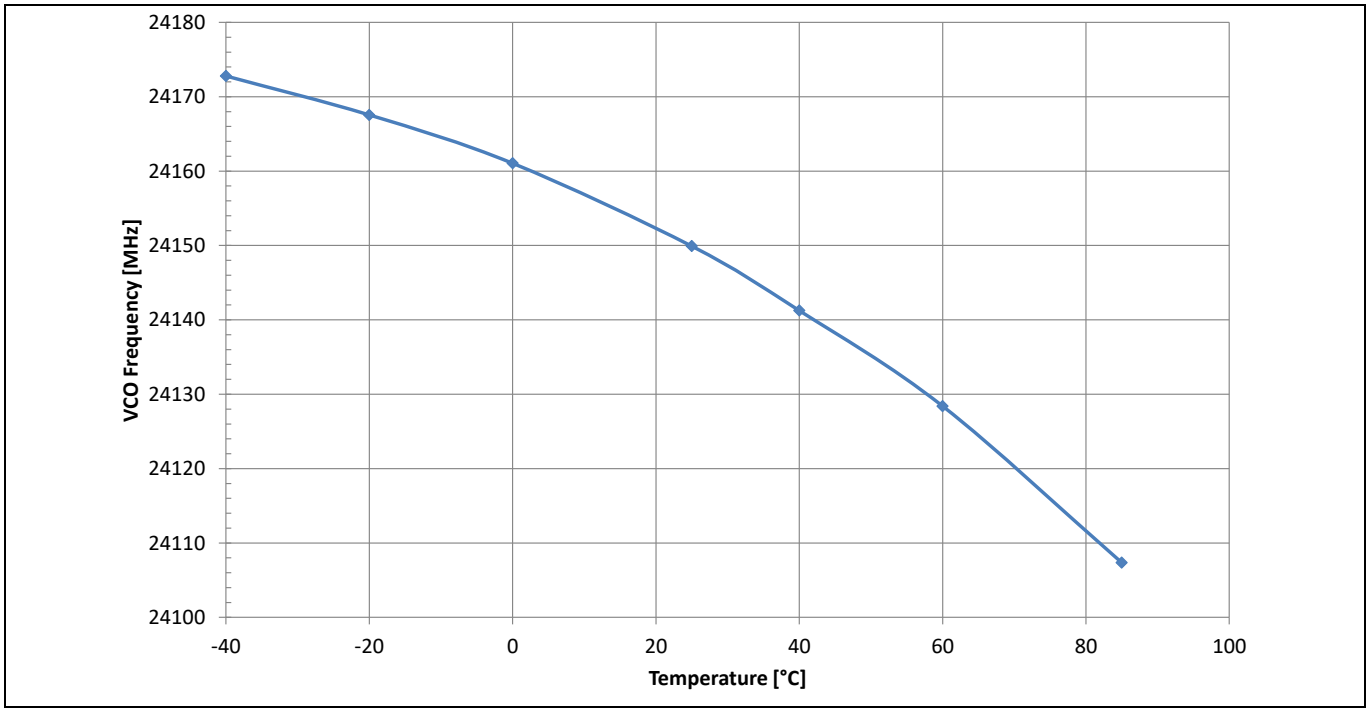

Figure 9 VCO frequency vs. temperature, VCO controlled by PTAT voltage source. Measured at random sample.

2.4 Proportional to absolute temperature (PTAT) voltage source

The PTAT voltage source generates a voltage V_{PTAT} at the V_PTAT pin (pin 15) which is proportional to the temperature of the chip. It is powered separate from VCC via the VCC_PTAT pin (pin 16).

The PTAT voltage source generates a tuning voltage for the VCO in Doppler mode, see section 4.1.

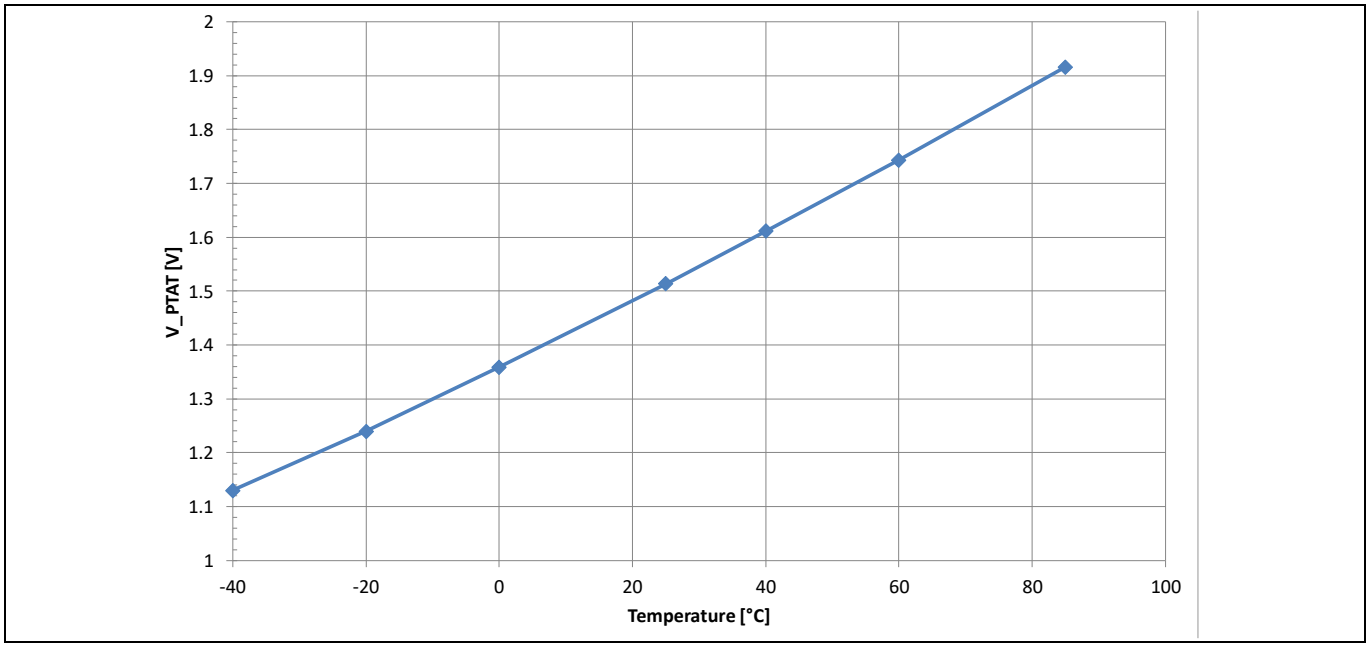

Figure 10 Voltage generated by PTAT voltage source vs. temperature for a random device.

2.5 Frequency divider

BGT24LTR11's frequency divider has two divider ratios, divide by 16 and divide by 8182 which result in output frequencies of 1.5 GHz and 3 MHz respectively.

Table 2 Setting the divider ratio

Divider ratio	Voltage at VCC_PTAT (pin 16)
16	< 0.8 V
8192	3.3 V

Setting the divider to a 3 MHz output will cause the PTAT to consume current. This ratio is usually used only in case of a software controlled VCO. In this use case, the V_{PTAT} is also required to check the validity of the used look-up table (LUT), as explained in section 4.3.

3 Evaluation board

3.1 Schematic diagram

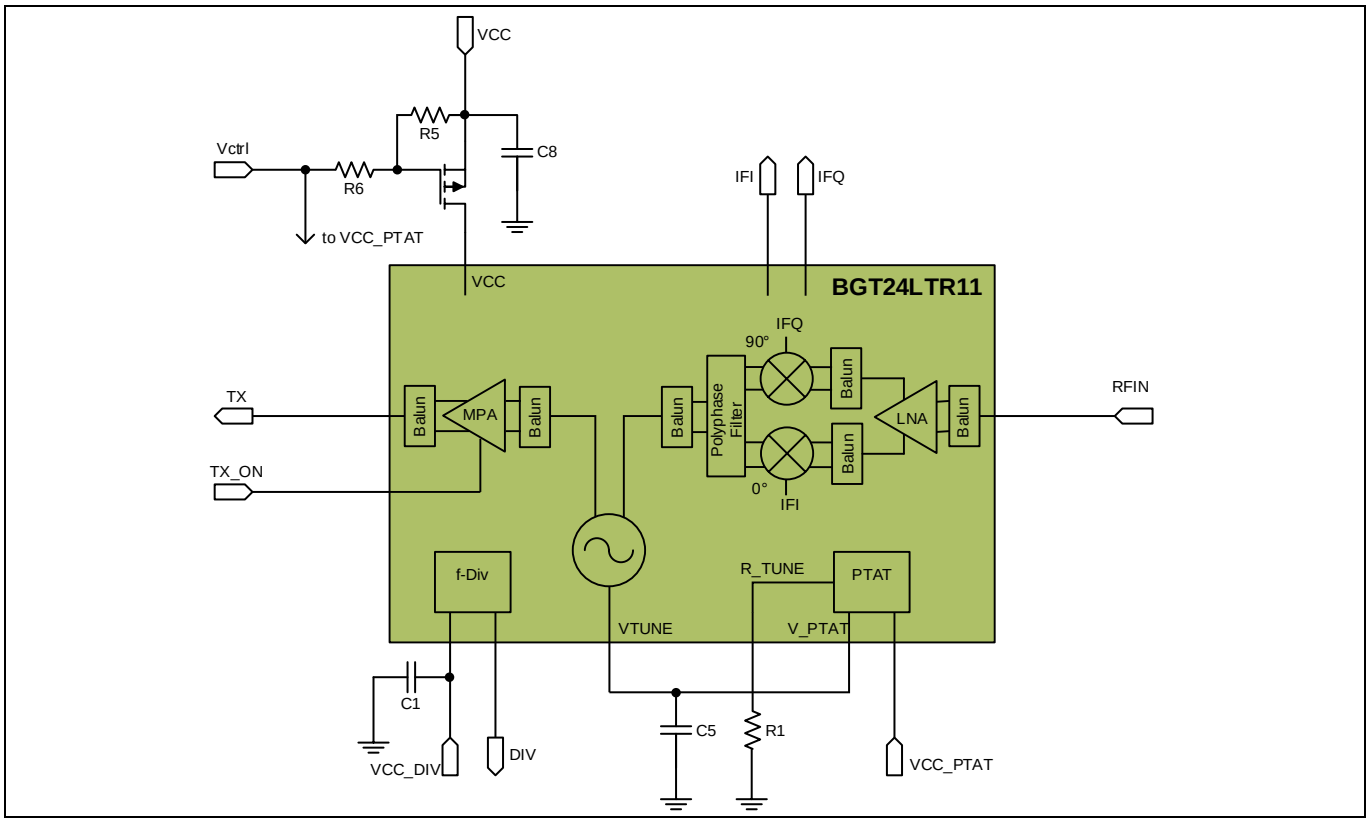

Figure 11 Schematic diagram of the BGT24LTR11 EVAL board

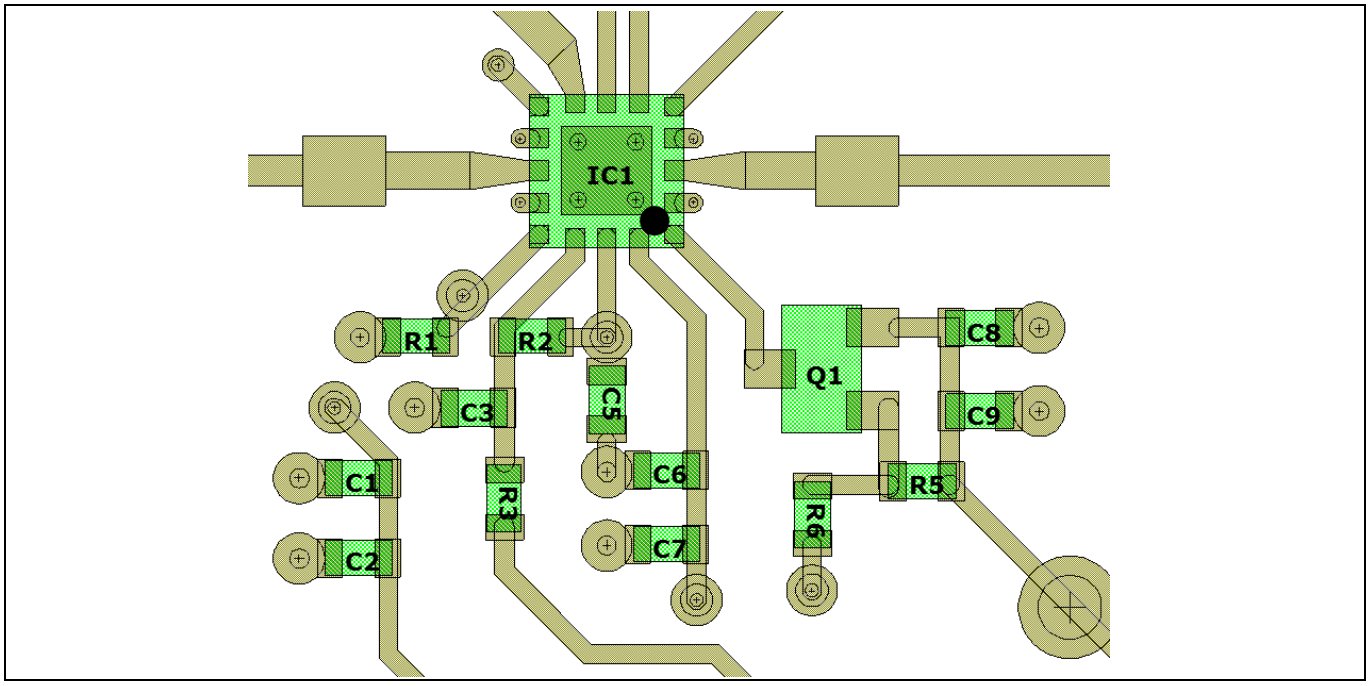

Figure 12 Component placement

Table 3 Bill of materials (BOM)

Designation	Part type	Value	Package	Manufacturer
C1, C5, C8	Chip capacitor	1 µF	0402	Various
C2, C3, C6, C7, C9		DNP	0402	
R1	Chip resistor	16 kΩ	0402	Various
R2,R3	Chip resistor	0 Ω	0402	Various
R5	Chip resistor	100 kΩ	0402	Various
R6	Chip resistor	1 kΩ	0402	Various
Q1	p-MOSFET	BSS209PW	SOT-323	Infineon
IC1	Radar MMIC	BGT24LTR11N16	TSNP-16-9	Infineon

3.2 Matching structures

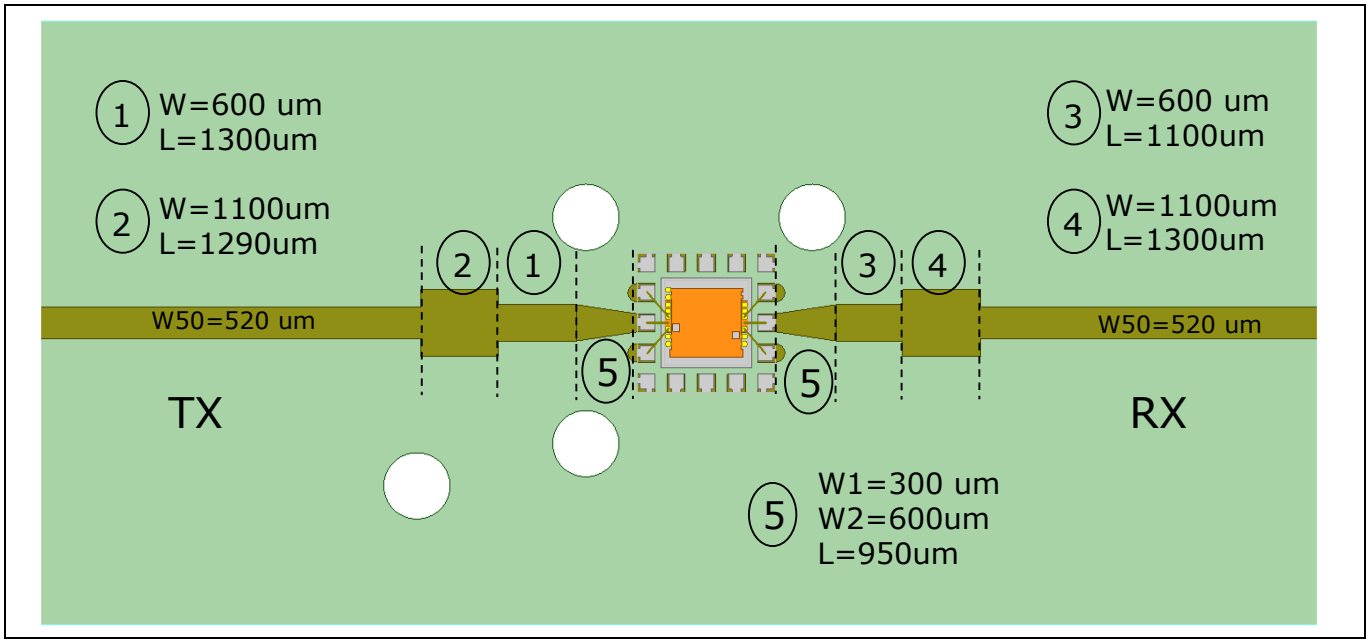

Figure 13 Matching structures on a Ro4350B substrate with a thickness of 0.254

3.3 Layout

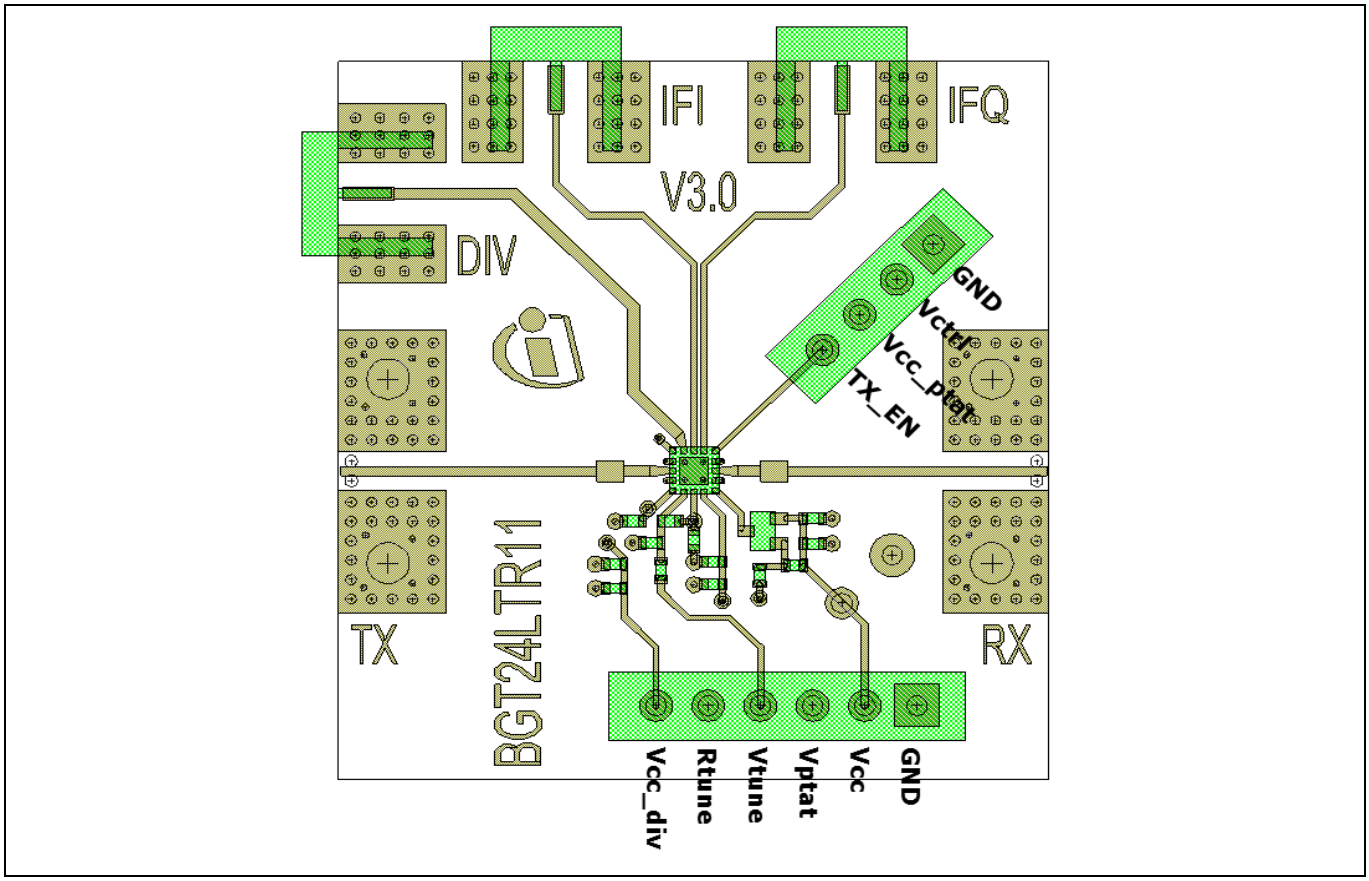

Figure 14 Layout with description of pin headers

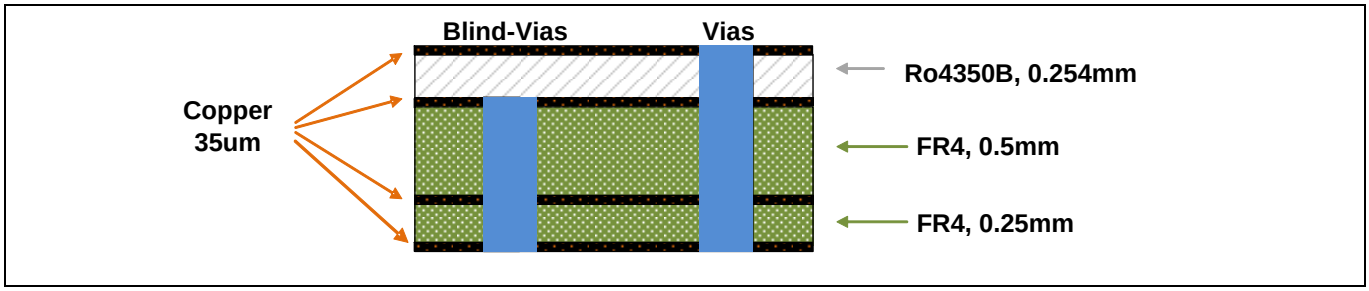

Figure 15 Layer stackup

3.4 Layout version improving TX to RX isolation

The isolation between the TX port and the RX port on the standard evaluation board is typically about 25 dB. This isolation can be improved to 35 dB by adding a grounded length of line at the ground pins next to the TX output pin, as shown in Figure 16. Details of the used compensation structures can be found in Figure 17.

Table 4 TX to RX isolation

	Standard evaluation PCB	PCB with compensation structures
TX to RX isolation (in dB)	25	35

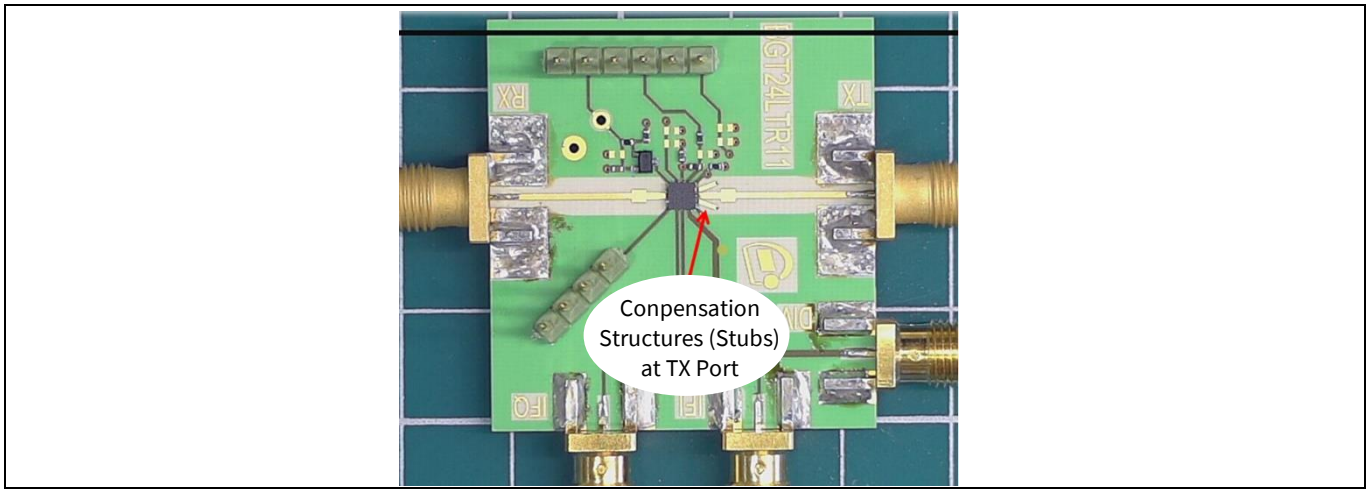

Figure 16 Addition of compensation structures to increase TX to RX isolation

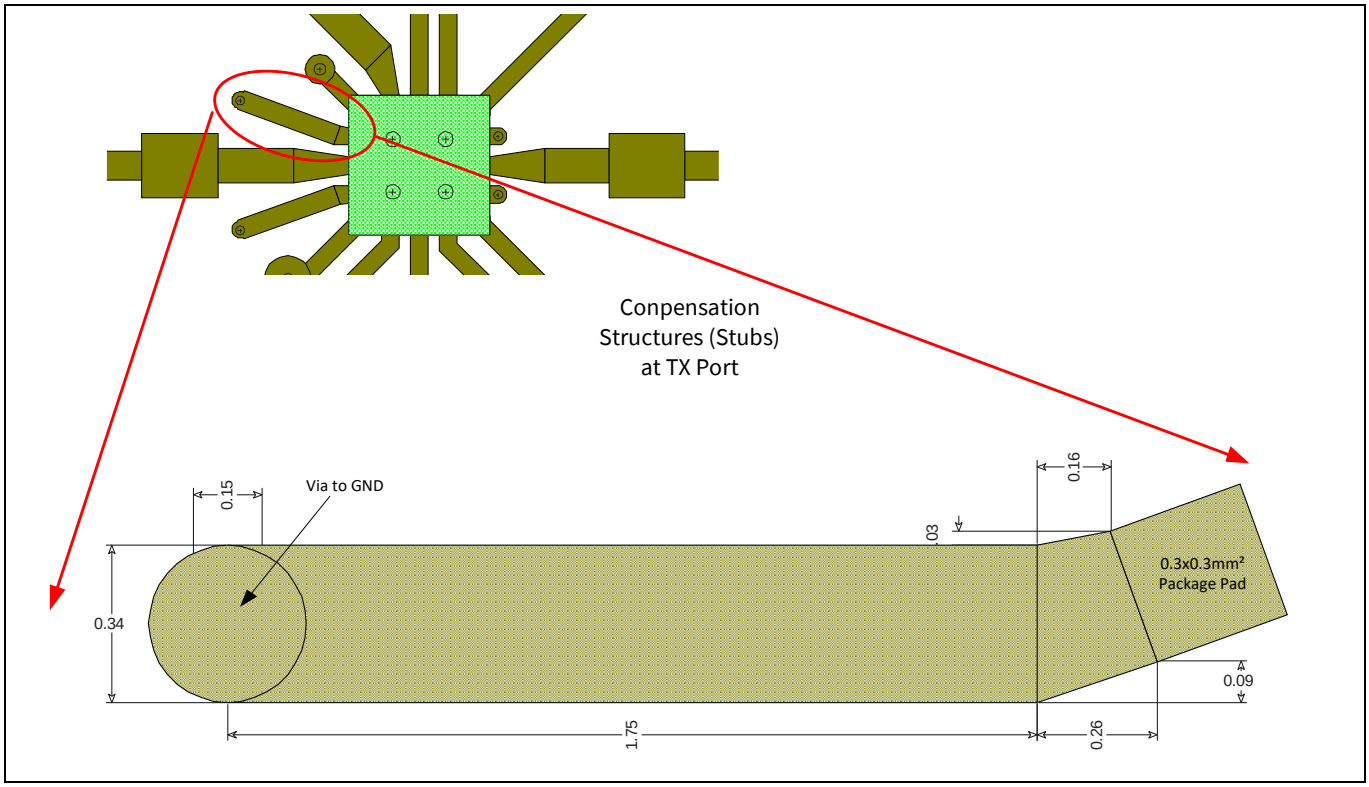

Figure 17 Compensation structures in detail – all dimensions in mm

4 VCO control

4.1 VCO control using PTAT

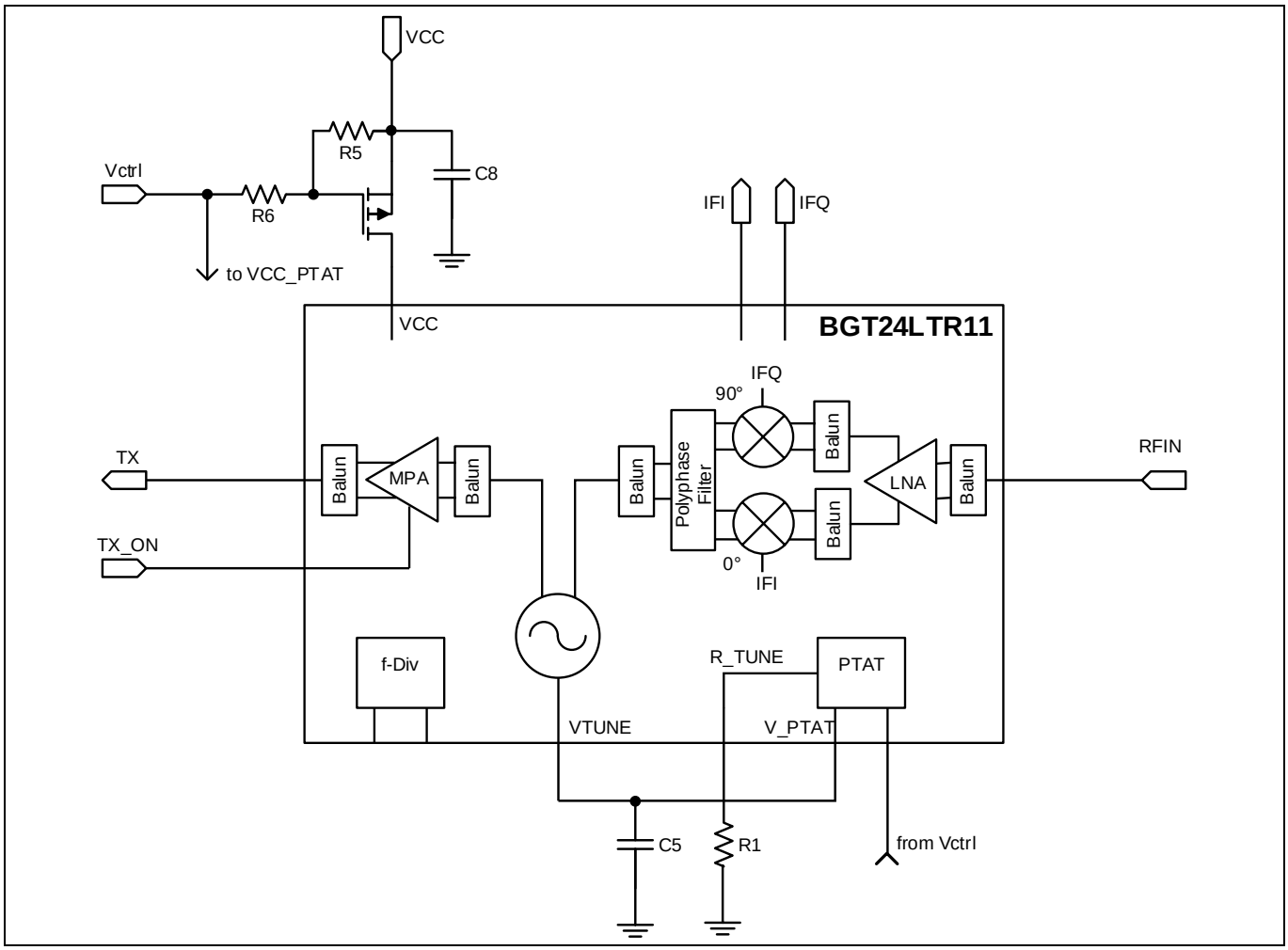

Figure 18 Block diagram of using V_PTAT to keep BGT24LTR11 in the ISM band

BGT24LTR11 was designed to keep its transmit frequency inside the ISM band without the need for a dedicated frequency control circuit like a PLL or an LUT based control of VTUNE. In Doppler radar mode, frequency adjustment via V_PTAT is the most efficient way.

Exact frequency control in Doppler radars in the 24 GHz ISM band is not really necessary for most applications. If we assume the transmit frequency to be at the lower edge of the band while it is actually at the upper edge, the introduced error is only 0.8%. However, it is necessary that the TX signal stays inside the ISM band under all conditions.

The analog V_{PTAT} control signal forces the VCO into the opposite direction in case of temperature drift. Doing so, the temperature effect of the VCO is strongly reduced. R1 adjusts the relative level of V_{PTAT}. To buffer and reduce noise on V_{tune} (V_{PTAT}), capacitor C5 (big capacitor) is charged by V_{PTAT} while the rest of the chip is turned OFF to save power during duty cycle OFF time. Going into duty cycle ON mode, the chip is fully supplied and VCC_PTAT (via V_{ctrl}) is disconnected to drive VTUNE from C5.

There are two reasons for toggling VCC and VCC_PTAT:

- Turning off VCC and VCC_PTAT reduces current consumption (45 mA and 1.5mA, respectively)
- The PTAT source generates noise at its output when running, and this noise on the tuning voltage will degrade the signal-to-noise ratio (SNR) of the system. However, for some short range this SNR might still be acceptable.

Operation:

1. TX_ON = 0 V. Disables TX output to prevent out of band emissions.
2. Vctrl = 3.3 V. This turns on the PTAT source (VCC_PTAT = 3.3 V) while VCC line for the entire RF stage including the VCO is disconnected from the power supply.
3. Wait for C5 to be charged. At the start-up of the system when the capacitor is fully discharged, this will require a longer time. During normal operation, the capacitor is only slightly discharged and will be very quickly recharged.
4. Vctrl = 0 V. Turn off PTAT and turn on the rest of the chip (RF with VCO).
5. Wait for VCO to settle its frequency. Settling time of the VCO is maximum 100 ns.
6. TX_ON = 3.3 V. Enables TX output.
   TX_ON should be delayed by about 200ns vs. RF section ON (Vctrl = 0 V) to keep TX signal clean.
7. Sample IF frequency.
8. Go to 1.

Further reduction of the power consumption is possible by introducing a time frame when both VCC and VCC_PTAT are disconnected. This would mean that VCC_PTAT needs to be disconnected from Vctrl and one more independent GPIO pin needs to be available at the microcontroller unit (MCU) in the system.

4.2 VCO control using a PLL

A PLL can be connected to the BGT24LTR11 to control the VCO as shown in Figure 19.
To implement this, the frequency divider needs to be set to a ratio of 16 by connecting VCC_PTAT to GND.

The VCO output is split into the TX antenna path and the local oscillator (LO) path. Furthermore, the VCO output signal gets divided by a factor of 16 (prescaler), producing a 1.5 GHz divider output signal for the PLL.

In the PLL, further dividers (N-divider) are applied to the input divider signal to further reduce the frequency. The phase detector (PD) in PLL compares the N-divider output signal with the reference from a crystal oscillator to control the PLL charge pump (CP). The CP_{out} is converted into an analog VCO tuning signal (VTUNE) via the loop filter (LF). VTUNE finally controls the VCO frequency to achieve a full signal fit between N-divider output signal and the reference signal to achieve a frequency and phase lock.

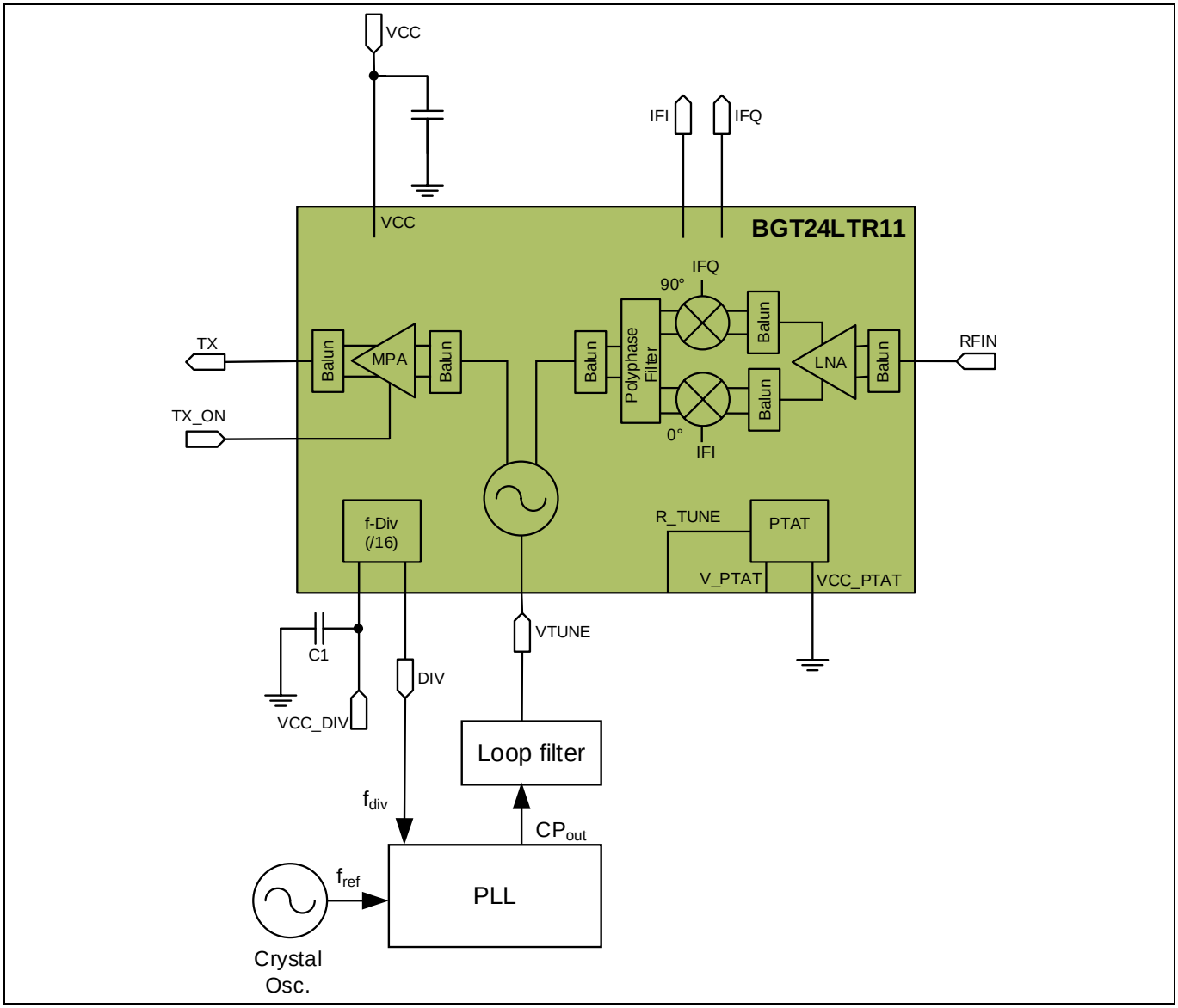

Figure 19 Block diagram of VCO control using a PLL

4.3 VCO control using a software based open-loop concept

It is possible to control BGT24LTR11 using a software-based open loop concept. In this approach, a loop is needed with a voltage source and feedback which is used to adapt the needed frequency changes. This implementation has the advantage of reducing the PCB space, BOM cost and power consumption by eliminating the HW PLL.

In this software based open-loop concept – often called as “Software PLL” – there is no VCO phase and frequency locking to a reference signal. Frequency is measured periodically and VCO is tuned accordingly. VCO Phase Noise (PN) is comparable to the freewheeling VCO (best case) and not improved like the HW PLL can do. However, VCO PN is less critical in Short Range Radar applications, because PN in the TX, RX and LO path stays mainly correlated for short target distances, resulting is a strong reduction of residual PN in the down-mixed IF. (referring to: Range Correlation Effect).

Both Doppler radar and stepped-FMCW radar can be realized with this software based open-loop VCO adjustment/sweeping concept. System-performance might be lower than a HW PLL, but is often sufficient for a lot of applications like smart lighting or proximity detection etc.

4.3.1 Hardware setup

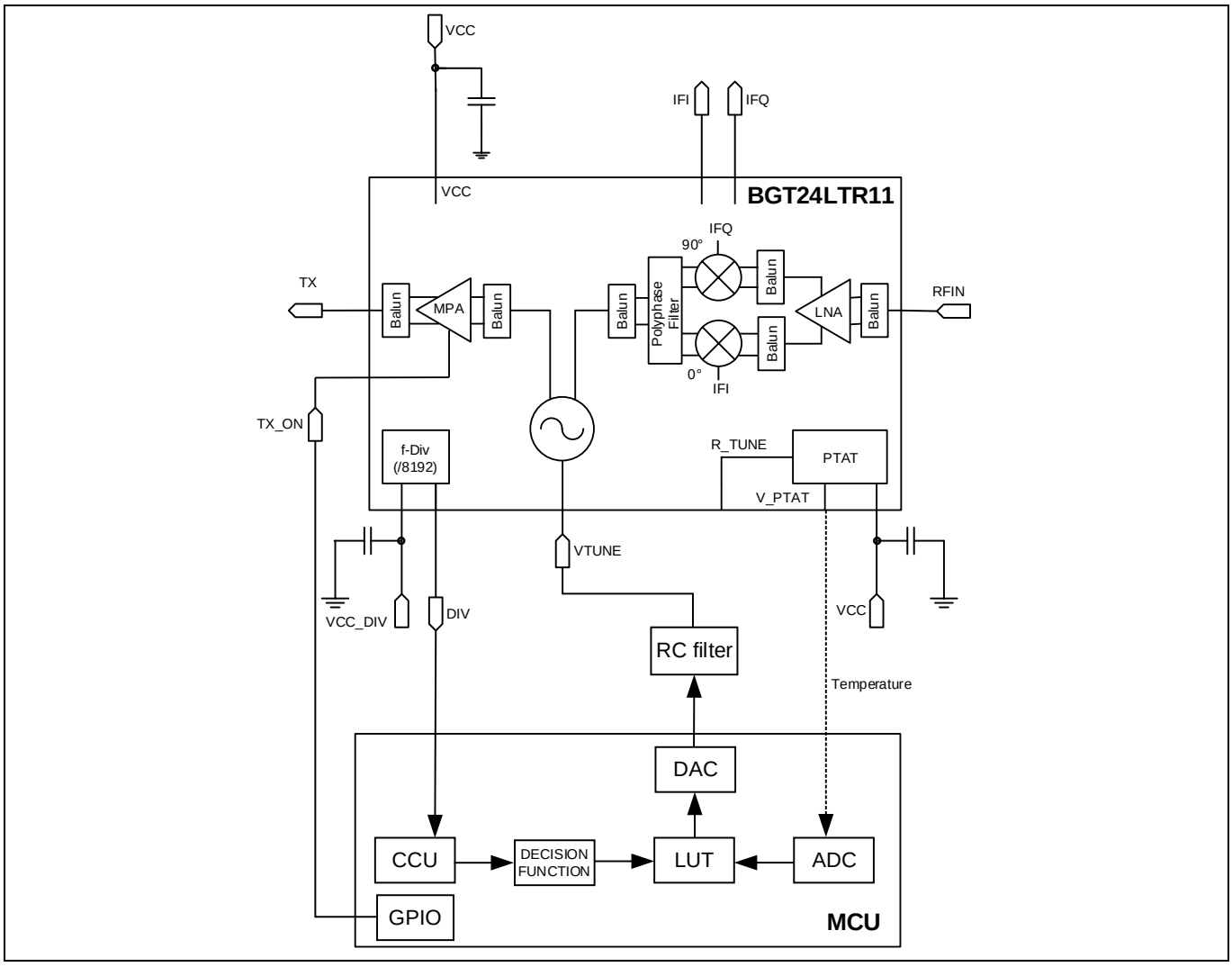

Figure 20 Block diagram of VCO control using a software-based open-loop concept

Figure 20 shows a block diagram on how to set up the system.

- Connect the VCC_DIV and VCC_PTAT to VCC to set the divider ratio to 8192.
- Connect the divider output to a Capture & Compare Unit (CCU) of the MCU to determine the frequency of the oscillator.
- Connect the MCU's digital-to-analog converter (DAC) output to the V_TUNE of BGT24LTR11 through a 2-stage RC filter to provide a tuning voltage to the VCO.
- The 2-stage RC DAC filter is required to filter the noise and reject the higher unwanted frequencies. It should be placed as close to the VCO V_TUNE input as possible.
- The design of this RC DAC filter is critical to avoid VCO modulation with noise and spurs. For a stepped-FMCW approach, the DAC filter needs to be optimized for the update rate based on the chirp time (Tc) and number of samples per chirp (Nsamples). For example, for a Tc = 1500 ms and Nsamples = 256, the update rate is 1500 ms / 256 = 6 µs (step-time). Therefore, the RC time constant for the DAC filter should be designed to settle at 5 µs (90…95% of the desired voltage step). This lets the DAC's output voltage and consequently the VCO frequency to be in a steady state at the end of step-time when the baseband analog-to-digital converter (ADC) is triggered for measurement.
- As an option, connect the V_PTAT output from BGT24LTR11 to an ADC channel of the MCU to determine the temperature of the chip. This would allow compensating the frequency shift due to temperature changes and would reduce the need to re-calibrate the SW PLL very frequently.

4.3.2 Concept

As shown in Figure 20, the DAC of the MCU is used to generate a tuning voltage for the VCO input. Vtune is generated by the DAC for the start frequency and then filtered in the RC-filter (2 stages). According to the Vtune input, the VCO produces the TX/LO signal. The VCO signal is also fed into a frequency divider and gets divided by a factor of 8192. This divided signal is captured by the CCU in the MCU. The divider output signal is measured by counting the number of rising/falling (or both) edges of the MCU's master clock inside a certain number of divider output signal periods (counting gate). The measured frequency is then compared with the required start frequency (24.025 GHz / 8192 = 2.9327 MHz). The difference between the measured and required frequency is then evaluated in the decision function. Depending on the result, the bit value gets adapted, and the loop starts again until the measured and wanted frequency to agree within a certain margin. This routine is repeated for the stop frequency as well (24.225 GHz / 8192 = 2.9571 MHz).

Note: To prevent out of band emissions, a guard band of 25 MHz between ISM band edges and the Start/Stop frequency of the stepped-FMCW sweep is implemented. Therefore, the chirps have a bandwidth of 200 MHz (24.025 GHz - 24.225 GHz) and calibration is done every frame. The guard band would change depending on the circuitry implemented and how often the calibration is done.

*Note: The 200 MHz bandwidth is split up into a certain number of points per chirp (Nsamples). Nsamples is related to unambiguous range and therefore impacts the maximum range (Rmax =Nsamples*ΔR), where Rmax is the maximum achievable range and ΔR is the range resolution.*

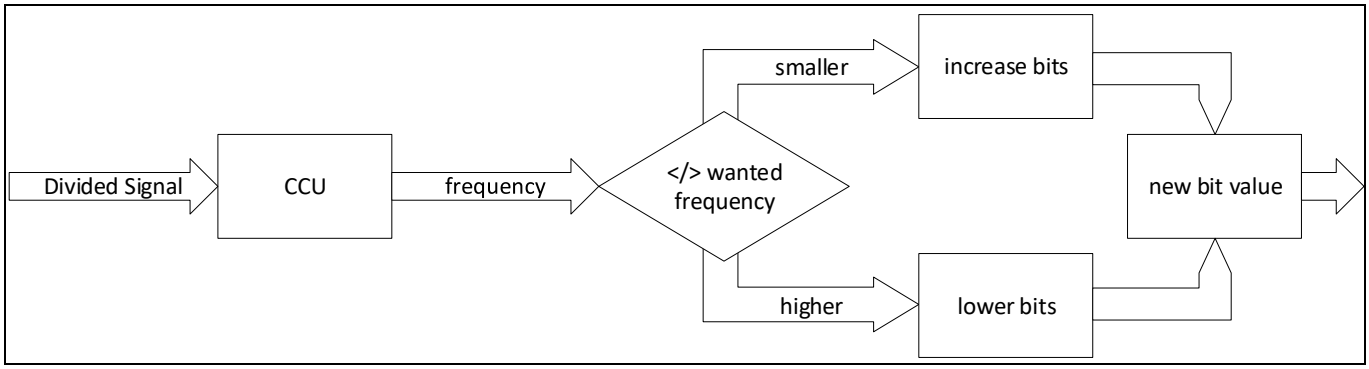

Figure 21 Decision function

The length of the counting gate has a strong impact on the accuracy of the VCO frequency measurement. At the start and at the end of the counting gate (N times the period of the divider output signal), there is a systematic error caused by the period of the MCU master clock. Longer counting gate time (i.e., a greater number of periods of the MCU master clock – e.g., 80 MHz – are counted) results in a lower impact of this systematic error on VCO frequency measurement accuracy. However, longer counting gate time results in a longer ON time for the BGT24LTR11 and impacts the overall power consumption.

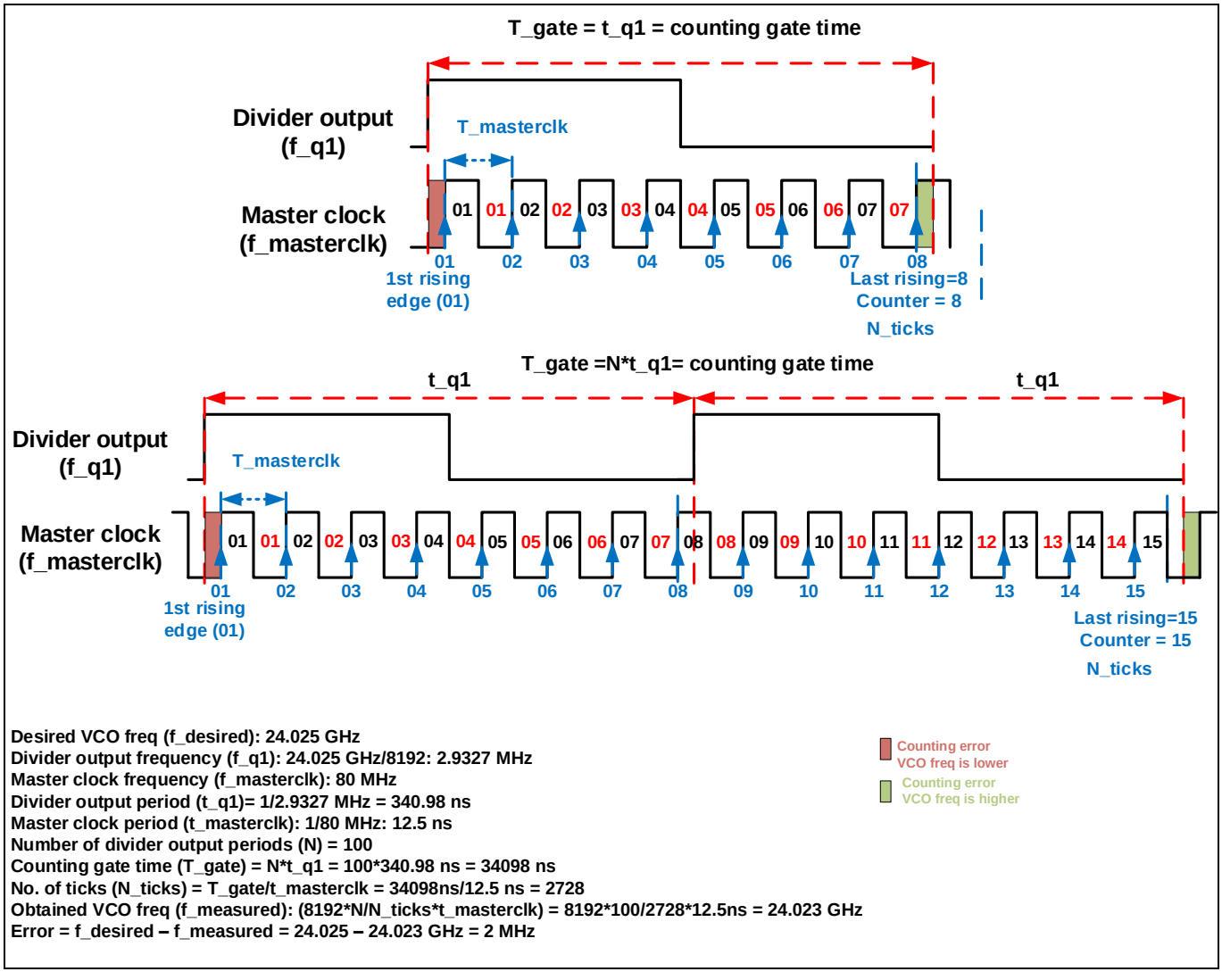

Figure 22 Systematic timing error at the start and the end of the counting gate

For a divider output frequency of ~3 MHz and an MCU master clock of 80 MHz, we recommend counting over 100 periods (N=100) of the divider output signal, to get a maximal frequency measurement error < 10 MHz.

Another way to reduce this systematic timing error would be to increase the master clock frequency (for example, a master clock of 120 MHz instead of 80 MHz will reduce the error as the T_clock time will be reduced from 12.5 ns to 8.3 ns, and the maximal frequency measurement error is < 6 MHz). However, higher master clock frequency leads to higher power consumption by the microcontroller.

Note: *To stay inside the ISM band during the frequency search process, the smart search for the start frequency always begins with a DAC value generating a VCO frequency **above** the desired start frequency. Similarly, stop frequency search should begin **below** the desired stop frequency.*

With the achieved start- and stop frequency DAC values (and Vtune values) a linear interpolation can be done and an LUT “DAC value vs. VCO Frequency” is generated. The contents of the LUT are clocked (e.g., via DMA) to the DAC and hence provide the modulation of the VCO.

To further improve the linearity of the chirps, it is possible to do a search for three or more frequency points and perform a polynomial approximation between these points to fit the Vtune vs. VCO Frequency in a more precise non-linear LUT. Also, by utilizing the chip’s temperature information (e.g., via PTAT), the LUT can be re-calibrated only when there is a change in the chip’s temperature. This would reduce the need to calibrate the LUT very frequently.

4.3.3 Operation

1. To get the best frequency measurement accuracy (No VCO pulling effect), TX should remain ON during the frequency search process. VTUNE must keep the VCO in the ISM band all the time by following the ‘smart search’ methodology from section 4.3.2.
2. Check the temperature of the chip using the V_{PTAT}. (if implemented)
3. Set the DAC to a fixed starting value for start frequency search to generate a VTUNE voltage for the VCO.
4. CCU measures the frequency of the divider output signal. The desired start frequency is already known and compared with the measured frequency. The DAC value is then adjusted using a decision function to achieve the best possible match for the desired frequency. (iterative frequency search process)
5. Once the DAC value for the start frequency is found, repeat the steps 3 and 4 to search the appropriate DAC value for the stop frequency.
6. Using these start and stop DAC values, generate an LUT that gives the DAC values corresponding to different VCO frequencies.
7. Use the generated LUT for the modulation of the VCO by clocking the LUT values (e.g., via DMA) to the DAC. Feed the DAC output to the DAC filter. After the DAC filter output has settled on the step, take the ADC measurement, and then move the DAC to the next LUT step, creating a stepped-FMCW chirp.
8. Check the temperature of the chip. If the temperature changed, or it is the beginning of a new frame go to 1 else go to 7 to generate the next chirp.

References

[1] Infineon Technologies AG. *BGT24LTR11N16 MMIC datasheet;* Available online

Revision history

Document revision	Date	Description of changes
1.30	2017-11-03	Initial release
1.40	2019-07-09	8 f: Corrections to PTAT source Section 4: Detailed description of the VCO control through PTAT, PLL and Software-controlled loop
1.50	2023-02-14	Miscellaneous document cleanup updates

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