

# TLE9018DQK

## Li-ion battery monitoring and balancing IC



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Simulation



Support



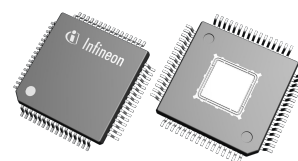
RoHS



ISO 26262  
compliant

## Features

- General
  - Voltage monitoring of up to 18 battery cells connected in series
  - Robust 120 V automotive technology for strong ESD performance and hot-plugging without external protection
  - Dedicated 16-bit delta-sigma ADC for each battery cell
  - High-accuracy measurement for SoC and SoH calculation
  - Integrated stress sensor with digital compensation algorithm and temperature-compensated measurements
  - Secondary ADC with advanced end-to-end safety mechanism averaging filter characteristics
  - Eight temperature measurement channels for external NTCs
  - Internal temperature measurement and monitoring
  - Integrated balancing switch allowing up to 300 mA balancing current per cell simultaneously
  - Galvanically isolated serial interface for daisy chain and ring mode communication
  - Supports capacitive coupling and transformer coupling
  - Differential robust serial 3 Mbit/s communication interface
  - SPI master interface
  - Several wake sources
- Diagnostics and safety
  - Internal round robin cycle routine to trigger safety mechanisms
    - Automatic balancing overcurrent and undercurrent detection scheme
    - Automatic open load detection scheme
    - Automatic NTC measurement unit monitoring scheme
  - End-to-end CRC-secured iso UART/UART communication
  - CRC-secured configuration registers
  - Emergency mode for communication
- ISO 26262 Safety Element out of Context (SEooC) for safety requirements up to ASIL D
- Green Product (RoHS compliant)



## Potential applications

- Multi-cell battery monitoring and balancing systems
- Li-ion battery packs used in hybrid electric vehicles (HEV)

## Product validation

- Plug-in hybrid electric vehicles (PHEV)
- Battery electric vehicles (BEV)
- 12 V Li-ion batteries
- Energy storage systems

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

## Description

The TLE9018DQK is a Li-ion battery monitoring and balancing IC. The main function is monitoring of the temperature of a battery system and the voltage of each cell to ensure its function as well as the safety of the vehicle occupants.

Type	Package	Marking
TLE9018DQK	PG-LQFP-64	TLE9018DQK

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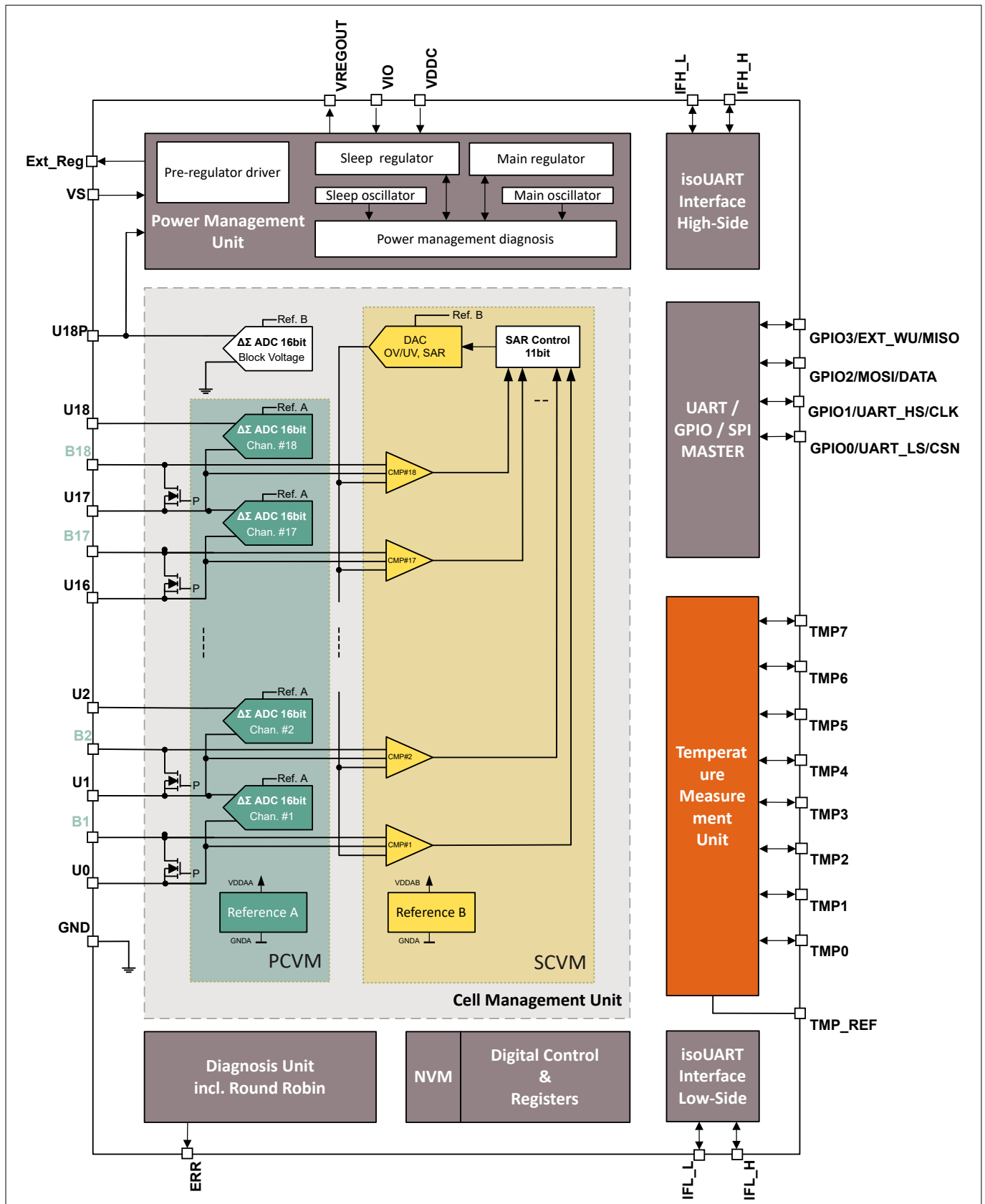
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## 1 Block diagram

### 1 Block diagram

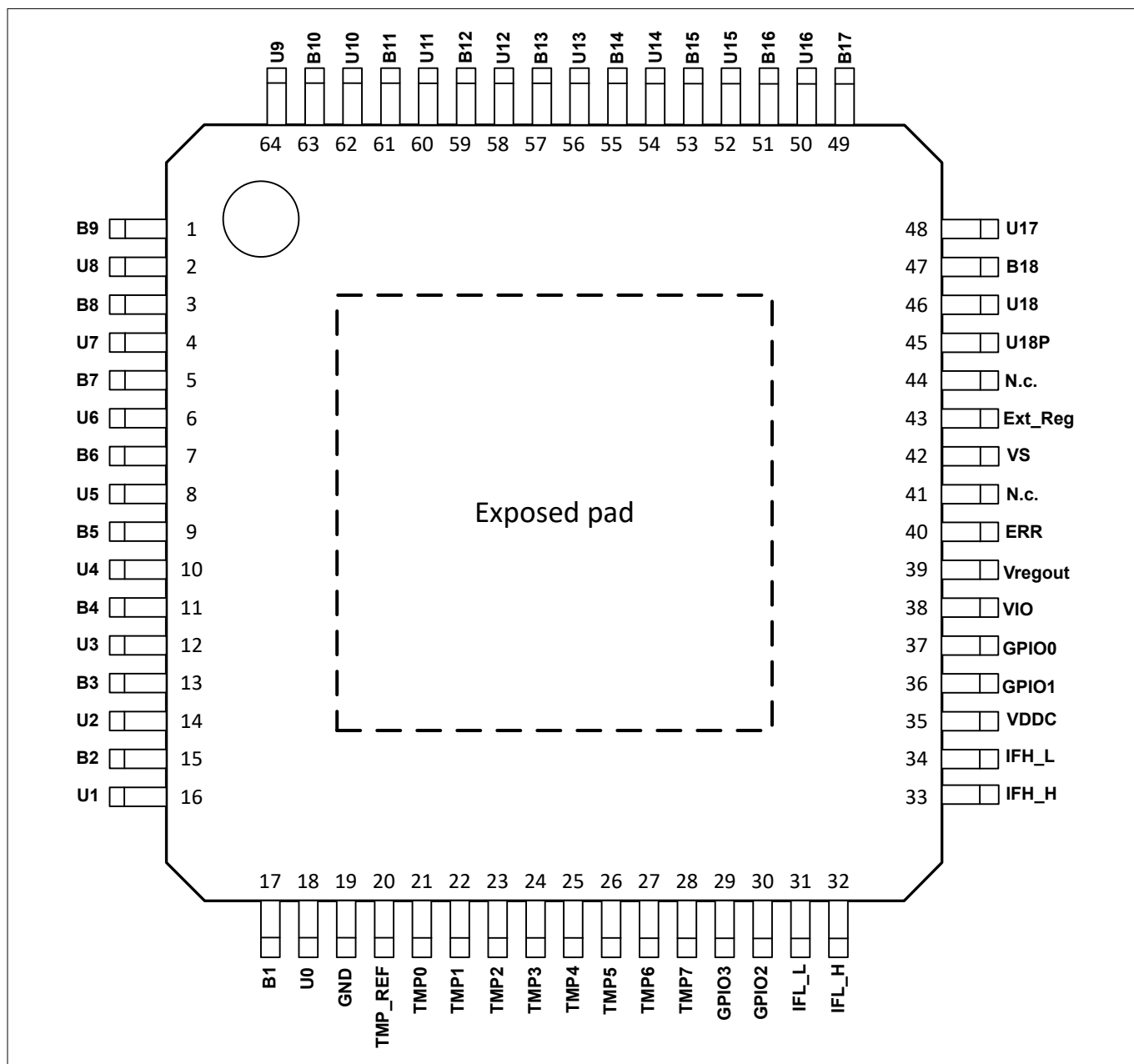


**Figure 1** Block diagram

## 2 Pin configuration

## 2 Pin configuration

### 2.1 Pin assignment



**Figure 2** Pin assingment PG-LQFP-64

### 2.2 Pin definitions and functions

Pin	Symbol	Pin type	Function
1	B9	A_I / O	Cell-balancing channel 9
2	U8	A_I	Cell voltage sense input channel 8
3	B8	A_I / O	Cell-balancing channel 8
4	U7	A_I	Cell voltage sense input channel 7

## 2 Pin configuration

Pin	Symbol	Pin type	Function
5	B7	A_I / O	Cell-balancing channel 7
6	U6	A_I	Cell voltage sense input channel 6
7	B6	A_I / O	Cell-balancing channel 6
8	U5	A_I	Cell voltage sense input channel 5
9	B5	A_I / O	Cell-balancing channel 5
10	U4	A_I	Cell voltage sense input channel 4
11	B4	A_I / O	Cell-balancing channel 4
12	U3	A_I	Cell voltage sense input channel 3
13	B3	A_I / O	Cell-balancing channel 3
14	U2	A_I	Cell voltage sense input channel 2
15	B2	A_I / O	Cell-balancing channel 2
16	U1	A_I	Cell voltage sense input channel 1
17	B1	A_I / O	Cell-balancing channel 1
18	U0	A_I	Cell voltage sense input channel 0, negative terminal (connect to local GND)
19	GND	GND	Local GND of CSC (Cell supervision circuit) device
20	TMP_REF	GND	Temperature sensor reference. Connect to local GND via filter or directly.
21	TMP0	A_I / O	Temperature sensor 0. If not used connect to GND. If TMP0 is disabled, the pin, can be used as a 0...2 V auxiliary ADC miscellaneous pin
22	TMP1	A_I / O	Temperature sensor 1. If not used connect to GND. If TMP1 is disabled, the pin can be used as a 0...2 V auxiliary ADC miscellaneous pin
23	TMP2	A_I / O	Temperature sensor 2. If not used connect to GND. If TMP2 is disabled, the pin can be used as a 0...2 V auxiliary ADC miscellaneous pin
24	TMP3	A_I / O	Temperature sensor 3. If not used connect to GND. If TMP3 is disabled, the pin can be used as a 0...2 V auxiliary ADC miscellaneous pin
25	TMP4	A_I / O	Temperature sensor 4. If not used connect to GND. If TMP4 is disabled, the pin can be used as a 0...2 V auxiliary ADC miscellaneous pin
26	TMP5	A_I / O	Temperature sensor 5. If not used connect to GND. If TMP5 is disabled, the pin can be used as a 0...2 V auxiliary ADC miscellaneous pin.
27	TMP6	A_I / O	Temperature sensor 6. If not used connect to GND. If TMP6 is disabled, the pin can be used as a 0...2 V auxiliary ADC miscellaneous pin. Input pin for bipolar auxiliary measurement

## 2 Pin configuration

Pin	Symbol	Pin type	Function
28	TMP7	A_I / O	Temperature sensor 7. If not used connect to GND. If TMP7 is disabled, the pin can be used as a 0...2 V auxiliary ADC miscellaneous pin. Input pin for bipolar auxiliary measurement
29	GPIO3/ Ext_WU/ MISO	D_I / O	General-purpose input/output channel 3. 4-wire SPI data input. This pin also functions as external wake-up input (high-active). If not used, connect pin to GND via pull-down resistor
30	GPIO2/ MOSI/ DATA	D_I / O	General-purpose input/output channel 2. 4-wire SPI data output. SPI half-duplex data interface pin. If not used, connect pin to GND via pull-down resistor
31	IFL_L	D_I / O	Lower isolated UART (iso UART) negative logic pin
32	IFL_H	D_I / O	Lower isolated UART (iso UART) positive logic pin
33	IFH_H	D_I / O	Upper isolated UART (iso UART) positive logic pin
34	IFH_L	D_I / O	Upper isolated UART (iso UART) negative logic pin
35	VDDC	S	Buffer capacitor pin for internal isolated UART (iso UART) supply
36	GPIO1/ UART_HS/ CLK	D_I / O	General-purpose input/output channel 1. UART high-side interface. SPI clock output pin. If not used, connect pin to GND via pull-down resistor
37	GPIO0/ UART_LS/ CSN	D_I / O	General-purpose input/output channel 0. UART low-side interface. SPI chip select pin. If not used, connect pin to GND via pull-down resistor
38	VIO	S	Input pin for digital GPIO reference. Place $C_{VIO}$ close to this pin
39	VREGOUT	S	Output pin for the internal 3.3 V regulator
40	ERR	D_O	Configurable high / low -active fault output to microcontroller. If not used, leave unconnected
41	n.c	n.c	Not connected. Leave unconnected in application
42	VS	S	Main supply pin
43	Ext_reg	S	Output pin for external regulator. If not used, leave unconnected
44	n.c	n.c	Not connected. Leave unconnected in application
45	U18P	S	Sleep mode supply pin. Connect to the positive terminal of topmost cell of the block. Input of the startup regulator
46	U18	A_I	Cell voltage sense input channel 18, positive terminal (uppermost cell in the block)



## 2 Pin configuration

Pin	Symbol	Pin type	Function
47	B18	A_I / O	Cell-balancing channel 18
48	U17	A_I	Cell voltage sense input channel 17
49	B17	A_I / O	Cell-balancing channel 17
50	U16	A_I	Cell voltage sense input channel 16
51	B16	A_I / O	Cell-balancing channel 16
52	U15	A_I	Cell voltage sense input channel 15
53	B15	A_I / O	Cell-balancing channel 15
54	U14	A_I	Cell voltage sense input channel 14
55	B14	A_I / O	Cell-balancing channel 14
56	U13	A_I	Cell voltage sense input channel 13
57	B13	A_I / O	Cell-balancing channel 13
58	U12	A_I	Cell voltage sense input channel 12
59	B12	A_I / O	Cell-balancing channel 12
60	U11	A_I	Cell voltage sense input channel 11
61	B11	A_I / O	Cell-balancing channel 11
62	U10	A_I	Cell voltage sense input channel 10
63	B10	A_I / O	Cell-balancing channel 10
64	U9	A_I	Cell voltage sense input channel 9
–	Exposed pad	GNDA	Connect to GND in the application

Pin types: A = analog, D = digital, S = supply, I = input, O = output, I/O = bidirectional, P = power

### 3 General product characteristics

## 3 General product characteristics

Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

### 3.1 Absolute maximum ratings

**Table 1 Absolute maximum ratings**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage VS	V <sub>VS_max</sub>	-0.3	–	90	V	–	PRQ-111
Supply voltage VS rel.	V <sub>VS_rel_max</sub>	V <sub>REGOUT</sub> T - 0.3	–	V <sub>U18P</sub> + 0.3	V	–	PRQ-113
Transient high voltage	V <sub>transient_high_max</sub>	90	–	120	V	Maximum accumulated transient duration 60 sec. Valid for following pins vs. GND: VS, Ext_reg, U18P, Un, Bn (0 ≤ n ≤ 18)	PRQ-114
Supply voltage U18P	V <sub>U18P_max</sub>	-0.3	–	90	V	–	PRQ-115
Supply voltage U18P rel.	V <sub>U18P_rel_max</sub>	V <sub>Ext_reg</sub> - 0.3	–	–	V	–	PRQ-663
Supply voltage VIO	V <sub>VIO_max</sub>	-0.3	–	5.5	V	–	PRQ-116
Regulator output VREGOUT	V <sub>REGOUT_max</sub>	-0.3	–	3.6	V	–	PRQ-117
Regulator output VDDC	V <sub>VDDC_max</sub>	-0.3	–	3.6	V		PRQ-118
External regulator output	V <sub>Ext_reg_max</sub>	-0.3	–	90	V	–	PRQ-568
Cell sense input voltage abs. Un	V <sub>Un_max</sub>	-0.3	–	90	V	0 ≤ n ≤ 18	PRQ-119
Cell sense input voltage rel. Un positive	V <sub>Un_rel_max</sub>	V <sub>Un-1</sub>	–	V <sub>Un-1</sub> + 10	V		PRQ-120
Cell sense input voltage rel. Un negative	V <sub>Un_max</sub>	V <sub>Un-1</sub> - 0.3	–	V <sub>Un-1</sub>	V	<b>1.</b> 1 ≤ n ≤ 18 <b>2.</b> R <sub>F</sub> at Un ≥ 4.5Ω <b>3.</b> R <sub>BAL</sub> at Bn ≥ 10Ω <b>4.</b> If voltage ≤ -0.5V, I <sub>Un</sub> < 1μA is not guaranteed.	PRQ-566

(table continues...)

### 3 General product characteristics

**Table 1** (continued) **Absolute maximum ratings**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cell balancing pin abs. Bn	$V_{Bn\_max}$	-0.3	–	90	V	$1 \leq n \leq 18$	PRQ-121
Cell balancing pins rel. Bn	$V_{Bn\_rel\_max}$	$V_{Un-1} - 0.3$	–	$V_{Un} + 0.3$	V	$1 \leq n \leq 18$	PRQ-122
General purpose I/O voltage abs. GPIOq	$V_{GPIOq\_max}$	-0.3	–	5.5	V	$0 \leq q \leq 3$	PRQ-123
General purpose I/O voltage rel. GPIOq	$V_{GPIOq\_rel\_max}$	-0.3	–	$V_{VIO} + 0.3$	V	$0 \leq q \leq 3$	PRQ-124
Open drain output pin abs. ERR	$V_{ERR\_max}$	-0.3	–	90	V	–	PRQ-125
Open drain output pin rel. ERR	$V_{ERR\_rel\_max}$	-0.3	–	$V_{VS} + 0.3$	V	–	PRQ-126
iso UART interface IFL_x	$V_{IFL\_L\_max}$ $V_{IFL\_H\_max}$	-2.7	–	5.5	V	<sup>2)</sup> BCI test max. 300 mA injected via twisted pair cable onto iso UART interface (max. pin current 150 mA)	PRQ-127
iso UART interface IFH_x	$V_{IFH\_L\_max}$ $V_{IFH\_H\_max}$	-2.7	–	5.5	V	<sup>2)</sup> BCI test max. 300 mA injected via twisted pair cable onto iso UART interface (max. pin current 150 mA)	PRQ-128
Temperature sensor input voltage abs. TMPz	$V_{TMPz\_max}$	-0.3	–	90	V	$0 \leq z \leq 7$	PRQ-129
Temperature sensor input voltage abs. TMP_REF	$V_{TMP\_REF\_max}$	-0.3	–	90	V	–	PRQ-131

#### ESD robustness

ESD robustness 2 kV	$V_{ESD\_2kV\_max}$	-2	–	2	kV	HBM; all pins <sup>1)</sup>	PRQ-145
ESD robustness 4 kV	$V_{ESD\_4kV\_max}$	-4	–	4	kV	HBM; robustness vs. GND for pins: Vs, Un, TMPz, TMP_REF, IFH_x, IFL_x, Bn <sup>1)</sup>	PRQ-146
ESD robustness CDM 500 V	$V_{ESD\_cdm\_all\_max}$	-500	–	500	V	CDM; all pins <sup>2)</sup>	PRQ-148
ESD robustness CDM 750 V	$V_{ESD\_Corner\_max}$	-750	–	750	V	CDM; corner pins <sup>2)</sup>	PRQ-149

(table continues...)

### 3 General product characteristics

**Table 1** (continued) **Absolute maximum ratings**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Temperatures							
Junction temperature Tj	Tj_max	-40	–	150	°C	–	PRQ-150
Storage temperature Tstg	Tstg_max	-55	–	150	°C	–	PRQ-151

- 1) ESD robustness, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).  
 2) ESD robustness, Charged Device Model JESD22-C101.

**Attention:** *Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the section “functional range” is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions the voltage on VDD pins with respect to ground shall not exceed the values defined by the absolute maximum ratings. Lifetime statements are an anticipation based on an extrapolation of Infineon’s qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. Lifetime statements shall in no event extend the agreed warranty period.*

### 3.2 Functional range

The following functional range shall not be exceeded in order to ensure correct operation of the device. All parameters specified in the following sections refer to these operating conditions unless otherwise indicated.

**Table 2** **Functional range**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage VS	$V_{VS\_functional}$	6	–	85	V	–	PRQ-152
Supply voltage U18P	$V_{U18P\_functional}$	6	–	85	V	–	PRQ-154
Supply voltage VIO	$V_{VIO\_functional}$	3	–	5.5	V	–	PRQ-155
Cell sense input voltage $U_n$	$V_{Un\_functional}$	$V_{Un-1}$	–	$V_{Un-1} + 7$	V	$1 \leq n \leq 18$	PRQ-156

### 3 General product characteristics

#### 3.3 Thermal resistance

**Table 3 Thermal resistance**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case $R_{thJC}$	$R_{thJC}$	–	–	5	K/W	–	PRQ-158
Junction to ambient $R_{thJA}$	$R_{thJA}$	–	25	–	K/W	<sup>1)</sup>	PRQ-160

1) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a  $76.2 \times 114.3 \times 1.5$  mm board with 2 inner copper layers ( $2 \times 70 \mu\text{m Cu}$ ,  $2 \times 35 \mu\text{m Cu}$ ). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.

#### 3.4 General electrical characteristics

**Table 4 General electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			

##### Input / Output definitions

Digital input low level	$V_{dig\_in\_lo}$	0	–	$V_{VIO} * 0.3$	V	GPIOq $0 \leq q \leq 3$	PRQ-356
Digital input high level	$V_{dig\_in\_hi}$	$V_{VIO} * 0.7$	–	$V_{VIO}$	V	GPIOq $0 \leq q \leq 3$	PRQ-357
Digital output low level	$V_{dig\_out\_low}$	0	–	0.45	V	1. GPIOq $0 \leq q \leq 3$ 2. $I_{GPIO} \leq 5 \text{ mA}$	PRQ-358
Digital output high level	$V_{dig\_out\_hi}$	$V_{VIO} - 0.45$	–	$V_{VIO}$	V	1. GPIOq $0 \leq q \leq 3$ 2. $I_{GPIO} \geq -5 \text{ mA}$	PRQ-359
GPIO output current	$I_{GPIO}$	-5	–	5	mA	GPIOq $0 \leq q \leq 3$	PRQ-360
External capacitance on GPIO	$C_{GPIO}$	–	–	30	pF	GPIOq $0 \leq q \leq 3$	PRQ-361

(table continues...)

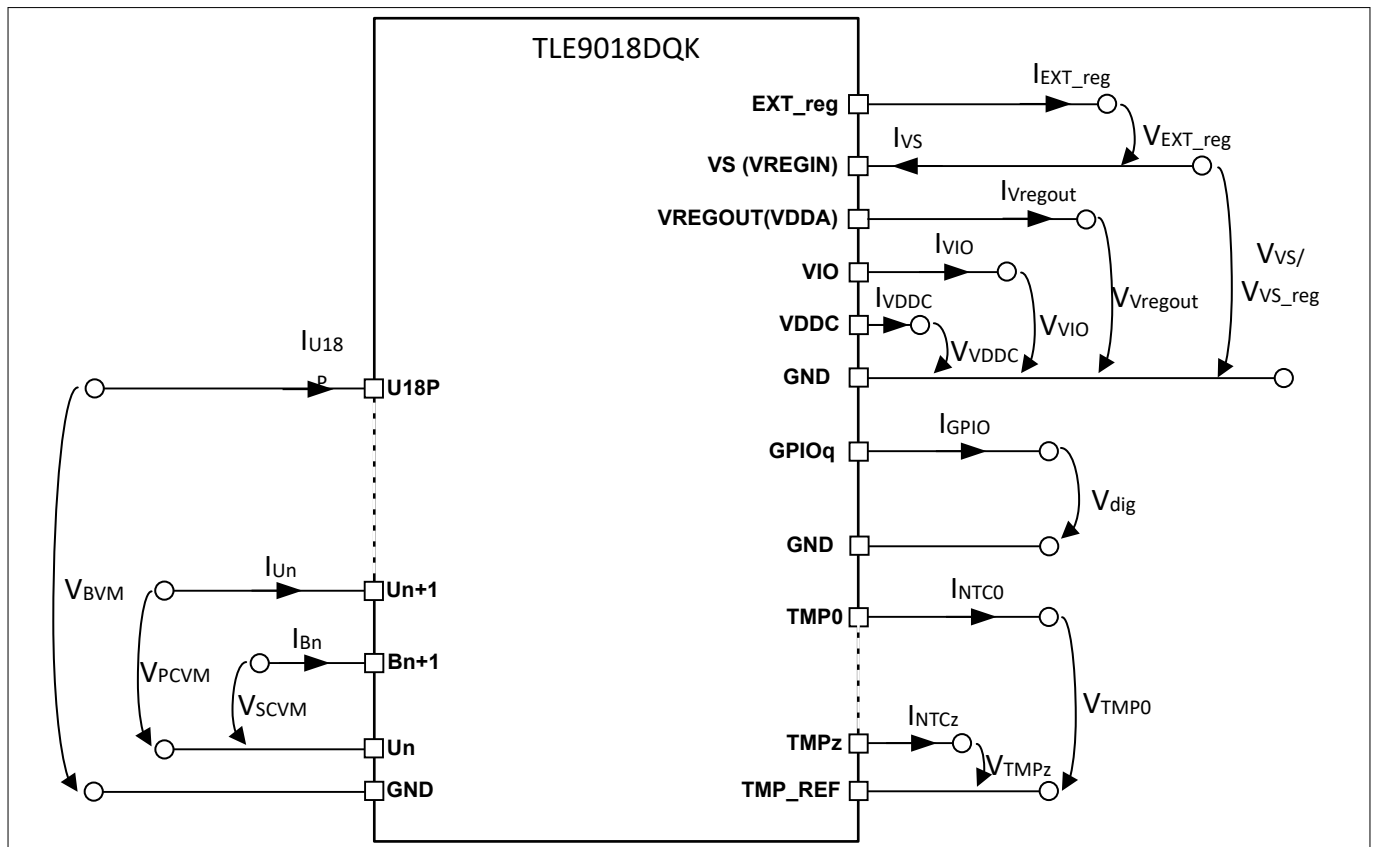
### 3 General product characteristics

**Table 4** (continued) General electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Leakage currents							
Input leakage current Un	$I_{Un\_leak}$	-500	–	500	nA	<b>1.</b> $0 \leq n \leq 18$ <b>2.</b> In sleep mode and idle mode <b>3.</b> $V_{Un} \leq 5.5\text{ V}$	PRQ-253
Input leakage current Bn	$I_{Bn\_leak}$	-500	0	500	nA	<b>1.</b> $1 \leq n \leq 18$ <b>2.</b> In sleep mode and idle mode. <b>3.</b> $V_{Bn} \leq 5.5\text{ V}$	PRQ-274

### 3.5 Definitions of voltages and currents



**Figure 3** Definitions of voltages and currents

## 4 Monitoring of internal oscillators (MIO)

### 4 Monitoring of internal oscillators (MIO)

The IC monitors two of the internal oscillators:

1. Main oscillator running at  $f_{\text{main\_osc}}$ . (Not running in sleep mode)
2. Sleep oscillator running at  $f_{\text{sleep\_osc}}$ .

During normal operation both oscillators are active. The oscillators monitor each other for drift and stuck-at errors. If an error is detected, the IC enters sleep mode. The incorrect functioning of the oscillator does not allow reliable writing to registers and hence the IC doesn't set error bits before entering sleep mode.

#### 4.1 Electrical characteristics monitoring of internal oscillators (MIO)

**Table 5**      **Electrical characteristics**

$V_{\text{VS}} = V_{\text{VS\_functional}}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Oscillator							
MIO Main unit oscillator frequency	$f_{\text{main\_osc}}$	13.44	14	14.56	MHz	–	PRQ-163
MIO Sleep unit oscillator frequency	$f_{\text{sleep\_osc}}$	90	100	110	kHz	–	PRQ-164

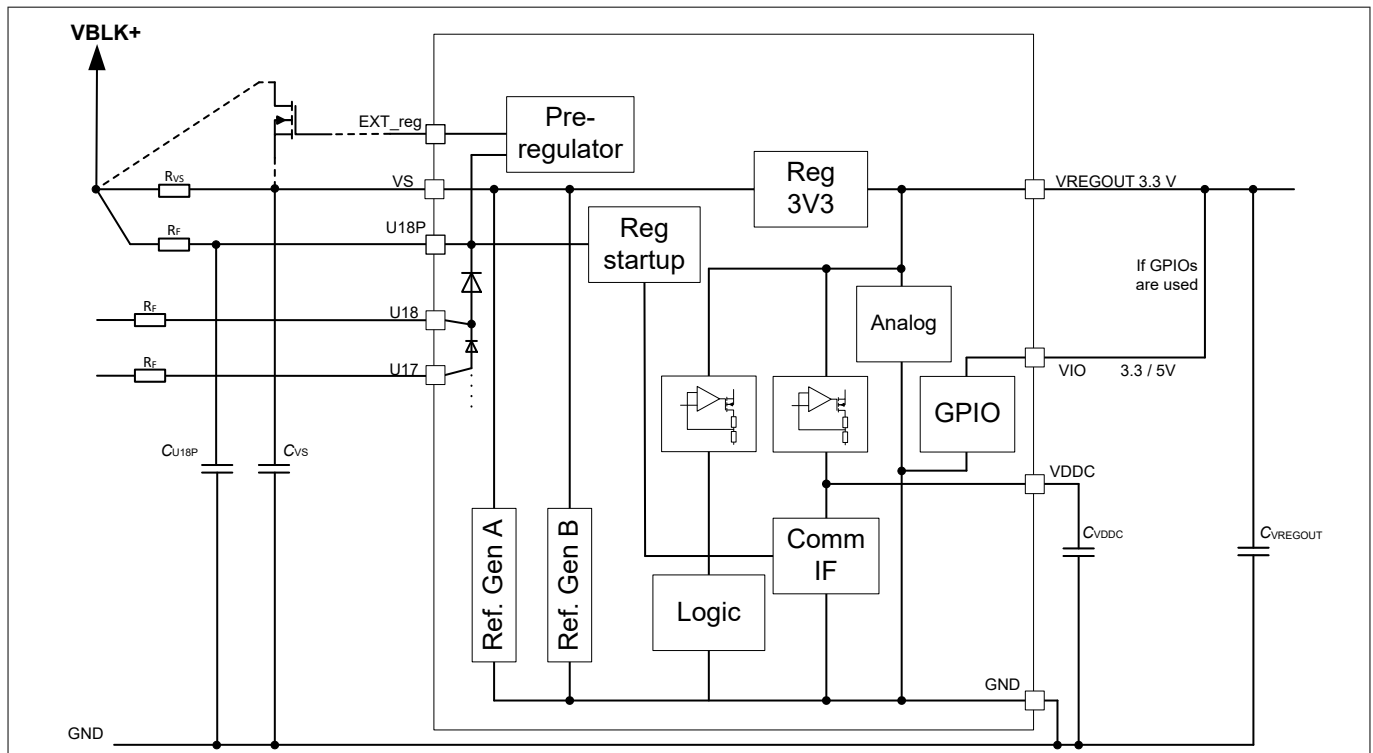
## 5 Power Management Unit (PMU)

### 5.1 Functional description

The IC has an internal power supply unit connected to the pins VS, U18P and GND. It consumes energy from the monitored battery cells and generates the internal supply voltages for the IC as well as the output voltages  $V_{VDDC}$  and  $V_{VREGOUT}$ .

*Note: The output pins VDDC and VREGOUT require a capacitance to ground as stated in the Application information/External components.*

*Note: No supply currents are drawn from Un pins.*



**Figure 4** Typical power supply configuration using the internal voltage regulator

The IC has a sleep mode with reduced current consumption,  $I_{U18P\_sleep}$ , via the sleep mode supply pin U18P. To enter this mode the PD bit in the OP\_MODE register has to be set.

*Note: If the watchdog is not being served the IC enters sleep mode as well.*

#### Reset:

To reset registers, except the supplied in sleep mode registers, the sleep mode bit PD in the OP\_MODE register has to be set. To reset all registers the bit SLEEP\_REG\_RESET in the OP\_MODE register has to be set.

#### Available voltages:

The device provides a regulated output voltage  $V_{VREGOUT}$  with an output current  $I_{VREGOUT}$  on pin VREGOUT which can supply the GPIOs of the device and other loads.

*Note: The output current is shared with GPIO supply, if the VIO pin is connected to VREGOUT.*

To supply the communication interface the device provides a regulated voltage  $V_{VDDC}$ .

To set the logic levels and supplying the GPIOs the VIO pin it used. The pin can be connected directly to the VREGOUT pin or to another desired voltage level using an external regulator.

#### Pre-regulator:



## 5 Power Management Unit (PMU)

Additionally to the internally regulated voltages the device provides the possibility to generate a configurable voltage called  $V_{EXT\_reg}$  by providing a reference output voltage at the EXT\_reg pin to bias an external pass device.

This feature is not mandatory and can be used to introduce a pre-regulator which lowers the supply voltage level of the device to  $V_{EXT\_reg}$  and hence reduces power dissipation within the IC. In case of an internal overtemperature event the device sets the internal overtemperature warning flag and is reducing the voltage  $V_{EXT\_reg}$  to its min value, if the flag is cleared the device returns to its configured voltage level. This feature works if the voltage at the pin U18P is higher than  $V_{U18P\_ext\_min}$ .

*Note: If not used the EXT\_reg pin has to be left open.*

### PMU protection functions:

The PMU incorporates an overcurrent protection. If the current  $I_{VREGOUT}$  exceeds  $I_{VREGOUT\_th\_OC}$  for a longer time than the deglitching time  $t_{PS\_ERR\_deg}$ , then it switches off the output voltage supply. The IC enters sleep mode after the deglitching time  $t_{PS\_ERR\_deg}$ . The power supply error sleep bit in the general diagnostics register indicates a fault, which can be read after waking up the IC

If the voltage  $V_{VDDC}$  falls below the undervoltage threshold  $V_{VDDC\_th\_UV}$  for a time longer than  $t_{PS\_ERR\_deg}$ , the IC enters sleep mode. The PS\_ERR\_SLEEP bit in the GEN\_DIAG register indicates a fault, which can be read after waking the IC.

If the voltage  $V_{VIO}$  falls below the undervoltage threshold  $V_{VIO\_th\_UV\_fall}$  for a longer time than  $t_{PS\_ERR\_deg}$ , the IC sets the VIO undervoltage error bit in the general purpose input/output register. After  $V_{VIO}$  has exceeded the  $V_{VIO\_th\_UV\_rise}$  threshold for longer than  $t_{PS\_ERR\_deg}$ , the UV\_VIO bit of the GPIO register is latched and can be cleared with a write command.

*Note: If the GPIO.VIO\_UV bit is 0, the GPIO functionality is enabled and wake-up via GPIO is possible.*

The IC ensures wake-up and operation even if any single wire connected to a cell is open in case of failure (assumption: supply pins connected on PCB level).

The device can activate a current sink to draw extra current into the VS pin with the defined current of  $I_{VS\_SINK}$ . To activate this current the bit VS\_SINK\_EN of the miscellaneous control register has to be set.

## 5.2 Electrical characteristics power management unit (PMU)

**Table 6**      **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Internal regulators							
Multi purpose output voltage	$V_{\text{REGOUT}}$	3.3	3.5	3.6	V	-10 mA ≤ $I_{\text{VREGOUT}}$ ≤ 0 mA No load on VIO	PRQ-176
Communication supply output voltage	$V_{\text{VDDC}}$	2.42	2.5	2.75	V	–	PRQ-177
VS sink current	$I_{\text{VS\_SINK}}$	19	20	21	mA	–	PRQ-557
Supply currents							
U18P idle current	$I_{\text{U18P\_idle}}$	–	5	8.2	μA	<ul style="list-style-type: none"><li>IC in idle mode</li><li>Pre-regulator feature not used</li></ul>	PRQ-578

(table continues...)

**5 Power Management Unit (PMU)**

**Table 6 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
U18P sleep mode current	$I_{U18P\_sleep}$	–	3.4	8.9	$\mu\text{A}$	<b>1.</b> Typical value at $T_j = 25^{\circ}\text{C}$ <b>2.</b> $-40^{\circ}\text{C} < T_j < 85^{\circ}\text{C}$ ; <b>3.</b> Round robin in sleep mode deactivated	PRQ-179
U18P sleep mode current low voltage	$I_{U18P\_sleep\_low}$	–	3.5	6	$\mu\text{A}$	<b>1.</b> Typical value at $T_j = 25^{\circ}\text{C}$ <b>2.</b> $-40^{\circ}\text{C} < T_j < 85^{\circ}\text{C}$ ; <b>3.</b> $0\text{ V} < U_{U18P} < 65\text{ V}$ <b>4.</b> Round robin in sleep mode deactivated	PRQ-669
U18P sleep mode current - room temperature	$I_{U18P\_sleep\_RT}$	–	3.5	4.6	$\mu\text{A}$	$T_j = 25^{\circ}\text{C}$	PRQ-180
U18P idle current - Ext_reg active	$I_{U18P\_idle, Ext\_reg}$	–	$I_{U18P\_idle, typ} + I_{Ext\_reg} + (V_{EXT\_reg} / 40\text{k}\Omega)$	$I_{U18P\_idle, max} + I_{Ext\_reg} + (V_{EXT\_reg} / 28\text{k}\Omega)$	$\mu\text{A}$	<ul style="list-style-type: none"> <li>IC in idle mode</li> <li>Pre-regulator feature used</li> <li><math>I_{EXT\_reg} = 0\text{A}</math></li> </ul>	PRQ-181
VS sleep mode leakage current	$I_{VS\_sleep}$	-500	–	500	nA	$-40^{\circ}\text{C} < T_j < 85^{\circ}\text{C}$	PRQ-183
VS Idle current	$I_{VS\_idle}$	–	6.5	7.7	mA	IC in idle mode	PRQ-184
VIO current consumption during GPIO communication	$I_{VIO\_comm}$	–	–	5	mA	–	PRQ-186
VIO current consumption during sleep mode	$I_{VIO\_sleep}$	–	3.5	24	$\mu\text{A}$	<ul style="list-style-type: none"> <li>If VIO is not connected to VREGOUT</li> <li><math>V_{VIO} = 5.5\text{V}</math></li> </ul>	PRQ-686

**(table continues...)**

**5 Power Management Unit (PMU)**

**Table 6 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VS current consumption during PCVM and SCVM and BVM measurement	$I_{VS\_meas}$	–	31	32.7	mA	<ul style="list-style-type: none"> <li>PCVM of all 18 cells.</li> <li>SCVM</li> <li>BVM</li> <li>VIO connected to Vregout</li> <li>Incl. idle consumption <math>I_{VS\_idle}</math></li> </ul>	PRQ-188
VS current consumption during round robin scheme running	$I_{VS\_RR}$	–	–	12.7	mA	<ul style="list-style-type: none"> <li>Only during round robin</li> <li>VIO connected to Vregout</li> <li>Incl. idle consumption <math>I_{VS\_idle}</math></li> </ul>	PRQ-189
VS current consumption during communication	$I_{VS\_comm}$	–	$I_{VS\_idle\_typ} + 0.5\text{mA}$	$I_{VS\_idle\_max} + 0.5\text{mA}$	mA	<ul style="list-style-type: none"> <li>GPIO or iso UART communication</li> <li>Current to charge external interface components not included</li> </ul>	PRQ-190
VS current consumption during communication - external iso UART interface components	$I_{VS\_comm\_ext}$	–	–	$I_{VS\_comm} + 7.6$	mA	<ol style="list-style-type: none"> <li><math>C_{SER} = 1\text{ nF}</math></li> <li><math>BR_{iso\_U} = 3\text{ MHz}</math></li> <li><math>R_{SER} = 39\ \Omega</math>.</li> <li>Excluding <math>I_{VS\_comm}</math></li> <li>Valid for one iso UART interface in TX mode</li> </ol>	PRQ-192
U18P current consumption during low-power balancing mode	$I_{U18P\_LP\_Bal}$	–	0.4	1	mA	<ul style="list-style-type: none"> <li>Low-power balancing mode</li> <li>Only balancing active</li> </ul>	PRQ-576

**Protection and detection**

VREGOUT overcurrent threshold	$I_{VREGOUT\_th\_OC}$	58	75	112	mA	–	PRQ-193
VIO undervoltage threshold falling	$V_{VIO\_th\_UV\_fall}$	2.2	–	2.76	V	–	PRQ-194
VIO undervoltage threshold rising	$V_{VIO\_th\_UV\_rise}$	2.24	–	2.9	V	Needed for wake-up via UART or GPIO (EXT_WU)	PRQ-195

**(table continues...)**

## 5 Power Management Unit (PMU)

**Table 6** (continued) **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VIO undervoltage threshold hysteresis	$V_{VIO\_th\_UV\_hys}$	40	100	160	mV	–	PRQ-196
VDDC undervoltage threshold	$V_{VDDC\_th\_UV}$	2.1	–	2.375	V	–	PRQ-197
VDDC undervoltage threshold hysteresis	$V_{VDDC\_th\_UV\_hys}$	80	100	140	mV	–	PRQ-198
Power supply error detection deglitch time	$t_{PS\_ERR\_deg}$	8	15	24	$\mu\text{s}$	–	PRQ-199

### Preregulator

U18P min voltage	$V_{U18P\_ext\_min}$	15	–	$V_{U18P\_max}$	V	–	PRQ-662
Pre-regulator output voltage	$V_{EXT\_reg}$	9	–	85	V	–	PRQ-547
Pre-regulator control output current	$I_{EXT\_reg}$	–	–	500	$\mu\text{A}$	–	PRQ-548

## **6 Watchdog and wake-up function (WD)**

### **6.1 Functional description**

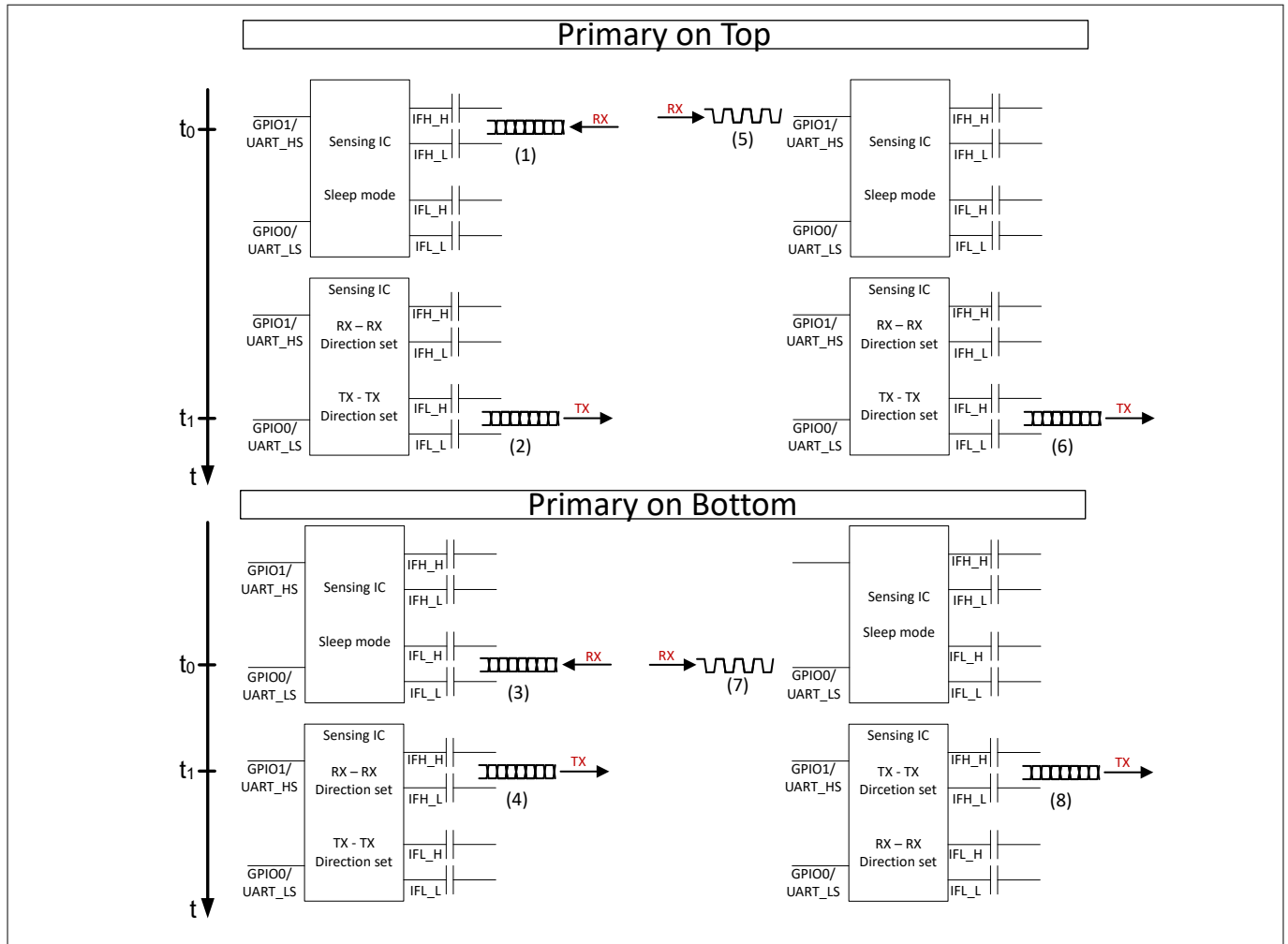
The following events trigger a wake-up:

- 1.** A wake-up pattern received via the iso UART or UART interfaces. The signal alternates with the frequency  $f_{\text{WAKEUP}}$ . After  $n_{\text{WAKE\_det}}$  signal periods received by the IC, it performs a wake-up. The IC completes the wake-up process within  $t_{\text{wake}}$ . After that the IC generates and forwards the wake-up signal for  $n_{\text{WAKEUP}}$  periods. A wake-up signal received via UART is forwarded on the iso UART interface, a wake-up signal received via iso UART is forwarded to the adjacent iso UART interface. In case of a wake-up via UART the voltage at the VIO pin has to be at least  $V_{\text{VIO\_th\_UV\_rise}}$ .
- 2.** A round robin sleep timeout.
- 3.** An EMM signal recognized as wake-up signal.
- 4.** A logic high level applied on the Ext\_WU pin, if the device is configured to use the external wake-up, which exceeds the external deglitch time  $t_{\text{Ext\_WU\_deg}}$ . In case of a wake-up via EXT\_WU the voltage at the VIO pin has to be at least  $V_{\text{VIO\_th\_UV\_rise}}$ .
- 5.** Connection to power for the first time.

The IC generates the wake-up pattern on:

- IFL, if the IC received a valid wake-up pattern on interface IFH.
  - (1) indicates the source of wake-up, (2) indicates the propagation on IFL\_x
- IFH, if the IC received a valid wake-up pattern on interface IFL.
  - (3) indicates the source of wake-up, (4) indicates the propagation on IFH\_x
- IFL, if the IC received a valid wake-up pattern on interface GPIO1/UART\_HS.
  - (5) indicates the source of wake-up, (6) indicates the propagation on IFL\_x
- IFH, if the IC received a valid wake-up pattern on interface GPIO0/UART\_LS.
  - (7) indicates the source of wake-up, (8) indicates the propagation on IFH\_x

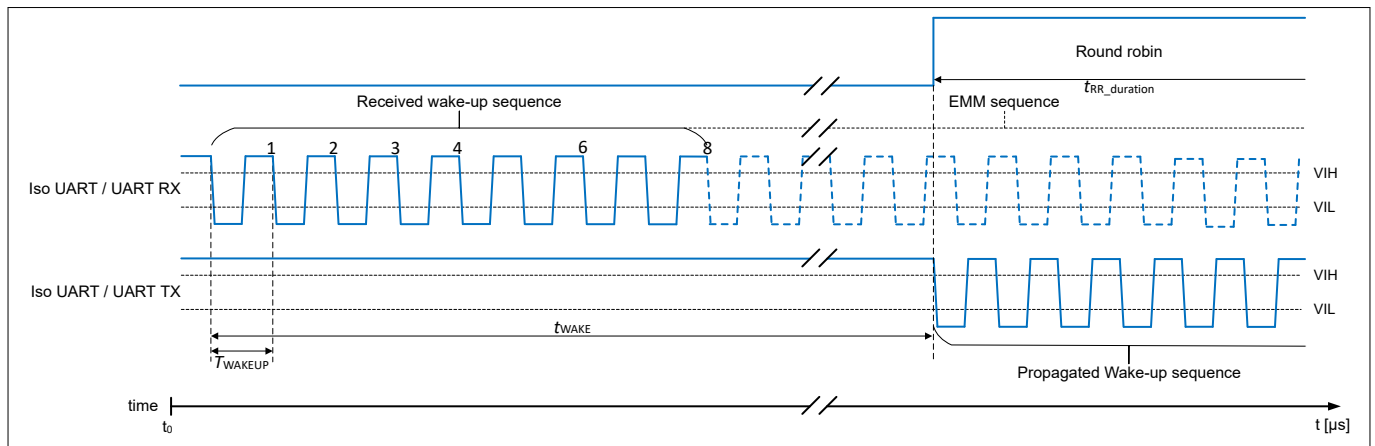
## 6 Watchdog and wake-up function (WD)



**Figure 5** Wake-up signal propagation

### Interface configuration:

The communication interface directions of the device are set automatically after wake-up. The iso UART interface on which the wake-up signal was received is configured as RX during idle mode (no communication) until the next wake-up. The adjacent iso UART communication interface is configured as TX until the next wake-up.



**Figure 6** Wake-up pattern

After waking-up the device using a standard wake-up signal the device's node ID is set to 0 by default. In case ID = 0 communication is not forwarded. In order to enable communication forwarding the node ID of each device

## 6 Watchdog and wake-up function (WD)

in the chain has to be set in consecutive order by setting the NODE\_ID bits in the IF\_CFG register before the watchdog has expired. The last device of the chain is indicated by setting the FN bit in the IF\_CFG register.

*Note: If an EMM signal is received, the device forwards it even though the device is not enumerated.*

### Watchdog:

The IC has a 7-bit watchdog counter which is counting downwards. The watchdog counter has to be served via an UART or iso UART command before the counter expires. Otherwise the device enters sleep mode. The counter can be set to maximum  $t_{WD\_max}$  with a step size of  $t_{WD\_LSB}$ , via the watchdog counter register.

*Note: After IC wake up, the watchdog counter is set to its maximum value.*

### Extended watchdog:

If a longer counter interval is needed the IC can be put into an extended mode by setting the operation mode register. In this mode the maximum time until the watchdog counter expires is defined by  $t_{WD\_EXT\_max}$  with a step size of  $t_{WD\_EXT\_LSB}$ . When the counter expires, the device enters sleep mode.

The device provides a free-running 9-bit main counter which is counting upwards and can be checked via the communication interface reading the main counter value of the watchdog register.

The maximum length is  $t_{Count\_max}$  with a step size of  $t_{Count\_LSB}$ . The precisely timed reading of the main counter gives an indication of the main oscillator frequency to the uC.

If bitfield RR\_CFG\_1.RR\_SYNC is set, then a WDOG\_CNT write command resets the main counter. This prepares for a broadcast read of all main counters.

## 6.2 Electrical characteristics watchdog and wake-up function (WD)

**Table 7**      **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Wake-up function							
WD wake-up signal frequency	$f_{\text{WAKEUP}}$	48	50	1040	kHz	–	PRQ-215
WD device wake-up time	$t_{\text{WAKE}}$	200	370	500	$\mu\text{s}$	<ul style="list-style-type: none"><li><math>f_{\text{WAKEUP\_min}}</math></li><li>From the first falling edge of the received pattern to the first edge of the propagated wake-up sequence.</li></ul>	PRQ-216
WD device wake-up time, Pre-regulator	$t_{\text{WAKE,PRE}}$	–	–	1.5	ms	<ul style="list-style-type: none"><li><math>f_{\text{WAKEUP\_min}}</math></li><li>From the first falling edge of the received pattern to the first edge of the propagated wake-up sequence.</li><li>Pre-regulator used</li></ul>	PRQ-667

(table continues...)

## 6 Watchdog and wake-up function (WD)

**Table 7 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
WD wake-up - number of detected periods	$n_{WAKE\_det}$	4	–	8	periods	–	PRQ-217
WD wake-up propagation - length in periods	$n_{WAKEUP}$	8	–	8	periods	–	PRQ-218
External wake-up deglitch time	$t_{Ext\_WU\_deg}$	5	–	55	$\mu\text{s}$	–	PRQ-570

### Watchdog counter

WD interval step	$t_{WD\_LSB}$	15.38	16	16.67	ms	EXT_WD = 0	PRQ-219
WD maximum interval	$t_{WD\_max}$	1.95	2.03	2.12	s	EXT_WD = 0	PRQ-220
WD interval step - extended	$t_{WD\_EXT\_LSB}$	13.5	15.07	17	min	EXT_WD = 1	PRQ-221
WD maximum interval - extended	$t_{WD\_EXT\_max}$	28.9	31.9	35.5	h	EXT_WD = 1	PRQ-222

### Main counter

WD main counter interval step	$t_{Count\_LSB}$	281	292.57	305	$\mu\text{s}$	–	PRQ-223
WD main counter maximum interval	$t_{Count\_max}$	144.03	149.8	156.03	ms	–	PRQ-224



## **7 Measurement control (MC)**

### **7.1 Functional description**

The various voltage measuring modules on the IC follow these rules:

- All voltage measurements (PCVM, SCVM, BVM, BAVM, AVM) can be manually triggered by a communication command.
- A manually triggered measurement sets a lock bit which inhibits a measurement triggered by a cyclical task. The device clears the lock bit after completion of the measurement.
- BVM, PCVM and SCVM can be triggered simultaneously.
- BAVM / AVM, PCVM and SCVM can be triggered simultaneously.

The IC provides two independent reference voltages which are used with the ADC blocks.

1. PCVM uses reference A.
2. BVM, AVM, and SCVM use reference B.

The resolution of the various voltage measurements is called  $V_{x\_LSB}$  and is defined by the LSB of the analog to digital conversion.

$x=PCVM; SCVM; AVM; BVM; BAVM$

**Voltage measurement time:** The measurement time  $t_{VM}$  of all voltage measurements is configurable using the MEAS\_CTRL or AVM\_CFG\_0 register.

PCVM/SCVM uses the cell voltage measurement mode bits, the AVM uses the auxiliary voltage measurement mode bits and the BVM and BAVM uses the block voltage measurement mode bits.

**Table 8 Voltage measurement modes**

<b>CVM_MODE/ BVM_MODE/A VM_MODE [2:0]</b>	<b>Resolution CVM / BVM /AVM [bit]</b>	<b>Resolution BAVM [bit]</b>	<b><math>t_{VM}</math> [ms]</b>
111	16	15	$t_{VM\_LR}$ (BVM / BAVM / CVM only)
110	16	15	4.68
101	15	14	2.34
100	14	13	1.17
011	13	12	0.59
010	12	11	0.29
001	11	10	0.15
000	10	9	0.07

*Note: The resolution of SCVM is fixed to 11 bit.  $t_{VM}$  of SCVM is adjusted by the CVM\_MODE configuration.*

A voltage measurement is initiated by setting the start bit of the desired measurement(s) in the measurement control register. The result of the measurement is the average of the cell voltage over the measurement time and is available in the RESULT register(s) of the triggered measurement.

The resolution of the measured value (in bit) can also be configured using the measurement control register. On completion of a measurement the device clears the corresponding start bit.

After a measurement is finished, the previous content of the result register is overwritten with the measured value.

The IC keeps the results of the manually triggered voltage measurements in its result registers even after an internal cyclic diagnostic check did occur.

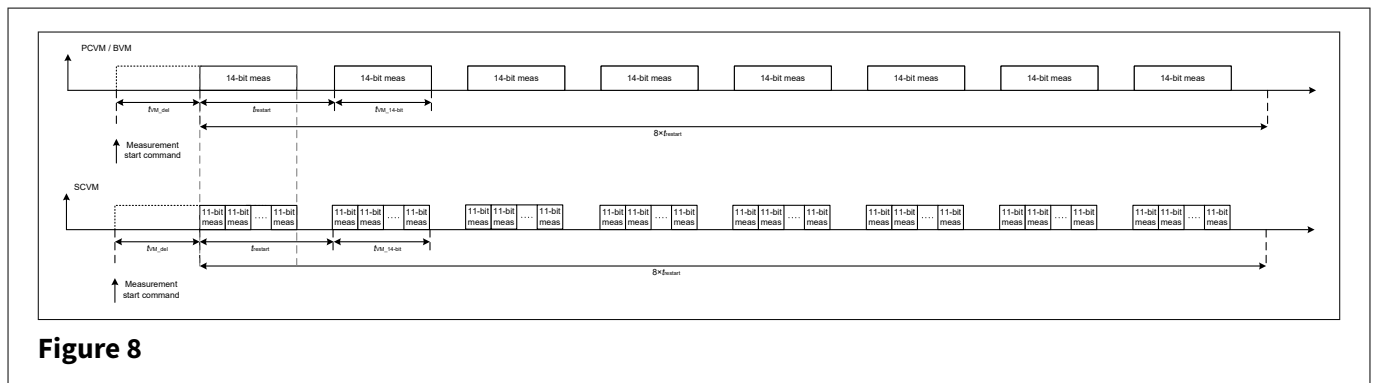
## 7 Measurement control (MC)

The IC provides a delay time  $t_{VM\_del}$  which delays the start of a voltage measurements (PCVM, SCVM, BVM and BAVM). The delay time is configurable with a resolution of  $t_{VM\_del\_LSB}$  up to the maximum delay time  $t_{VM\_del\_max}$  using the measurement control register. If Balancing is active but paused for voltage measurement, the delay time allows for stabilization of cell and block voltages, before starting the voltage measurement cycle.

If the long-running mode is selected for PCVM and/or BVM/BAVM by writing the corresponding bits in the measurement control register, the IC measures eight times in a row using the 14-bit measurement mode. If the long-running mode is selected for SCVM by writing the corresponding bits in the measurement control register, the IC performs eight times several 11-bit measurements while the measurement time  $t_{VM}$  of a 14-bit measurement. After the long running measurements are finished the PCVM result register contains the average of all 14-bit measurements while the SCVM result register contains the average value of all 11-bit measurements.

Each of those measurements starts automatically after the time  $t_{restart}$ , for a total measurement time  $t_{VM\_LR}$  equals  $t_{VM\_LR} = 8 * t_{restart}$ .

The time  $t_{restart}$  is defined by the configurable 6-bit field of the filter configuration register (FILTER\_CFG.LR\_TIME) with a resolution of  $t_{restart\_LSB}$  within the range of  $t_{restart\_range}$ .



**Figure 7 Voltage measurement long-running mode**

### Advanced Filter Mode:

The device features an advanced filter mode that can process manually triggered measurement results with a resolution of 14 bits or higher using an integrated IIR filter. This function is activated by setting the FILTER\_CFG.IIR\_UPD\_EN bit. Once enabled, each manually initiated measurement result is transferred to the measurement result registers (PCVM\_x.RESULT, BVM.RESULT, BAVM.RESULT), and the respective filter is updated with the measurement result. The output of the post-processing filter can be accessed through the filter output registers (PCVM\_IIR\_x.RESULT, BVM\_IIR.RESULT and BAVM\_IIR.RESULT).

Additionally, the device supports the use of an automated IIR mode measurements. When an automated IIR mode measurement starts, the device pre-loads the internal IIR filter memory with the first measurement result. After 32 samples, the result registers are updated with the filtered results (PCVM\_x.RESULT, BVM.RESULT, BAVM.RESULT, SCVM\_HIGH.RESULT, SCVM\_LOW.RESULT).

The post-processing filter output is available through the filter output registers (PCVM\_IIR\_x.RESULT, BVM\_IIR.RESULT, BAVM\_IIR.RESULT, SCVM\_HIGH\_IIR.RESULT, SCVM\_LOW\_IIR.RESULT).

*Note 1: In automated IIR mode, the SCVM provides an 11-bit result.*

## 7 Measurement control (MC)

### 7.2 Electrical characteristics measurement control (MC)

**Table 9**      **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
MC PCVM, BAVM, AVM and BVM ADC sampling frequency	$f_{s\_ADC}$	13.4	14	14.56	MHz	–	PRQ-233
MC PCVM, SCVM, BAVM and BVM propagation delay within IC	$t_{VM\_prop}$	$2.75\mu\text{s} - 1/BR_x$	–	$3.75\mu\text{s} - 1/BR_x$	$\mu\text{s}$	Time between completion of a received measurement start command and the actual start of the measurement delay time $t_{VM\_del}$ $x = \text{GPIO}; \text{isoU}$	PRQ-234
MC PCVM, SCVM, BAVM and BVM start delay timer resolution	$t_{VM\_del\_LSB}$	–	36.6	–	$\mu\text{s}$	–	PRQ-235
MC PCVM, SCVM, BAVM and BVM start delay timer maximum interval	$t_{VM\_del\_max}$	1.09	1.13	1.18	ms	–	PRQ-236
MC Voltage measurement time	$t_{VM}$	–	$2^m / f_{s\_ADC}$	–	s	<ol style="list-style-type: none"> <li>m bits: <math>10 \leq m \leq 16</math></li> <li>Mode: CVM_MODE; BVM_MODE; AVM_MODE</li> <li>Except for long-running mode</li> </ol>	PRQ-237

#### Long running mode

MC long-running mode restart time - 1	$t_{restart\_1}$	1.13	1.17	1.22	ms	For LR_TIME = 00 <sub>H</sub>	PRQ-673
MC long-running mode restart time - 2	$t_{restart\_2}$	1.20	1.25	1.3	ms	For LR_TIME = 01 <sub>H</sub>	PRQ-674
MC long-running mode restart step	$t_{restart\_LSB}$	100.1	104.1	108.5	$\mu\text{s}$	For LR_TIME > 01 <sub>H</sub>	PRQ-238
MC long-running restart range	$t_{restart\_range}$	1.13	–	8.03	ms	–	PRQ-239

**(table continues...)**

## 7 Measurement control (MC)

**Table 9 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Full scale ranges							
MC PCVM, SCVM and comparator full-scale range	$FSR_{PCVM}$ $FSR_{SCVM}$ $FSR_{Comp}$	0	–	5	V	–	PRQ-240
MC BVM full-scale range	$FSR_{BVM}$	0	–	90	V	$V_{BVM} = V_{U18P} - V_{GND}$	PRQ-241
MC BAVM full-scale range	$FSR_{BAVM}$	-2	–	2	V	$V_{BAVM} = V_{TMP7} - V_{TMP6}$	PRQ-242
MC AVM and TMP full-scale range	$FSR_{AVM}$ $FSR_{TMP}$	0	–	2	V	–	PRQ-243
Measurement resolution							
MC PCVM resolution	$V_{PCVM\_LSB}$	–	$FSR_{PCVM} / 2^m$	–	V	m bits: $10 \leq m \leq 16$	PRQ-244
MC SCVM resolution	$V_{SCVM\_LSB}$	–	$FSR_{SCVM} / 2^{11}$	–	V	–	PRQ-245
MC BVM resolution	$V_{BVM\_LSB}$	–	$FSR_{BVM} / 2^m$	–	V	m bits: $10 \leq m \leq 16$	PRQ-246
MC BAVM resolution	$V_{BAVM\_LSB}$	–	$FSR_{BAVM} / 2^m$	–	V	m bits: $9 \leq m \leq 15$	PRQ-247
MC AVM resolution	$V_{AVM\_LSB}$	–	$FSR_{AVM} / 2^m$	–	V	m bits: $10 \leq m \leq 16$	PRQ-248

## 8 Primary cell voltage measurement (PCVM)

## 8 Primary cell voltage measurement (PCVM)

### 8.1 Functional description

The primary cell voltage measurement (PCVM) unit of the IC measures every cell voltage individually and simultaneously using the  $U_n$  pins.

The measured voltage is defined as  $V_{PCVM} = (V_{U_{n+1}} - V_{U_n})$  ( $0 \leq n \leq 17$ ) and is measured with the defined accuracy  $PCVM_{ERR}$  and a relative accuracy of  $PCVM_{ERR\_rel}$ .

A manual measurement is triggered by setting the PCVM\_START bitfield in the MEAS\_CTRL register. The primary cell voltage is calculated using:  $V_{PCVM} [V] = (FSR_{PCVM} / 2^{16}) \times RESULT[LSB16]$

The measurement is triggered by a host controller command synchronously for all cells connected to the IC. These conditions apply:

- The maximum start measurement propagation delay is  $t_{VM\_prop}$ .
- The maximum PCVM time deviation across all ICs in a chain is  $Dev_{PCVM\_chain}$ .
- The start of the measurement is delayed by the configurable time  $t_{VM\_del}$ .
- The maximum iso UART propagation delay is  $t_{isoU\_prop\_del}$ .

The number of activated cells can be configured via the EN\_CELL\_x bits in the PART\_CFG\_x registers. The highest 16 channels can be activated in the PART\_CFG\_0 register, while the lower two cells are activated by using the PART\_CFG\_1 register.

After the completion of a PCVM, the IC will also provide the sum of all measured PCVM voltages in the PCVM\_SUM register. The sum is calculated with the following formula:

$$PCVM\_SUM = \frac{\sum_{i=1}^n PCVM_i \cdot RESULT}{2^5}$$

#### Equation 1

Where n is the number of cells activated by EN\_CELL\_x = 1. Cells not activated (EN\_CELL\_x = 0) are not included in the calculation.

In order to calculate  $V_{PCVM\_SUM}$ , the full scale range of each measurement and the division by  $2^5$  to fit in the 16-bit register has to be considered:

$$V_{PCVM\_SUM} = \frac{FSR_{PCVM}}{2^{16}} \times PCVM\_SUM \times 2^5$$

#### Equation 2

## 8 Primary cell voltage measurement (PCVM)

### 8.2 Electrical characteristics primary cell voltage measurement (PCVM)

**Table 10** Electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cell sense inputs							
PCVM differential input current Un	$I_{Un\_PCVM}$	20	–	25	μA	<div><div>1.</div>During PCVM</div> <div><div>2.</div><math>V_{PCVM} = 5\text{ V}</math></div> <div><div>3.</div>This differential current flows into Un+1 and has the opposite direction on Un for the channels (<math>0 \leq n \leq 18</math>)</div> <div><div>4.</div>The typical average value <math>I_{Un\_PCVM} = V_{PCVM} / 200\text{ k}\Omega</math></div> <div>PRQ-252</div>	
Synchronization timing							
Maximum PCVM time deviation across ICs	$Dev_{PCVM\_chain}$	-4	–	4	%	–	PRQ-255
Primary cell voltage measurement							
PCVM relative accuracy	$PCVM_{ERR\_rel}$	-1	–	1	mV	<div><div>1.</div>16-bit mode</div> <div><div>2.</div><math>\Delta(V_{Un+1} - V_{Un}) = 100\text{ mV}</math></div> <div><div>3.</div><math>2.5\text{ V} \leq (V_{Un+1} - V_{Un}) \leq 4.3\text{ V}</math></div> <div><div>4.</div><math>\Delta T_j = 10\text{ K}</math> within <math>-40^{\circ}\text{C} \leq T_j \leq 85^{\circ}\text{C}</math></div> <div><div>5.</div>Over a period of <math>t_0</math> and <math>t_{0+x}</math> (<math>x \leq 12\text{ hours}</math>)</div> <div>PRQ-257</div>	
PCVM accuracy EoL - 1	$PCVM_{ERR\_EOL\_1}$	-1.1	–	1.1	mV	<div><div>1)</div></div> <div><div>1.</div>16-bit mode</div> <div><div>2.</div><math>2.5\text{ V} &lt; (V_{Un+1} - V_{Un}) \leq 3.6\text{ V}</math></div> <div><div>3.</div><math>T_j = 25^{\circ}\text{C}</math></div> <div>PRQ-258</div>	

(table continues...)

**8 Primary cell voltage measurement (PCVM)**

**Table 10 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PCVM accuracy EoL - 2	$PCVM_{ERR\_EO\ L\_2}$	-1.3	–	1.3	mV	1) 1) <b>1.</b> 16-bit mode <b>2.</b> $3.6\text{ V} < (V_{Un+1} - V_{Un}) \leq 4.3\text{ V}$ <b>3.</b> $T_j = 25^\circ\text{C}$	PRQ-259
PCVM accuracy EoL - 3	$PCVM_{ERR\_EO\ L\_3}$	-1.9	–	1.9	mV	1) 1) <b>1.</b> 16-bit mode <b>2.</b> $1\text{ V} \leq (V_{Un+1} - V_{Un}) \leq 3.6\text{ V}$ <b>3.</b> $-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$	PRQ-260
PCVM accuracy EoL - 4	$PCVM_{ERR\_EO\ L\_4}$	-2.8	–	2.8	mV	1) 1) <b>1.</b> 16-bit mode <b>2.</b> $3.6\text{ V} < (V_{Un+1} - V_{Un}) \leq 4.3\text{ V}$ <b>3.</b> $-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$	PRQ-261
PCVM accuracy EoL - 5	$PCVM_{ERR\_EO\ L\_5}$	-2.4	–	2.4	mV	1) 1) <b>1.</b> 16-bit mode <b>2.</b> $1\text{ V} \leq (V_{Un+1} - V_{Un}) \leq 3.6\text{ V}$ <b>3.</b> $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$	PRQ-262
PCVM accuracy EoL - 6	$PCVM_{ERR\_EO\ L\_6}$	-3.4	–	3.4	mV	1) 1) <b>1.</b> 16-bit mode <b>2.</b> $3.6\text{ V} < (V_{Un+1} - V_{Un}) \leq 4.3\text{ V}$ <b>3.</b> $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$	PRQ-263
PCVM accuracy EoL - 7	$PCVM_{ERR\_EO\ L\_7}$	-3	–	3	mV	1) 1) <b>1.</b> 16-bit mode <b>2.</b> $0.05\text{ V} \leq (V_{Un+1} - V_{Un}) \leq 1\text{ V}$ <b>3.</b> $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$	PRQ-264
PCVM accuracy EoL - 8	$PCVM_{ERR\_EO\ L\_8}$	-3.9	–	3.9	mV	1) 1) <b>1.</b> 16-bit mode <b>2.</b> $4.3\text{ V} < (V_{Un+1} - V_{Un}) \leq 4.8\text{ V}$ <b>3.</b> $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$	PRQ-265

**(table continues...)**

## 8 Primary cell voltage measurement (PCVM)

**Table 10** (continued) **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PCVM accuracy EoL - 9	$PCVM_{ERR\_EO\ L\_9}$	-1.9	–	1.9	mV	<sup>1)</sup> <sup>1)</sup> <b>1.</b> 16-bit mode <b>2.</b> $1\text{ V} < (V_{Un+1} - V_{Un}) \leq 3.6\text{ V}$ <b>3.</b> $-40^{\circ}\text{C} \leq T_j \leq 50^{\circ}\text{C}$	PRQ-266
PCVM accuracy EoL - 10	$PCVM_{ERR\_EO\ L\_10}$	-2.3	–	2.3	mV	<sup>1)</sup> <sup>1)</sup> <b>1.</b> 16-bit mode <b>2.</b> $3.6\text{ V} < (V_{Un+1} - V_{Un}) \leq 4.3\text{ V}$ <b>3.</b> $-40^{\circ}\text{C} \leq T_j \leq 50^{\circ}\text{C}$	PRQ-267
PCVM accuracy EoL - 10-bit	$PCVM_{ERR\_EO\ L\_10bit}$	-15	–	15	mV	<sup>1)</sup> <b>1.</b> 10-bit mode <b>2.</b> $0.05\text{ V} \leq (V_{Un+1} - V_{Un}) \leq 4.8\text{ V}$ <b>3.</b> $-40^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}$	PRQ-268

<sup>1)</sup> End-of-Life (EoL) accuracy; according to AEC-Q100 Grade 1 Rev. H automotive qualification. In case of lower resolution settings additional quantization error e.g.  $PCVM_{ERR\_EOL} \pm 2\text{ LSB}[m]$ ; m bits:  $14 \leq m \leq 15$  need to be considered.



## **9 Secondary cell voltage measurement (SCVM)**

### **9.1 Functional description**

The device includes a secondary cell voltage measurement (SCVM) unit.

The measured voltage  $V_{SCVM} = (V_{Bn} - V_{Un-1})$  ( $1 \leq n \leq 18$ ) is measured with the accuracy  $SCVM_{ERR\_EOL}$  and a resolution of  $V_{SCVM\_LSB}$ .

The secondary cell voltage measurement is initiated by setting the SCVM\_START bitfield in the MEAS\_CTRL register. The secondary cell voltage is calculated using:  $V_{SCVM} [V] = (FSR_{SCVM} / 2^{11}) \times RESULT[LSB11]$

*Note: If triggered together with a PCVM the device is averaging the SCVM results over the whole conversion time*

The SCVM unit can measure the voltage of at least one cell simultaneously with the primary cell voltage measurement within  $t_{VM\_prop}$ . At least one cell has to be enabled in the SCVM configuration register SCVM\_CFG\_0 / SCVM\_CFG\_1. The corresponding cells for SCVM must also be activated in the PART\_CFG\_0 / PART\_CFG\_1 register. If only one cell is enabled, the IC will compare the PCVM and SCVM values. The difference voltage between PCVM and SCVM is available in the PCVM\_SCVM\_DIFF register. If the difference between SCVM and PCVM is greater than the threshold configured in PCVM\_SCVM\_CFG.THRESHOLD, the PCVM\_SCVM\_ERR bit of the GEN\_DIAG register is set.

*Note: A binary search algorithm follows the highest and the lowest cell voltage of all cells enabled in the SCVM\_CFG\_0 / SCVM\_CFG\_1 register for each sample. Within the sampling time  $1/f_{s\_SCVM\_ADC}$  both voltages are sampled once. The SCVM averages all samples of the lowest and all samples of the highest voltage over the entire measurement time.*

#### **Measurement result:**

After the measurement time, the SCVM needs additional time  $t_{SCVM\_ave}$  to calculate the average results.

After  $t_{SCVM\_ave}$ , the value of the highest (lowest) SCVM result is stored in SCVM\_HIGH (SCVM\_LOW) register .

*Note: If only one single cell is measured, calculation of the SCVM\_HIGH and SCVM\_LOW registers average improves filtering.*

A 2 bit upwards counter in each SCVM register, SCVM lowest cellvoltage and SCVM highest cellvoltage, indicates the availability of a new secondary cell voltage measurement.

## 9 Secondary cell voltage measurement (SCVM)

### 9.2 Electrical characteristics secondary cell voltage measurement (SCVM)

**Table 11** Electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cell sensing inputs							
SCVM differential input current Bn	$I_{Bn\_SCVM}$	0	4	5	$\mu\text{A}$	<div><div>1.</div>Averaged during SCVM</div> <div><div>2.</div><math>V_{SCVM} = 5\text{ V}</math></div> <div><div>3.</div>This current is differential, which means that it flows into B<sub>n</sub> and has the opposite direction on U<sub>n-1</sub> for channels 1 ≤ n ≤ 18</div>	PRQ-273
Synchronization timing							
SCVM to PCVM time deviation	$Dev_{SCVM\_PCVM}$	-0.5	–	+0.5	%	<div><div>•</div>Within one IC</div> <div><div>•</div>Maximum deviation between SCVM (11-bit) time and PCVM (11-bit) time.</div>	PRQ-275
SCVM data averaging time	$t_{SCVM\_ave}$	286	298	311	$\mu\text{s}$	–	PRQ-276
Secondary cell voltage measurement							
SCVM ADC sampling frequency	$f_{s\_SCVM\_ADC}$	–	$f_{s\_ADC} / 64$	–	MHz	–	PRQ-277
SCVM accuracy EoL - 1	$SCVM_{ERR\_EoL\_1}$	-16	–	16	mV	<div><div>1.</div><math>2.7\text{ V} \leq (V_{Bn} - V_{Un-1}) \leq 4.3\text{ V}</math></div> <div><div>2.</div><math>-40^{\circ}\text{C} \leq T_j \leq 50^{\circ}\text{C}</math></div>	PRQ-278
SCVM accuracy EoL - 2	$SCVM_{ERR\_EoL\_2}$	-16	–	16	mV	$1\text{ V} \leq (V_{Bn} - V_{Un-1}) < 4.8\text{ V}$	PRQ-279
Max deviation between SCVM and PCVM	$\Delta_{SCVM\_vs\_PCVM}$	-15	–	15	mV	<div><div>•</div>PCVM: 14-bit to 16bit mode</div> <div><div>•</div><math>1.0\text{ V} \leq U_{n+1} - U_n \leq 4.8\text{ V}</math></div>	PRQ-280

(table continues...)

**9 Secondary cell voltage measurement (SCVM)**

**Table 11 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Analog undervoltage and overvoltage comparators							
Cell OV/UV comparator resolution	$FSRV_{Comp\_LSB}$	–	$FSR_{Co_{mp}} / 2^{10}$	–	V	–	PRQ-281
Comparator accuracy - limited range	$COMP_{ERR\_1}$	-30	–	30	mV	<b>1.</b> $(V_{Bn} - V_{Un-1}) = 3.6\text{ V}$ <b>2.</b> $-40^{\circ}\text{C} \leq T_j \leq 25^{\circ}\text{C}$ <b>3.</b> $\pm 3$ sigma distribution within absolute minimum and maximum limits	PRQ-282
Cell OV/UV comparator accuracy	$Comp_{ERR}$	-30	–	30	mV	<b>1.</b> $1.0\text{ V} \leq (V_{Bn} - V_{Un-1}) \leq 4.8\text{ V}$ <b>2.</b> $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$	PRQ-283
Cell OV/UV comparator sampling frequency	$f_{CMP\_OVUV}$	1	–	–	MHz	–	PRQ-284
Cell OV/UV comparator checking time	$t_{CMP\_OVUV}$	–	$2^{10} / f_{s\_ADC}$	–	$\mu\text{s}$	–	PRQ-285

## 10 Block voltage measurement (BVM)

# 10 Block voltage measurement (BVM)

## 10.1 Functional description

The IC can measure the sum total voltage of all the cells connected to the device using the U18P and GND pin, called block voltage. The block voltage  $V_{BVM} = (V_{U18P} - V_{GND})$  is measured with the accuracy  $BVM_{ERR\_EOL}$  and a configurable resolution of  $V_{BVM\_LSB}$ .

The block voltage measurement is initiated by setting the BVM\_START bitfield in the MEAS\_CTRL register. The block voltage is calculated:  $V_{BVM} [V] = (FSR_{BVM} / 2^{16}) \times RESULT\_BVM [LSB16]$

The block voltage measurement (BVM) unit can measure the voltage of the battery pack simultaneously with the primary cell voltage measurement within  $t_{VM\_prop}$ . The BVM has to be enabled in the MEAS\_CTRL configuration register.

The IC will compare the sum of all configured PCVM to the BVM value, the difference voltage between the sum of PCVM and BVM is available in the PCVM\_BVM\_DIFF register. If the difference between BVM and the sum of PCVM is greater than the threshold configured in PCVM\_BVM\_CFG.THRESHOLD, the PCVM\_BVM\_ERR bit of the GEN\_DIAG register is set.

## 10.2 Electrical characteristics block voltage measurement (BVM)

**Table 12** Electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}C$  to  $+150^{\circ}C$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cell sense inputs							
BVM input current U18P	$I_{U18P\_BVM}$	–	–	400	μA	Within the functional range	PRQ-287
Block voltage measurement							
Maximum BVM to PCVM time deviation within IC	$Dev_{BVM\_PCVM\_IC}$	-0.5	–	+0.5	%	Deviation between BVM $t_{VM}$ and PCVM $t_{VM}$ with the same resolution setting within one IC	PRQ-288
Maximum BVM time deviation across ICs	$Dev_{BVM\_Chain}$	-4	–	4	%	Deviation between BVM $t_{VM}$ over all ICs with the same resolution setting.	PRQ-289
BVM accuracy EoL -1	$BVM_{ERR\_EOL\_1}$	-90	–	90	mV	<ul style="list-style-type: none"><li>14-bit to 16-bit mode</li><li><math>6\text{ V} \leq V_{BVM} \leq 78\text{ V}</math></li><li><math>-40^{\circ}\text{C} \leq T_j \leq 50^{\circ}\text{C}</math></li></ul>	PRQ-291
BVM accuracy EoL -2	$BVM_{ERR\_EOL\_2}$	-95	–	95	mV	<ul style="list-style-type: none"><li>14-bit to 16-bit mode</li><li><math>6\text{ V} \leq V_{BVM} \leq 90\text{V}</math></li><li><math>-40^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}</math></li></ul>	PRQ-290
BVM accuracy EoL - 10-bit	$BVM_{ERR\_10Bit}$	-250	–	250	mV	<ul style="list-style-type: none"><li>10-bit mode</li><li><math>6\text{ V} \leq V_{BVM} \leq 90\text{V}</math></li><li><math>-40^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}</math></li></ul>	PRQ-292

(table continues...)

**10 Block voltage measurement (BVM)**

**Table 12 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Relative ADC error margin - sum of PCVM versus BVM EoL	$ERR_{PCVM\_BVM\_10bit}$	-110	–	110	mV	<b>1.</b> 10-bit mode <b>2.</b> $1\text{ V} \leq (V_{Un+1} - V_{Un}) \leq 4.8\text{ V}$ <b>3.</b> $-40^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}$ <b>4.</b> Plausibility check as part of the round robin scheme	PRQ-294

## 11 Auxiliary voltage measurement (AVM)

# 11 Auxiliary voltage measurement (AVM)

## 11.1 Functional description

Apart of the cell voltage measurement the IC also provides the possibility to measure other voltages, called auxiliary voltage measurement. The auxiliary voltage  $V_{AVMz} = (V_{TMPz} - V_{TMP\_REF})$ , ( $0 \leq z \leq 7$ ) is measured with the accuracy  $AVM_{ERR\_EOL}$  and a resolution of  $V_{AVM\_LSB}$ .

The auxiliary voltage measurement is initiated by setting the AVM\_START bitfield in the MEAS\_CTRL register. The auxiliary voltage is calculated using:  $V_{AVMz} [V] = (FSR_{AVM} / 2^{16}) \times RESULT [LSB16]$

### Bipolar auxiliary voltage measurement:

Additional to the unipolar AVM the device can be configured to measure a bipolar voltage applied on the TMP6 and TMP7 pins instead. The voltage  $V_{BAVM} = (V_{TMP7} - V_{TMP6})$  is measured with the accuracy  $BAVM_{ERR\_EOL}$  and a configurable resolution of  $V_{BAVM\_LSB}$ .

The BAVM measurement is enabled by setting the AVM\_CFG\_0.AUX\_BIPOLAR bitfield, the resolution is set by the MEAS\_CTRL.BVM\_MODE and the measurement is triggered by the MEAS\_CTRL.BVM\_START bit. The BAVM measurement result is stored in the BAVM result register.

The bipolar voltage is calculated using:  $V_{BAVM} = (BAVM.RESULT[\text{signed LSB15}] \times 2 V) / 2^{15}[LSB15]$

*Note: Either BVM or BAVM can be performed synchronized to the PCVM/SCVM.*

All external temperature measurement channels can be selected to be manually measured by the AVM function. To measure an auxiliary voltage using a TMP channel, the temperature measurement function have to be deactivated using the temperature measurement configuration register. Since only one auxiliary voltage can be measured at a time, all configured auxiliary channels are measured sequentially after the AVM START bit is set.

## 11.2 Electrical characteristics auxiliary voltage measurement (AVM)

**Table 13** Electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
AVM accuracy EoL	$AVM_{ERR\_EOL}$	-2	–	2	mV	<b>1.</b> 14-bit to 16-bit mode <b>2.</b> $0.05 V \leq V_{AVMz} \leq 1.95 V$ <b>3.</b> $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$	PRQ-564
BAVM accuracy EoL	$BAVM_{ERR\_EOL}$	-40	–	40	mV	<b>1.</b> 13-bit to 15-bit mode <b>2.</b> $-2 V \leq V_{TMP6/7} \leq 2 V$	PRQ-299
BAVM accuracy EoL - long-running mode	$BAVM_{ERR\_EOL\_LR}$	-40	–	40	mV	<b>1.</b> Long-running mode <b>2.</b> $-2 V \leq V_{TMP6/7} \leq 2 V$	PRQ-300

## **12 Temperature measurement unit (TMP)**

### **12.1 Functional description**

The temperature measurement unit provides the possibility to measure up to eight external NTC thermistors as well as two internal temperature sensors and provides the results in the corresponding temperature registers.

A valid bit, which is cleared after readout, indicates a new measurement result.

The NTCs are measured with an accuracy of  $TMP_{ERR}$  whilst the internal sensor accuracy is defined by  $T_{ERR\_int\_abs}$ .

#### **TMP channel selection:**

If not all provided external NTC thermistors measurement channels are needed they have to be deactivated by setting the temperature configuration register.

*Note: The TMP channels have to be connected in consecutive order starting with TMP0. Deactivated channels can be used as AVM / BAVM inputs.*

The internal temperature measurement as well as the measurement of the selected NTC channels are triggered by the round robin. Within three round robin cycles all NTCs are updated.

*Note: First round robin after wake-up is not measuring a NTC channels*

#### **Current level selection:**

The device provides three current sources, with eight individual current levels,  $ITMPz\_i$  ( $0 \leq z \leq 7, 0 \leq i \leq 7$ ) to measure external NTCs. The current level for each channel is configured in the bitfield  $EXT\_TEMP\_CTRL\_y.INTC\_z$  ( $0 \leq y \leq 1$ ). The bit  $EXT\_TEMP\_CTRL\_y.SEL\_INTC\_z$ , is used to apply the individual current level settings of the  $EXT\_TEMP\_CTRL\_y$  register.

If the  $EXT\_TEMP\_CTRL\_y.SEL\_INTC\_z$  bit is not set for an active NTC channel, or during a round robin sleep cycle, the device automatically determines the most suitable current level using an auto-ranging function. This function is selecting the current level for every NTC channel individually by applying a reference voltage. The current sources must be active at least for the settling time  $t_{settle}$  before the RR sequence begins by setting the  $MISC\_CTRL.INTC\_ON$  bit. To calculate the settling time please refer to the user manual of the device. The sequence of measured channels is predefined by the round robin (RR) configuration and cannot be manually altered.

The device checks if the measurement result is in a valid range with the  $TH_{src\_underflow}$  and  $TH_{src\_overflow}$  thresholds. If the measurement result is outside of this range, the  $RANGE\_ERR$  bit in  $EXT\_TEMP\_DIAG\_y$  is set after the error counter reaches its maximum value.

*Note: A valid result is available (or NTC short/open is detected) once the measurement is settled. Note: If the RR is periodically run by the round robin timer, the current source is automatically activated  $t_{settle}$  prior to the measurement. Note: If the RR is triggered by the host controller with the  $RR\_SYNC$  option, the selection of the correct current source and the activation of the current sources has to be done prior to running the round robin.*

#### **Measurement result:**

For every TMP channel, a result register  $EXT\_TEMP\_z$  is available. The results register contains the following information:

- The result of the measurement.
- The used current level (defined either by autoranging or by selection).
- The valid bit is set to indicate a new measurement. Reading the result clears the valid bit.
- Whether the pull-down of this channel was activated.

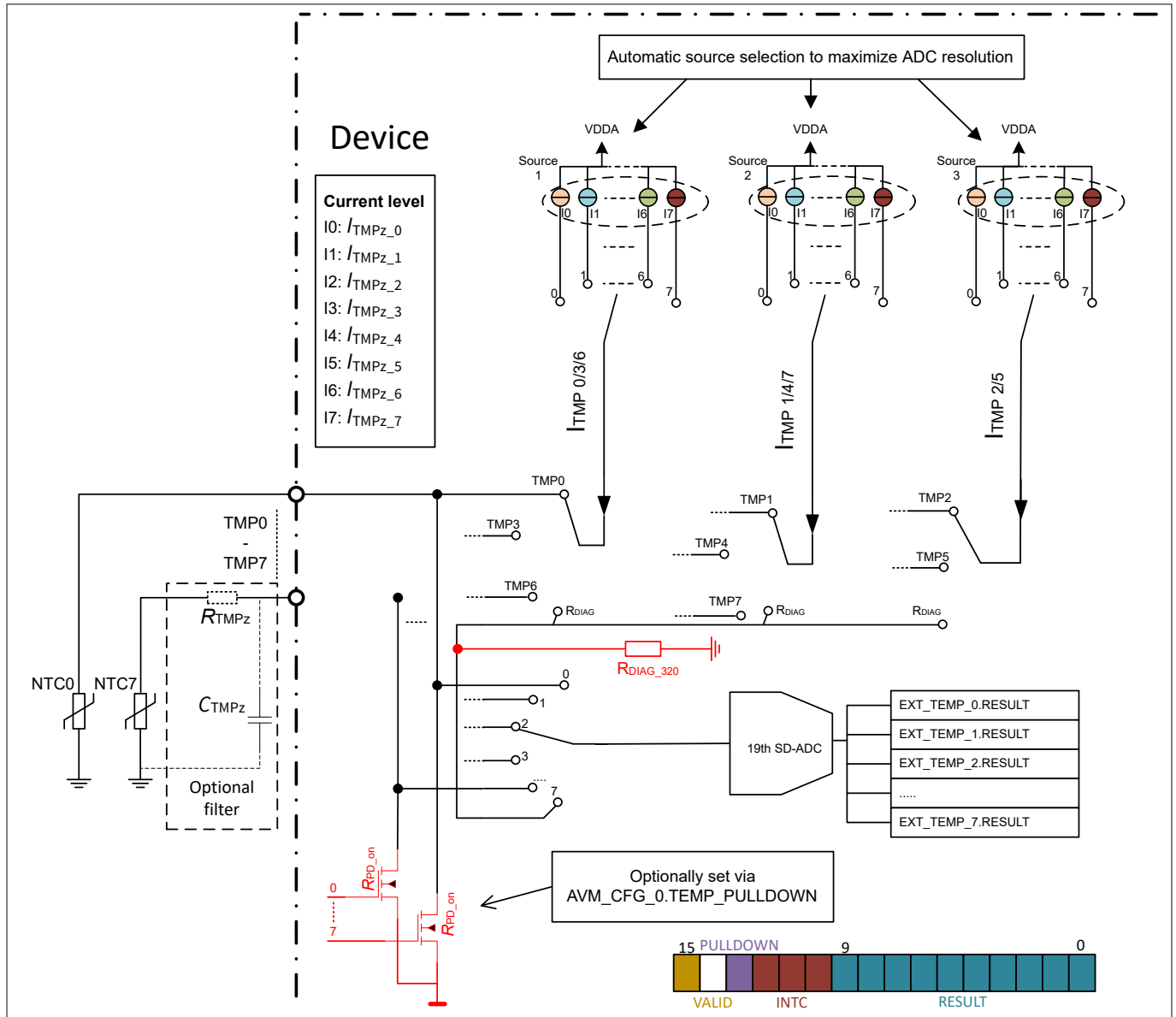
Whether a pull-down error occurred can be checked in the  $TMP\_REF\_DIAG$  register.

The NTC resistor value is calculated by using the voltage measurement result and the used current level.

## 12 Temperature measurement unit (TMP)

$R_{NTC} [\Omega] = (EXT\_TEMP\_z.RESULT [LSB10] \times FSR_{TMP} [V] \times 2^{7-EXT\_TEMP\_z.INTC}) / (2^{10} \times 640 \mu A) - R_{TMP}$ ; INTC = 0 to 7 (used current level);

z = 0 to 7 (selected temperature channel).



**Figure 9 External temperature measurement**

### TMP unit diagnostics:

To check if the temperature measurement unit works correctly the IC performs two internal diagnostics checks as part of the round robin:

1. It measures an internal diagnostics resistor  $R_{DiAG\_x}$  with the current source and level  $I_{TMPz\_x}$  ( $0 \leq x \leq 7$ ,  $0 \leq z \leq 7$ ) used for TMPz.
2. It activates the pull down switch of the selected TMP channel after the measurement and measures the channel again. The measured value is then compared with the expected value  $R_{PD\_ON}$ . An open wire or increased resistance value can be detected and is indicated by setting the GEN\_DIAG.EXT\_T\_ERR (external temperature error).

*Note: Only the TMP channel which was measured first within in the RR cycle is checked. The pull down resistor can be activated by setting the corresponding bits in the auxiliary voltage measurement configuration register*

### NTC overtemperature detection:



## 12 Temperature measurement unit (TMP)

The device checks whether an overtemperature condition at the NTC exists by comparing the voltage measurement result against the external overtemperature threshold in combination with a current level. There are two different thresholds available which can be configured using the EXT\_TEMP\_CFG\_0 and EXT\_TEMP\_CFG\_1 register. The overtemperature threshold is configurable with a resolution of  $V_{\text{TMP\_LSB}}$ , the current level can be configured with the INTC\_THR\_0 / INTC\_THR\_1 bits. The THR\_EXT\_TEMP\_i (i = 0 to 7) bits in the EXT\_TEMP\_CFG\_2 register define which threshold is active for which TMP channel.

### Internal overtemperature detection:

The device has two internal temperature sensors. It checks if an overtemperature condition on the active internal temperature sensor is present. The measurement result is compared against the internal overtemperature threshold INT\_OT\_THR.

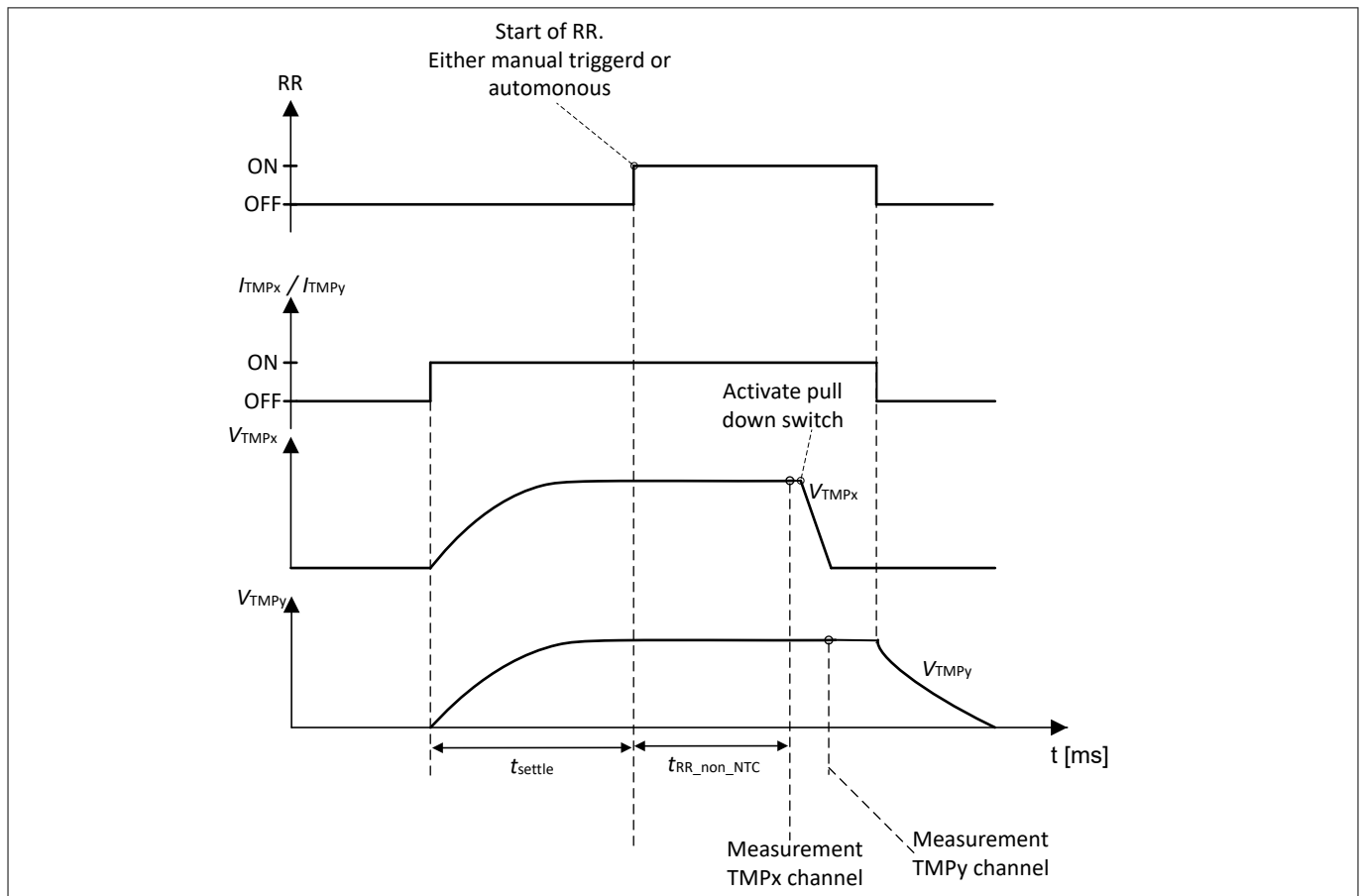
The internal overtemperature threshold is configurable with a resolution of  $T_{\text{int\_LSB}}$  using the internal overtemperature threshold bits of the internal temperature measurement configuration register INT\_TEMP\_CFG.INT\_OT\_THR (recommended value:  $T_j = 150^\circ\text{C}$ ).

If the overtemperature threshold is reached, the device disables the balancing function and sets the internal overtemperature error flag. The junction temperature  $T_j$  can be calculated using the formula:

$$\text{Temperature } [^\circ\text{C}] = -T_{\text{int\_LSB}} \times \text{INT\_TEMP\_0.RESULT} + 541;$$

Additionally, the device checks the integrity of the temperature sensors by comparing the results internally. If the difference between the measurements exceeds the threshold INT\_TEMP\_DELTA\_THR, the device stops balancing and sets the internal temperature delta error flag.

The current source and level which is selected to be used is activated prior to every NTC channel measurement. The time is defined as  $t_{\text{settle}}$  and is configurable with a step size of  $t_{\text{settle\_LSB}}$  until the maximum time  $t_{\text{settle\_max}}$  is reached using the temperature measurement register.



**Figure 10** Definition of  $t_{\text{settle}}$

**12 Temperature measurement unit (TMP)**

**12.2 Electrical characteristics temperature measurement (TMP)**

**Table 14**      **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Internal temperature sensor							
TMP internal temperature resolution	$T_{\text{int\_LSB}}$	–	0.1597	–	K	–	PRQ-309
TMP internal temperature accuracy EoL abs.	$T_{\text{ERR\_int\_abs}}$	-10	–	10	°C	–	PRQ-310
External temperature sensors							
TMP measurement resolution	$V_{\text{TMP\_LSB}}$	–	$\text{FSR}_{\text{TM}}/2^{10}$	–	V	–	PRQ-311
TMP measurement accuracy - 1	$TMP_{\text{ERR\_1}}$	-1.5	–	1.5	%	Accuracy of measured NTC resistance value in the range of 1.22 kΩ to 390 kΩ	PRQ-312
TMP measurement accuracy - 2	$TMP_{\text{ERR\_2}}$	-1.7	–	1.7	%	Accuracy of measured NTC resistance value in the range of 610 Ω to 1.22 kΩ	PRQ-313
TMP measurement accuracy - 3	$TMP_{\text{ERR\_3}}$	-3	–	3	%	Accuracy of measured NTC resistance value in the range of 400 Ω to 610 Ω	PRQ-314
TMP pull-down switch on-state resistance	$R_{\text{PD\_on}}$	–	–	360	Ω	–	PRQ-315
TMP level selection overflow threshold	$\text{TH}_{\text{src\_overflow}}$	–	1000	–	LSB10	–	PRQ-316
TMP level selection underflow threshold	$\text{TH}_{\text{src\_underflow}}$	–	200	–	LSB10	–	PRQ-317
TMP measurement current level 0	$I_{\text{TMPz\_0}}$	4.70	5.0	5.35	μA	$0 \leq z \leq 7$	PRQ-322
TMP measurement current level 1	$I_{\text{TMPz\_1}}$	9.35	10.00	10.65	μA	$0 \leq z \leq 7$	PRQ-321
TMP measurement current level 2	$I_{\text{TMPz\_2}}$	18.75	20.00	21.25	μA	$0 \leq z \leq 7$	PRQ-320
TMP measurement current level 3	$I_{\text{TMPz\_3}}$	37.50	40.00	42.50	μA	$0 \leq z \leq 7$	PRQ-319

**(table continues...)**

## 12 Temperature measurement unit (TMP)

**Table 14** (continued) **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

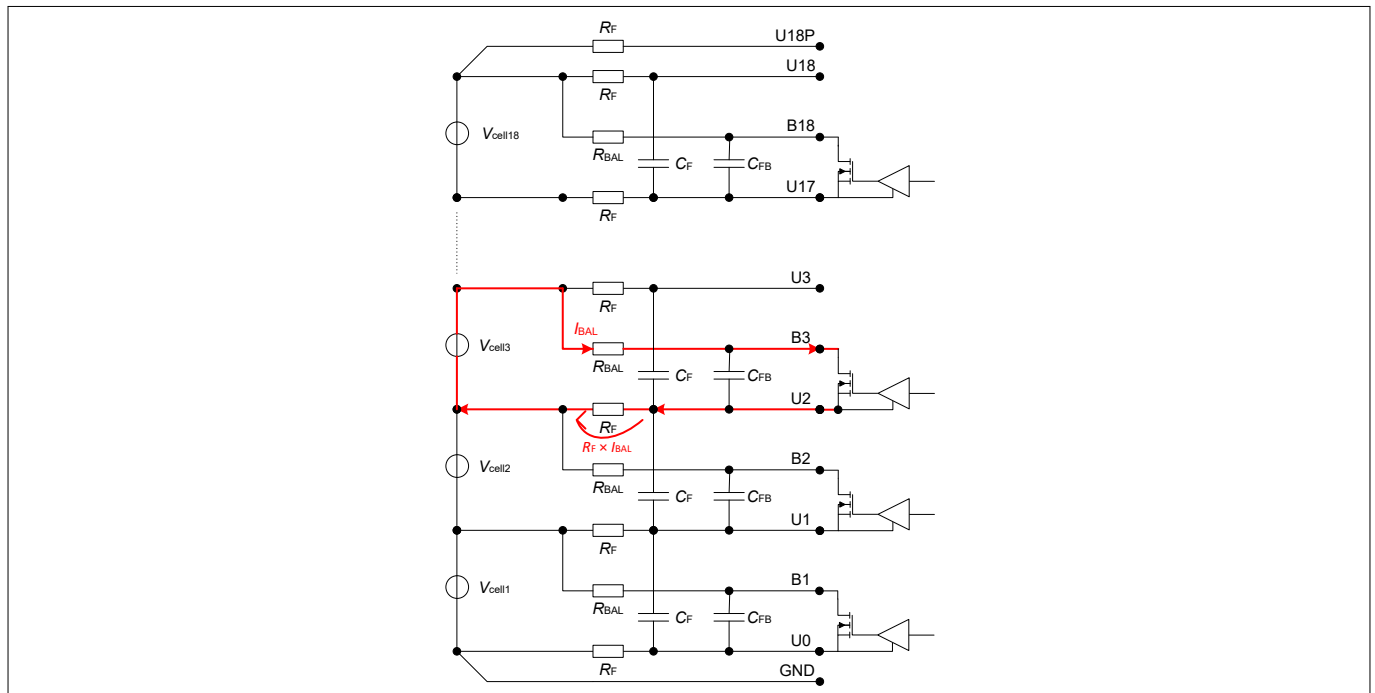
Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
TMP measurement current level 4	$I_{TMPz\_4}$	75.95	80.00	85.05	$\mu\text{A}$	$0 \leq z \leq 7$	PRQ-680
TMP measurement current level 5	$I_{TMPz\_5}$	149.9	160	170.1	$\mu\text{A}$	$0 \leq z \leq 7$	PRQ-679
TMP measurement current level 6	$I_{TMPz\_6}$	299.00	320.00	341.00	$\mu\text{A}$	$0 \leq z \leq 7$	PRQ-678
TMP measurement current level 7	$I_{TMPz\_7}$	599.00	640.00	681.00	$\mu\text{A}$	$0 \leq z \leq 7$	PRQ-685
TMP internal diagnostics resistor level 0_5 $\mu\text{A}$ _10 $\mu\text{A}$	$R_{\text{Diag\_5\_10}}$	95	125.8	158	$\text{k}\Omega$	–	PRQ-326
TMP internal diagnostics resistor level 1_20 $\mu\text{A}$ _40 $\mu\text{A}$	$R_{\text{Diag\_20\_40}}$	25	33	42	$\text{k}\Omega$	–	PRQ-325
TMP internal diagnostics resistor level 2_80 $\mu\text{A}$ _160 $\mu\text{A}$	$R_{\text{Diag\_80\_160}}$	6	8.55	11	$\text{k}\Omega$	–	PRQ-324
TMP internal diagnostics resistor level 3_320 $\mu\text{A}$ _640 $\mu\text{A}$	$R_{\text{Diag\_320\_640}}$	1.4	2	2.6	$\text{k}\Omega$	–	PRQ-323
TMP current source activation before RR starts step	$t_{\text{settle\_LSB}}$	–	10	–	ms	–	PRQ-560
TMP current source activation before RR starts maximum time	$t_{\text{settle\_max}}$	–	–	100 + $t_{VM}$	ms	$t_{\text{settle}}$ can be 0ms in case RR_SYNC bit is set in RR_CFG_1.	PRQ-561

## 13 Cell balancing (CB)

### 13.1 Functional description

The IC supports balancing (passive discharge) of each cell of the cell stack individually in all combination(s), including all channels in parallel with a balancing current per cell of  $I_{BAL}$ .

Overview of balancing current for one cell:



**Figure 11**

To activate cell balancing, the respective bit in the balancing settings register has to be set for each cell individually. To activate balancing on all cells the bit BAL\_CTRL\_1.ALL\_ON can be set.

Stopping the cell balancing can happen either individually or for all cells

#### Individually:

1. clearing the respective bit or
2. if the balancing timer reached the threshold
3. In case of an balancing overcurrent / undercurrent error
4. In case of an overvoltage / undervoltage error

#### All cells:

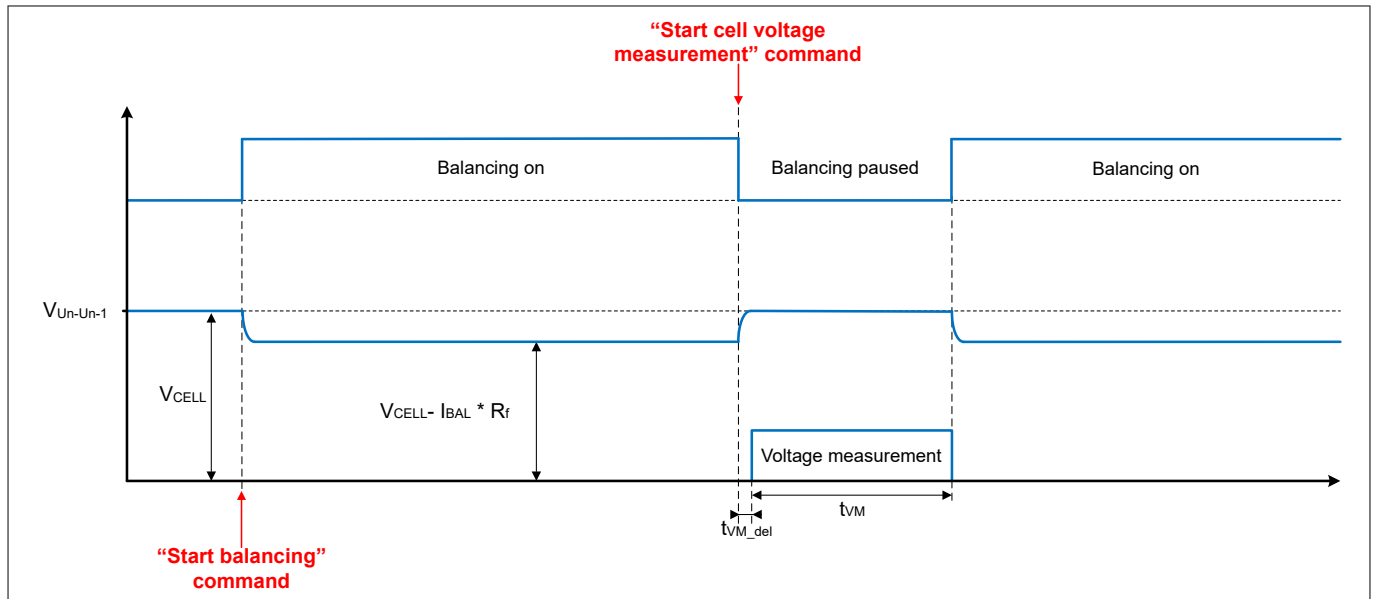
1. In case of an internal error
2. Internal overtemperature
3. External temperature error
4. Register EDC error
5. ADC error (if not masked by GEN\_CFG.BAL\_DIS\_ADC\_ERR)
6. Open load error
7. Internal temperature sensor mismatch error
8. Thermal runaway error
9. Error pin short circuit detection
10. Sum of PCVM vs. BVM mismatch error (if not masked by GEN\_CFG.BAL\_DIS\_PCVM\_BVM\_ERR)
11. PCVM vs. SCVM mismatch error (if not masked by GEN\_CFG.BAL\_DIS\_PCVM\_SCVM\_ERR)

### 13 Cell balancing (CB)

12. SCVM overvoltage (SCVM\_DIAG.SCVM\_OV\_ERR, can be deactivated by setting SCVM\_OV\_CFG.OV\_THR = 0x7FF<sub>H</sub>)
13. SCVM undervoltage (SCVM\_DIAG.SCVM\_UV\_ERR, can be deactivated by setting SCVM\_UV\_CFG.UV\_THR = 0x000<sub>H</sub>)

The IC pauses balancing automatically if the PBOFF bit in the measurement control register is set.

The balancing is paused for the entire duration of a PCVM/SCVM/BVM/BAVM ( $t_{VM} + t_{VM\_del}$ ) so that the cell voltage measurement is not corrupted by ongoing balancing. The same also applies in long running mode.



**Figure 12 Balancing and cell voltage measurement with balancing pause function active**

#### Individual time goal balancing:

The IC can balance each cell for an individual time, without generally needed periodic WDOG communication. The individual configured time  $t_{Bal}$  is compared to the balancing counter.  $t_{Bal}$  is defined by  $t_{BAL\_OFFn\_LSB}$  with a maximum interval defined by  $t_{BAL\_OFFn\_max}$ . The balancing of each cell is active until the balancing counter reaches the cell individual threshold. The balancing timer counter starts if the BAT\_CTRL\_1.START\_CNT bit is set. The device deactivates time goal balancing as soon as the counter reaches the individual threshold  $t_{BAL}$ .

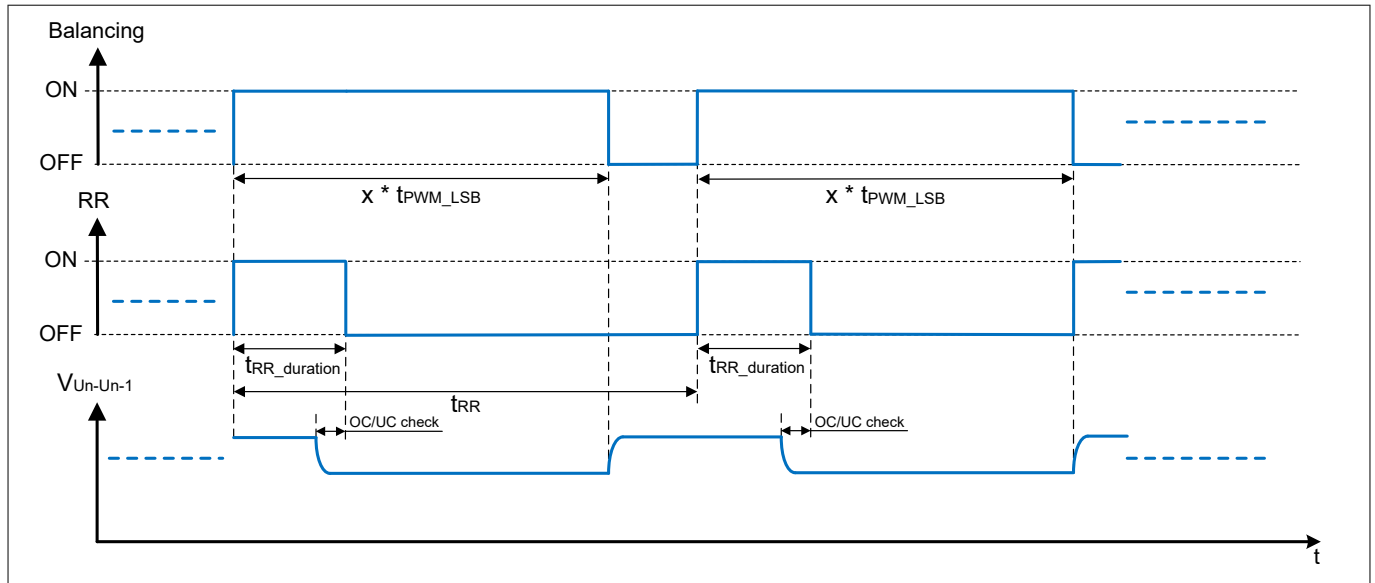
*Note: The device stays in normal mode until the extended watchdog runs out even if all balancing counter reached zero.*

#### PWM balancing:

The IC supports PWM balancing, by setting the balancing PWM control register. Balancing is started every time the RR is initiated which results in a PWM period of  $t_{RR}$ . The balancing on time can be configured with a resolution of  $t_{PWM\_LSB}$  up to the maximum time  $t_{RR}$  using the BAL\_PWM\_CFG register. If balancing for one or more cells is activated, the balancing switch is activated during the on-time of the PWM and is deactivated during the off-time of the PWM.

Other functions such as the voltage measurements can overrule the PWM balancing function.

### 13 Cell balancing (CB)

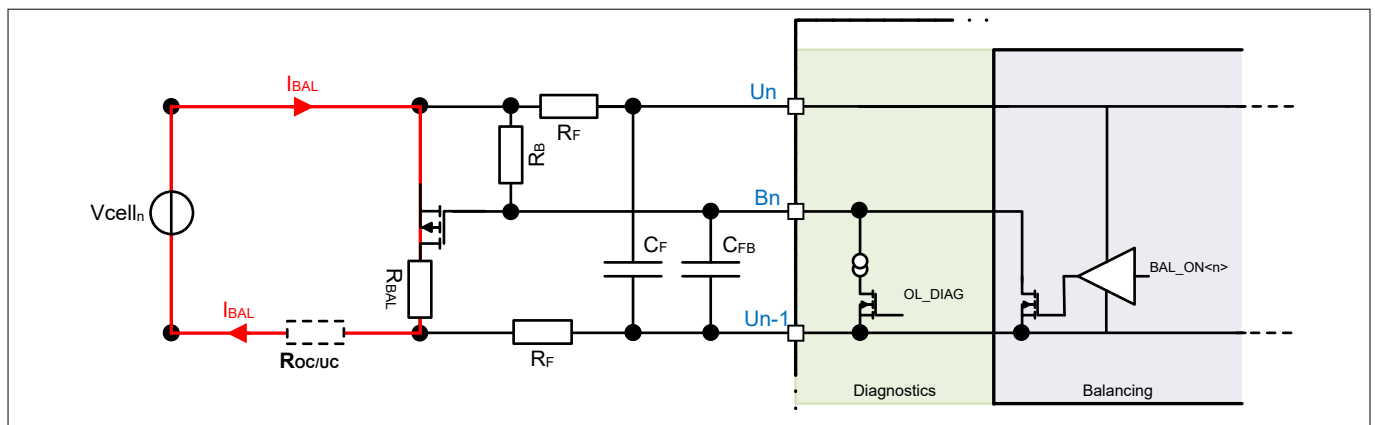


**Figure 13** PWM balancing function

Balancing is available during long-running mode measurements. In case of MEAS\_CTRL.PBOFF = 1, the device pauses cell balancing during the delay time of the measurement and during the measurement itself for PCVM, SCVM and BVM.

*Note: Only if  $t_{vm\_del} + t_{vm\_14bit} < t_{restart}$ .*

In addition to the internal balancing function, the IC also supports the use of an external balancing device. It is recommended to use a PMOS logic level type device to the corresponding Bn pin as an external balancing device.



**Figure 14** External balancing device

The IC supports overcurrent and undercurrent diagnostics, during the RR, also for the external balancing device, using an additional resistor  $R_{OC/UC}$ .

*Note: For the calculation of the overcurrent and undercurrent thresholds the voltage drop  $I_{BAL} \times R_{OC/UC}$  is used.*

#### Low power balancing mode:

The device is able to maintain individual cell balancing after transition to sleep mode if the balancing timer is set before the device is sent into sleep mode via setting the sleep mode bit or an expired watchdog.

All configured balancing switches are active until the balancing counter reaches the cell individual threshold, if all thresholds are reached the device reaches sleep mode.

In case of an event which stops balancing the device is freezing its current balancing counter value. The counter value is copied individually into balancing counter error time registers and can be read, after wake-up. The balancing counter error time registers can be cleared by a write command.

## 13 Cell balancing (CB)

### 13.2 Electrical characteristics cell balancing (CB)

**Table 15** Electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CB balancing switch on-state resistance	$R_{BAL\_on}$	–	1.0	1.7	$\Omega$	<b>1.</b> $1.5\text{ V} \leq U_{n+1} - U_n \leq 5\text{ V}$ <b>2.</b> $I_{BAL} = 300\text{ mA}$	PRQ-335
CB balancing current	$I_{BAL}$	–	–	300	mA	$1.5\text{ V} \leq (U_{n+1} - U_n) \leq 5\text{ V}$	PRQ-337
<b>Balancing timer</b>							
CB individual balancing time interval step	$t_{BAL\_OFFn\_LSB}$	7.27	8.00	8.89	min	$1 \leq n \leq 18$ ; BAL_CNT_TIMEBASE=2	PRQ-338
CB individual balancing timer maximum interval	$t_{BAL\_OFFn\_max}$	3.75	4.13	4.59	h	$1 \leq n \leq 18$ ; BAL_CNT_TIMEBASE=2;	PRQ-339
<b>PWM balancing</b>							
CB balancing PWM multiplier	$t_{BAL\_PWM\_LSB}$	0	–	126	LSB	–	PRQ-340

## 14 Cell diagnostics (CD)

### 14.1 Functional description

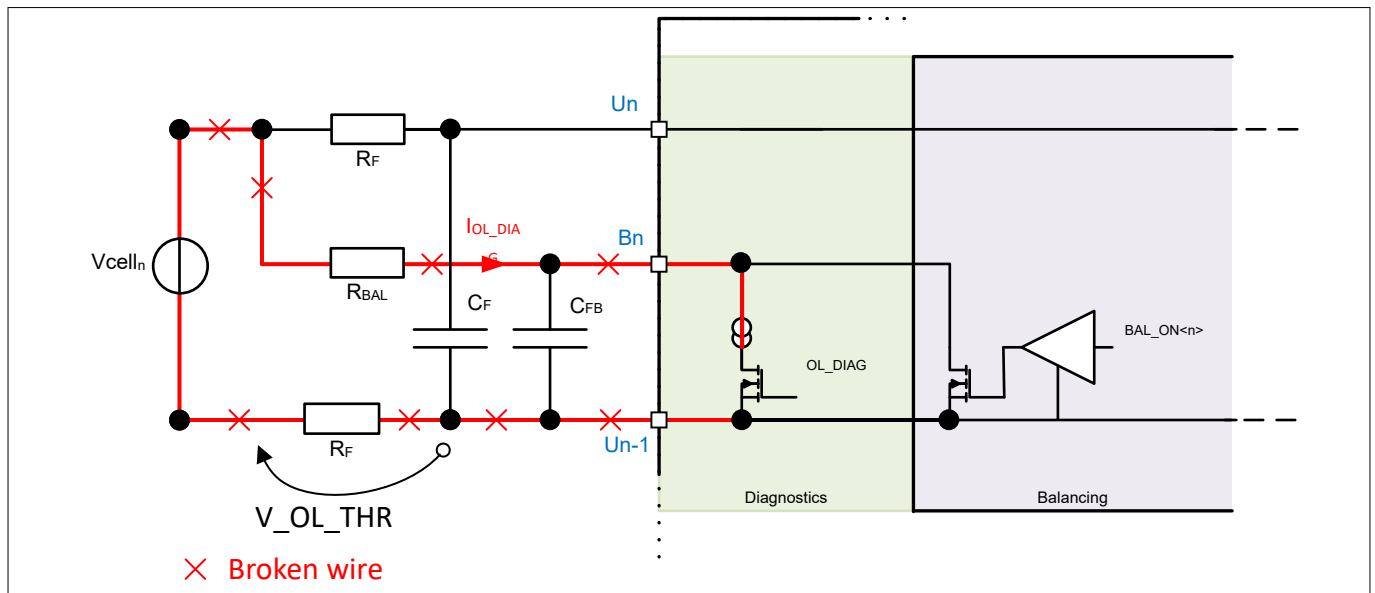
The IC provides automatic open wire/open load detection for all wires connected to a cell.

The detection is performed by voltage measurement while sinking the current  $I_{OL\_DIAG}$  into the balancing pin during a round robin cycle. It checks the odd channels in the first cycle and the even channels in the subsequent cycle.

A failure is detected if the voltage difference  $\Delta V_{OL\_THR}$  with and without the diagnostic current is activated is not between the minimum and maximum of the set open load threshold.

$$\Delta V_{OL\_THR} = [V_{Un+1} - V_{Un}]_{OL\_DIAG=disabled} - [V_{Un+1} - V_{Un}]_{OL\_DIAG=enabled}$$

The open wire and open load- detection threshold can be configured with a resolution of  $OL_{thr\_LSB}$  up to the maximum threshold of  $OL_{thr\_max}$  using the cell voltage thresholds register

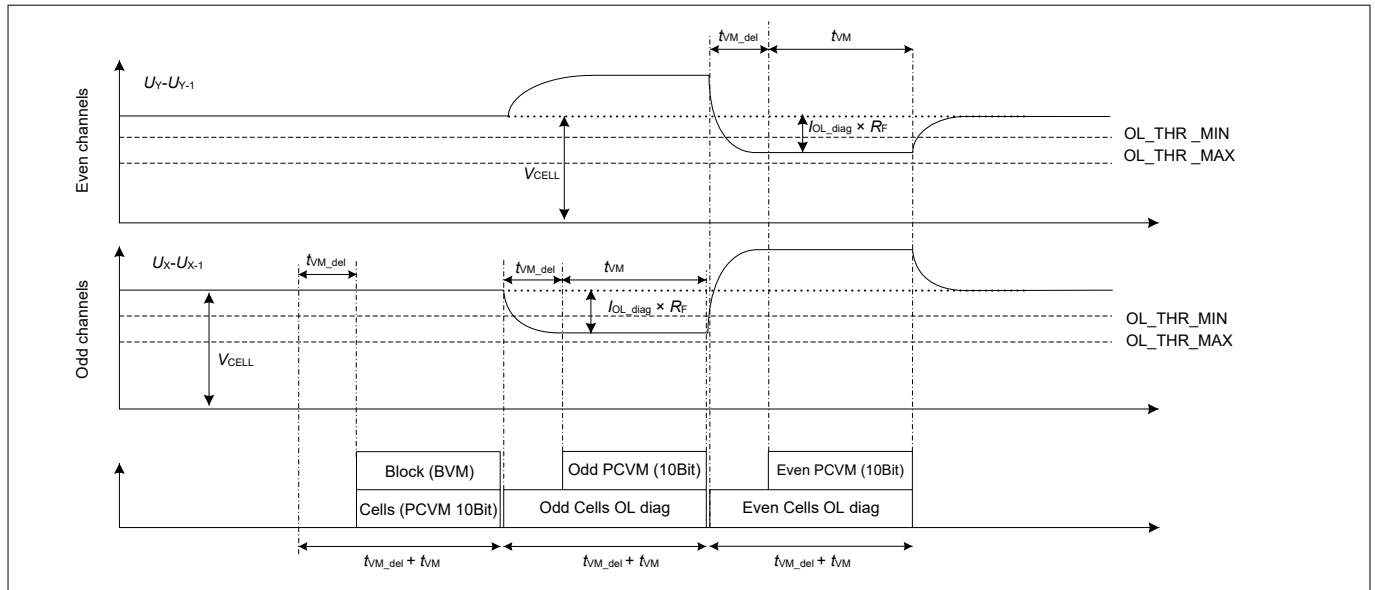


**Figure 15 Principle of open-wire diagnosis**

If the device detects an open wire or open load, it indicates it individually for each cell in the corresponding bitfield of the diagnostics open load register as well as in the summary OL error bit of the general diagnostic register.



## 14 Cell diagnostics (CD)



**Figure 16** Open wire and open load diagnostics detection process

An open wire or open load is detected if the cell voltage is not decreased during activated OL diagnosis current. An open wire or open load is also detected if the cell voltage is decreased more during activated OL diagnosis current than the value in the OL\_THR\_MAX register.

*Note: Setting the thresholds to 0, deactivates the check and diagnostic current.*

As part of the round robin the device performs a balancing overcurrent and a undercurrent check for each cell for which the balancing function is active. The overcurrent threshold  $OC_{thr}$  and the undercurrent threshold  $UC_{thr}$  is configurable with a resolution of  $CD_{thr\_LSB}$  up to the maximum threshold of  $OC_{thr\_max}$  or  $UC_{thr\_max}$  respectively is reached using the balancing current thresholds register.

If the device detects an balancing overcurrent or balancing undercurrent error, it deactivates balancing of the affected cell. In the DIAG\_x\_y (x=1; 3; 5; 7; 9; 11; 13; 15; 17 y=0; 2; 4; 6; 8; 10; 12; 14; 16) register containing the error details. The error is summarized in the GEN\_DIAG.BAL\_ERR\_OC/BAL\_ERR\_UC bitfields.

By setting the configuration bit OP\_MODE.I\_DIAG\_EN, the device activates the diagnostic current  $I_{OL\_DIAG}$  an all configured channels regardless of the BAL\_CTRL\_0/BAL\_CTRL\_1 registers and independent of round robin.

*Note: the cells are discharged by  $I_{OL\_DIAG}$*

### 14.2 Electrical characteristics cell diagnostics (CD)

**Table 16** Electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Open load							
CD diagnostic current for open load detection	$I_{OL\_DIAG}$	10	15	21	mA	$0.75\text{ V} < (V_{Bn} - V_{Un-1}) < 5\text{V}$	PRQ-345
CD open load threshold resolution	$OL_{thr\_LSB}$	–	19.5	–	mV	–	PRQ-346

(table continues...)

**14 Cell diagnostics (CD)**

**Table 16 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CD open load threshold maximum value	$OL_{thr\_max}$	–	1.23	–	V	–	PRQ-347
<b>Overcurrent &amp; undercurrent</b>							
CD balancing over- or undercurrent error threshold resolution	$CD_{thr\_LSB}$	–	19.5	–	mV	Undercurrent and overcurrent can be configured independently.	PRQ-348
CD maximum balancing overcurrent error threshold	$OC_{thr\_max}$	–	4.98	–	V	<ul style="list-style-type: none"> <li><math>I_{OC\_thr}</math> = Overcurrent threshold</li> <li><math>I_{OC\_thr} = OC\_THR [V] / R_F</math></li> </ul>	PRQ-349
CD maximum balancing undercurrent error threshold	$UC_{thr\_max}$	–	4.98	–	V	<ul style="list-style-type: none"> <li><math>I_{UC\_thr}</math> = undercurrent threshold</li> <li><math>I_{UC\_thr} = UC\_THR [V] / R_F</math></li> </ul>	PRQ-350
CD balancing overcurrent detection time	$t_{BAL\_OC\_DET}$	–	–	$t_{RR\_max}$	ms	Equivalent to the maximum round robin cycle time if the error counter is disabled.	PRQ-351

## **15 General-purpose input/output (GPIO)**

### **15.1 Functional description**

The device provides four individual GPIO pins which can be used as a digital input or digital output pins using the GPIO register or with their alternative function. After receiving a wake-up signal via iso UART all GPIOs can be configured using the GPIO register.

A logic high level on GPIO3 can wake-up the device and initiate an EMM signal if configured by the EXT\_WU\_EN bit in the general configuration register GEN\_CFG.

#### **UART mode:**

GPIO0 and GPIO1 are configured to act as UART pins, if the wake-up was received via UART.

- GPIO0 = UART\_LS
- GPIO1 = UART\_HS

#### **SPI mode:**

GPIOq ( $0 \leq q \leq 3$ ) can be configured to act as SPI pins using the GPIO register.

- GPIO0 = CSN
- GPIO1 = CLK
- GPIO2 = DATA / MOSI
- GPIO3 = MISO

## **16 Communication**

### **16.1 Functional description**

The device supports two main types of communication interfaces:

1. UART
2. iso UART

It is possible to stack multiple devices by using iso UART communications. Additionally a SPI master functionality is available by using the GPIO pins.

#### **SPI Master functionality:**

The following GPIO pins have an alternative function and have to be used if the SPI master functionality is desired:

1. GPIO0/UART\_LS/CSN
2. GPIO1/UART\_HS/CLK
3. GPIO2/MOSI/DATA
4. GPIO3/MISO

The SPI master module supports a 4-wire SPI as well as a half duplex 3-wire SPI. In case of the 3-wire SPI GPIO2 is configured as a push-pull output or as an high impedance (High-Z) input.

**SPI modes:** The SPI master can be configured to act in all SPI modes using the SPI master configuration register.

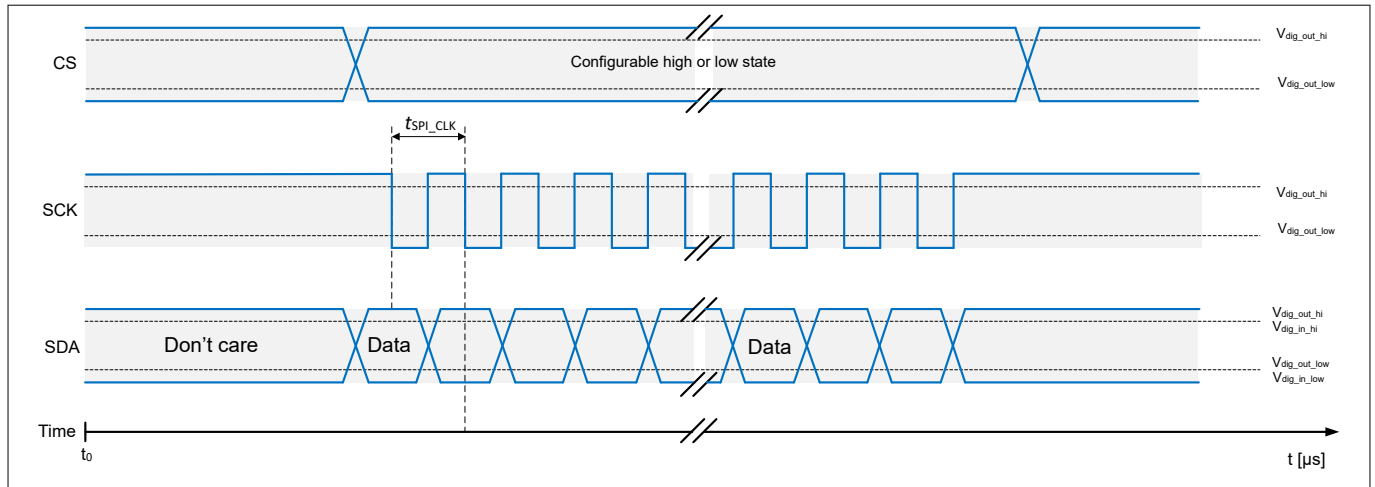
Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

The SPI interface operates as following:

- To write or to receive a message the SPI registers have to be set in order to configure the SPI communication.
- To send data via the SPI interface the data has to be send into the SPI data transmission (SPI\_TX) register. After receival of the message transfer the device writes the register contents via the SPI interface to the SPI secondary device, the received data is stored in the SPI data receive register (SPI\_RX) register.
- To read data via the SPI interface from the SPI secondary device, the host controller has to write a read command to the SPI\_TX register and subsequently read the result from the SPI\_RX register.

It is also possible to manually operate the SPI interface. In this case the SPI\_CFG.CSN\_LVL bit controls the CSN pin polarity so that multiple TX requests can be send to the SPI secondary device one after another.

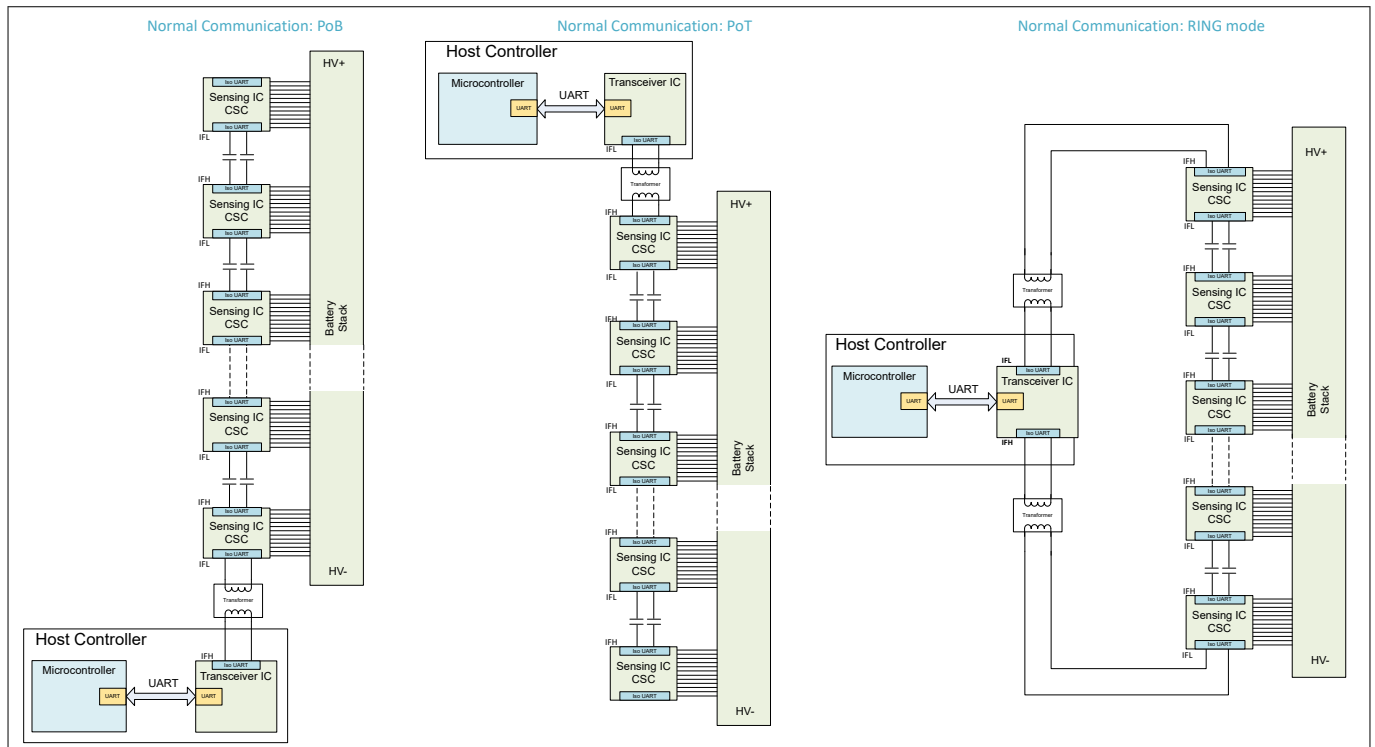
## 16 Communication



**Figure 17** 3-pin SPI timing diagram

The device can communicate in different configurations:

- Direct connection via UART, for low voltage applications
- Primary on bottom (PoB) communication with EMM function
- Primary on top (PoT) communication with EMM function
- Ring communication with EMM function



**Figure 18** Communication configurations

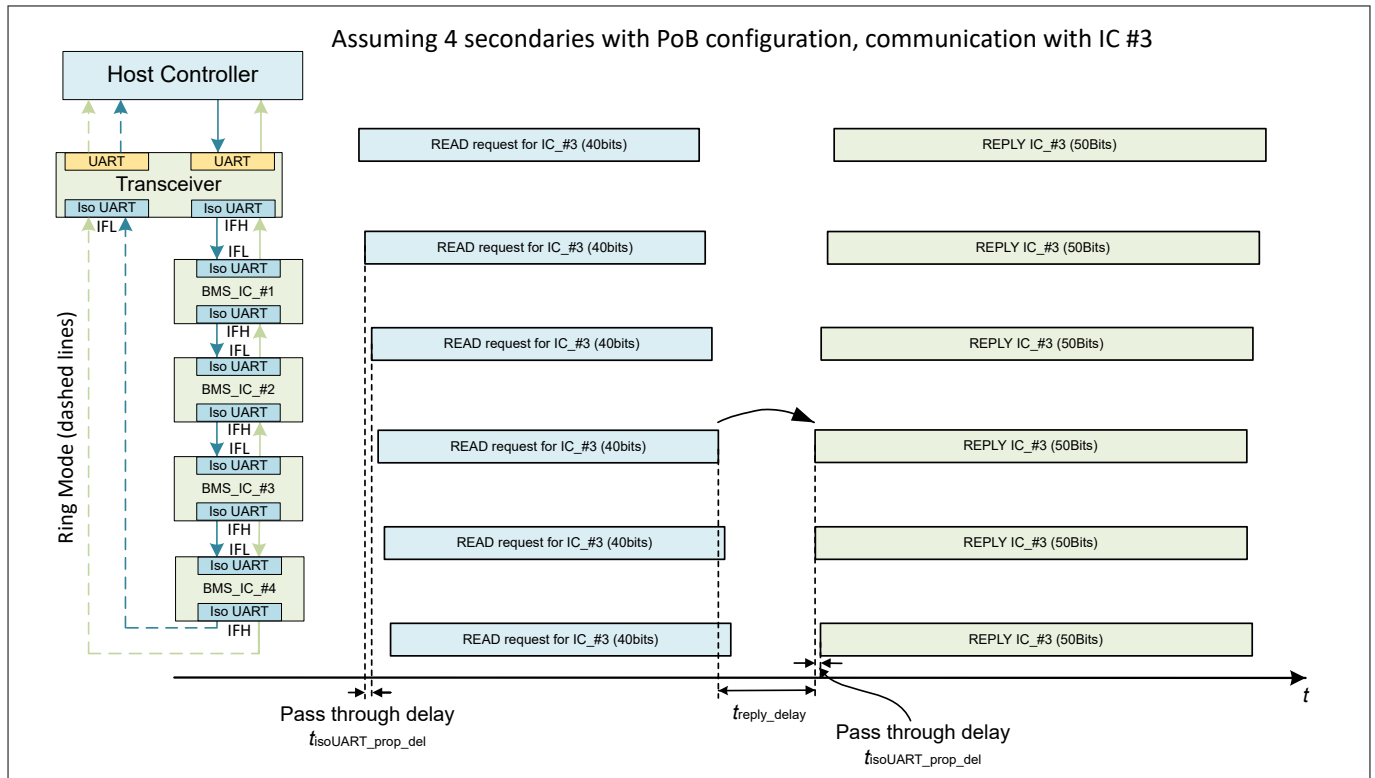
The IC communication direction is determined during a wake-up cycle. The iso UART interface or GPIO interface which receives the wake-up pattern is configured as RX while the other one is configured as TX. To change the direction, the device has to be put to sleep and woken up again.

There is a reply delay  $t_{reply\_delay}$ , which determines the time between the last stop bit of the read/write command (incoming command from the primary) and the first falling edge of the reply frame from the secondary.

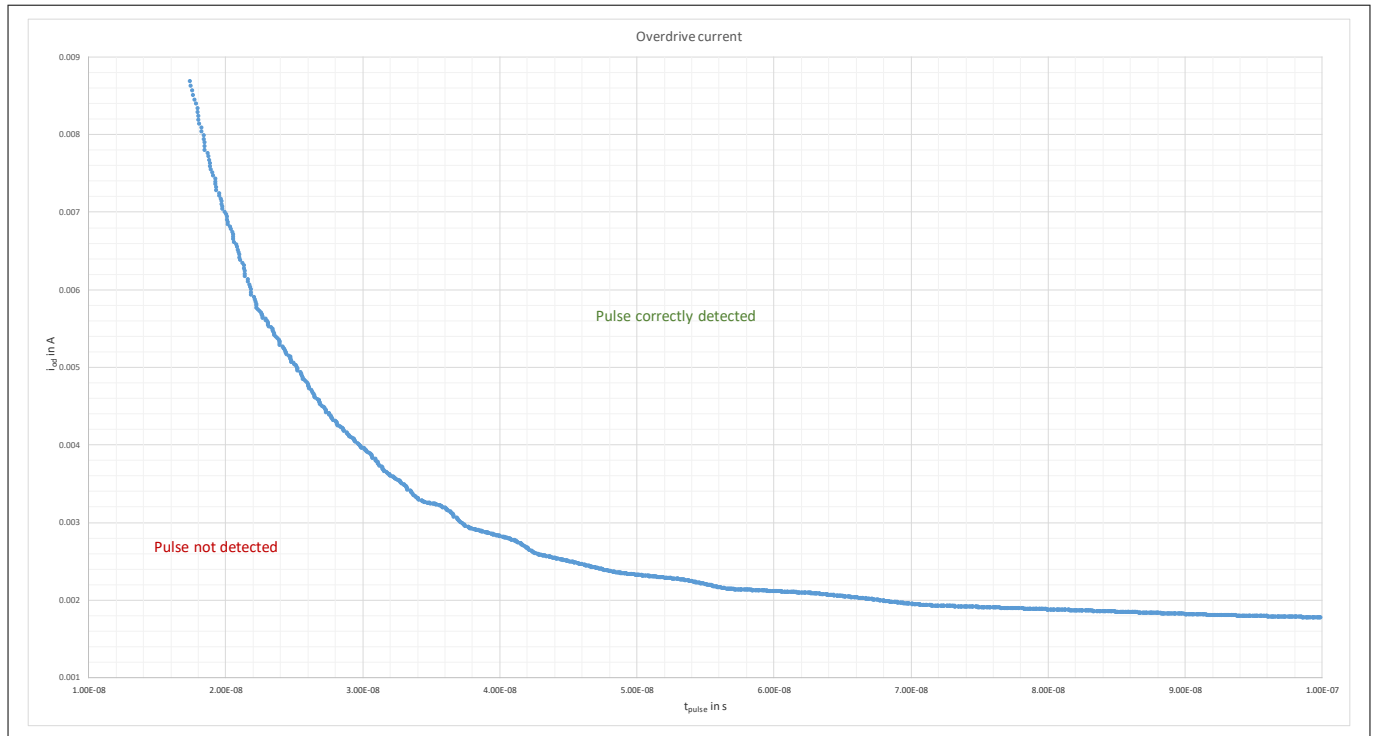
## 16 Communication

The device forwards a received message to the next device in the system. The time between receiving and forwarding the message depends upon the receiving interface:

- Receiving on UART and forwarding on iso UART:  $t_{\text{UART\_isoU\_del}}$
- Receiving on iso UART and forwarding on iso UART:  $t_{\text{isoU\_prop\_del}}$
- Receiving on iso UART and forwarding on UART:  $t_{\text{UART\_isoU\_del}}$



**Figure 19**      **Communication propagation delays**  
**iso UART waveform specification**



**Figure 20** iso UART waveform specification

### 16.1.1 Register write modes

There are two different approaches for writing content in the device:

- **Direct write:** Writing a single register in a single device.
- **Broadcast write:** Writing a single register in all devices in the same stack with one write command.

With broadcast write, each device of the chain first writes data. On successful write it switches its RX and TX units to allow the reply frame to be transferred. The last device in the chain (final node) initiates the reply frame. After completion of the reply frame all the device switch their RX and TX units back to their initial state.

*Note: The host controller only receives the reply frame if all other devices in the chain received and executed the message correctly and thus are forwarding it.*

### 16.1.2 Register read modes

There are three different approaches for reading content from the device:

- **Direct read:** Reading a single register from a single device.
- **Broadcast read:** Reading a single register from all devices in the same stack with one read command.
- **Multi read:** Reading multiple registers from a single device. The read command for multiple registers is configurable in the multi read registers MULTI\_READ\_SEL and MULTI\_READ\_CFG\_0 to MULTI\_READ\_CFG\_3. It can be used to read the measurement results of the following measurements with one read command of the MULTI\_READ:
  - PCVM
  - BVM
  - AVM/BAVM
  - SCVM
  - External temperature measurement

## 16 Communication

- Internal temperature measurement
- R\_Diag measurement
- **Broadcast multi read:** Reading multiple registers from all ICs in the stack. The list of registers read from all ICs can be configured in the MULTI\_READ\_SEL and MULTI\_READ\_CFG\_0 to MULTI\_READ\_CFG\_3 registers.

### 16.1.3 Communication frames

UART and iso UART communications consist of sending or retrieving sets of frames. A frame consists of 8 bits which are initiated by a start bit and concluded by a stop bit.

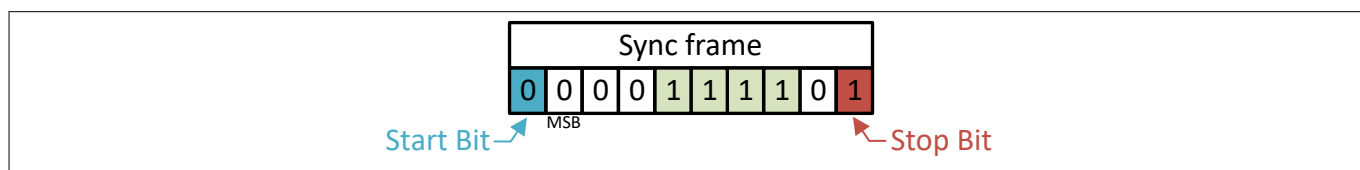
The following frames are available:

- Synchronization frame
- ID frame
- Address frame
- Data frames
- CRC frame
- Reply frame

*Note: Frames start with the most significant bit (MSB).*

#### Synchronization frame

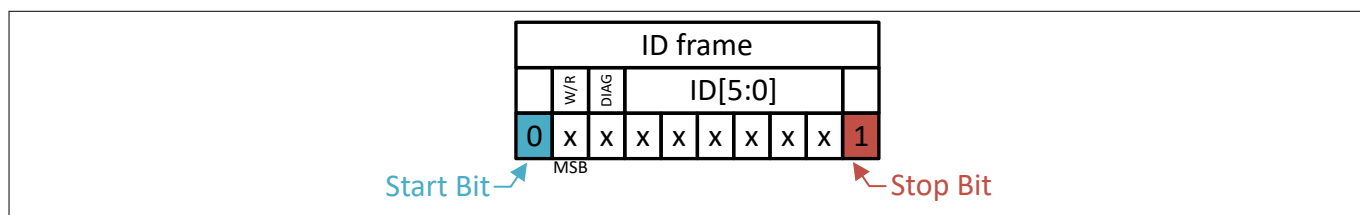
The communication is always initiated by sending a fixed synchronization frame.



**Figure 21** Synchronization frame

#### ID frame

The ID frame defines which device is intended to receive the message. It also determines the type of command.



**Figure 22** ID frame

**Table 17** Bit assignment ID frame

ID frame bits	Function
W/R[7]	1: Write command 0: Read command
DIAG[6]	0: No error in GEN_DIAG 1: Error in GEN_DIAG
ID[5:0]	000000: Default x: ID 111111: Broadcast command



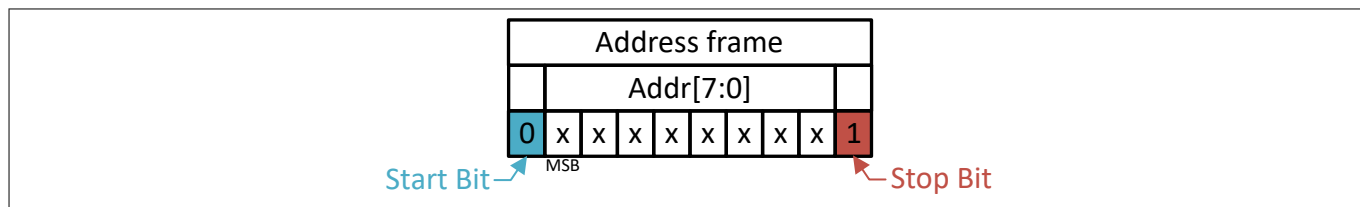
## 16 Communication

*Note: The ID 00<sub>H</sub> is only available after reset, before enumeration. The ID 3F<sub>H</sub> is exclusively used for broadcast commands.*

*Note: The DIAG bit is set by the secondary in the ID frame of a response message if there is an error indicated in the GEN\_DIAG register. When the primary sends an ID frame to the secondary, this bit should be set to 0.*

### Address frame

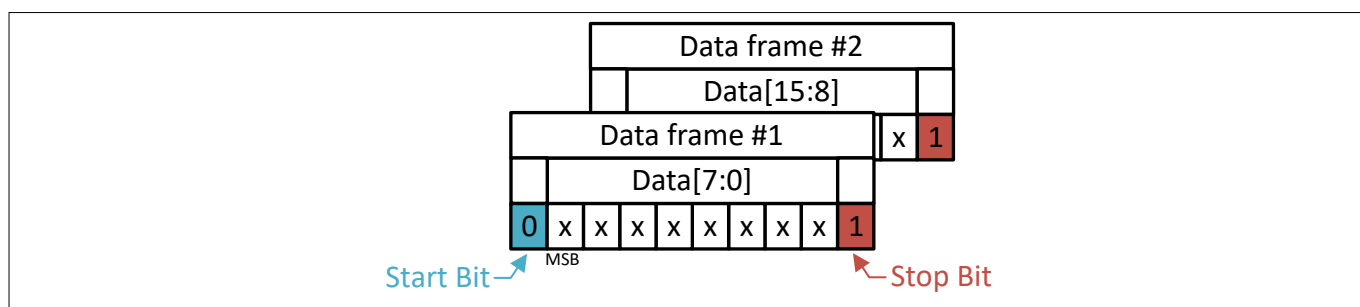
The address frame determines which register is targeted by the read or write command.



**Figure 23** Address frame

### Data frame

The data frame contains the sent or received data.



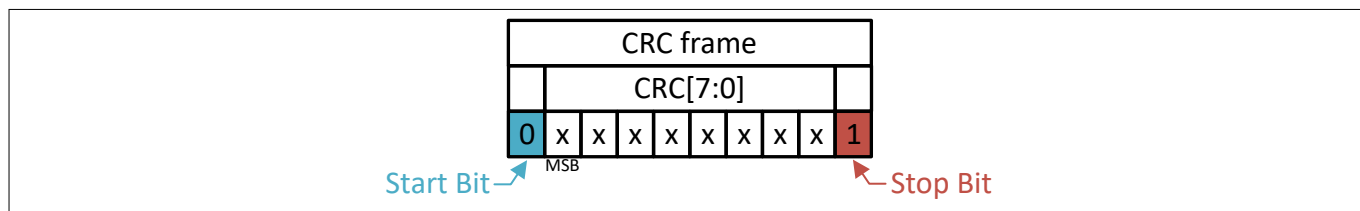
**Figure 24**

*Note: If the device encounters an invalid CRC, it neither accepts the message nor replies to it.*

### CRC frame

For read and write commands, an 8-bit CRC protection conforming to SAE J1850 for the entire message including the synchronization frame is calculated and appended to the frames.

8-bit polynomial:  $G(z) = z^8 + z^4 + z^3 + z^2 + 1$  (initial value = FF<sub>H</sub>; XOR value = FF<sub>H</sub>)



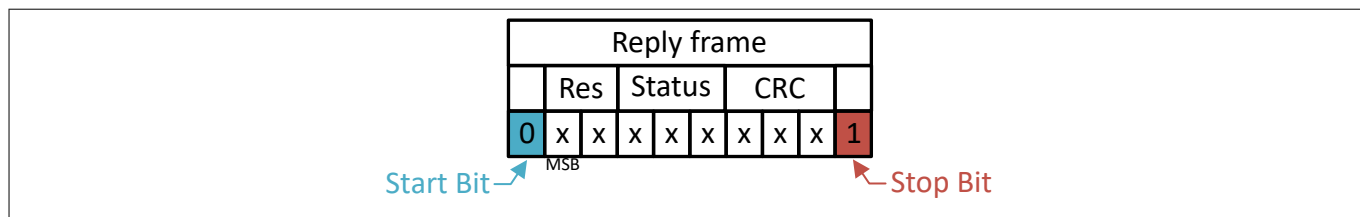
**Figure 25** CRC frame

*Note: If the device encounters a faulty CRC, it neither accepts the message nor replies to it.*

### Reply frame

The device acknowledges a received write command with a reply frame. In case of a broadcast write command only the device configured as final node generates the reply frame

## 16 Communication



**Figure 26** Reply frame

The message reply frame is protected by a 3-bit CRC calculated as:  $G(z) = z^3 + z + 1$ .

**Table 18** Bit assignment

Status bit	Function
Res[7:6]	Reserved
Status[5]	0: Write command successfully transmitted 1: CRC protected register error
Status[4]	0: Register address for write command valid 1: Register address for write command invalid
Status[3]	0: No fault in general diagnostics register 1: Fault in general diagnostics register
CRC[2:0]	3-bit reply CRC

Subject to change

## 16.2 Electrical characteristics communication

**Table 19** Electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GPIO physical layer							
UART to iso UART propagation delay	$t_{\text{UART\_isoU\_deI}}$	–	25	70	ns	<ul style="list-style-type: none"><li>From 50% rising or falling of UART/iso UART to 50% rising or falling of UART/iso UART.</li><li>Default external components</li></ul>	PRQ-388
GPIO bitrate	$BR_{\text{GPIO}}$	-	3	-	Mbit/s	–	PRQ-389

(table continues...)

**16 Communication**

**Table 19 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
iso UART physical layer							
iso UART current threshold high	$I_{isoU\_high}$	2.25	4.5	6.5	mA	$(I_{IFX\_H} - I_{IFX\_L}) / 2$ $I_{IFX\_H}$ : Current in the iso UART high pin $I_{IFX\_L}$ : Current in the iso UART low pin	PRQ-390
iso UART current threshold low	$I_{isoU\_low}$	-6.5	-4.5	-2.25	mA	$(I_{IFX\_H} - I_{IFX\_L}) / 2$ $I_{IFX\_H}$ : Current in the iso UART high pin $I_{IFX\_L}$ : Current in the iso UART low pin	PRQ-391
iso UART propagation delay	$t_{isoU\_prop\_del}$	20	–	60	ns	Propagation delay from IFH to IFL and IFL to IFH	PRQ-392
iso UART overdrive current	$I_{od}$	3	–	–	mA	$t_{pulse} = 38 \text{ ns}$	PRQ-393
Reply delay time	$t_{reply\_delay}$	–	1.4μs +2*1/ $BR_x$	1.9μs +2*1/ $BR_x$	μs	internal reply delay time of one IC x=GPIO; isoU	PRQ-394
iso UART bit rate	$BR_{isoU}$	0.97	-	3.1	Mbit/s	–	PRQ-395
Series resistor value	$R_{SER}$	37.05	39	40.95	Ω	External RC network needs to be adjusted depending on the application constraints (i.e. cable length)	PRQ-396
Series capacitor value	$C_{SER}$	0.95	1	1.05	nF	<ul style="list-style-type: none"><li>External RC network needs to be adjusted depending on the application constraints (i.e. cable length)</li><li>Voltage rating of <math>C_{SER}</math> has to be considered with respect to battery voltage level</li></ul>	PRQ-397
Transceiver Ron @100mA	$R_{ON}$	19	22	27	Ω	–	PRQ-672

**(table continues...)**

**16 Communication**

**Table 19 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI Master							
SPI min. clock frequency	$f_{\text{SPI,min}}$	–	50	–	kHz	–	PRQ-539
SPI max. clock frequency	$f_{\text{SPI,max}}$	–	1.75	–	MHz		PRQ-690
SPI chip select lead time	$t_{\text{CSN\_lead}}$	100	–	–	ns	–	PRQ-544
UART broadcast read bus release time	$t_{\text{UART\_rel\_BR}}$	–	–	$15 \times 1/BR_x$	s	Time to wait before sending a new command after end of broadcast read reply. x=GPIO; isoU	PRQ-695
UART read, write, broadcast write, multiread release time	$t_{\text{UART\_rel}}$	–	–	$3 \times 1/BR_x$	s	Time to wait before sending a new command after end of read/write/ broadcast write/ multiread reply. x=GPIO; isoU	PRQ-697

## **17 Round robin (RR)**

### **17.1 Functional description**

The device performs a round robin (RR) scheme triggered by internal timer or via host-controller command. During this scheme several measurements as well as internal diagnostics to check for possible faults independent of communication commands are triggered.

The automatic RR can be deactivated by setting the round robin period to 0 in the round robin configuration register.

The setting of the partition configuration register determines, which cells are covered by the RR.

The RR feature can be used in two different ways:

1. Autonomous RR: In this mode the device is performing a RR if the configurable time  $t_{RR}$  expires
2. Manual RR: In this mode the uC can trigger the execution of a RR by setting the RR\_CFG\_1.RR\_SYNC bit. A write command to WD\_CNT bits triggers the RR.

*Note: A running RR must not be interrupted by an expired RR period or by the RR\_CFG\_1.RR\_SYNC bit.*

The automatic round robin diagnostic cycle is performed periodically every  $t_{RR}$  or manually by a communication command. The period is configurable from  $t_{RR\_min}$  to  $t_{RR\_max}$  with a step size of  $t_{RR\_LSB}$ . The duration of the actual diagnostic checks is defined by  $t_{RR\_duration}$ .

#### **RR measurements:**

The following measurements are performed once during one round robin cycle:

- Temperature measurements of both internal temperature sensors.
- Stress sensor compensation measurements and calculations.
- PCVM (10-bit) for all activated cells.
- BVM (10-bit).
- NTC resistance measurement.
- NTC diagnostic measurements

*Note: To measure all connected NTCs up to three cycles a be needed.*

*Note: The result registers of PCVM and BVM are not updated by the RR. The measured data is available in the PCVM\_RR\_x registers and in the BVM\_RR and is updated upon every RR execution.*

#### **RR checks:**

During a round robin, the following checks are performed subsequent to the corresponding measurements, if set active:

1. Internal overtemperature and plausibility check
  - a. Comparing the measured value with the internal overtemperature threshold
  - b. Check if both temperature values are within a delta of  $2 \times T_{ERR\_int\_abs}$ .
2. The sum of all PCVMs is compared to the BVM for a plausibility check.
3. Cell voltage over- and undervoltage check to determine if the voltage of a cell is violating the programmed threshold.
4. Open load diagnostic an all voltage sensing and balancing pins of all activated cells.
5. Balancing overcurrent and undercurrent check for each cell where the balancing function is active.
6. NTC overtemperature check.
7. NTC diagnostics checks.
8. Ground loss check.

Each fault detected in a RR check increases the respective error counter by the configured value.

#### **NTC diagnostics checks:**

During a round robin cycle, the connections on the activated TMPz channels are checked for open or short conditions. If an open or short failure is detected and the error counter is exceeded, the corresponding fault bit in the external temperature diagnosis register is set. Additionally, the external temperature error bit of

## 17 Round robin (RR)

the general diagnostics register is set. If the measured NTC value violates the corresponding thresholds, then an error flag is set.

$$NTC_{open\_thr} \leq EXT\_TEMP\_z.RESULT \leq NTC_{short\_thr}$$

Clearing the external temperature error bit of the general diagnostics register resets the external temperature diagnosis register.

*Note: Manual setting of the current source range selection can lead to invalid measurements.*

### Cell under- and overvoltage check:

After the 10-bit cell voltage measurement task in the round robin cycle has been performed, the measurement results are compared to configurable under- and overvoltage thresholds. To configure the thresholds, the corresponding bits in the cell voltage OV/UV thresholds registers can be set with a resolution of  $V_{Comp\_LSB}$  until the maximum value  $V_{OVUV\_max}$  is reached.

The undervoltage detection can be disabled by setting  $UV\_THR = 000_H$ .

The overvoltage detection is disabled by setting  $OV\_THR = 3FF_H$ .

If the device detects an error during a round robin cycle, the individual error counter is increased by a configurable value which can be defined using the error counter increment value bits of the error counter configuration register.

If the error counter reaches its maximum value of 15, the respective error bit is set. A RR which is not detecting the specific error, the error counter is decreased, until its minimum value of 0, by a configurable value which can be defined using the error counter decrement value bits of the error counter configuration register. It is possible to deactivate a specific error counter by a setting a mask bit.

*Note: If the increment value is set to 15 a error flag is set with the first detection of the failure condition.*

### RR diagnostic registers:

The status of the diagnostic registers which have been updated during a round robin cycle can be read via a command. If a fault was detected, considering the respective error counter, the information is latched and can be cleared via a clear command.

*Note: The following diagnostics registers are available:*

- General diagnosis  $GEN\_DIAG$
- Channel diagnosis  $DIAG\_1\_0$
- Channel diagnosis  $DIAG\_3\_2$
- Channel diagnosis  $DIAG\_5\_4$
- Channel diagnosis  $DIAG\_7\_6$
- Channel diagnosis  $DIAG\_9\_8$
- Channel diagnosis  $DIAG\_11\_10$
- Channel diagnosis  $DIAG\_13\_12$
- Channel diagnosis  $DIAG\_15\_14$
- Channel diagnosis  $DIAG\_17\_16$
- External temperature diagnosis  $EXT\_TEMP\_DIAG\_0$
- External temperature diagnosis  $EXT\_TEMP\_DIAG\_1$
- Temperature reference diagnosis  $TMP\_REF\_DIAG$

The IC keeps all diagnostic results in sleep mode, as long as the sleep mode supply is available on U18P pin.

The IC has an automatic overvoltage and undervoltage detection, based on comparator and on SD-ADC.

1. A comparator monitors the  $V_{Bn} - V_{Un-1}$  voltage and sets the  $OV\_ANA\_COMP\_x/UV\_ANA\_COMP\_x$  bits in the registers channel diagnosis registers.
2. A delta sigma ADC monitors the  $(V_{Un+1} - V_{Un})$  voltage and sets the  $OV\_DIG\_COMP\_x/UV\_DIG\_COMP\_x$  bits in the registers.

In either case the error counter is increased if an OV/UV is detected. ( $0 \leq x \leq 17$ )

During a round robin cycle, the balancing function is paused while overvoltage and undervoltage check.

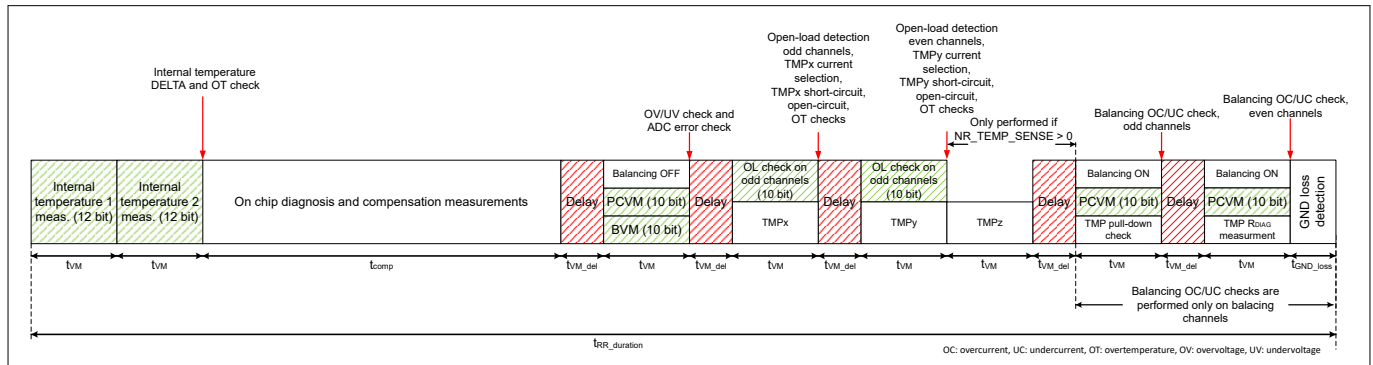
## 17 Round robin (RR)

After manually triggering a PCVM, SCVM, BVM, or AVM/BAVM, the IC executes the triggered measurement and an ongoing RR is terminated. After the measurement is finished, the round robin task is restarted.

If there are conflicts, the round robin cycle has a lower priority than the triggered measurement. After the round robin cycle has been skipped once, it is not possible to skip it a second time.

*Note: This applies also in case of a long running mode measurement*

If a round robin is delayed by a manual triggered measurement, the further RR scheme is re-synchronized. By end of the measurement time  $t_{vm}$ , the RR counter is reset

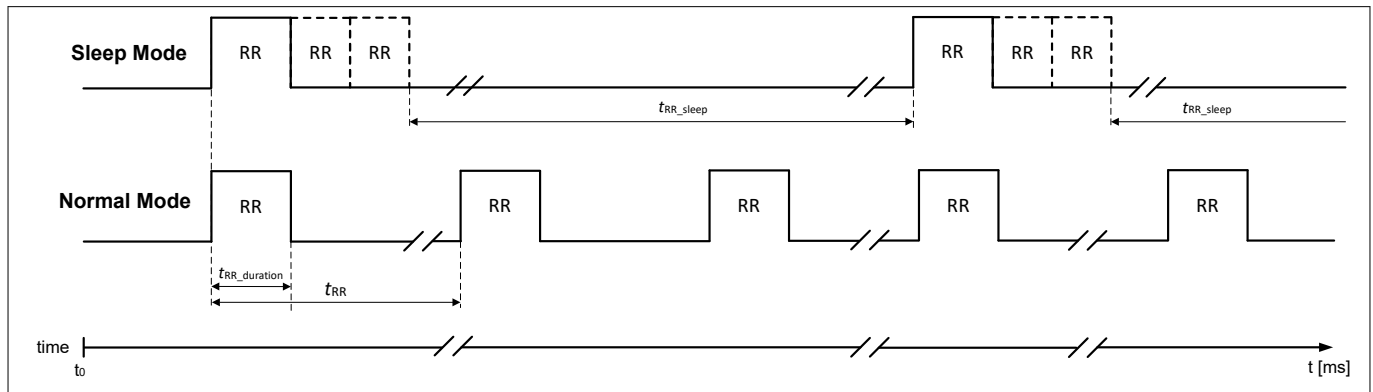


**Figure 27** RR task timing diagram

*Note: Diagram is not to scale,  $t_{vm}$  depends on the actual measurement depth.*

### Round robin during sleep mode:

The IC includes a feature to periodically wake-up from sleep mode to perform diagnostic checks and external temperature measurements. The wake-up period,  $t_{RR\_sleep}$ , is configurable with a step size of  $t_{RR\_sleep\_LSB}$  up to the maximum period  $t_{RR\_sleep\_max}$ .



**Figure 28** Round robin diagnostics timing during sleep and normal mode

### Pulse check:

The device can be configured to initiate an EMM after the configurable threshold  $n_{RR\_Pulse}$  has been reached. Every RR sleep cycle increases the counter value. A RR burst in sleep mode is increasing the counter also by 1. If an EMM was initiated the host-controller can clear the counter to 0 by writing "7FF" to the RR\_SLEEP\_STAT.WAKEUP\_CNT bit-field after receiving the EMM wake-up sequence. The threshold can be set in PLS\_CHK bits of the round robin configuration register, RR\_CFG\_0.PLS\_CHK.

If the devices wake-up was triggered by the round robin sleep time function the round robin is repeated in burst mode until all configured NTC channels are measured and providing a valid result.

*Note: Valid means a result between the  $TH_{Src\_overflow}$  and  $TH_{Src\_underflow}$  thresholds and long enough settling time.*

### Temperature rise in sleep:

## 17 Round robin (RR)

Additional to the checks which are performed by the round robin function in normal mode, the round robin sleep function is comparing the current NTC result to the previous one. The difference of these results is checked against the configurable threshold  $NTC_{threshold}$ . An error occurs if  $(NTC_{t-1} - NTC_t) > NTC_{threshold}$ .

The threshold is set in the THRESHOLD bits of the TEMP\_RISE\_CFG register. It is configurable which NTC channels are supervised by setting the EXT\_TEMP\_CFG\_2.NR\_TEMP\_SENSE bits.

### 17.2 Electrical characteristics round robin (RR)

**Table 20**      **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overvoltage and undervoltage detection							
OV/UV threshold resolution	$V_{OVUV\_LSB}$	–	$FSR_{PC\_VM}/2^{10}$	–	mV	–	PRQ-422
OV/UV threshold maximum value	$V_{OVUV\_max}$	0	–	$FSR_{PC\_VM}$	V	–	PRQ-423
Round robin timing							
RR scheme duration	$t_{RR\_duration}$	–	2.036	2.122	ms	Only valid if the measurement delay time $t_{VM\_del}$ is not higher than $t_{VM\_del\_LSB}$ .	PRQ-424
RR interval step	$t_{RR\_LSB}$	1.12	1.17	1.22	ms	–	PRQ-425
RR minimum interval time	$t_{RR\_min}$	6.7	–	7.4	ms	–	PRQ-426
RR maximum interval time	$t_{RR\_max}$	148.54	154.47	160.91	ms	7-bit counter	PRQ-427
RR sleep interval step	$t_{RR\_sleep\_LSB}$	–	2	–	s	–	PRQ-428
RR sleep maximum interval time	$t_{RR\_sleep\_max}$	–	2.28	–	h	12-bit counter	PRQ-429
Error counter increment	$n_{ERROR\_inc}$	1	–	15	-	4-bit counter	PRQ-430
Error counter decrement	$n_{ERROR\_dec}$	0	–	15	–	4-bit counter	PRQ-618
RR Pulse	$n_{RR\_pulse}$	0	–	2047	–	Setting the counter to 0 deactivates the feature	PRQ-602
CRC check cyclic interval	$t_{EDC\_check}$	47	49.15	52	ms	–	PRQ-431
RR compensation measurement and calculation	$t_{comp}$	–	800	–	μs	–	PRQ-432

**(table continues...)**



**17 Round robin (RR)**

**Table 20 (continued) Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RR GND loss detection	$t_{\text{GND\_loss}}$	9.1	9.7	10.8	$\mu\text{s}$	–	PRQ-688
ADC ERROR result (sum PCVM vs. BVM) comparison error threshold	$\text{ADC\_ERR}_{\text{th}}$	–	560	–	mV	Not valid if a busbar is connected in within the cellstack	PRQ-433

**NTC Open / short diagnostics**

NTC short threshold	$V_{\text{NTC\_short}}$	–	0.25	–	V	Using $I_{\text{TMPz\_7}}$	PRQ-434
NTC open threshold	$V_{\text{NTC\_open}}$	–	2	–	V	Using $I_{\text{TMPz\_0}}$	PRQ-435
NTC value change during sleep maximum threshold	$\text{NTC}_{\text{threshold}}$	0	–	65535	[LSB1 0]	Configuration register: TEMP_RISE_CFG.THRESH OLD[15:0]; Valid in round robin sleep	PRQ-559

## 18 Emergency mode (EMM) and ERR pin (ERR)

### 18.1 Functional description

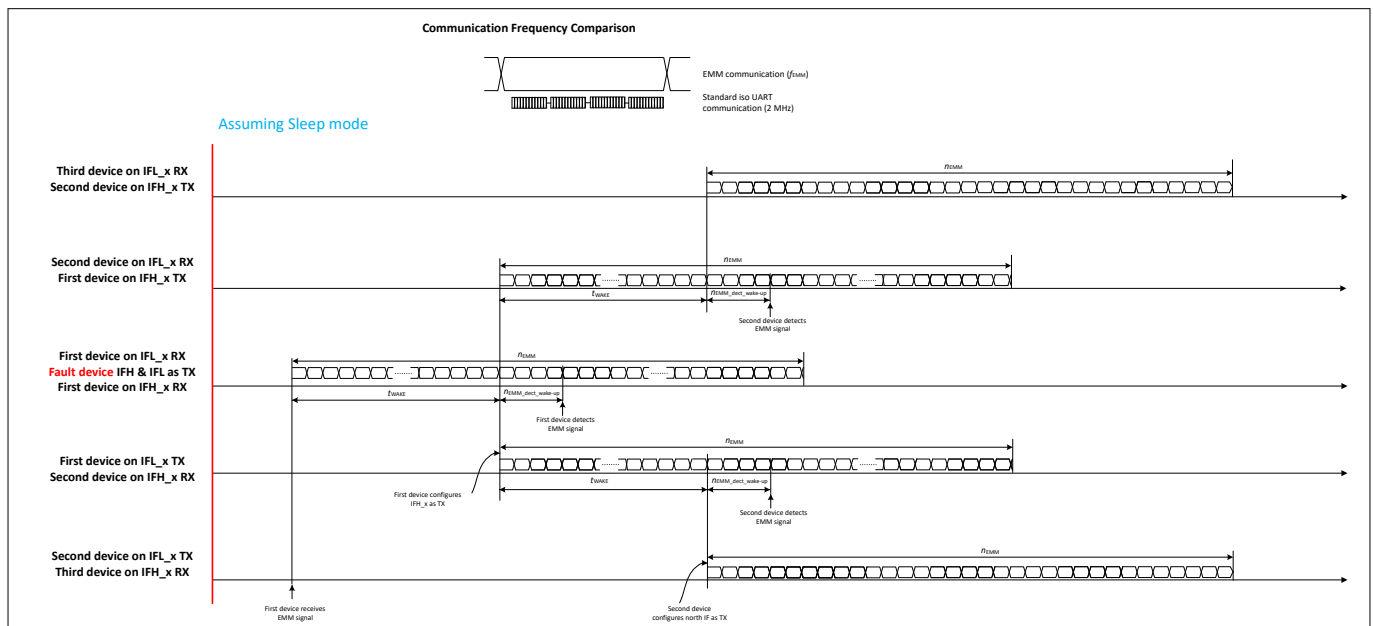
The device is able to indicate an error or a life signal to the host controller by the ERR pin or the emergency signal (EMM). One of the following reactions can be configured in the ERR pin / EMM mask configuration register:

- Indicate the issue on the configurable ERR pin:
  - Either via a "high" level if the bit GEN\_CFG.ERR\_POL is set to 1.
  - Or a "low" level if the bit GEN\_CFG.ERR\_POL is set to 0.
- Send an EMM via iso UART to the neighboring device(s) in the chain, if the bit FAULT\_MASK\_CFG.ERR\_PIN is set to 0.
  - Send an EMM signal after the RR\_SLEEP\_STAT.WAKEUP\_CNT reaches or exceeds the threshold configured via RR\_CFG\_0.PLS\_CHK.

The ERR pin is protected against shorts to GND and VS. If a short of the ERR pin to GND or VS is detected by the IC, the ERR\_PIN\_SC bit in the GEN\_DIAG register is set.

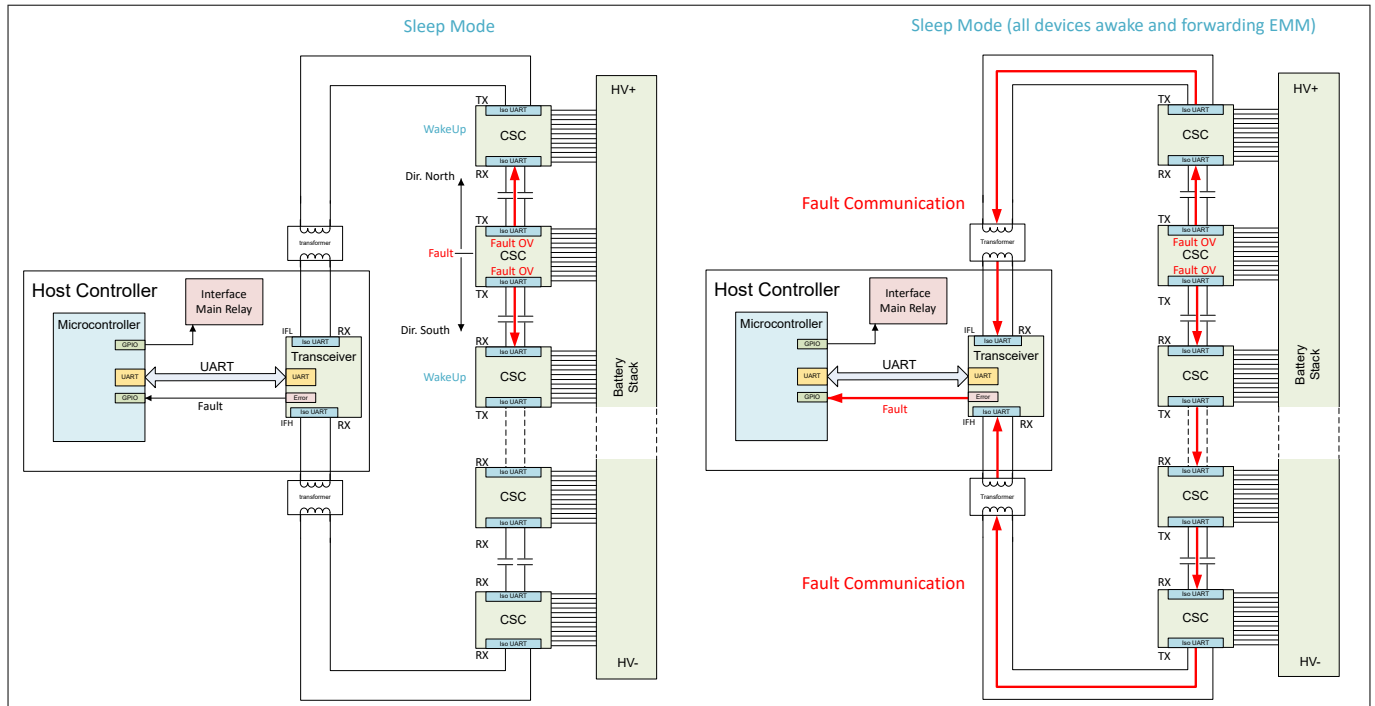
The emergency signal is defined by an alternating signal with the frequency  $f_{EMM}$  and a length of  $n_{EMM}$ . The EMM is received and sent via the iso UART communication interfaces.

The IC can detect and forward an EMM signal in sleep mode. The EMM signal is used for the IC wake-up. On detecting an EMM signal, the IC reproduces and forwards it to the opposite iso UART interface after the wake-up is finished. After the transmit process the IC returns to sleep mode.



**Figure 29** EMM in sleep mode process

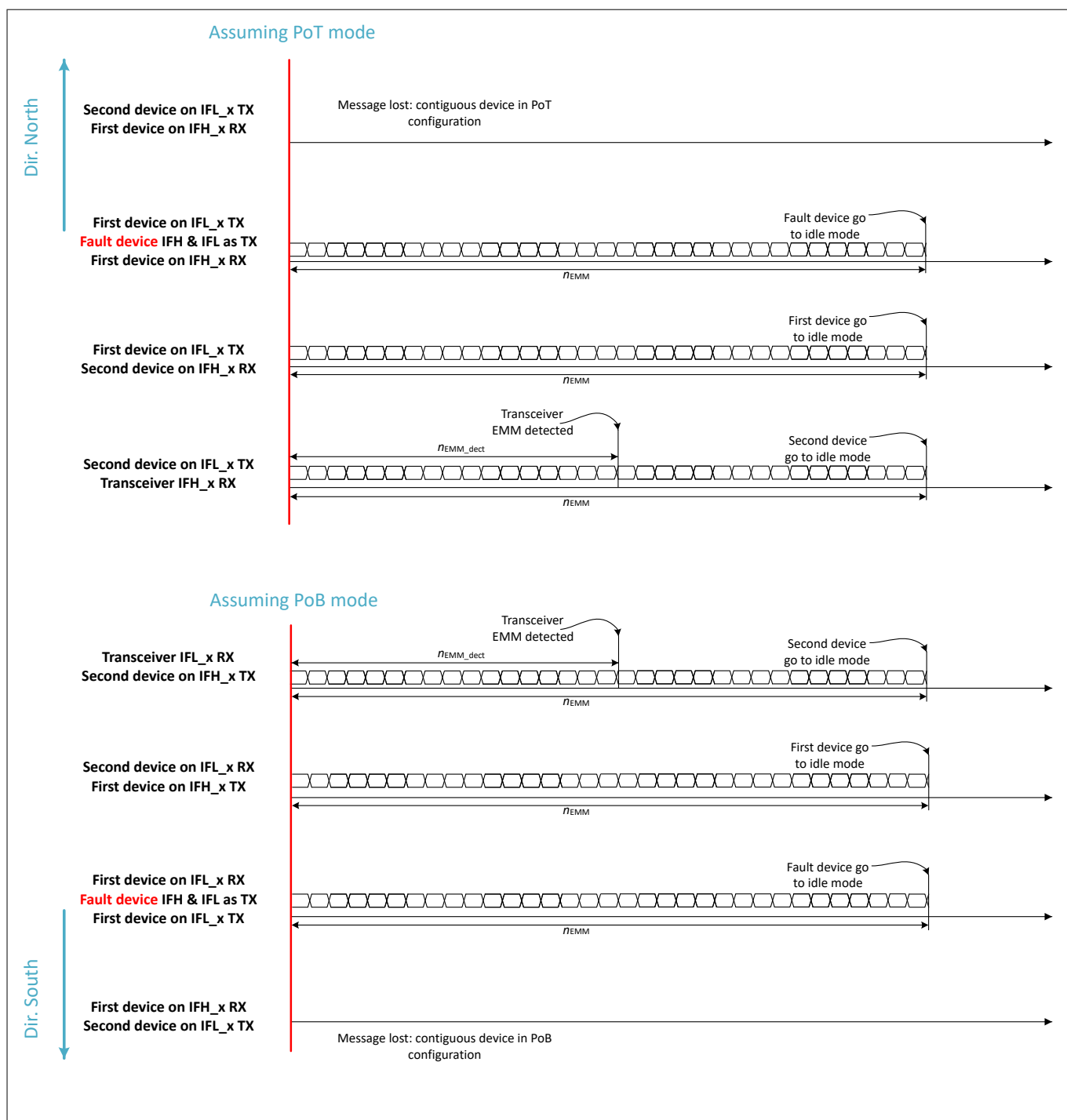
**18 Emergency mode (EMM) and ERR pin (ERR)**



**Figure 30** EMM in sleep mode path, with a chain in sleep mode, the EMM signal reaches the transceiver from both sides.

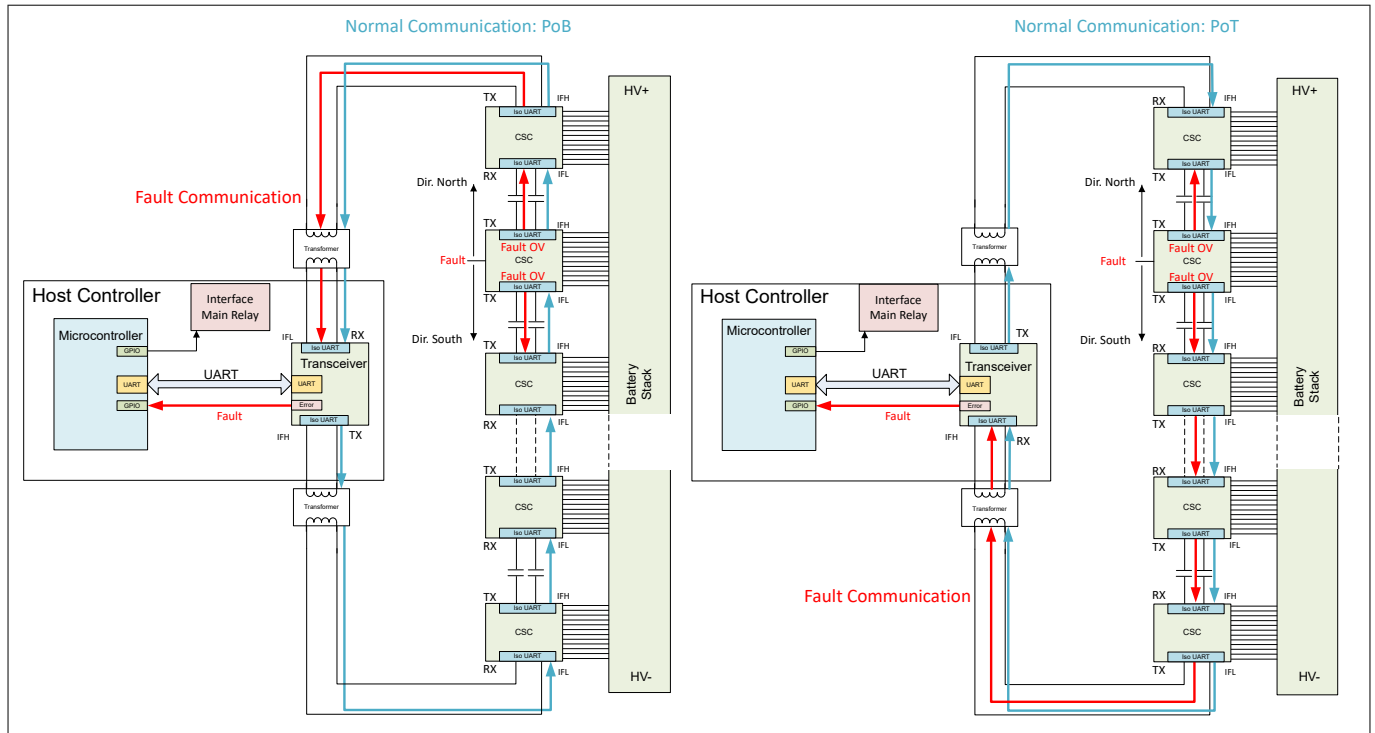
In normal operation, the communication mode (PoT or PoB) is already defined and the contiguous device shows either a TX or RX interface. In case of EMM, the contiguous device showing a TX interface does not forward the EMM signal. Therefore, the EMM signal follows the path that shows the RX interface back to the microcontroller.

**18 Emergency mode (EMM) and ERR pin (ERR)**



**Figure 31**      **EMM in normal mode**

## 18 Emergency mode (EMM) and ERR pin (ERR)



**Figure 32 EMM propagation in normal mode**

The device which sends the EMM signal transmits it for  $n_{EMM}$  periods. For a receiving device, the number of periods to detect and forward an EMM signal is depending on the operation mode:

1. Idle mode:  $n_{EMM\_dect}$
2. Straight after wake-up:  $n_{EMM\_dect\_wake-up}$

### ERR pin:

The IC's ERR pin default state is "low" and it is pulled down using the external pull-down resistor  $R_{ERR\_PD}$ . If the device detects an error, it switches the ERR pin to VS until the following actions are performed:

- The microcontroller clears the fault which triggered the ERR signal.
- The IC enters sleep mode.

### ERR pin in open drain mode (Default setting after POR):

Alternatively, the ERR pin can be configured to act as an open drain output. The default state of the ERR pin in open drain mode is "high" and the pin is pulled high by the pull-up resistor  $R_{ERR\_PU}$ . If the device detects an error, it switches the ERR pin to GND until the following actions are performed:

- The microcontroller clears the fault which triggered the ERR signal.
- The IC enters sleep mode.

If a fault which activates the ERR pin is detected during a round robin, the IC will remain in normal mode until the watchdog counter expires. If no trigger for the watchdog is received, this will happen after  $t_{WD\_max}$ .

### EMM / ERR triggers:

The following faults can trigger the EMM mode and/or the ERR pin, depending on which configuration is set in the FAULT\_MASK\_CFG

- Over- or undervoltage of a cell
- External NTC resistance measurement fault
- Open-load diagnostics error for all voltage sensing and balancing pin(s).
- Balancing overcurrent and undercurrent error
- ADC cross-check error
- Internal overtemperature detected

## 18 Emergency mode (EMM) and ERR pin (ERR)

- Register EDC check fault detected
- Sum of PCVM vs. BVM mismatch error
- PCVM vs. SCVM mismatch error
- NTC Temp increase error (during RR sleep mode)
- Internal Temperature delta error (mismatch in internal temperature measurements detected)
- Internal IC error

The following faults can only trigger the EMM mode:

- Logic high level at pin Ext\_WU
- Pulse check

### EMM / ERR masking:

The ERR pin and EMM mask register FAULT\_MASK\_CFG can be used to inhibit individual faults from generating an emergency signal (EMM) emission or an ERR pin reaction.

## 18.2 Electrical characteristics emergency mode (EMM) and ERR pin (ERR)

**Table 21** Electrical characteristics

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Emergency mode EMM							
EMM signal frequency	$f_{\text{EMM}}$	48	50	52	kHz	–	PRQ-452
EMM number of periods to detect EMM signal - wake-up by EMM	$n_{\text{EMM\_dect\_wake-up}}$	4	–	–	periods	<ul style="list-style-type: none"><li>Wake-up due to the EMM signal</li><li>During forwarding of the wake-up signal</li></ul>	PRQ-453
EMM number of periods to detect EMM signal - idle mode	$n_{\text{EMM\_dect}}$	16	–	–	periods	<ul style="list-style-type: none"><li>IC is in idle mode and not enumerated (ID = 0)</li><li>Enumerated IC forwards the signal after 0 periods</li></ul>	PRQ-455
Transmitted EMM signal periods	$n_{\text{EMM}}$	62	–	64	periods	–	PRQ-457
ERR pin function							
ERR fault indication voltage	$V_{\text{ERR}}$	$V_{\text{VS}} - 0.25\text{ V}$	–	$V_{\text{VS}}$	V	$I_{\text{ERR}} \leq I_{\text{ERR\_max}}$	PRQ-458
ERR fault indication voltage open drain	$V_{\text{ERR\_OD}}$	0	–	0.3	V	$I_{\text{ERR}} \leq 1.2\text{ mA}$	PRQ-616
ERR sink/source current	$I_{\text{ERR}}$	-1.2	–	1.2	mA	Current capacity of pin additionally to $R_{\text{ERR\_PU}}/R_{\text{ERR\_PD}}$ (= 100 kΩ) current	PRQ-459

(table continues...)

**18 Emergency mode (EMM) and ERR pin (ERR)**

**Table 21** (continued) **Electrical characteristics**

$V_{VS} = V_{VS\_functional}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERR external pull-down resistor	$R_{ERR\_PD}$	70	100	–	k $\Omega$	External pull-down resistor	PRQ-460
ERR external pull-up resistor	$R_{ERR\_PU}$	70	100	–	k $\Omega$	–	PRQ-689

## **19 Advanced Calibration**

### **19.1 Functional description**

The device is able to measure the mechanical stress which it is encountering and uses this information to digitally compensate error impact if desired.

The digital compensation mechanism is enabled by default and can be deactivated by setting the STRESS\_COMP\_DIS bit in the OP\_MODE register.

The correction value of the PCVM can be read by accessing the STRESS\_PCVM register. The correction value of the other voltage measurements can be read by accessing the STRESS\_AUX register.

The mechanical stress on the device is measured during every RR execution. Setting the automatic calibration bit AUTO\_CALIB in the miscellaneous control register starts a 14 Bit initialization measurement which overwrites the compensation data after  $t_{\text{Sensor\_init}}$  has passed.

### **19.2 Electrical characteristics advanced calibration**

**Table 22 Electrical characteristics**

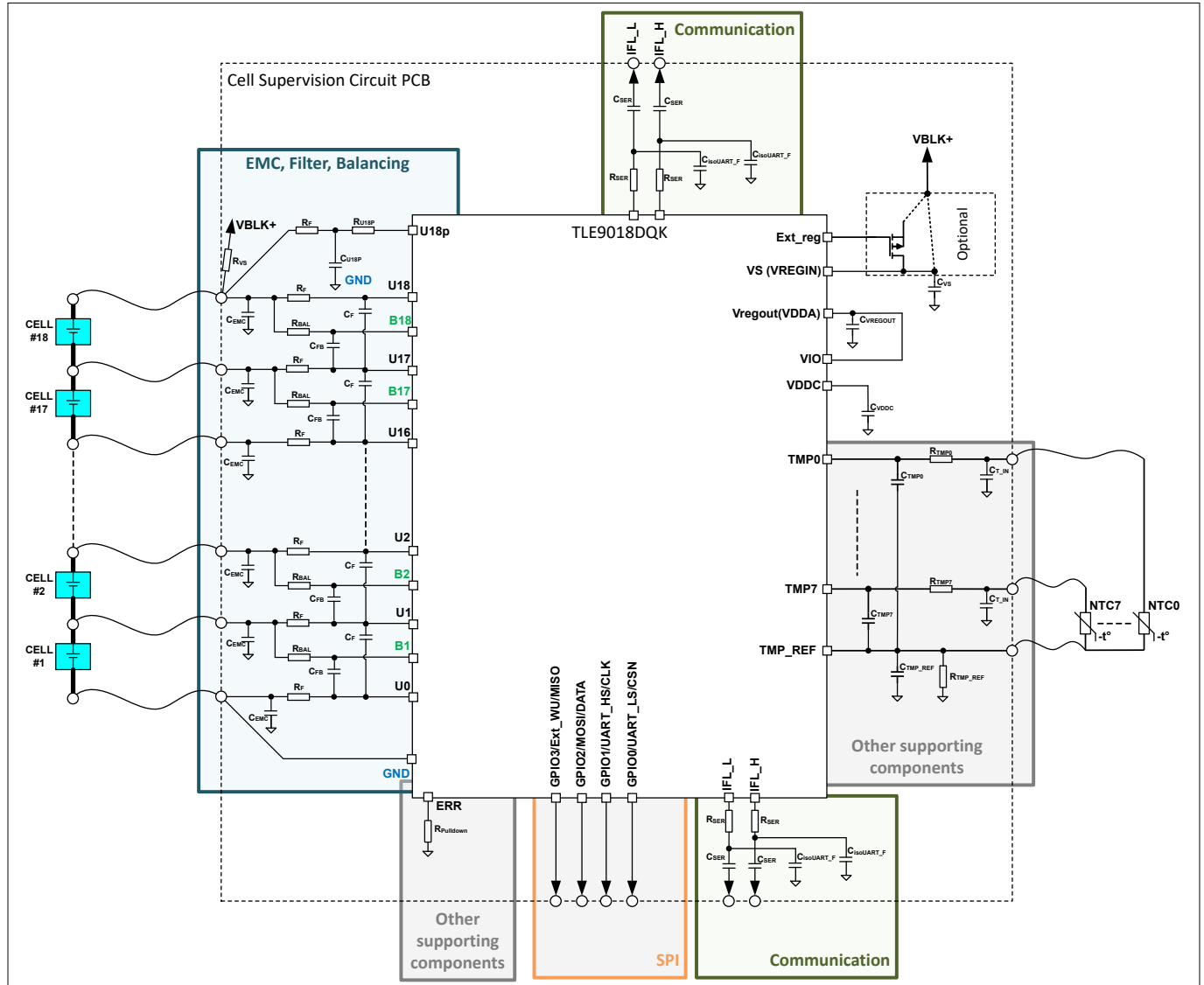
$V_{\text{VS}} = V_{\text{VS\_functional}}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Stress sensor compensation							
Stress sensor initialization	$t_{\text{Sensor\_init}}$	–	4.75	4.95	ms	–	PRQ-595



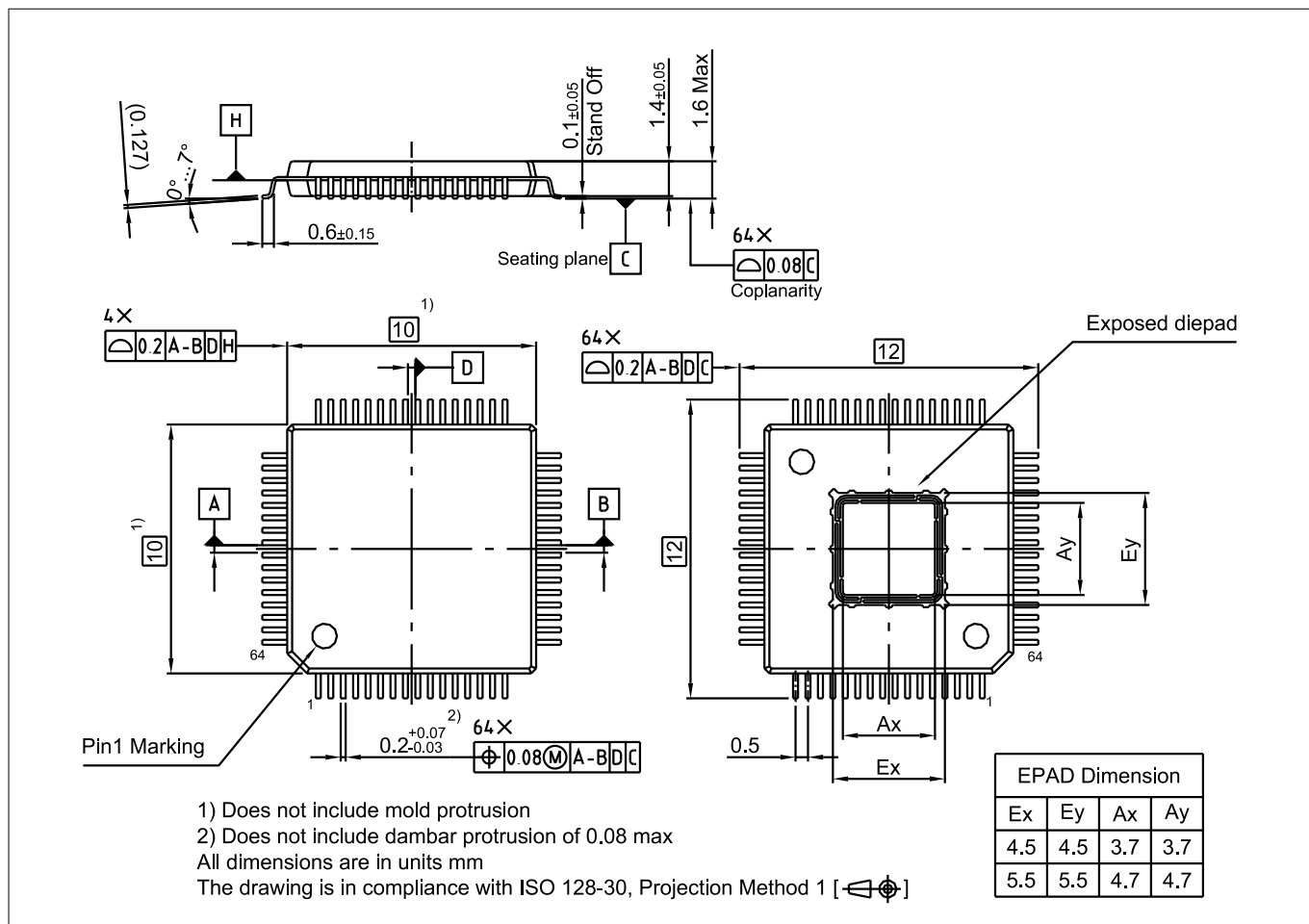
## 20 Application information

### 20.1 Typical application diagram



**Figure 33** Typical application diagram

## 21 Package information



**Figure 34 PG-LQFP-64**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Information on packages

For more information on packages, such as recommendations on assembly, refer to [www.infineon.com/packages](http://www.infineon.com/packages).

**22 Revision history**

**22 Revision history**

1.00	2025-05-19	• Initial Release
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**Email:** [erratum@infineon.com](mailto:erratum@infineon.com)

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