DSO16-300mil magnetic current sensor

Features

RoHS

AEC Qualified

ISO 26262 compliant

The TLI4971/TLE4971 is a highly accurate coreless magnetic current sensor in a 300mil wide body allowing high isolation voltages.

A differential measurement principle allows effective stray field suppression.

Additionally, two separate interface pins (OCD) provide a fast output signal in case a current exceeds a pre-set threshold.

The TLI4971/TLE4971 is a high-precision analog current sensor with measurement range up to ±65A.

Superior ±0.35% sensitivity error & ±65mA offset error

The sensor is based on Infineon's well-established and robust Hall technology.

The internal EEPROM allows the customer to program several output characteristics.

The TLI4971/TLE4971 is based on a digital assisted analog concept. While the high bandwidth current sensing signal is processed in an analog way, the proprietary stress and temperature compensation information is processed in a digital manner and combined with the main signal path within a high performance operational amplifier.

The sensor is provided in a DSO16-300mil widebody SMD package.

Potential applications

The TLI4971/TLE4971 is suitable for AC as well as DC current measurement applications:

- Electrical drives
- Current monitoring
- On Board Charger
- Auxilary Drives
- Inverters
- Over current detection
- etc.

Product validation

Product validation according to AEC-Q100, Grade 0. Qualified for automotive applications.

Description

Product type	Product Type	Package	Marking	Ordering code
TLI4971-A050W2-U-S0001	50A range, UL-certified	PG-DSO-16-50	H71I2AOW01	SP005989457
TLI4971-A040W2-U-S0001	40A range, UL-certified	PG-DSO-16-50	H71I3AOW01	SP005989452
TLI4971-A035W2-U-S0001	35A range, UL-certified	PG-DSO-16-50	H71I4AOW01	SP005990095
TLI4971-A030W2-U-S0001	30A range, UL-certified	PG-DSO-16-50	H71I5AOW01	SP005989438
TLI4971-A020W2-U-S0001	20A range, UL-certified	PG-DSO-16-50	H71I7AOW01	SP005989434
TLI4971-A016W2-U-S0001	16A range, UL-certified	PG-DSO-16-50	H71I8AOW01	SP005989426
TLE4971-A050W2-S0001	50A range, ASIL-B	PG-DSO-16-50	H71E2AIW01	SP005989410

Product type	Product Type	Package	Marking	Ordering code
TLE4971-A040W2-S0001	40A range, ASIL-B	PG-DSO-16-50	H71E3AIW01	SP005989402
TLE4971-A035W2-S0001	35A range, ASIL-B	PG-DSO-16-50	H71E4AIW01	SP005990087
TLE4971-A030W2-S0001	30A range, ASIL-B	PG-DSO-16-50	H71E5AIW01	SP005989387
TLE4971-A020W2-S0001	20A range, ASIL-B	PG-DSO-16-50	H71E7AIW01	SP005989374
TLE4971-A016W2-S0001	16A range, ASIL-B	PG-DSO-16-50	H71E8AIW01	SP005989353

All devices come in Semi Differential Output configuration and ratiometricity switched off.

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1 Functional block diagram

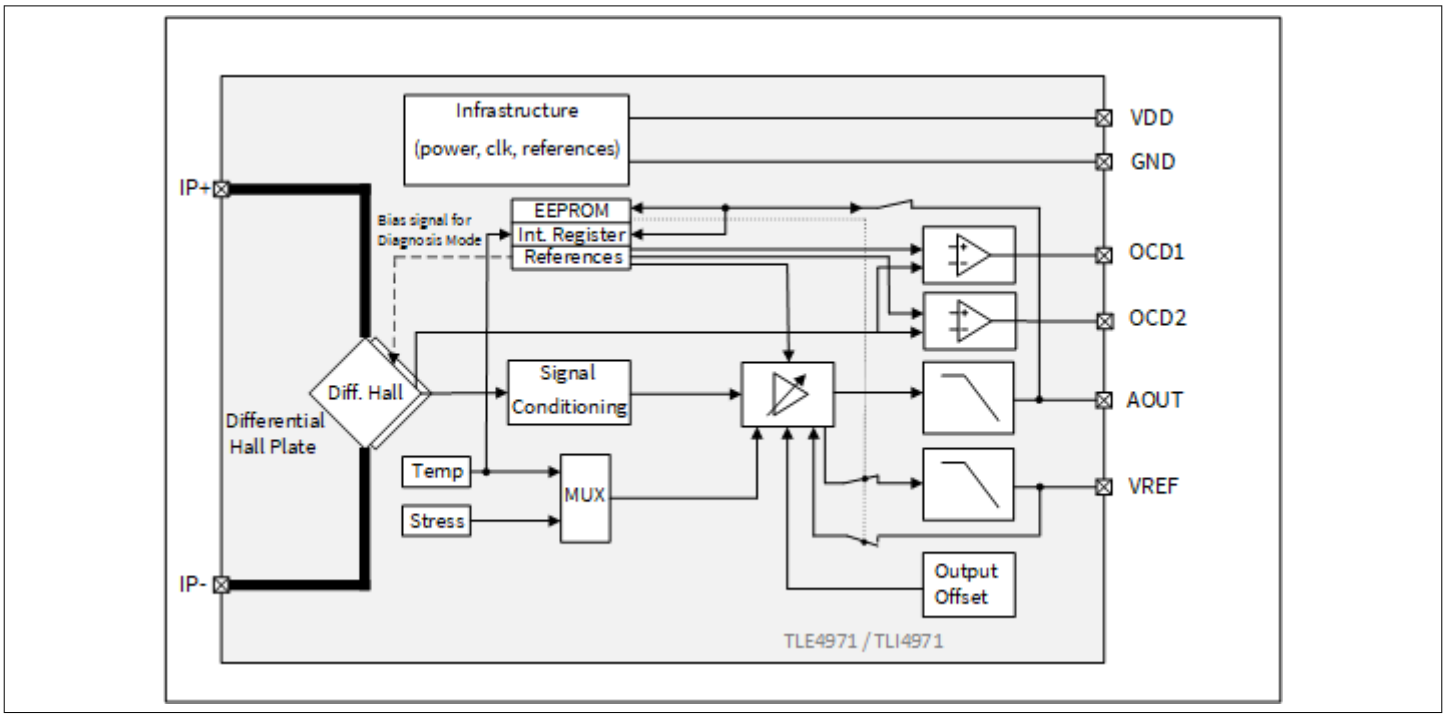

Figure 1 Functional Block Diagram

The current flowing through the current rail on the primary side induces a magnetic field that is measured by two Hall probes differentially. Depending on the selected programming option, the analog output signal can be provided either as

- Single ended,
- Fully differential,
- Semi-differential.

In single ended mode, the pin VREF is used as a reference voltage input; the analog output signal is provided on pin AOUT.

In fully differential mode, both AOUT (positive polarity) and VREF (negative polarity) are used as signal outputs whereas VDD is used as reference voltage input. Compared to the single ended mode, the fully differential mode enables doubling of the output voltage swing.

In semi differential mode a chip-internal reference voltage is used and provided on VREF (output). The current sensing information is provided in a single-ended way on AOUT.

For fast over current detection, the raw analog signal provided by the Hall probes is fed into comparators with programmable switching thresholds.

A user-programmable de-glitch filter is implemented to enable the suppression of fast switching transients.

The open-drain outputs of the OCD pins are active low and they can be directly combined into a wired-AND configuration on board level to have a general over-current detection signal.

All user-programmable parameters such as OCD thresholds, blanking times and output configuration mode are stored in an embedded EEPROM memory.

2 Pin configuration

Figure 2 Picture of TLx4971 in DSO16-300mil

Table 1 Pin definitions and functions

Pin No.	Symbol	Function	Comment
1-4	IP+	Positive current terminal pin	Current-in
5-8	IP-	Negative current terminal pin	Current-out
9	NC	Not Connected	Open
10	VDD	Supply voltage	–
11	GND	Ground	–
12	VREF	Reference voltage input or output	–
13	AOUT	Analog output	–
14	OCD1	Over Current Detection output #1	Open drain output, short to GND if not used
15	OCD2	Over Current Detection output #2	Open drain output, short to GND if not used
16	NC	Not Connected	Open

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage maximum ratings	V_{DD}	-0.3	-	+3.6	V	-
Supply voltage maximum ratings - extension for limited time	Vdd_{max}	-	-	6.5	V	Shall withstand mentioned voltage for mentioned time without damage. Duration < 1 minute
Voltage on Interface pin OCD2	V_{IO_OCD2}	-0.3	-	+21	V	-
Primary Current	I_{PN}	-32	-	+32	A	-
Primary Current	I_{PNS}	-	-	250	A	Single peak for 10 µs, 10 assertions per lifetime
Primary Surge Current	I_{PNS}	-10	-	+10	kA	At Ta = 25 °C Single peak for 8/20 µs, 1 assertion per lifetime, used standard is IEC 61000-4-5: Surge: Pulse (Short Circuit)
Junction Temperature maximum ratings	T_{j_max}	-	-	+165	°C	-
Storage Temperature	T_{A_STORE}	-40	-	+150	°C	-
Absolute Magnetic field	-	-	-	0.5	T	-
ESD voltage HBM	V_{ESD_HBM} [1)]	-	-	±2	kV	Human Body Model (HBM), according to standard AEC-Q100-002
ESD voltage CDM	V_{ESD_CDM} [1)]	-	-	±0.5	kV	Charged Device Model (CDM), according to AEC - Q100-011
Voltage on interface pins VREF, OCD1, AOUT	V_{IO}	-0.3	-	VDD + 0.3	V	-

1) According to standard IEC 61000−4−2 Electrostatic discharge immunity test

Attention: Stresses above the limit values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Attention**: **Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the section "functional range" is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions the voltage on VDD pins with respect to ground shall not exceed the values defined by the absolute maximum ratings. Lifetime statements are an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. Lifetime statements shall in no event extend the agreed warranty period.

3.2 Functional range

V_{DD} = 3.3 V; T_S = Temperature at soldering point = -40°C ... +150°C; (unless otherwise specified).

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Operating Supply voltage	V_{DD}	3.1	-	3.5	V	-
Ambient temperature at soldering point - automotive	T_s	-40	-	+150	°C	Measured at solder point (heating from primary current included); duration according automotive mission profile specified in Temperature mission profile
Ambient temperature at soldering point - OBC (Onboard Charger)	T_s	-40	-	+105	°C	Measured at solder point (heating from primary current included); 8 years of operation at maximum allowed T_s for OBC use-case: 32A continuous current;
Reference Input Voltage	V_{REF_nom}	-	1.65	-	V	in single ended mode, default value; allowed values: 1.5V, 1.65V, 1.8V. The chosen nominal value has to be programmed in EEPROM.
Reference Input Voltage Variation	VREF_var	-10	-	+10	%	in single ended mode
Capacitance on Analog Output Pin	C_O	4.7	6.8	8	nF	w/o decoupling resistor; including parasitic cap on the board. Valid always for AOUT, also for VREF in semi or fully differential modes.

The requirements contained in this folder are valid as conditions for all the other requirements, unless otherwise specified.

These conditions are not explicitly repeated in all the requirements.

3.3 Functional Output

In single ended mode the device receives a reference voltage on the VREF pin and provides a single ended output on the AOUT pin. The quiescient voltage at the AOUT pin (output at zero input conditions) is equal to the reference voltage.

The output sensitivity shall be programmable and ratiometric with respect to the reference voltage applied on VREF pin as defined in the following formulas, if the single ended mode is selected and if the sensitivity ratio-metricity is enabled.

$$S\left(Vref\right) = S\left(Vref_{NOM}\right) \times \left[1 + \frac{(Vref - Vref_{NOM}) \times K_S}{Vref_{NOM}}\right] \quad (1)$$

The proportionality between the sensitivity *S* and the reference voltage *Vref* is defined with the sensitivity ratiometry factor (K_S).

Note:

Since the ratiometry factor K_S nominal value is 1 the formula becomes:

$$S\left(Vref\right) = S\left(Vref_{NOM}\right) \times \frac{Vref}{Vref_{NOM}} \quad (2)$$

The possible nominal values of VREF are indicated in the output characteristics table.

The possible programmable nominal values of the sensitivity (*S*) when *Vref* is equal to the nominal value, are indicated in the output characteristics table.

If the sensitivity ratio-metricity is not enabled the sensitivity is always equal to the nominal value independently from the value of *Vref*

Maximum deviation from the nominal value is also indicated in the output characteristics table as Sensitivity error (ESENS)

In fully differential mode the devices provides a differential output on the AOUT and VREF pins. For instance at zero input, both AOUT and VREF nominally provide a voltage level at VDD/2.

In this case the chip internal reference voltage is derived from the supply pins VDD and GND.

Compared to the Single Ended Output mode, the available voltage swing at the output is doubled.

The nominal quiescent voltage value at the two pins AOUT (V_{QAOUT}), VREF (V_{QVREF}) shall be programmable at 2 different values, if the fully differential mode is selected.

It shall be ratiometric with respect to VDD as defined in the following formulas, when the nominal quiescent voltage is 1.65 and the offset ratiometricity is enabled.

In this case the quiescent voltages can be expressed as follows to show the dependency from the actual VDD value:

$$V_{QAOUT}\left(VDD\right) = V_{QVREF}\left(VDD\right) = V_{QAOUT}\left(3.3V\right) \times \left[1 + \frac{(VDD - 3.3V) \times K_{OQ}}{3.3V}\right] \quad (3)$$

Note:

Since nominal value of the ratiometric factor K_{OQ} is 1 and nominal value of V_{QAOUT}(3.3 V) is 3.3 V / 2 = 1.65 V, the formula becomes:

$$V_{QAOUT}\left(VDD\right) = V_{QVREF}\left(VDD\right) = \frac{VDD}{2} \quad (4)$$

The output sensitivity shall be programmable and ratiometric with respect to VDD, according to the following formula, if fully differential mode is selected and if the sensitivity ratio-metricity is enabled.

$$S\left(VDD\right),diff = S\left(3.3V\right),diff \times \left[1 + \frac{(VDD - 3.3V) \times K_S}{3.3V}\right] \quad (5)$$

Note:
Since the nominal value of the ratiometric factor is 1 the formula simplifies as follows:

$$S\left(VDD\right),diff = S\left(3.3V\right),diff \times \frac{VDD}{3.3V} \quad (6)$$

The possible programmable nominal values of the sensitivity when *Vref* is equal to 3.3 V, *S(3.3 V)* are indicated in the output characteristics table (considering the differential output voltage, for the fully differential mode the values are double with respect to the ones referred to single ended mode).

If the sensitivity ratio-metricity is not enabled, the sensitivity will always be equal to the nominal value, independently from VDD.

Maximum deviation from the nominal value is also indicated in the output characteristics table as Sensitivity error (ESENS).

The semi-differential output mode provides a single-ended output signal on AOUT pin, and also provides the chip-internal reference as an output on the VREF pin. This mode does not require the application to provide a precise reference voltage to the device

The Quiescent Voltage V_{OQ} shall be programmable at 3 different values when the semi-differential output mode is selected.

Note:
The Quiescient voltage on AOUT is nominally equal to the internal reference voltage that is provided as an output on VREF pin.

For the applications in which the current to be measured is bidirectional the Quiescent Voltage will be set to a value in the middle of the voltage range or at 1.5V (V_{OQbid}), whereas when the direction of the current is already known by the application, the Quiescent Voltage can be set to a lower value (V_{OQuni}) in order to better exploit the full voltage range.

The nominal values of the quiescent voltage corresponding to the different programming options are indicated in the output characteristics table.

Maximum deviation from the nominal value is indicated in the output characteristic table as output offset (EOFF)

The output sensitivity shall be programmable and ratiometric with respect to VDD, according to the same formula specified for the fully differential mode, if semi-differential mode is selected and if the sensitivity ratio-metricity is enabled.

4 Product features

4.1 Operating charcteristics

Table 4 Operating characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption	I_{DD}	-	18	25	mA	$I_{(AOUT)}$ = 0mA
Current consumption during programming	I_{OCD2}	-	-	10	mA	through OCD2 pin, during programming
Primary Path Resistance	R_{PN}	-	550	-	µΩ	25°C soldered on 140µm Cu
Power-On Delay time	t_{POR}	-	-	1.5	ms	VDD rising 0 V to 3.3 V. Starts when the VDD reaches the minimum allowed operating conditions and stops when the device is fully operational.
Undervoltage Threshold	U_{VLL}	-	-	2.93	V	VDD rising
Overvoltage Threshold	O_{VH}	3.55	-	-	V	-
OCD undervoltage condition	V_{DD_OCD}	1.8	-	U_{VLL}	V	OCD pulled to "low" level
Undervoltage/ Overvoltage Delay	t_{UVLOe}	1	-	3	µs	Min delay defines when the comparator shall switch in case of fast glitches on VDD is valid for triggering transition, release can be faster. Min limit is valid for a voltage drop 100mV below the threshold
Voltage on Analog Output AOUT	V_{AOUT}	-0.3	-	VDD + 0.3	V	-
Voltage on Interface pin OCD1	V_{IO}	-0.3	-	+3.5	V	-
Voltage on Interface pin OCD2	V_{IO_OCD2}	-0.3	-	+3.5	V	Voltage will be higher during EEPROM-programming mode as stated in absolute maximum ratings

4.2 Analog output characteristics

Table 5 Analog Output Characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Quiescent Output voltage	V_{OQbid}	-	1.65	-	V	I_{PN} = 0A; programmable options in fully differential or semi-differential (bidirectional) modes
Analog Output drive capability	I_O	-2	-	+2	mA	DC current
Analog Output Saturation Voltage, Source	V_{CLH}	-	-	300	mV	V_{DD}-V_O; Output current source = 2 mA
Analog Output Saturation Voltage, Sink	V_{CLL}	-	-	300	mV	Ouput current sink = 2 mA
Transfer function cutoff frequency	BW	120	210	-	kHz	-3dB criterion, $C_{(AOUT)}$ = 6.8nF
Output phase delay	φ_{delay}	-	43.2	60.5	°	f_{signal} = 120KHz
Output group delay	φ_{G_DELAY}	-	1	1.4	µs	-
Output group delay variation	$\varphi_{G\_DELAY\_VAR}$	-20	-	+20	%	Over temperature and lifetime
External Homogeneous magnetic field suppression	B_{SR}	34	40	-	dB	Frequency up to 4kHz.
Sensitivity, Range S1	S1 [1)]	-	18.7	-	mV/A	±64A FS
Sensitivity, Range S2	S2 [1)]	-	23.4	-	mV/A	±51A FS
Sensitivity, Range S3	S3 [1)]	-	30.4	-	mV/A	±39A FS
Sensitivity, Range S4	S4 [1)]	-	35.1	-	mV/A	±34A FS
Sensitivity, Range S5	S5 [1)]	-	39.8	-	mV/A	±30A FS
Sensitivity, Range S6	S6 [1)]	-	49.1	-	mV/A	±24A FS
Sensitivity, Range S7	S7 [1)]	-	60.9	-	mV/A	±20A FS

(table continues...)

Table 5 (continued) Analog Output Characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sensitivity, Range S8	S8 [1]	-	76.4	-	mV/A	±16A FS
Output Noise density	I_{NOISE} [2]	-	300	581	uA/√Hz	Referenced to input differential magnetic field. Typical value is at 25°C, FD mode, S7 range. Max value is over all modes, for Tj < 125°C.

1) Values refer to semi-differential mode or single-ended mode, with V_{REF} = 1.65 V. In fully differential mode the sensitivity value is doubled.
2) Noise density = Output_noise_rms / SQRT(PI() / 2 * BW)

Table 6 Accuracy, All ranges S1 till S8 (±65A till ±16A)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nonlinearity Error	Lin_{Err}	-	0.1	-	%	V_{out} = 0.3V to V_{dd}-0.3V
Sensitivity error	E_{SENS}	-0.65	±0.35	+0.65	%	@ T_s = 25ºC
Sensitivity error over temperature	E_{SENST}	-0.80	±0.45	+0.80	%	At 0h
Sensitivity error over temperature and lifetime	E_{SENSL} [1]	-1.00	±0.65	+1.00	%	-
Output Offset	E_{OFF}	-120	±65	+120	mA	@ T_S = 25°C; 0h
Output Offset error over temperature	E_{OFF_T}	-150	±85	+150	mA	-
Output Offset error over temperature and lifetime	E_{OFF_L} [1]	-150	±105	+150	mA	-
Total error over temperature	E_{TOTT}	-0.85	±0.50	+0.85	%	Percentage of FS; includes gain and offset error
Total error over temperature and lifetime	E_{TOTL} [1]	-1.00	±0.70	+1.00	%	Percentage of FS; includes gain and offset error

1) Based on High-Temperature-Over-Lifetime test according to AEC-Q100. Min/Max values are 1ppm. Typical values are ±3 sigma.

4.3 Fast over current detection

Table 7 Fast over current detection (OCD)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OCD Load capacitance	C_L	-	-	1	nF	-
Pull-up resistor	R_{PU}	4.7	-	10	kΩ	To V_{DD}
Open-drain current	I_{OD_ON}	-	-	1	mA	DC current
OCD de-glitch filter basic time	t_{OCDgl} 1)	400	500	600	ns	-
Threshold level tolerance	I_{THT1} 1)	-10	-	+10	%	type tested

1) Not tested in production, guaranteed by design/characterization

The threshold level of the OCD1 output is programmable. Threshold level is used symmetrically for positive and negative over current events. The possible thresholds levels can be calculated with the formulas below.
For sensitivity values *S1* and *S2* the following formula applies:

$$OCD1_{THR} = ((OCD1_{CODE} \times 5.5) + 31)\,[A]$$

Figure 3

For sensitivity values between *S3* and *S7* the following formula applies:

$$OCD1_{THR} = ((OCD1_{CODE} \times 2.2) + 11)\,[A]$$

Figure 4

Where:

- $OCD1_{THR}$ is the OCD1 threshold level in [A];
- $OCD1_{CODE}$ is the decimal value of a 6 bits code. Minimum allowed value for S3 - S8 is 4.

Table 8 OCD1 thresholds *S1* and *S2*

$OCD1_{CODE}$	$OCD1_{THR}$ [A]	Notes
63	378	Maximum setting
8	75	Pre-programmed setting for *S1*
6	64	Pre-programmed setting for *S2*
0	31	Minimum setting

Table 9 OCD1 thresholds between *S3* and *S8*

$OCD1_{CODE}$	$OCD1_{THR}$ [A]	Notes
63	150	Maximum setting
17	50	Pre-programmed setting for *S3*
14	42	Pre-programmed setting for *S4*
12	37	Pre-programmed setting for *S5*
9	31	Pre-programmed setting for *S6*
6	24	Pre-programmed setting for *S7*
4	20	Pre-programmed setting for *S8*
4	20	Minimum setting

Table 10 OCD1 specific Requirements

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OCD1 response time	t_{D_OCD1} 1)	-	0.7	1	µs	I_{PN} = 2 x $I_{THR1.x}$
OCD1 fall time	t_{f_OCD1} 1)	-	100	150	ns	Falling edge level of OCDx-pin < 0.5xV_{DD}
OCD1 Response time jitter	Δt_{D_OCD1} 1)	-	-	0.11	µs	1σ, type tested, I_{PN} = 2 x $I_{THR1.x}$, input rise time 0.5 us
De-glitch filter setting	$OCD1_{gl\_mul}$	0	-	7	-	$t_{deglitch}$ = $OCD1_{gl\_mul}$*t_{OCDgl}

1) All OCD timing related requirements refer to the maximum load capacitance specified

The threshold level of the OCD2 output is programmable. Threshold level is used symmetrically for positive and negative over current events. The possible thresholds levels can be calculated with the formulas below.
For sensitivity values *S1* and *S2* the following formula applies:

$$OCD2_{THR} = ((OCD2_{CODE} \times 2.8) + 14)\ [A]$$

Figure 5

For sensitivity values between *S3* and *S8* the following formula applies:

$$OCD2_{THR} = ((OCD2_{CODE} \times 1.1) + 3.5)\ [A]$$

Figure 6

Where:

- $OCD2_{THR}$ is the OCD2 threshold level in [A];
- $OCD2_{CODE}$ is the decimal value of a 6 bits code. Minimum allowed value for S3 - S8 is 5.

Table 11 OCD1 thresholds *S1* and *S2*

$OCD2_{CODE}$	$OCD2_{THR}$ [A]	Notes
63	190	Maximum setting
14	53	Pre-programmed setting for *S1*
10	42	Pre-programmed setting for *S2*
0	14	Minimum setting

Table 12 OCD2 thresholds between *S3* and *S8*

$OCD2_{CODE}$	$OCD2_{THR}$ [A]	Notes
63	73	Maximum setting
26	32	Pre-programmed setting for *S3*
22	28	Pre-programmed setting for *S4*
19	24	Pre-programmed setting for *S5*
15	20	Pre-programmed setting for *S6*
11	15.6	Pre-programmed setting for *S7*
9	13.4	Pre-programmed setting for *S8*
5	9	Minimum setting

Table 13 OCD2 specific Requirements

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OCD2 response time	t_{D_OCD2} 1)	-	0.7	1.2	µs	I_{PN} = 2 x $I_{THR2.x}$
OCD2 fall time	t_{f_OCD2} 1)	-	200	300	ns	Falling edge level of OCD2-pin < 0.5xV_{DD}
OCD2 Response time jitter	Δt_{D_OCD2} 1)	-	-	0.11	µs	1σ, type tested, B_{rail} = 2 x $I_{THR2.x}$, input rise time 0.5 us
De-glitch filter setting	$OCD2_{gl\_mul}$	0	-	15	-	$t_{deglitch}$ = OCD_{gl_mul}*t_{OCDgl}

1) All OCD timing related requirements refer to the maximum load capacitance specified

4.4 Other functional requirements

Figure below shows the OCD output pin nominal behavior during an overcurrent event and defines important timing quantities for which the requirements are listed in the parameters table.

Overcurrent Pulse 1 is a overcurrent event, where the duration of the overcurrent condition exceeds the overcurrent response time t_{D_OCDx} + response time jitter Δt_{D_OCDx} + deglitch filter time $t_{deglitch}$. Overcurrent condition 2 and 3 is not long enough to trigger the OCD output. Pulse 2 is shorter than the overcurrent response time t_{D_OCDx} and therefore no OCD event is generated. In overcurrent condition 3, the overcurrent condition is longer than the response time t_{D_OCDx} + response time jitter Δt_{D_OCDx}, but is not exceeding the glitch filter time $t_{deglitch}$ and no OCD event is generated.

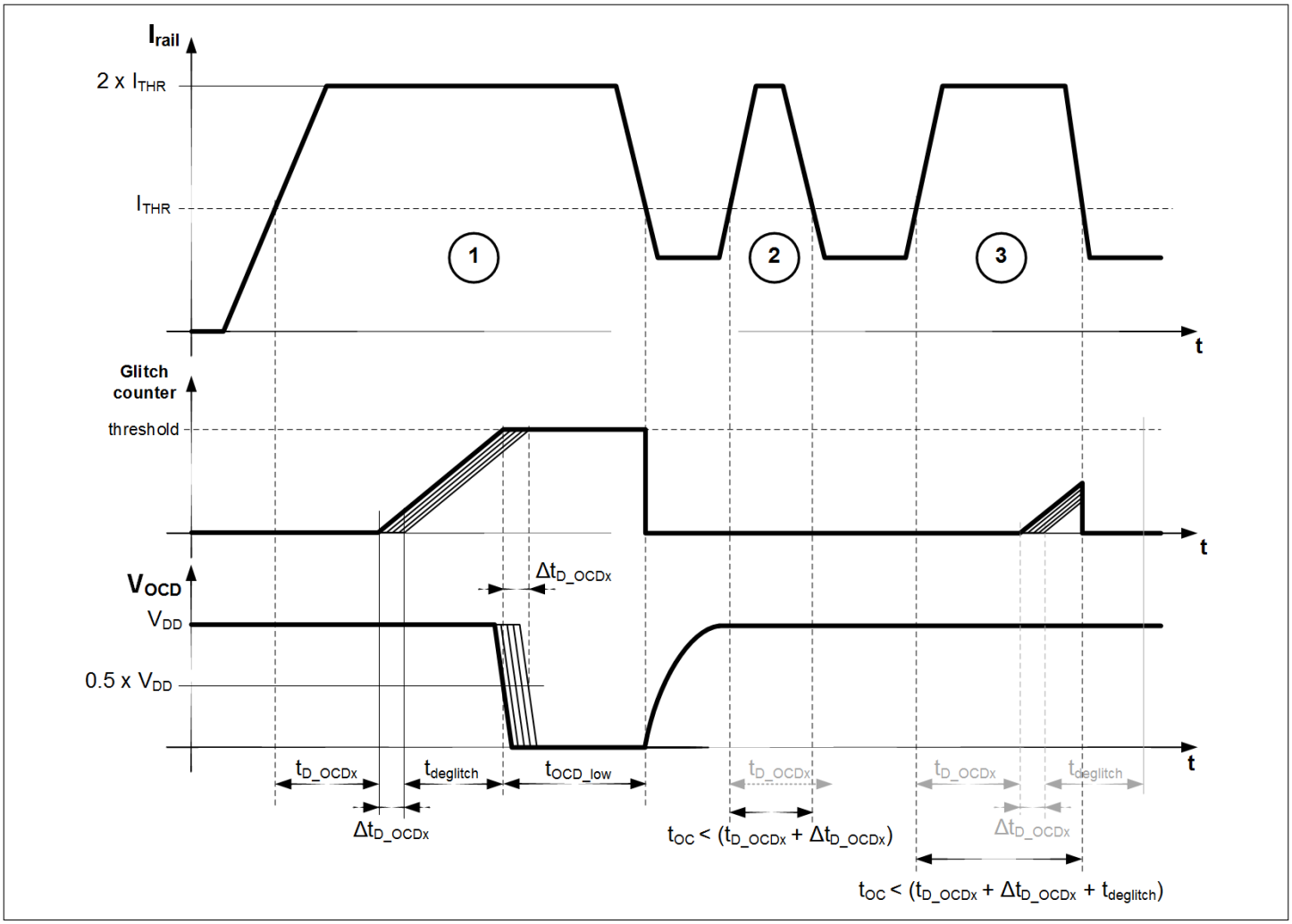

Figure 7 Fast over current detection output timing

4.4.1 Other functional requirements

The device shall activate both OCD outputs if its own voltage power supply (V_{DD}) is in an under-voltage or in an over-voltage condition.

Note:

Over-voltage condition is present if V_{DD} higher than the over-voltage threshold parameter (OV_{LOH}), whereas an under-voltage condition is present when V_{DD} is between the values indicated in the V_{DD_OCD} parameter.

5 Application information

5.1 System Integration

Application circuit with external components. In-circuit-programming not included.

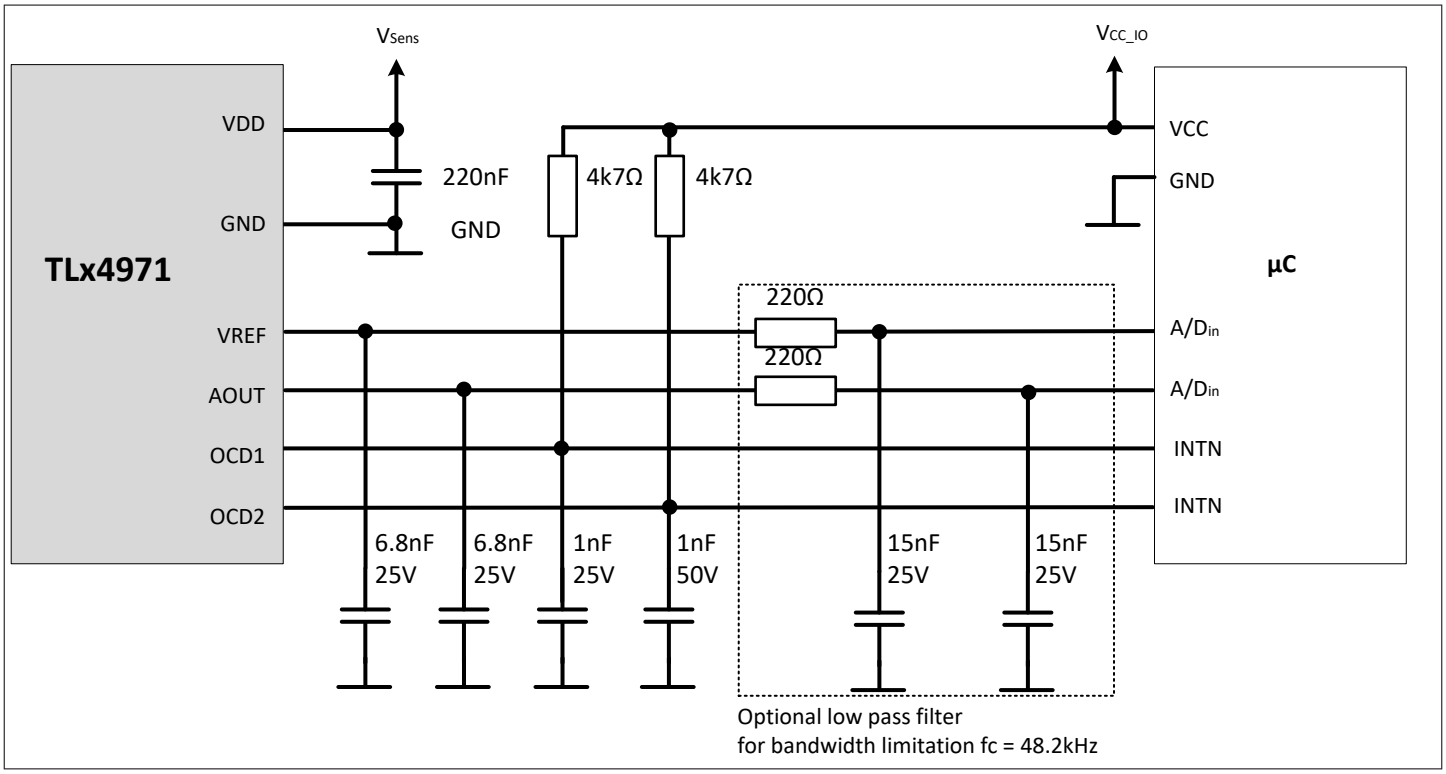

Figure 8 Application circuit with external components

For bandwidth limitation an external filter is recommended as shown in the above application circuits.

In order to protect the OCD1 pin against over voltage while programming the EEPROM, the OCD1 and OCD2 pin shall not be shorted together. Do not connect OCD2 pins from different sensors together if diagnosis mode is enabled in the EEPROM (default). If all OCD2s are tied together, the OCD2 fault indication of one sensor might unintentionally activate the diagnosis mode on the other sensors by forcing the pin to ground. Details about the diagnosis mode are provided in the safety manual of the device. If the sensor is programmed in the application, a protection circuit between OCD2 pins and GPIO pins of the microcontroller shall be implemented. Please refer to the user manual for additional details.

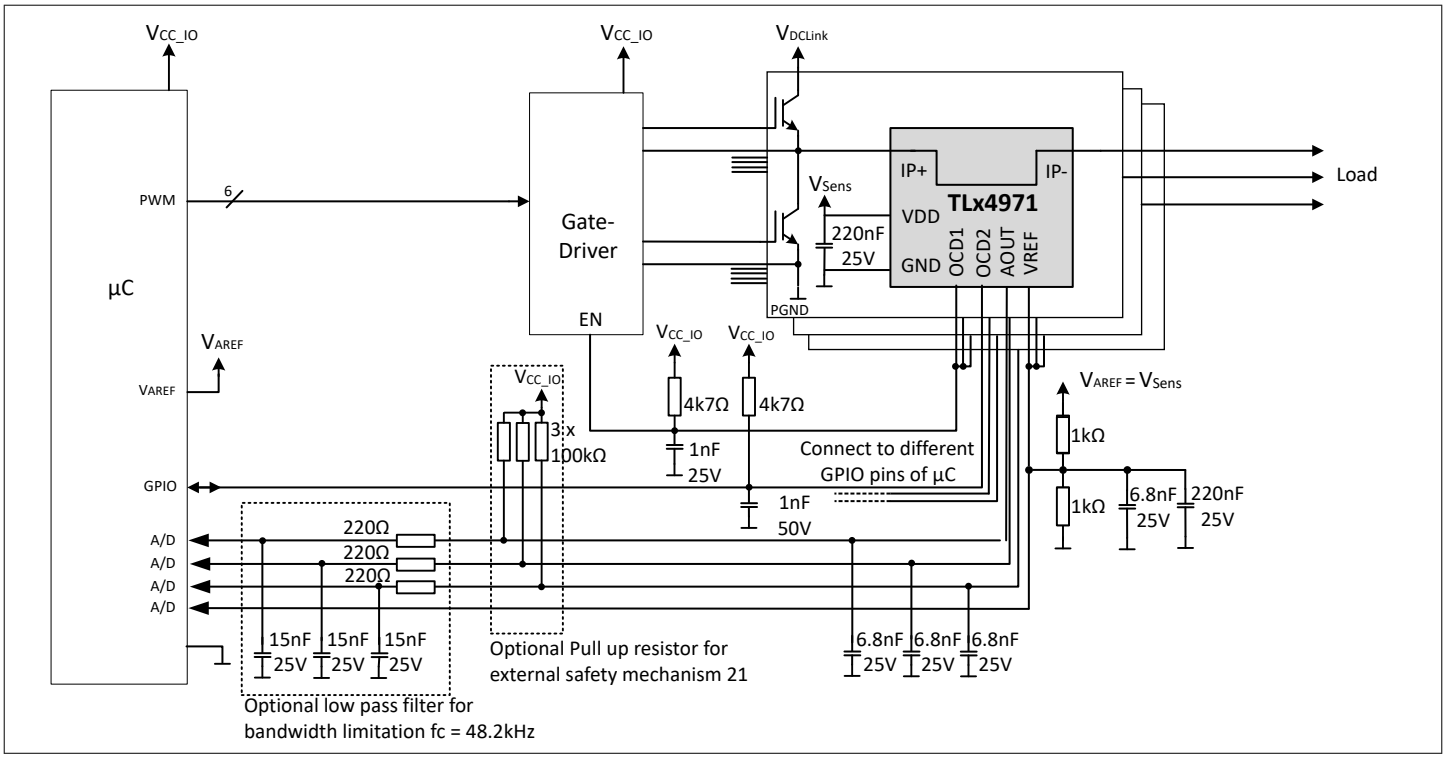

Figure 9 **Application circuit for three phase system in single ended configuration. In-circuit-programming not included.**

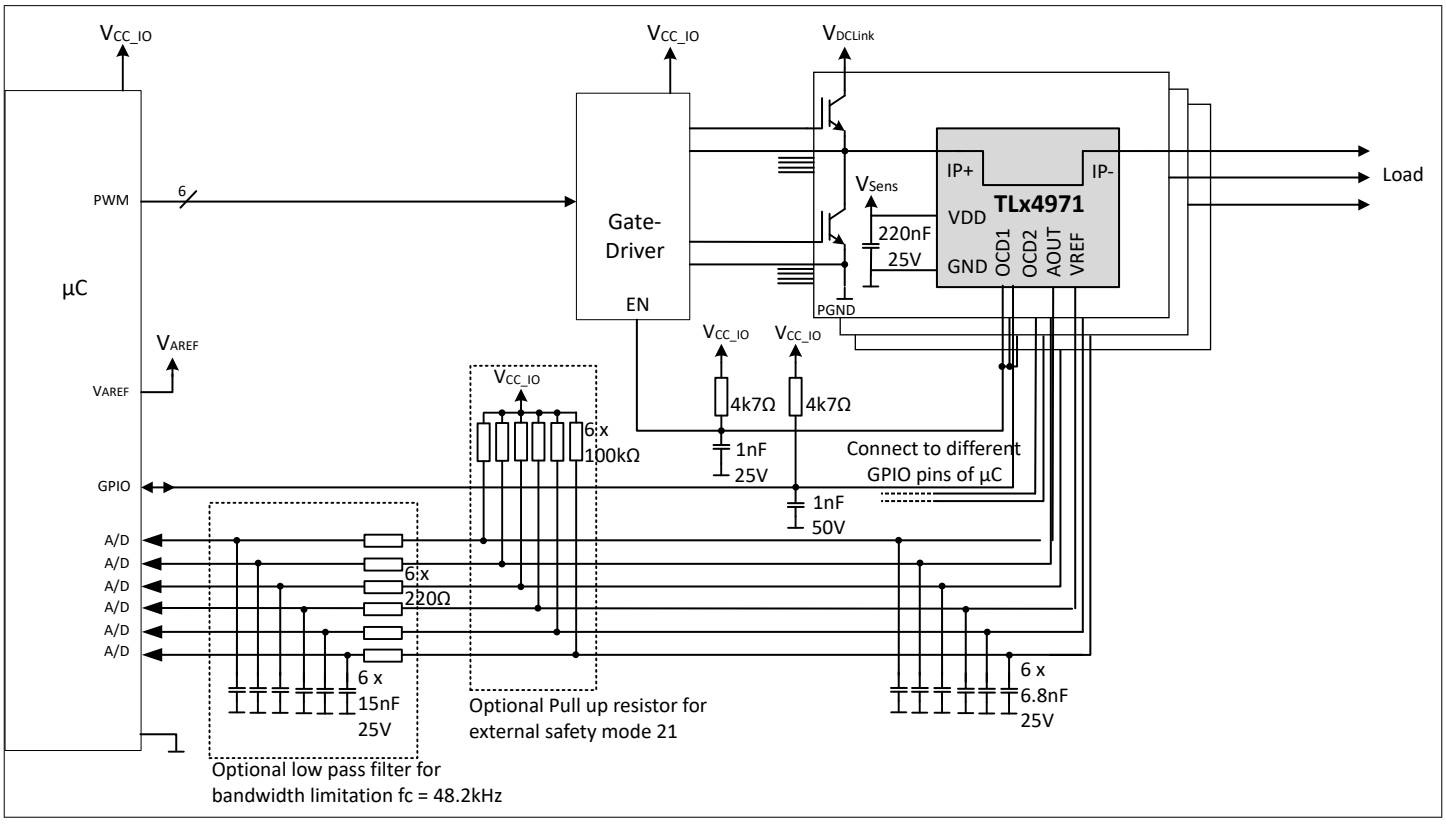

Figure 10 **Application circuit for three phase system in differential configuration. In-circuit-programming not included.**

6 Isolation Characteristics

The device is certified according to UL 1577 and to IEC62368-1.

Table 14 Isolation Characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Working voltage, Reinforced	V_{IOWM}	-	-	1060	V_{pk}	Equal to V_{DC}
Repetitive isolation voltage, Reinforced	V_{IORM}	-	-	1500	V_{pk}	Maximum approved working voltage for reinforced isolation according to IEC 62368 (edition 1).
Working voltage, Basic	V_{IOWM}	-	-	1700	V_{pk}	Equal to V_{DC}
Repetitive isolation voltage, Basic	V_{IORM}	-	-	1700	V_{pk}	Maximum approved working voltage for basic isolation according to IEC 62368 (edition 1)
Maximum rated transient isolation voltage	V_{IOTM}	-	-	6	kV_{pk}	$V_{TEST} = V_{IOTM}$ for t_{ini} = 60 s (type tests) V_{TEST} = 1.2 x V_{IOTM} for t_{ini} = 1 s
Surge capability	V_{IOSM}	-	-	8000	V_{pk}	Type tested, waveform 1.2µs/50µs, 25pulses positive followed by 25pulses negative
External clearance	CRP	8.0	8.2	-	mm	Shortest distance in air between any CR pin to any LV output pin
External creepage	CLR	8.0	8.2	-	mm	Shortest distance over package surface between any CR pin to any LV output pin
Comparative Tracking Index	CTI	600	-	-		According to DIN EN 60112 (VDE 0303-11)
Altitude	-	-	-	4000	m	-

7 Package

The device is mounted in the PG-DSO-16-50 Package.

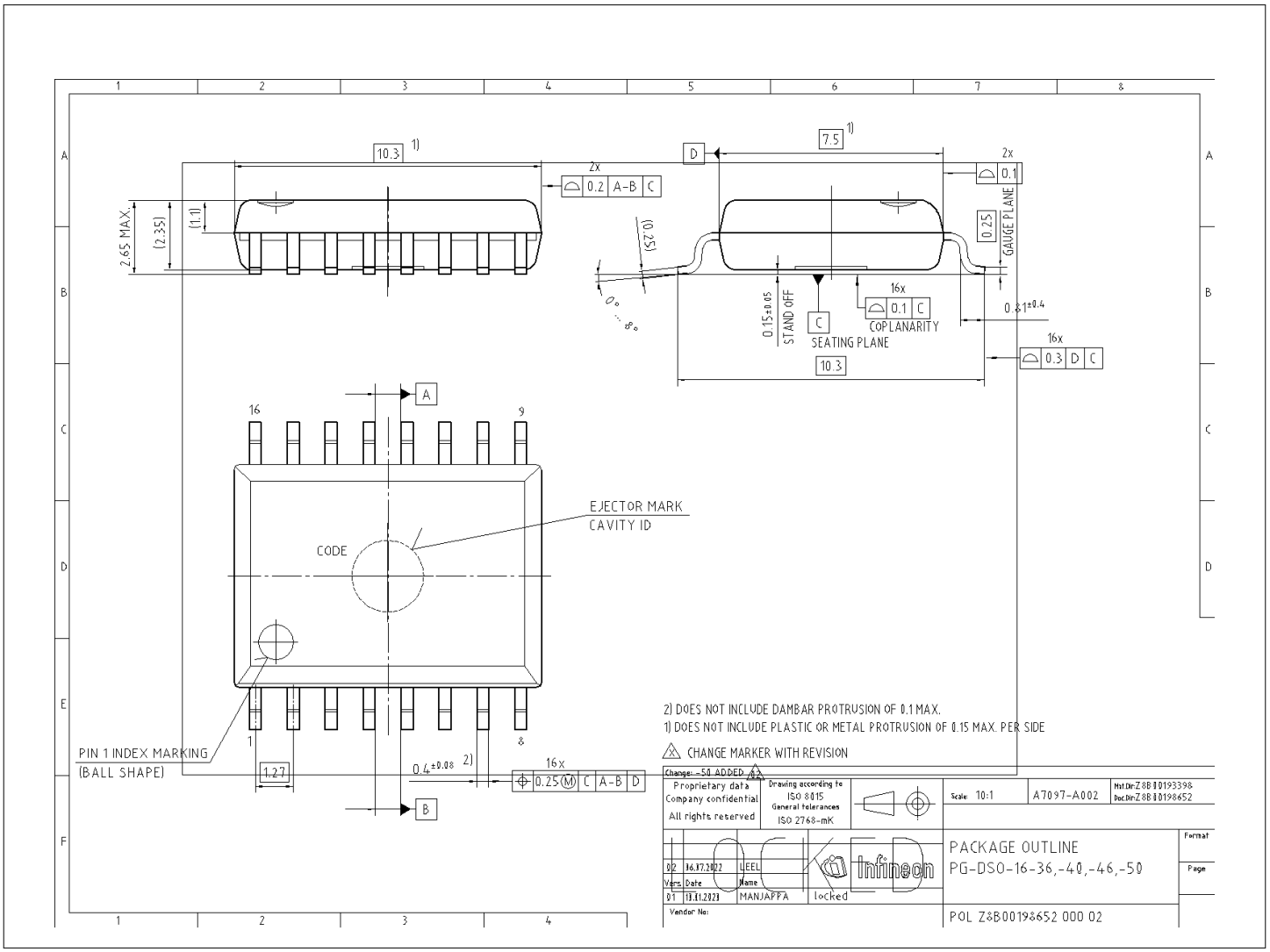

Figure 11 PG-DSO-16 package outline

Package	MSL
PG-DSO-16-50	3

The package is Halogen-free and Lead-free.

8 Revision History

Table 15 Revision History

Revision number	Date of release	Description of changes
1.0	2025-05-22	Initial version of datasheet

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