CoolGaN™ Transistor Dual 650V G5

140 mΩ / 650 V GaN half-bridge

Features

- Two 140 mΩ GaN switches in half-bridge configuration
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Kelvin source connection
- Thermally enhanced 6 x 8 mm QFN-32 package
- Qualified according to JEDEC Standard

Description

IGI65D1414A3MS combines a half-bridge power stage consisting of two 140 mΩ (typ. R_{dson}) / 650 V enhancement-mode CoolGaN™ HEMTs in a small 6 x 8 mm QFN-32 package. In the low-to-medium power area (example application in **Figure 1**), it is thus ideally suited to support the design of high-density AC/DC chargers and adapters, utilizing the superior switching behavior of CoolGaN™ HEMTs. Infineon's CoolGaN™ and related power switches provide a very robust gate structure. When driven by a continuous gate current of a few mA in the "on" state, a minimum on-resistance R_{dson} is always guaranteed.

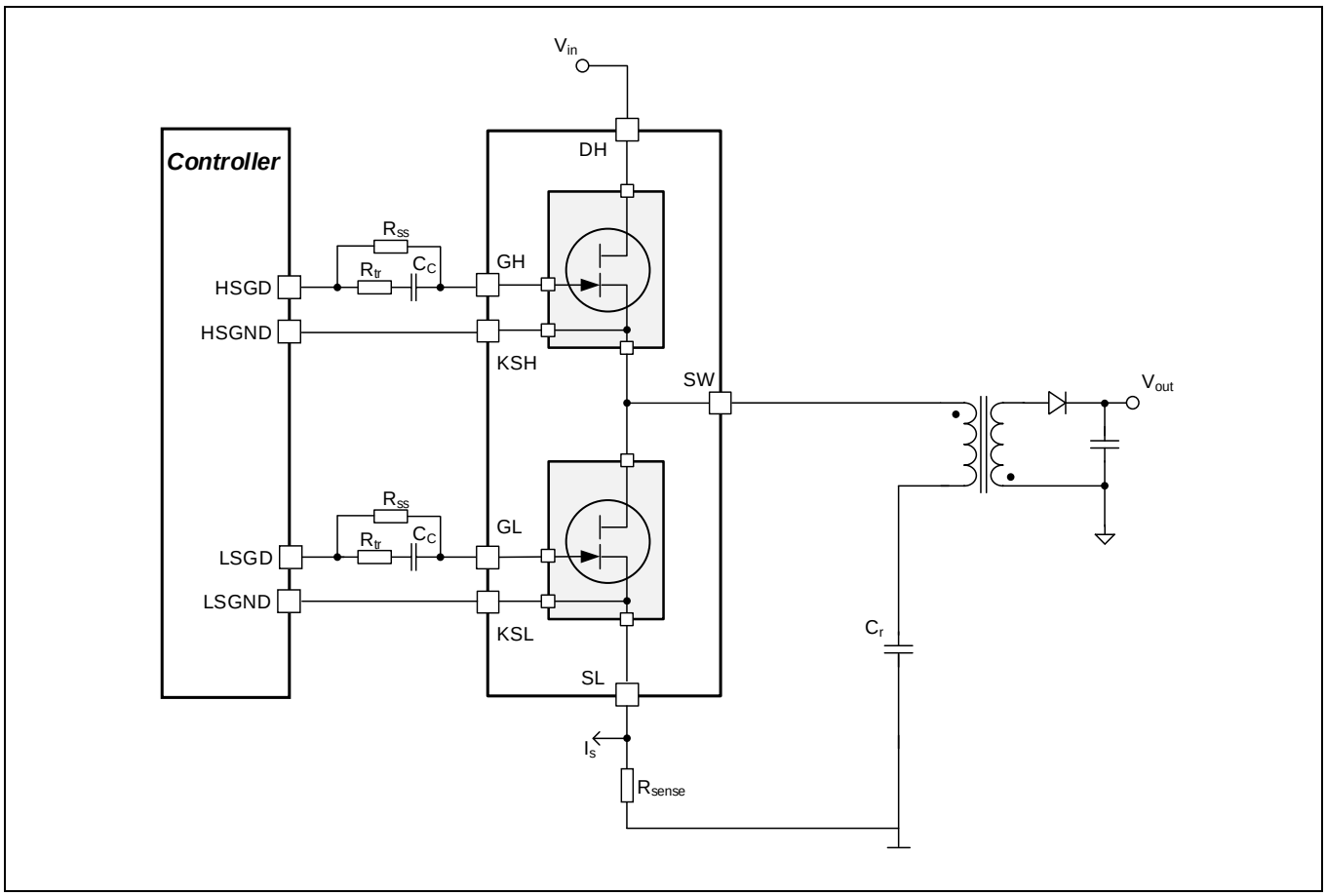

Figure 1 Typical application circuit (hybrid flyback converter)

Due to the GaN-specific low threshold voltage and the fast switching transients, a negative gate drive voltage is required in certain applications to both enable fast turn-off and avoid cross-conduction effects. This can be achieved by the well-known RC interface between driver and switch. A few external SMD resistors and capacitors enable easy adaptation to different power topologies.

Applications

- Charger and adapters
- Low-power motor drive
- LED lighting

Power Topologies

- Active clamp flyback or hybrid flyback converters
- LLC resonant converters
- Single or interleaved synchronous buck or boost converter
- Single-phase or multiphase two-level inverters

Product Versions

Table 1 CoolGaN™ integrated power stage half bridge products overview

Part Number / Ordering code	OPN	Package	Typ. R_{dson} high- / low-side	Marking
IGI65D1414A3MS	IGI65D1414A3MS XUMA1	PG-VIQFN-32-1 6 x 8 mm	140 mΩ / 140 mΩ	65D1414A

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1 Pin configuration and description

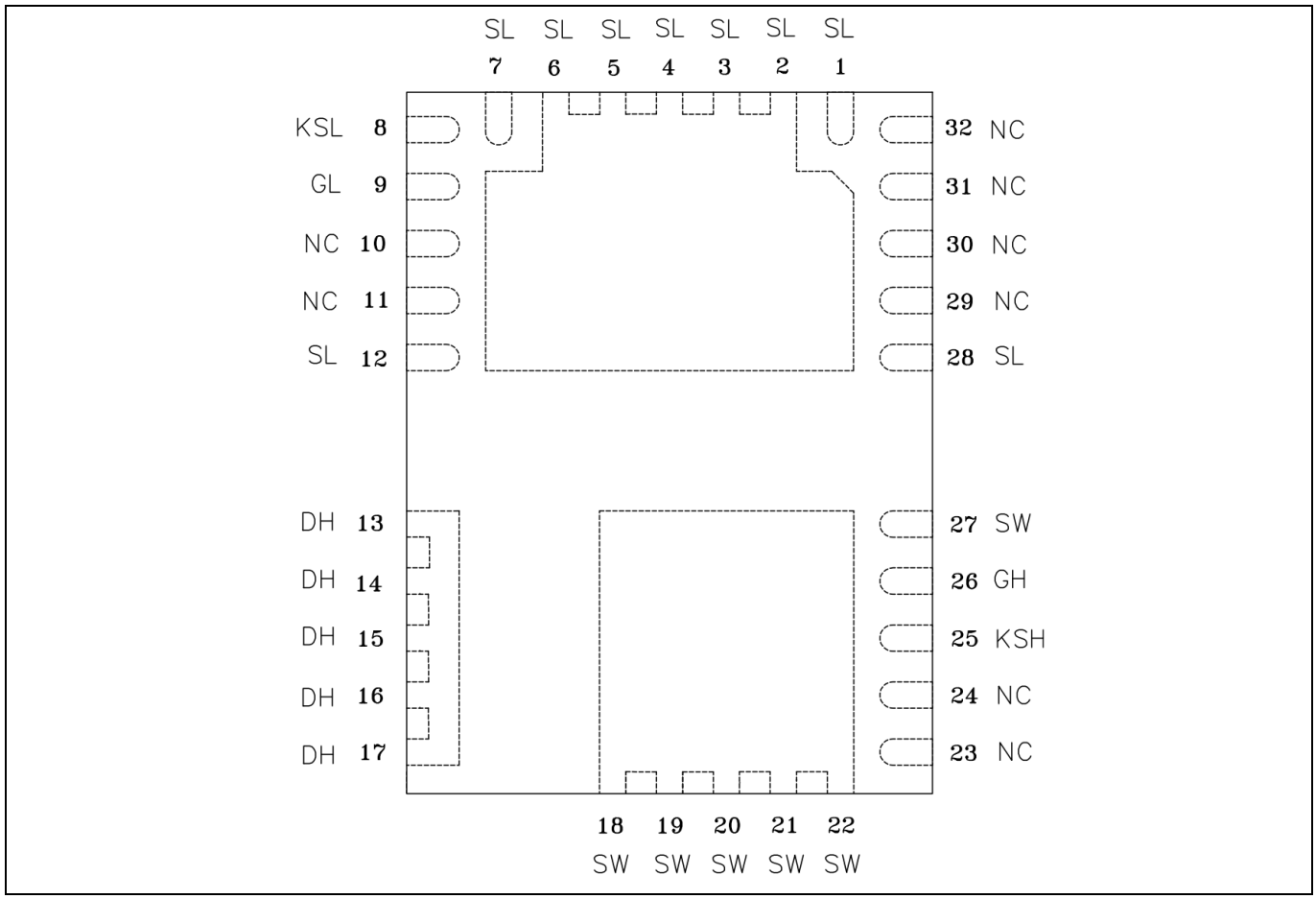


Figure 2 Pin configuration and exposed pads for PG-VIQFN-32-1 6 x 8 mm package, top view (not to scale)

Table 2 Pin description

Pin No.	Symbol	Description
1 – 7, 12, 28	SL	Source connection low-side switch
8	KSL	Kelvin source connection low-side switch
9	GL	Gate connection low-side switch
13 – 17	DH	Drain connection high-side switch
18 – 22, 27	SW	Half-bridge output (switching node)
25	KSH	Kelvin source connection high-side switch
26	GH	Gate connection high-side switch
10, 11, 29 – 32	NC	Not connected, can be connected to SL pad for more thermal cooling
23, 24	NC	Not connected, can be connected to SW pad for more thermal cooling

2 Representative block diagram

A simplified functional block diagram of the CoolGaN™ Power Stage is given in **Figure 3**. Two discrete CoolGaN™ switch are connected in half bridge configuration and co-packed in QFN 6x8 package. Kelvin source connection is available for both high-side and low-side gate drive, which enables superior commutation ruggedness.

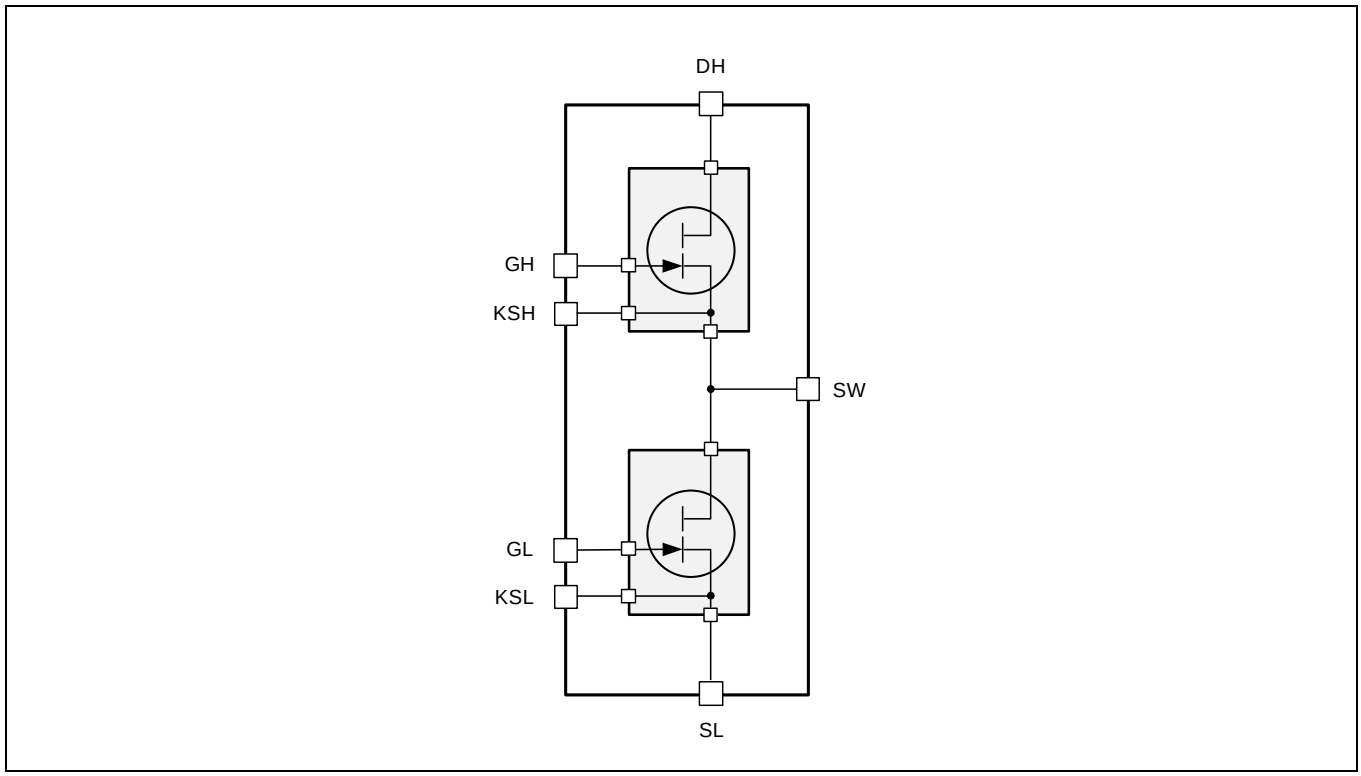


Figure 3 Block diagram IGI65D1414A3MS

3 Characteristics

3.1 Absolute maximum ratings

The absolute maximum ratings are listed in **Table 3**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Voltage between output pins DH, SW and SL	V_{DHSW}	—	—	650	V	
	V_{SWSL}	—	—	650	V	V_{GHSW} = 0 V, V_{GLSL} = 0 V
Drain-to-source voltage pulsed[1]	$V_{DS,pulse}$	—	—	750	V	T_J = 25°C, V_{GS} ≤ 0 V, cumulated stress time ≤ 1h
		—	—	650	V	T_J = 125°C, V_{GS} ≤ 0 V, cumulated stress time ≤ 1h
Continuous drain current [2]	I_D	—	—	13.7	A	T_{Case} = 25°C
		—	—	6.5	A	T_{Case} = 125°C
Pulsed drain current [3][4]	$I_{D,pulse}$	—	—	23	A	T_J = 25°C; I_G = 10 mA
		—	—	14	A	T_J = 125°C; I_G = 10 mA
Gate current, continuous	$I_{G, avg}$	—	—	7.7	mA	T_J = -55 °C to 150 °C (see **Figure 5**)
Gate current, pulsed	$I_{G, pulse}$	—	—	770	mA	T_J = -55 °C to 150 °C T_{pulse} = 50 ns, f = 100kHz open drain (see **Figure 5**)
Junction temperature	T_J	- 55	—	150	°C	
Storage temperature	T_S	- 55	—	150	°C	Max shelf life depends on storage conditions
Soldering temperature	T_{solder}	—	—	260	°C	reflow/wave soldering[5]
ESD capability	V_{ESD_HBM}	—	—	2	kV	Human Body Model[6]
	V_{ESD_CDM}	—	—	1.0	kV	Charged Device Model[7]

[1] Acc to JEDEC-JEP180

[2] Limited by T_{jmax}. Maximum Duty Cycle D=0.5 in the First-Quadrant Operation. Frequency > 1kHz

[3] Limits derived from product characterization and limited by T_{jmax}, parameter not measured during production

[4] Parameter is influenced by reliability requirements. Please contact the local Infineon Sales Office to get an assessment of your application

[5] Acc. to JESD22A111

[6] Acc. to ANSI/ESDA/JEDEC JS-001

[7] Acc. to ANSI/ESDA/JEDEC JS-002

3.2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Thermal resistance junction-case	R_{thJC}	—	—	2.3	°C/W	
Thermal resistance junction-ambient	R_{thJA}	—	45	—	°C/W	Device mounted on four-layer PCB with 600 mm² total cooling area

3.3 Electrical characteristics

at T_J =25°C, unless specified otherwise

Table 5 Output characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
R_{dson} high-side	R_{dshs}	—	140	170	mΩ	I_G = 10 mA, I_D = 3.1 A, T_J = 25°C
		—	300	—	mΩ	I_G = 10 mA, I_D = 3.1 A, T_J = 150°C
R_{dson} low-side	R_{dsls}	—	140	170	mΩ	I_G = 10 mA, I_D = 3.1 A, T_J = 25°C
		—	300	—	mΩ	I_G = 10 mA, I_D = 3.1 A, T_J = 150°C
Drain-source leakage current	I_{DSShs}, I_{DSSls}	—	0.39	39	µA	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 25°C
		—	7.8	—	µA	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 150°C
Total gate charge (per switch)[1]	Q_G	—	1.8	–	nC	VGS = 0 to 3 V, VDS = 400 V, ID = 3.1 A

Table 6 Static characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 —	1.2 1.0	1.6 —	V	I_{DS} = 1 mA, V_{DS} = 10 V, T_j =25 °C I_{DS} = 1 mA, V_{DS} = 10 V, T_j=150°C
Gate-source reverse clamping voltage	$V_{GS,\ clamp}$	—	—	-8	V	I_{GSS}[1] = -1 mA, T_j =25 °C
Gate resistance	$R_{G,int}$	—	0.92	—	Ω	LCR impedance measurement

Table 7 Dynamic characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	—	155	—	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1 MHz
Output capacitance	C_{oss}	—	22	—	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1 MHz
Reverse transfer capacitance	C_{rss}	—	0.31	—	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1 MHz
Effective output capacitance, energy related[2]	$C_{o(er)}$	—	26	—	pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Effective output capacitance, time related[3]	$C_{o(tr)}$	—	35	—	pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Output charge	Q_{oss}	—	14	—	nC	V_{DS} = 0 to 400 V

[1] Gate-Source leakage current

[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 8 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	—	2.2	2.5	V	V_{GS} = 0V, I_{SD} = 3.1 A
Pulsed current, reverse	$I_{S,pulse}$	—	—	23	A	I_G = 10 mA
Reverse recovery charge	Q_{rr}[1]	—	0	—	nC	I_{SD} = 3.1 A, V_{DS} = 400V
Reverse recovery time	t_{rr}	—	0	—	ns	
Peak reverse recovery current	I_{rrm}	—	0	—	A	

[1] Excluding Q_{oss}

4 Driving CoolGaN™ HEMTs

Although Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) with ohmic connection to a pGaN gate are robust enhancement-mode (“normally-off”) devices, they differ significantly from MOSFETs. The gate module is not isolated from the channel, but behaves like a diode with a forward voltage V_F of 3 to 4 V. Equivalent circuit and typical gate input characteristic are given in **Figure 4**. In the steady “on” state a continuous gate current is required to achieve stable operating conditions. The switch is “normally-off”, but the threshold voltage V_{th} is rather low (~ +1 V). This is why in many applications a negative gate voltage $-V_N$, typically in the range of several Volts, is required to safely keep the switch “off” (**Figure 4b**).

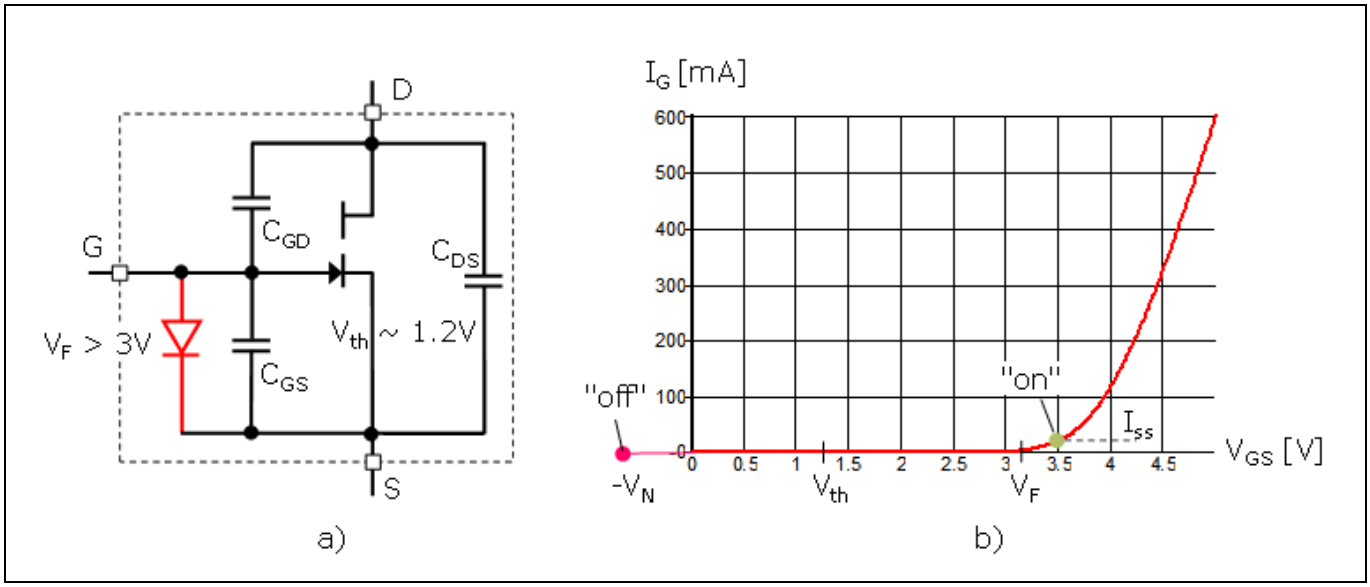


Figure 4 Equivalent circuit (a) and gate input characteristics (b) of typical normally-off GaN HEMT

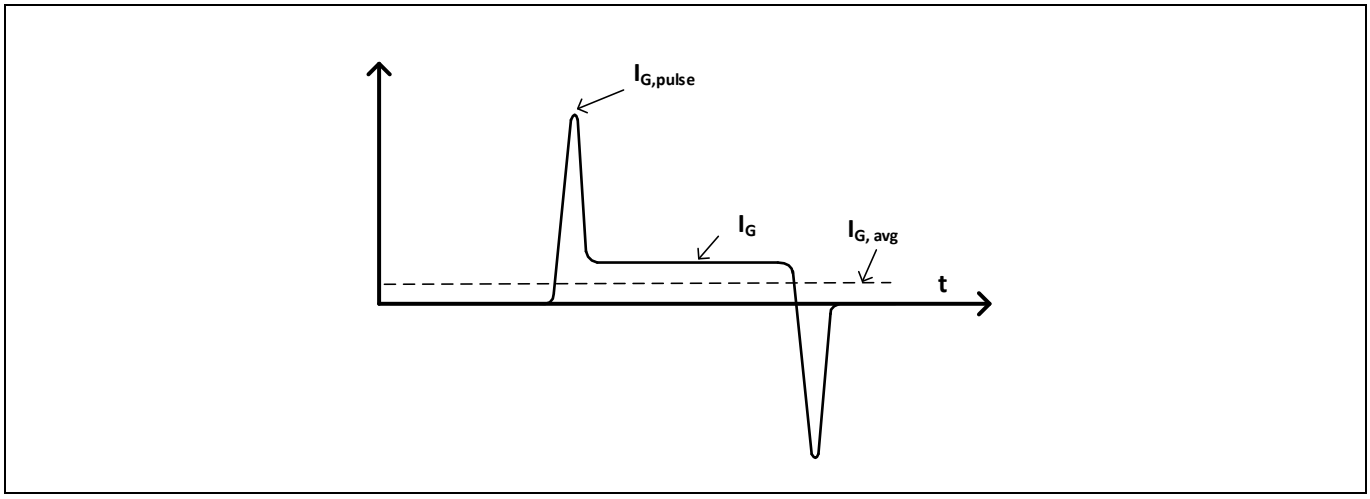


Figure 5 Gate current switching waveform

Obviously the transistor in **Figure 4** cannot be driven like a conventional MOSFET due to the need for a steady-state “on” current I_{ss} and a negative “off” voltage $-V_N$. While an I_{ss} of a few mA is sufficient, fast switching transients require gate charging currents I_{on} and I_{off} in the 1 A range. Typical gate current switching waveform is shown in **Figure 5**, where gate charging currents I_{on} and I_{off} are denoted as $I_{G,pulse}$, and gate holding current I_{ss} is denoted as I_G. To avoid a dedicated driver with 2 separate “on” paths and bipolar supply voltage, the solution depicted in **Figure 6** is usually chosen, combining a standard gate driver with a passive RC circuit to achieve the intended behavior. The high-current paths containing the small gate resistors R_{tr} and R_{off}, respectively, are connected to the gate via a coupling

capacitance C_C. C_C is chosen to have no significant effect on the dynamic gate currents I_{on} and I_{off}. In parallel to the high-current charging path the much larger resistor R_{ss} forms a direct gate connection to continuously deliver the small steady-state gate current I_{ss}. In addition, C_C can be used to generate a negative gate voltage. Obviously, in the "on"-state C_C is charged to the difference of driver supply V_{DD} and diode voltage V_F. When switching off, this charge is redistributed between C_C and C_{GS} and causes an initial negative V_{GS} of value:

$$V_N = \frac{C_C \cdot (V_{DD} - V_F) - Q_G}{C_C + C_{GS}} \tag{2}$$

with Q_G denoting the total gate charge Q_{GS} + Q_{GD}. V_N can thus be controlled by proper choice of V_{DD} and C_C. During the „off" state the negative V_{GS} decreases, as C_C is discharged via R_{SS}. The associated time constant cannot be chosen independently, but is related to the steady-state current and is typically in the 1 µs range. The negative gate voltage at the end of the "off" phase (V_{Nf} in **Figure 6b**) thus depends on the "off" duration. It lowers the effective driver voltage for the following switching-on event, resulting in a slight dependence of switching dynamics on frequency and duty cycle. However, in most applications the impact of this effect is negligible.
Another situation requires attention, too. If there is by any reason a longer period with both switches of a half-bridge in "off"-state (e.g. during system start-up, burst mode operation etc.), both capacitors C_C will be discharged. That means, for the first switching pulse after such an extended non-switching period no negative voltage is available. To avoid instabilities due to spurious turn-on effects in such a situation, C_C should be chosen to guarantee sufficient negative gate voltage during device turn-off.

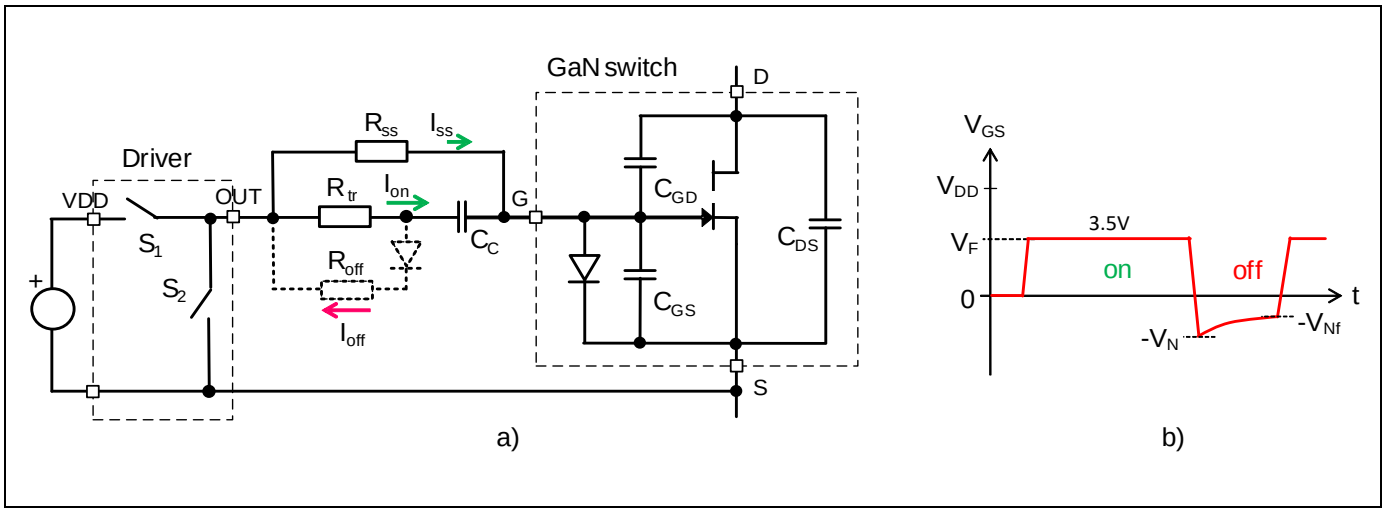


Figure 6 Equivalent circuit of GaN switch with RC gate drive (a) and gate-to-source voltage V_{GS} (b)

In the topology of **Figure 6** often a single resistor R_{tr} can be used for setting the maximum transient charging and discharging current. If this is not acceptable by any reason, an additional resistor R_{off} with series diode in parallel with R_{tr} can be used to realize independent gate impedances for the "on" and "off" transient, respectively.
All relevant driving parameters are easily programmable by choosing V_{DD}, R_{ss}, R_{tr}, R_{off} and C_C according to the relations

$$V_N = \frac{C_C \cdot (V_{DD} - V_F) - Q_G}{C_C + C_{GS}}$$

$$I_{ss} = \frac{V_{DD} - V_F}{R_{ss}}, \qquad I_{on,max} \sim \frac{V_{DD} - V_{Nf}}{R_{tr}}, \qquad I_{off,max} \sim \frac{(V_{th} + V_N) \cdot (R_{off} + R_{tr})}{R_{off} \cdot R_{tr}} \tag{3}$$

The main guidelines for dimensioning gate drive parameters are as follows:

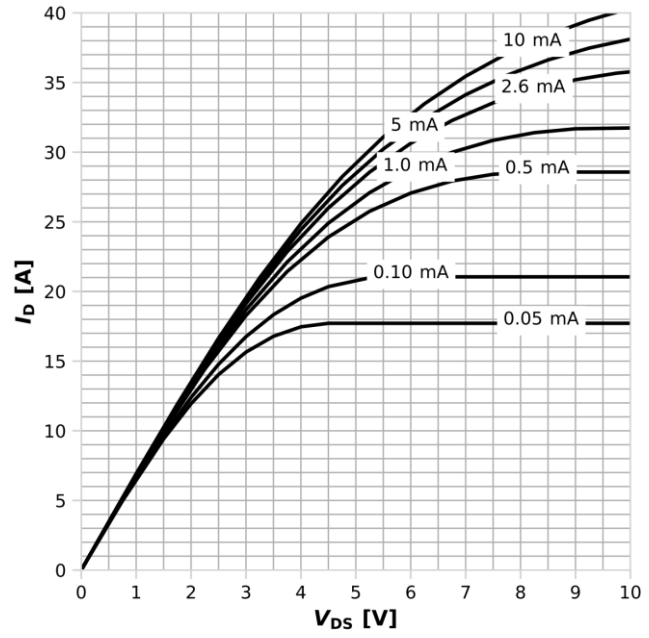
- V_N must always be positive; a target value of 2 V in soft-switching and 4 V to 5 V in hard-switching systems is recommended

- A target value of I_{ss} is around few mA, a higher I_{ss} current normally comes with a higher drain-source saturation current. R_{ss} has to be chosen according to the desired output characteristics.
- R_{tr} sets the transient speed for a hard switching “on” event. For soft switching systems R_{tr} is anyway uncritical.
- If a separate R_{off} is used, it should guarantee sufficient damping of oscillations in the gate loop.

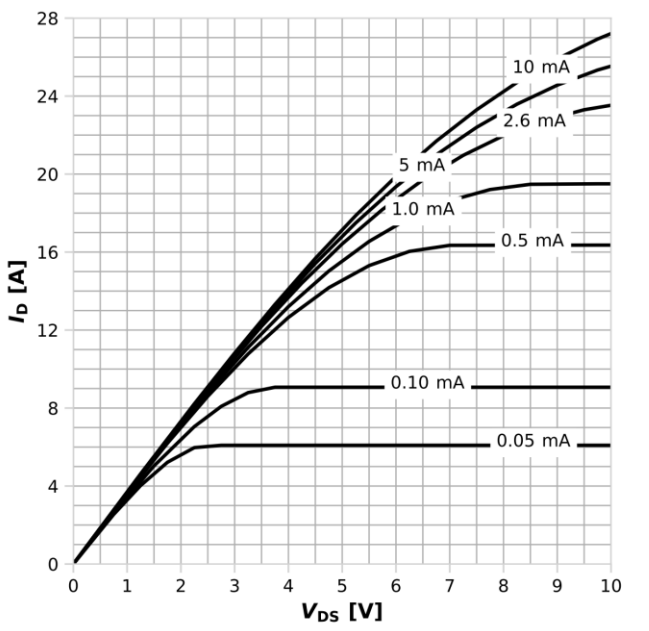
For more information regarding how to drive GaN HEMT refer to Gate drive configurations for GaN power transistors.

5 Typical characteristics

The following graphs refer to a single GaN switch.

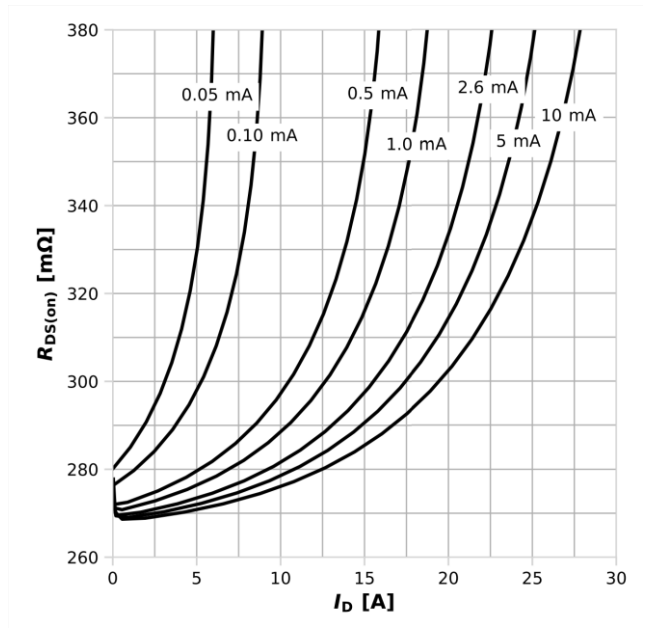


$I_D=f(V_{DS},I_{GS})$; $T_j=25°C$

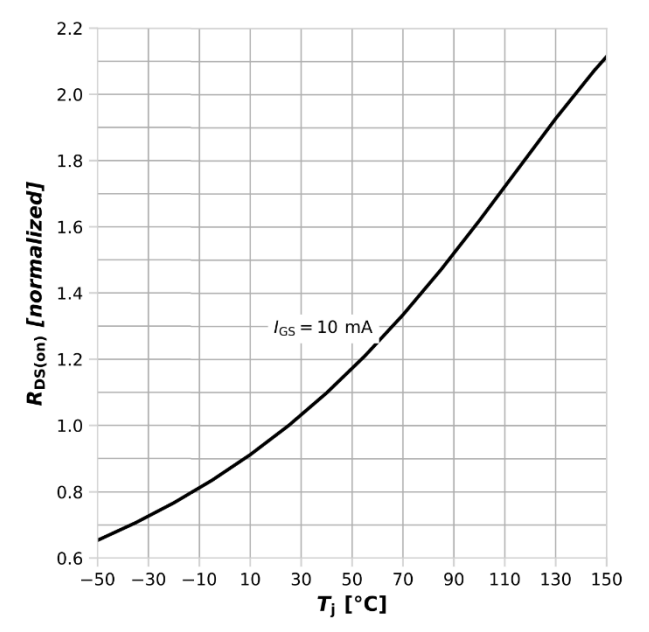


$I_D=f(V_{DS},I_{GS})$; $T_j=125°C$

Figure 7 Typical output characteristics

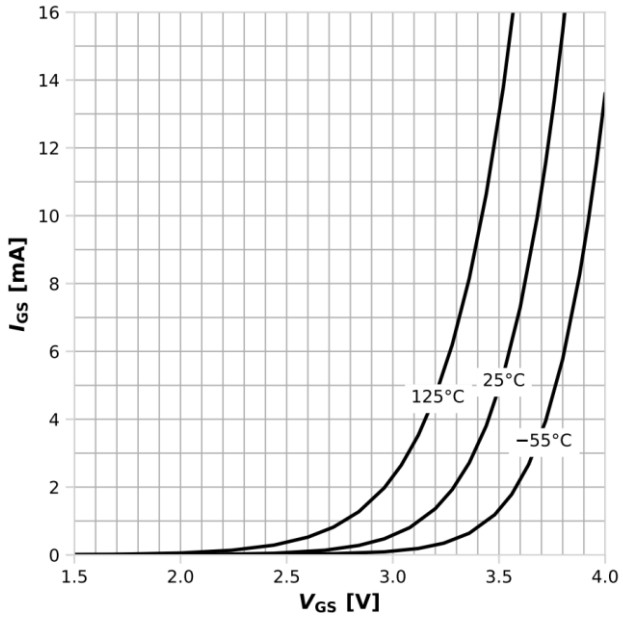


$R_{DS(on)}=f(I_D,I_G)$; $T_j=125°C$

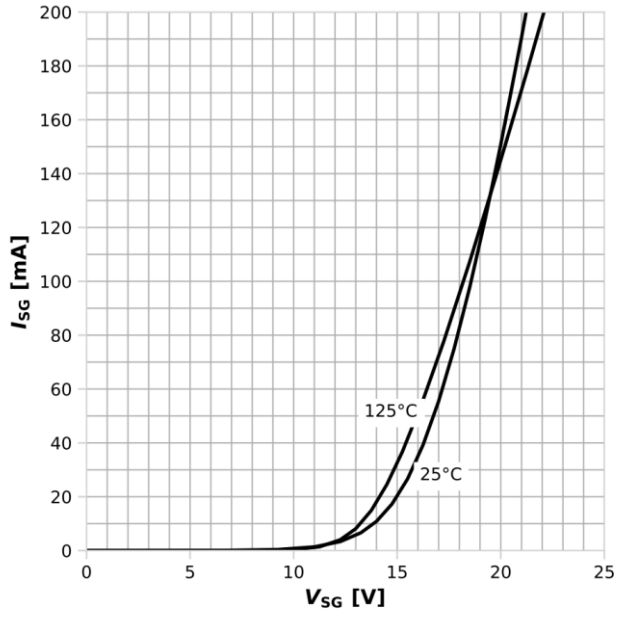


$R_{DS(on)}=f(T_j)$; $I_D=3.1$ A

Figure 8 Typical drain-source on-resistance

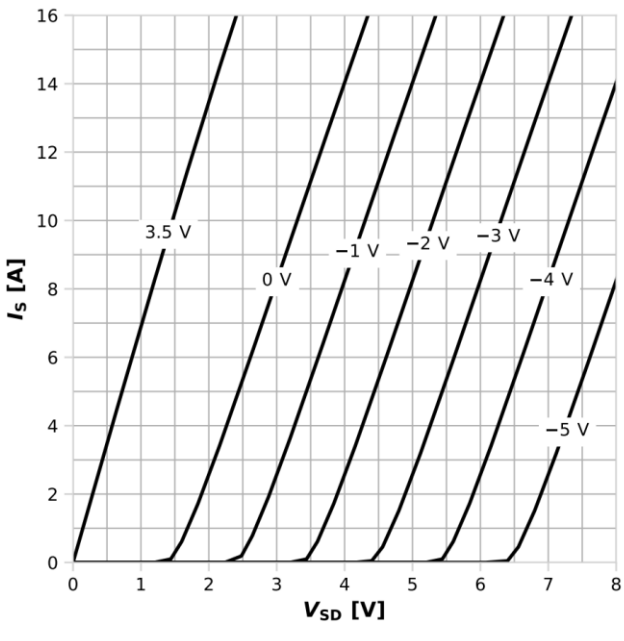


$I_{GS}=f(V_{GS},T_j)$; open drain

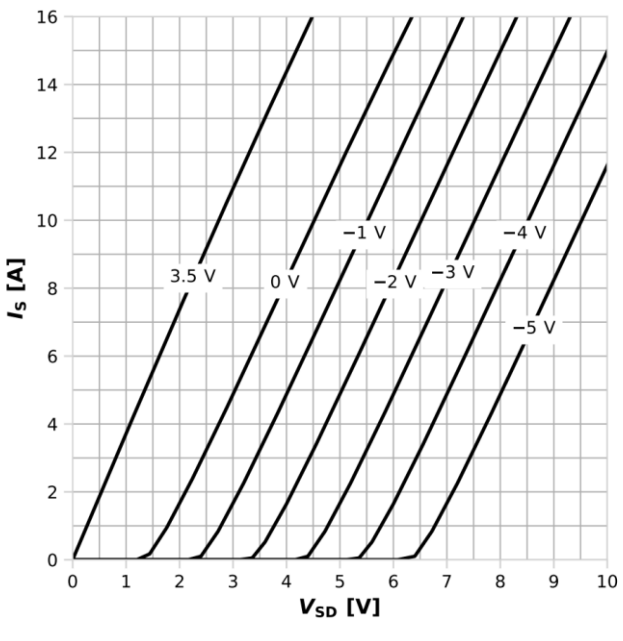


$I_{SG}=f(V_{SG},T_j)$; open drain

Figure 9 Typical gate characteristics forward and reverse

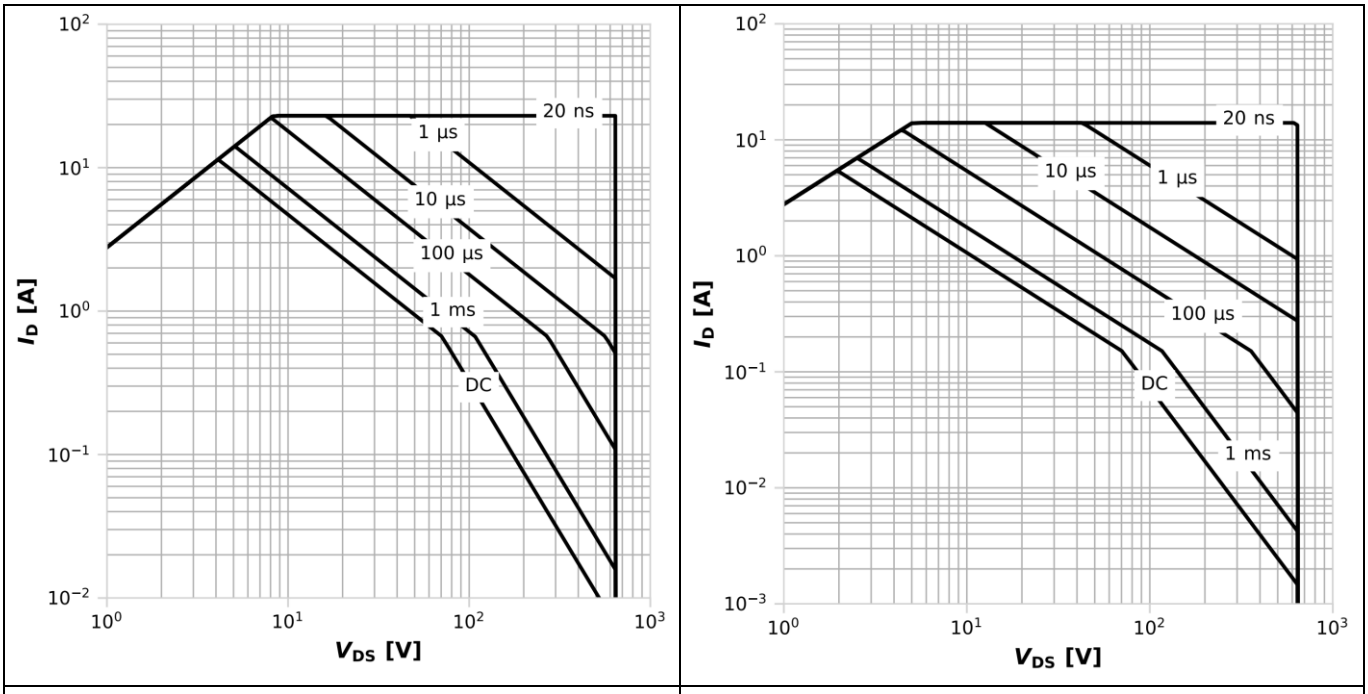


$I_S=f(V_{SD},V_{GS})$; T_j=25°



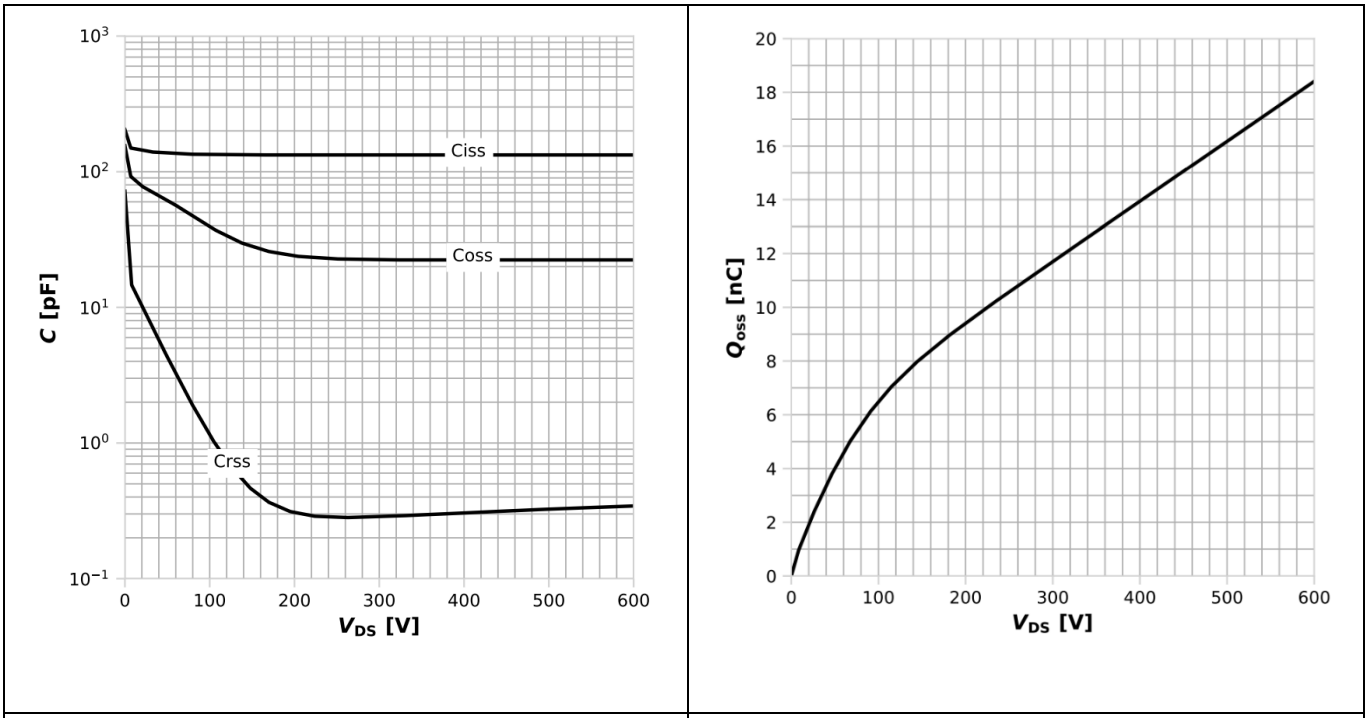
$I_S=f(V_{SD},V_{GS})$; T_j=125°

Figure 10 Output characteristic I_{ds} (V_{ds}) in normal and reverse operation (parameter V_{gs})



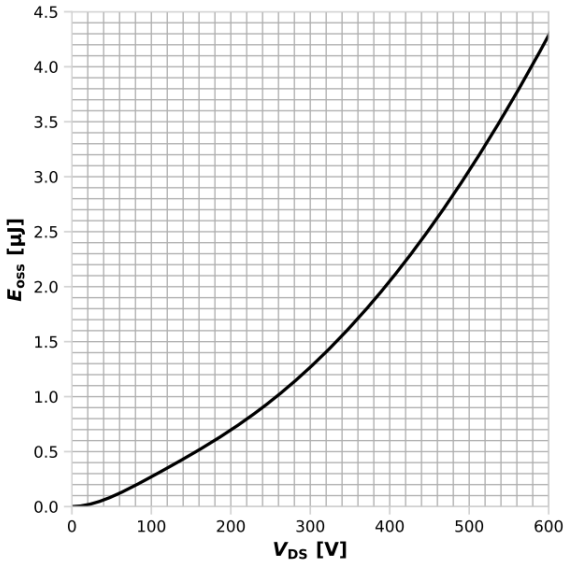
$I_D=f(V_{DS})$; $T_{Case}=25°C$	$I_D=f(V_{DS})$; $T_{Case}=125°C$

Figure 11 Safe Operating Area (SOA)



$C=f(V_{DS})$; $V_{GS}=0$ V	$Q_{OSS}=f(V_{DS})$

Figure 12 Terminal capacitances and output charge (single switch)



E=f(V_{DS})

Figure 13 Typical output energy (single switch)

6 Package information

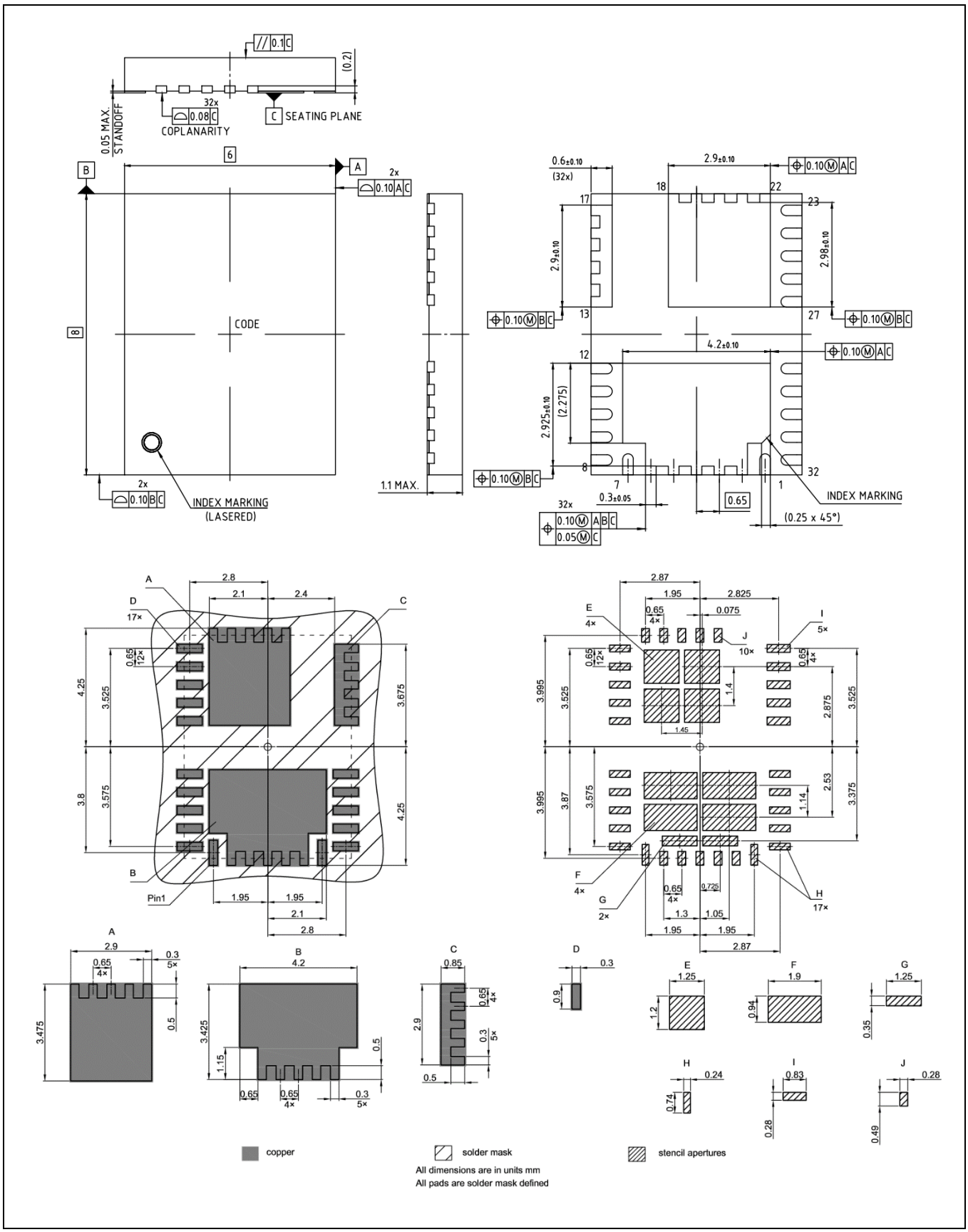


Figure 14 QFN-32 6x8 package outline and footprint

7 Layout guidelines

Figure 15 shows the complete circuitry required. The suggested arrangement of the components around the chipset on the PCB is depicted in **Figure 16**.

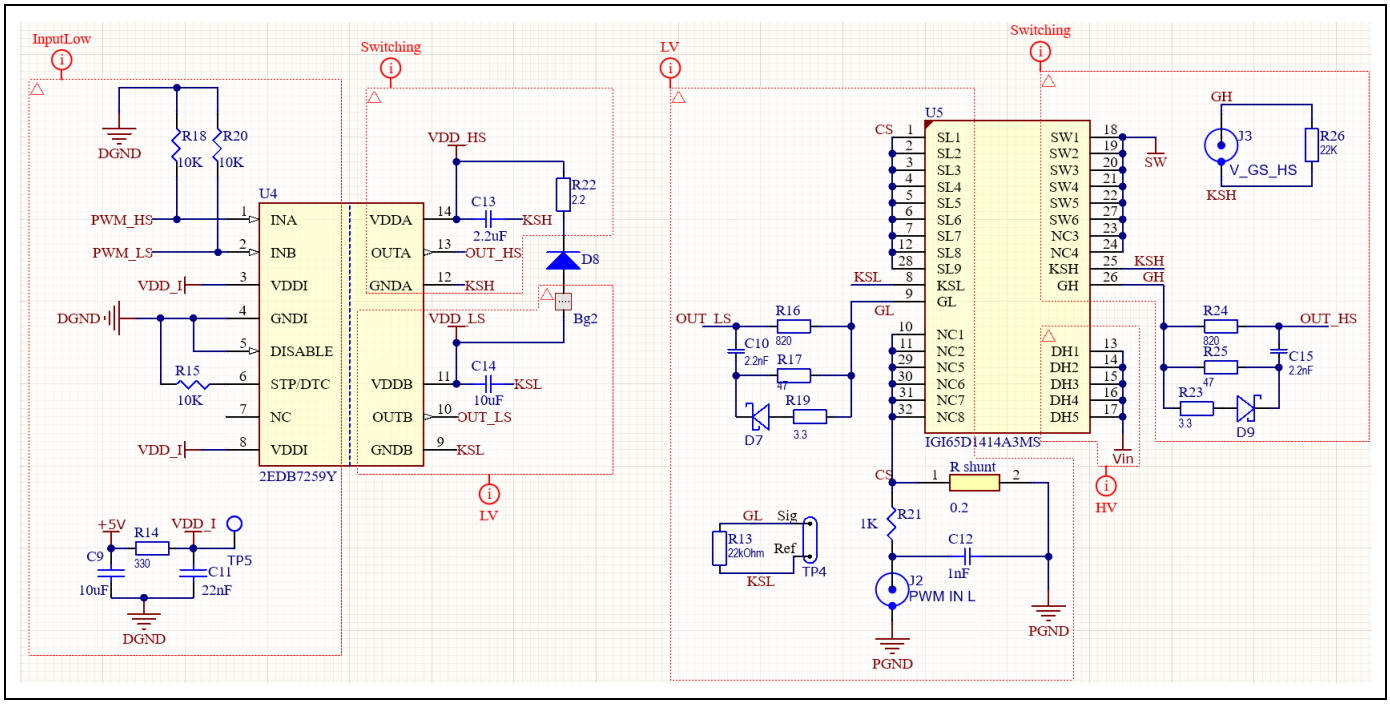


Figure 15 CoolGaN™ Transistor Dual driving circuitry with external passive components

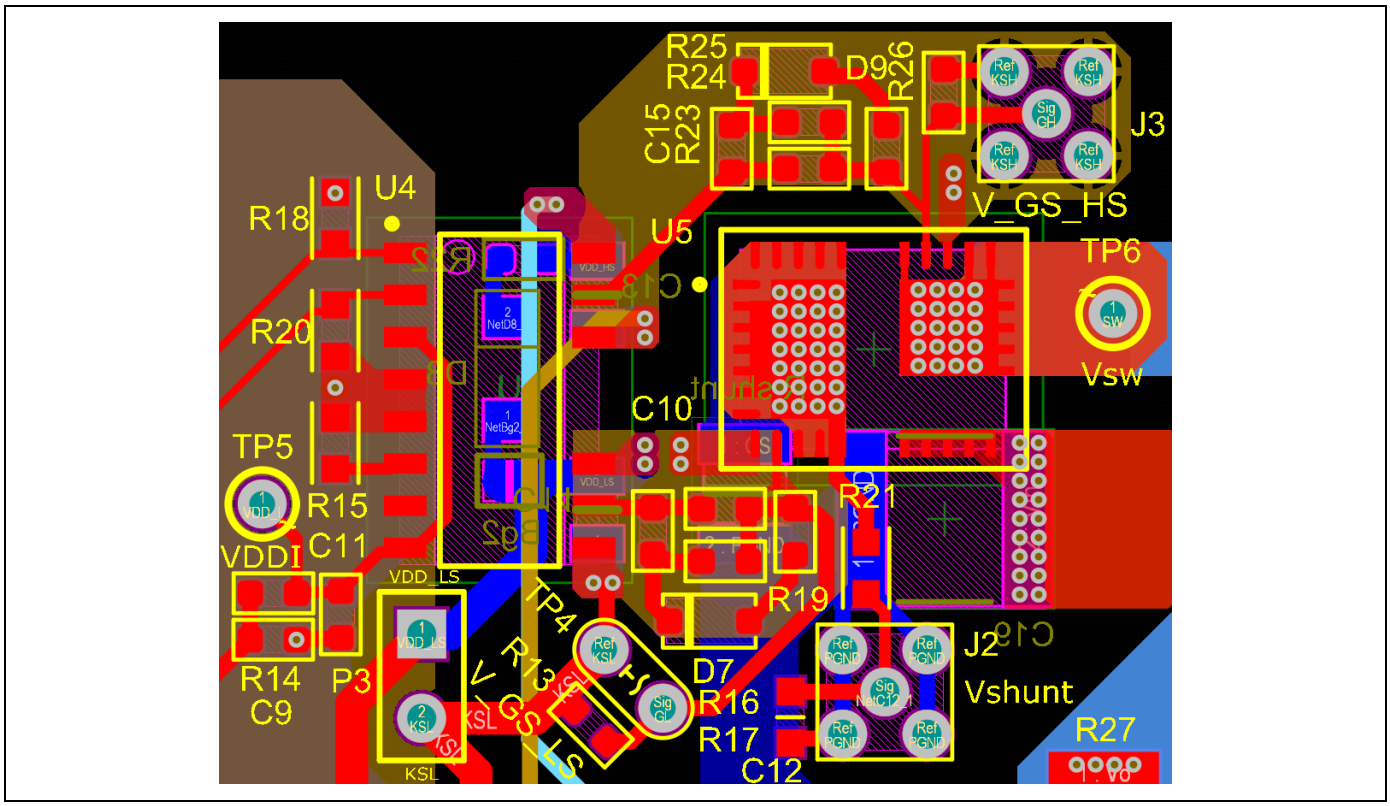


Figure 16 Reference PCB layout

Top and bottom layer of the PCB are shown above. The following layout recommendations should be considered:

1. On the exposed pads' landing area, place vias with 0.3mm hole size with <0.7mm space (center to center).
2. Use solder mask expansion of 0.05 ~ 0.075mm for the chipset footprint pins and pads.
3. Place and align the GND trace (PGND node for power return) beneath the DC bus trace on the top layer to minimize the inductance loop in the power path.
4. For the low voltage controller reference (DGND) on the PGND trace select a location free of any switching current to avoid switching-induced noise in DGND (do not connect the DGND trace to any trace which connects the bypass cap to GaN power loop).

8 Appendix

I. PCB footprint and Altium file for the reference PCB design can be found in the CoolGaN™ Half-bridge IPS webpage (evaluation board registration is needed to access the design files)

II. Related Links

IFX CoolGaN™ webpage: www.infineon.com/why-coolgan

IFX CoolGaN™ reliability white paper: www.infineon.com/gan-reliability

IFX CoolGaN™ applications information:

www.infineon.com/gan-in-server-telecom

www.infineon.com/gan-in-wirelesscharging

www.infineon.com/gan-in-adapter-charger

Revision history

Document version	Date of release	Description of changes
V1.0	2025-01-31	First final datasheet release

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Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems reintended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.