XDPL8221 Digital PFC+Flyback Controller IC

XDP™ Digital Power

Data Sheet
Revision 1.1

Features

- UART interface to control driver output and reading operating status
- Flicker-free output dimming by analog reduction of driving current down to 1%
- Integrated two stage digital controller allows a reduced number of external parts, optimizes ***Bill of Materials (BOM)*** and form factor.
- Two-stage design eliminates AC ripple on output.
- Supports universal AC and DC input voltage (90 V rms to 305 V rms) nominal.
- High efficiency up to 90%
- Multi-control output (***Constant Current (CC)***/***Constant Voltage (CV)***/***Limited Power (LP)***)
- Performance and protection related driver parameters are configurable via UART interface allowing for design flexibility and optimization.
- Low harmonic distortion (***Total Harmonic Distortion (THD)*** < 15%) down to 30% nominal load
- Integrated 600V high voltage start-up cell ensures fast time to light (< 250 ms)
- Configurable Adaptive Temperature Protection
- Automatic switching of the ***Power Factor Correction (PFC)*** between ***Quasi-Resonant Mode (QRM)*** and ***Discontinuous Conduction Mode (DCM)***
- Automatic switching of the ***Flyback (FB)*** between ***QRM***, ***DCM*** and ***Active Burst Mode (ABM)***
- ***Pulse Width Modulation (PWM)*** dimming input

For safe operation, the XDPL8221 contains a comprehensive set of protection features with configurable reaction like auto-restart or latch:

- Output over-voltage protection (open load)
- Output under-voltage protection (output short)
- VCC over- and under-voltage lockout
- Input over- and under-voltage protection
- Bus over- and under-voltage protection
- Over-current protection for both ***PFC*** and ***FB*** stages

Applications

- AC/DC LED Drivers for ***Light Emitting Diode (LED)*** luminaires

Description

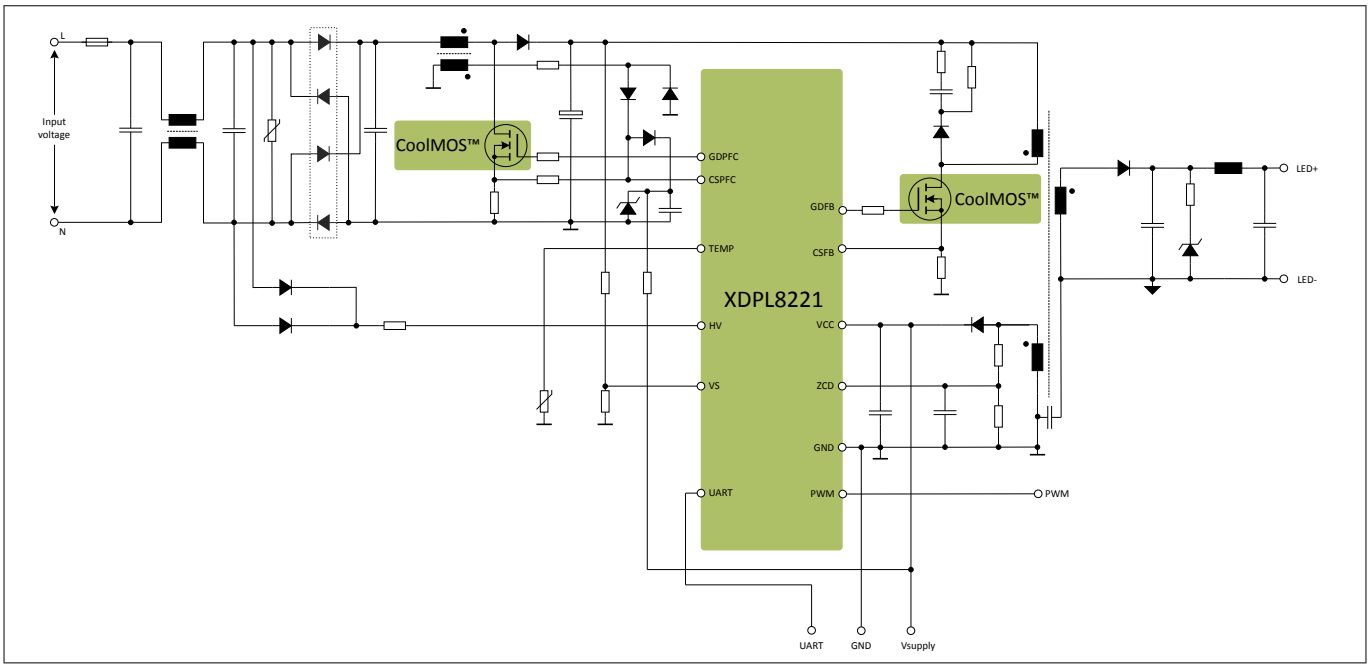

Figure 1 Typical Application for XDPL8221

Product Type	Package
XDPL8221	PG-DSO-16

Description

XDPL8221 is a highly integrated next-generation device combining a multimode (***QRM*** and ***DCM***) ***PFC*** plus a multimode (***QRM***, ***DCM*** and ***ABM***) ***FB*** with primary-side regulation. The integration of ***PFC*** and ***FB*** into a single controller enables reduction of external parts and optimizes performance by harmonized operation of the two stages.

The two-stage approach divides the ***PFC*** responsibilities from the output current regulations functions. This ensures low variation in the output current (flicker) to a non-visible level and allows for low ***THD*** , high power factor and a greater ability to withstand AC line perturbations.

XDPL8221 ***PFC*** comprises of constant on-time scheme with a ***THD*** improvement algorithm to provide a high power factor and excellent performance down to 30% nominal load.

XDPL8221 ***FB*** can be configured to operate in Constant Voltage (CV), Constant Current (CC) or Limited Power (LP) mode offering a large degree of flexibility.

The on-chip ***One Time Programmable Memory (OTP)*** memory allows user to adjust electrical and performance parameters that control the behavior of the circuit. Examples of this include: output current limit or the maximum output power. This enables the user of the device to create a platform concept with significantly fewer different hardware versions while still covering the same application range.

The ***Universal Asynchronous Receiver Transmitter (UART)*** command interface allows connecting XDPL8221 to any microcontroller, wireless interface or sensor for many different applications.

During low power mode, the XDPL8221 power consumption is less than 100mW.

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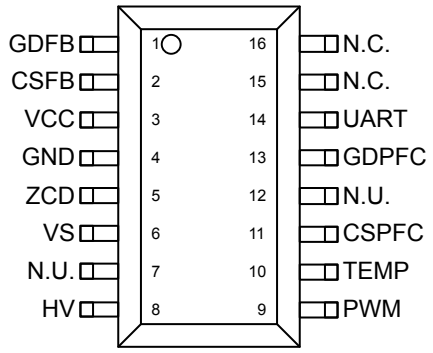
1 Pin Configuration

Pin assignments and basic pin description information are shown below.



PG-DSO-16 (150mil)

Figure 2 Pinning of XDPL8221

Table 1 Pin Definitions and Functions

Name	Pin	Type	Function
GDFB	1	O	Gate driver for ***FB***: The *GDFB* pin is an output for directly driving a power MOSFET of the ***FB*** stage.
CSFB	2	I	Current sensing for ***FB***: The *CSFB* pin is connected to an external shunt resistor and the source of the power MOSFET of the ***FB*** stage.
VCC	3	I	Voltage supply
GND	4	-	Power and signal ground
ZCD	5	I	Zero-crossing detection of the ***FB***: The *ZCD* pin is connected to an auxiliary winding of the ***FB*** stage for zero-crossing detection as well as primary-side output voltage and additional bus voltage sensing for functional safety.
VS	6	I	Bus voltage sensing
N.U.	7	-	Not used. Externally to be connected to *GND*.
HV	8	I	High voltage: The *HV* pin is connected to the rectified input voltage via an external resistor. An internal 600 V HV startup-cell is used to initially charge *VCC*. In addition, sampled high-voltage sensing is also used for synchronization with the input frequency.
PWM	9	I	***PWM*** dimming: The *PWM* pin is used as a dimming input.
TEMP	10	I	External temperature sensor: Measurement of external temperature using an ***Negative Temperature Coefficient Thermistor (NTC)***.
CSPFC	11	I	Current sensing for ***PFC***: The *CSPFC* pin is connected to an external shunt resistor and the source of the power MOSFET of the ***PFC*** stage.

Table 1 Pin Definitions and Functions (continued)

Name	Pin	Type	Function
N.U.	12	-	Not used. Externally to be connected to *GND*.
GDPFC	13	O	Gate driver for ***PFC***: The *GDPFC* pin is an output for directly driving a power MOSFET of the ***PFC*** stage.
UART	14	I/O	***UART*** communication: The *UART* pin is used for the ***UART*** interface to support parametrization and for application commands during run-time.
N.U.	15	-	Not used. Externally to be connected to *GND*.
N.U.	16	-	Not used. Externally to be connected to *GND*.

2 Functional Block Diagram

The functional block diagram shows the basic data flow from input pins via signal processing to the output pins.

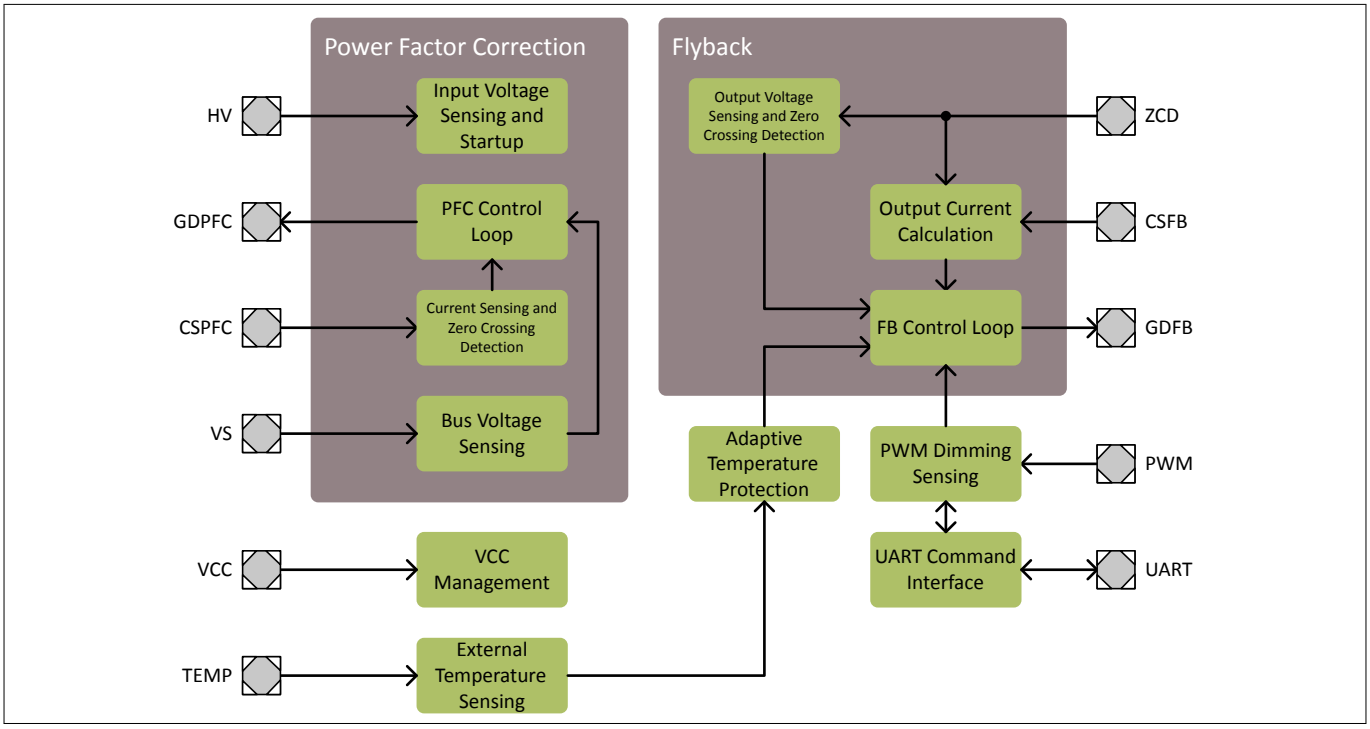


Figure 3 XDPL8221 Simplified Functional Block Diagram

3 Functional Description

This chapter provides a summary of the integrated functions and features, and describes the relationships between them. The parameters and equations are based on typical values at T_A = 25 °C.

XDPL8221 is a digital dual-stage ***PFC*** and ***FB*** controller IC supporting ***PWM*** dimming functionality. Both stages use configurable multi-mode operation to select the best mode of operation for every operation condition. Multi-mode operation automatically switches between ***QRM***, ***DCM*** and ***ABM*** (only for ***FB***)

XDPL8221 features a comprehensive set of configurable protection modes to detect fault conditions.

XDPL8221 provides a high degree of flexibility in design-in of the application. A ***Graphic User Interface (GUI)*** tool supports users in the configuration of the operational and protection parameters.

3.1 PFC Controller Features

The ***PFC*** stage ensures high power quality by maximizing the power factor and minimizing harmonic distortion.

The ***PFC*** stage operates in ***Quasi-Resonant Mode, switching in first valley (QRM1)*** and ***Quasi-Resonant Mode, switching in valley n (QRMn)***, to support light load conditions and ensure efficient operation.

The ***PFC*** stage is implemented as a boost converter and provides stabilized ***Direct Current (DC)*** voltage rail.

3.1.1 Shared CS/ZCD Function

The ***PFC*** stage makes use of combined Current Sense and Zero-Crossing Detection (CS/ZCD) functionality at the CSPFC pin.

During the ***PFC*** MOSFET on-time, the CSPFC pin has the function of sensing the ***PFC*** inductor current ensuring inductor does not enter saturation, and the converter limits maximum switching current.

The CSPFC pin is connected to an external shunt resistors, which converts the inductor current to voltage. The sensed voltage at the CSPFC pin is compared with reference voltages on internal comparators to either limit the on-time cycle by cycle or enter the protection mode when over-current happens.

During the ***PFC*** MOSFET off-time, the CSPFC pin has the function of current zero crossing detection (ZCD). This detection minimizes the turn-on losses of the ***PFC*** MOSFET by ensuring the MOSFET turns-on during the resonant valley of the ***PFC*** MOSFET drain-source voltage (V_{DS}) (***QRM***). The CSPFC pin is connected via an external resistor divider composed of $R_{ZCD,1,PFC}$ and $R_{ZCD,2,PFC}$ and a set of diodes to the auxiliary winding of the ***PFC*** inductor.

Diode D_1 allows positive voltage at the CSPFC pin as the valley detection is implemented by the internal hysteretic comparator with a positive reference of nominal THR_{HYS} for falling edges.

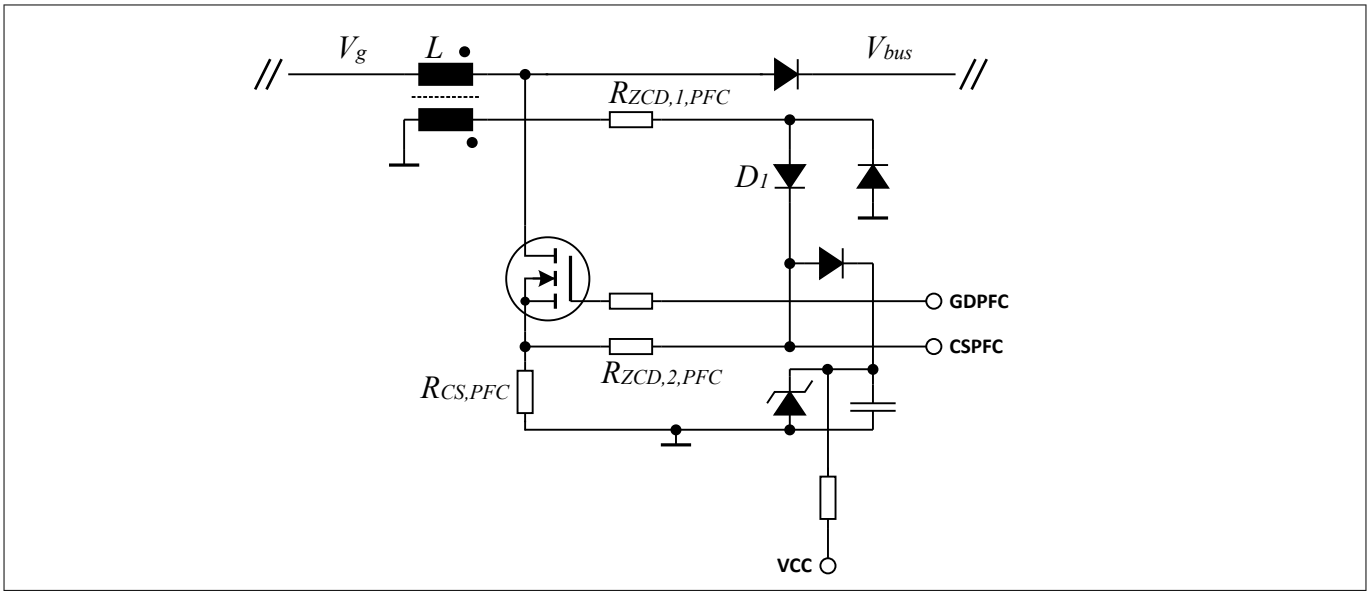


Figure 4 Shared CS/ZCD Schematic

3.1.2 Quasi-resonant Mode

The quasi-resonant mode maintains a high efficiency level.

XDPL8221 ***PFC*** Quasi-resonant mode reduces ***PFC*** MOSFET switching losses and ensures highest possible efficiency of the system. See Multi-mode Scheme description for detailed ***QRM*** operation in section 3.1.6.

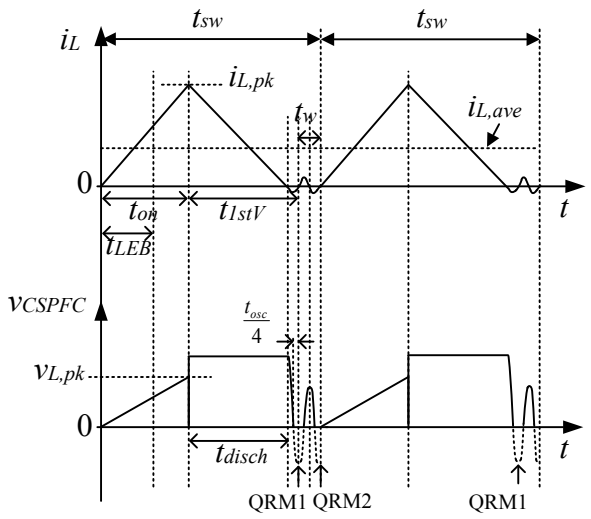


Figure 5 PFC QRM2 Waveforms

Equations for the quasi-resonant operation are shown below. Delay time t_w is an additional delay realized in each switching cycle when ***PFC*** MOSFET turn-on beyond first resonant valley and valley n (n>1) is selected (***QRMn***).

$$i_{L,pk} = \frac{V_g \cdot t_{on}}{L}$$

$$t_{disch} = \frac{i_{L,pk} \cdot L}{V_{bus} - V_g}$$

$$t_{1stV} = t_{disch} + t_{osc}/2$$

$$t_w = t_{osc} \cdot (n-1)$$

$$t_{sw} = t_{on} + t_{1stV} + t_w$$

$$t_{off} = t_{1stV} + t_w$$

Equation 1

3.1.3 Bus Voltage Sensing

The ***PFC*** output bus voltage is scaled down using a simple resistor divider and measured at the pin VS. A capacitor shall be added at the pin to ground to filter high-frequency switching noise.

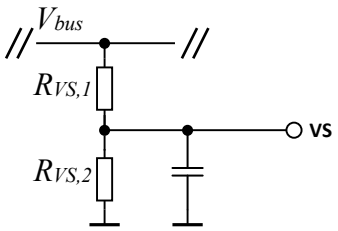


Figure 6 PFC Bus Voltage Sensing Circuit

The ***Analog-to-Digital Converter (ADC)*** input at the VS pin utilizes two voltage ranges. The wider voltage range from 0 to V_{REF} results in lower resolution. The narrower voltage range from 5/6 V_{REF} to 7/6 V_{REF} gives better voltage resolution. Steady state operation therefore normally takes place in the high-resolution range and soft start operation in the low-resolution range.

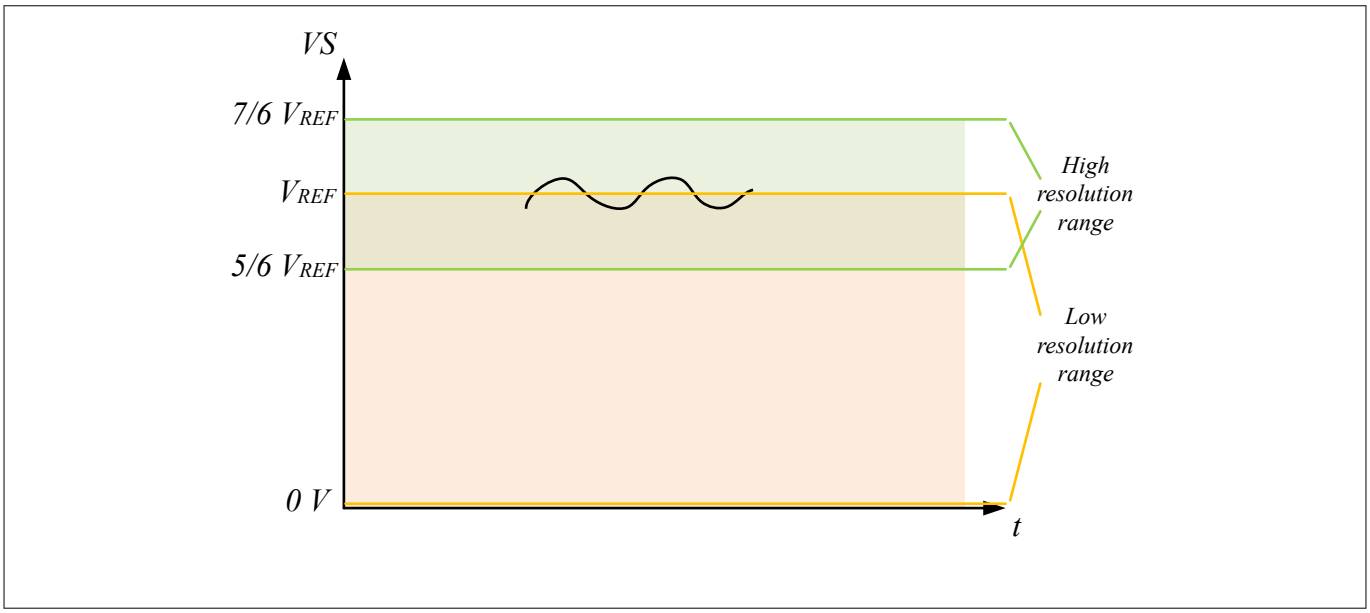


Figure 7 Sensing Ranges

3.1.4 Input Voltage Sensing

The input voltage is sensed at the HV pin for ***Alternating Current (AC)*** zero-crossing detection and protection features.

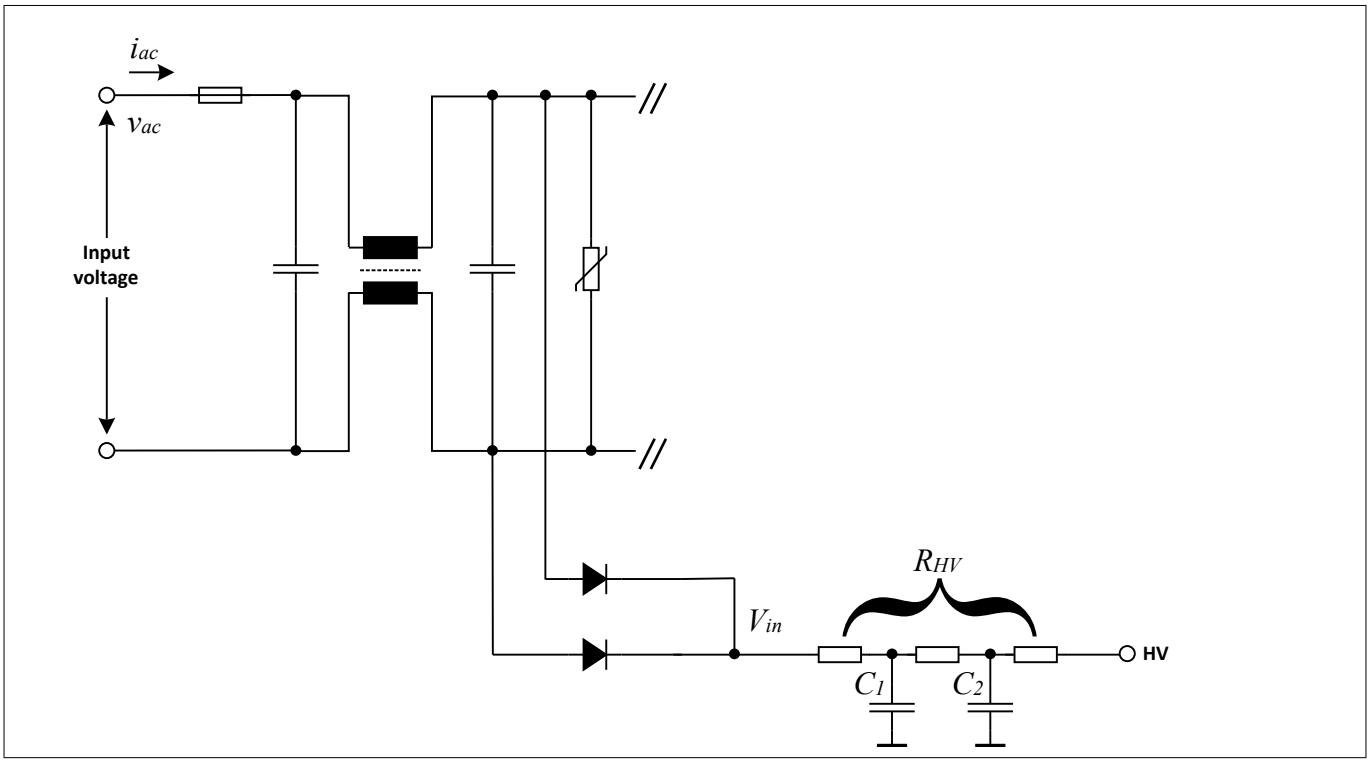


Figure 8 Input Voltage Sensing Schematic

The R_{HV} sense resistor is usually split into two or more resistors for redundancy and safety purposes. A RC filter structure to the HV pin is implemented as shown above to reduce the unwanted noise.

3.1.5 Control Scheme

The ***PFC*** bus voltage controller embeds a controller that calculates a control output representing load and line conditions from the bus voltage error signal.

The bus voltage controller implements regulation during both soft start and steady states.

3.1.5.1 Startup

At system startup, the ***PFC*** initiates soft start to minimize the switching stress on the power MOSFET, diode and inductor.

PFC soft start is executed once the ***PFC*** bus voltage is charged due to rectified AC line to a voltage threshold $V_{bus,start,PFC}$ but lower than $V_{bus,OVP1}$. The ***PFC*** soft start is aborted if the input under- or over-voltage protections are triggered. During soft start, the ***PFC*** operates in ***QRM1***mode. Once the $V_{bus,stdy,entr,UV}$ threshold is reached, the steady state ***PFC*** operation starts.

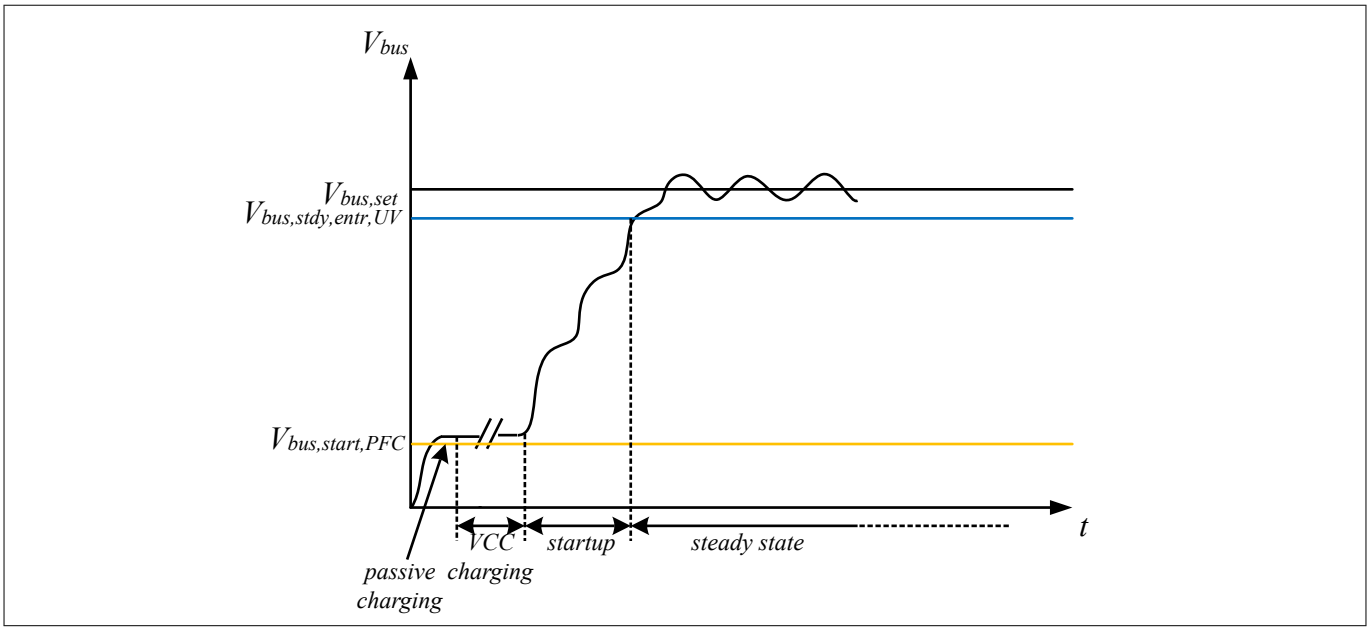


Figure 9 V_{bus} Soft Start and Regulation

3.1.6 Multimode Control Scheme

The XDPL8221 multi-mode control scheme provides an option to dynamically change the operating point by switching between the MOSFET V_{ds} voltage valleys while following a frequency law and applying ***THD*** optimization.

The multi-mode controller uses three different modes of operation:

- ***QRM1***: operation occurs during normal operation of the ***PFC*** converter at nominal to heavy loads. This operation maximizes the efficiency by switching on at the 1st valley of the ***PFC*** ZCD signal. This ensures zero current switching with a minimum switching losses. During ***QRM1***, the ***PFC*** MOSFET is turned on with a constant on-time for a line and load condition, while the off- time varies within an AC half-cycle depending on the instantaneously rectified AC input voltage. Subsequently, the PFC switching frequency varies within each AC half-cycle with the lowest switching frequency at the peak of the AC input voltage and the highest switching frequency near the zero crossings of the input voltage.
- ***QRMn***: ***PFC*** MOSFET on-time reduces as the load decreases, this results in higher switching frequencies, particularly near the zero-crossing of the input voltage. Higher switching frequencies will increase switching losses, resulting in poor efficiency at light loads. The XDPL8221 controller extends to the next switching valley after the 1st valley to control the bus voltage following a frequency law which limits the switching frequency to minimize the switching losses.
- ***DCM***: The controller regulates the power transfer by adjusting the switching frequency with fixed minimum on-time. This enables the light load optimization.

The multimode optimization consists of the following:

- Frequency law
- THD optimization
- DC switching frequency dithering
- Light load optimization

3.1.6.1 Frequency Law

A ***PFC*** converter is used to emulate a resistive load r_e to the ***AC*** input such that i_{ac} follows v_{ac} in both wave shape and phase. The output of the ***PFC*** bus voltage controller $t_{on,des,PFC}$ is inversely proportional to the emulated resistive load r_e such that a smaller r_e or a higher $I_{ac,rms}$ will give a larger $t_{on,des,PFC}$. Thus, $t_{on,des,PFC}$ varies as the ***AC*** line voltage magnitude varies and is proportional to the RMS input current $I_{ac,rms}$.

The rule for selecting ***QRMn*** is based on the frequency law. A maximum switching frequency f_{swmax} and a minimum switching frequency f_{swmin} are defined for the complete $t_{on,des,PFC}/I_{ac,rms}$ range. The frequency law ensures that the switching frequency is within the desired frequency range. The frequency law is depicted in the figure below.

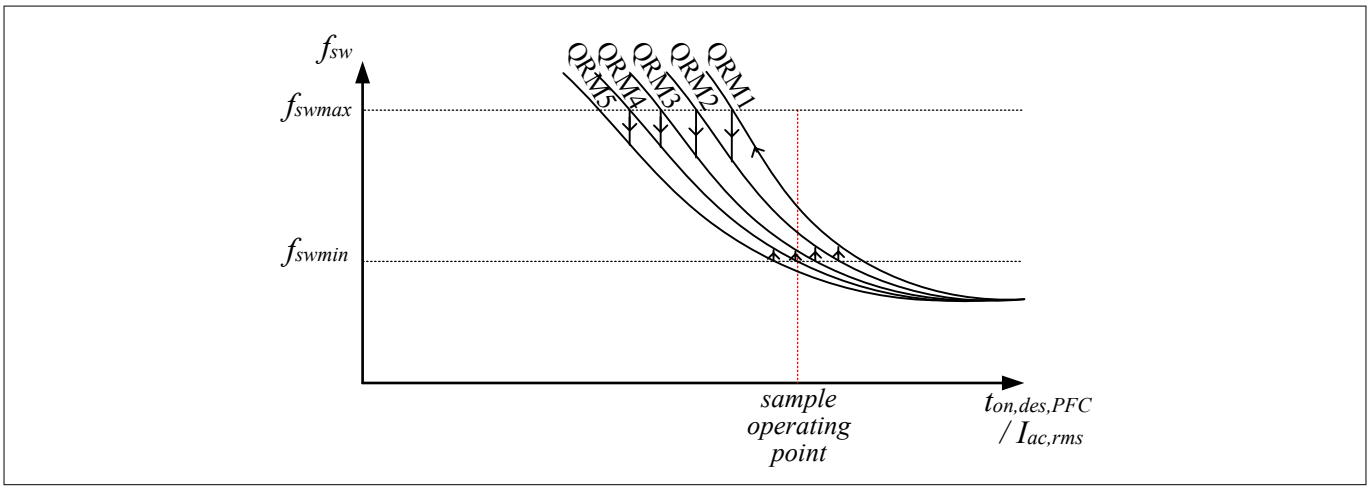


Figure 10 PFC Frequency Law

As long as the ***PFC*** controller operating mode satisfies the frequency law, the operating mode does not change. The QR-valley is increased when the highest frequency limit is reached. The QR-valley is decremented when the lowest frequency limit is reached.

To ensure proper ZCD detection before the ZCD signal becomes too small in amplitude, only the first up to $N_{valley,max,PFC}$ valleys operations are supported.

3.1.6.2 THD Optimization

QRMn selection beyond the first valley during light load and/or ***AC*** high line reduces the switching frequency but distorts the input current waveform with constant on-time control and***THD*** may suffer. The multi-mode ***PFC*** control consists of a ***THD*** optimization algorithm that optimizes the applied on-time in order to ensure good input current shaping and improved ***PFC THD*** performance.

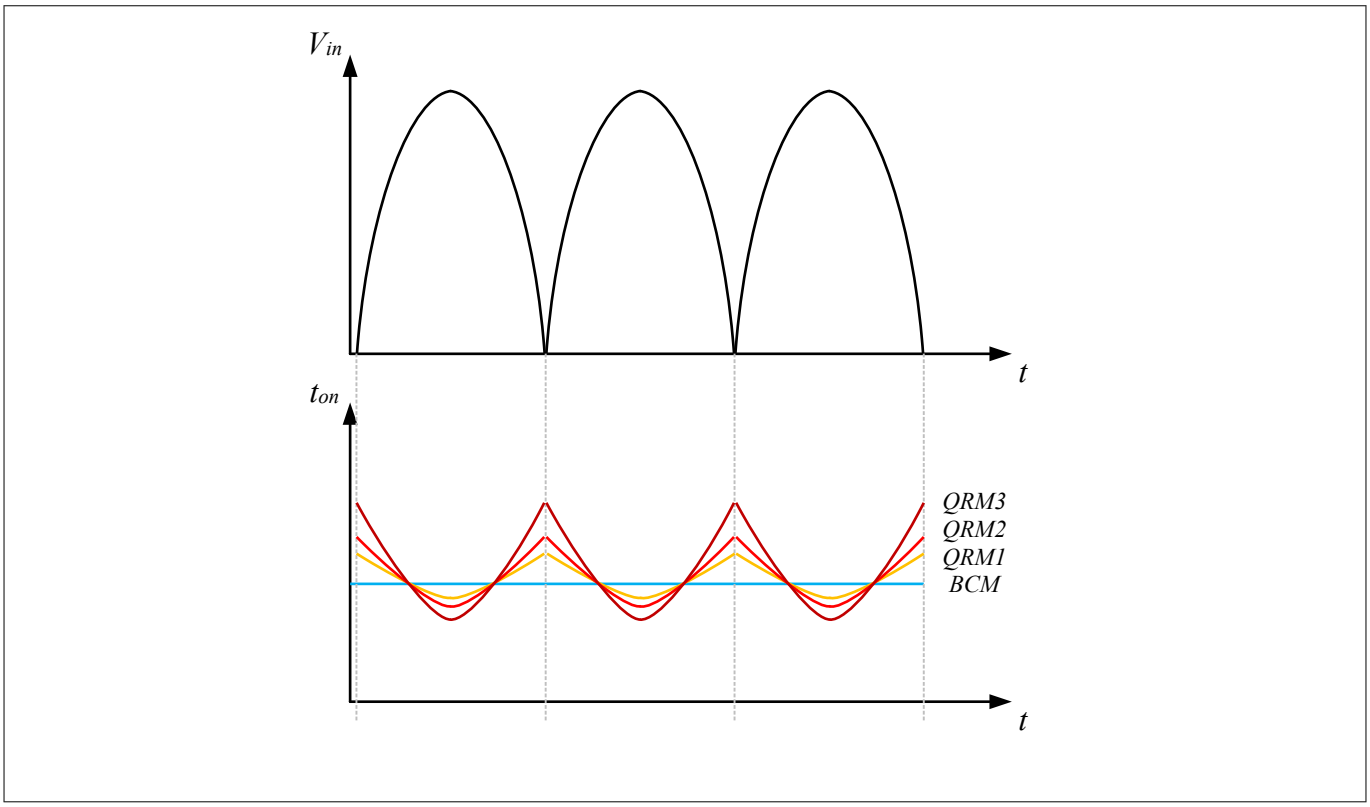


Figure 11 THD optimization on-time

Figure 11 shows the on-time at different valley selection at the same line and load conditions.

Note: Boundary Conduction Mode (BCM) is an operating mode where the switch turns on at the first occurrence of inductor zero current .

3.1.6.3 Light Load Optimization

This paragraph describes how the ***PFC*** manages light load conditions.

DCM

PFC converter will eventually enter DCM operation as load decreases and/or ***AC*** line increases to reduce the switching frequency and switching losses. XDPL8221 ***PFC*** control enters ***DCM*** when the internal on-time is less than $t_{on,dcm}$. The ***PFC*** leaves ***DCM*** when the switching period is less than $t_{sw,min,dcm}$. When the ***PFC*** is operating in ***DCM***, the bus voltage controller regulates the switching period keeping the on-time constant. Due to the on-time dependency on the input voltage, the ***PFC*** enters and exits ***DCM*** at different power levels. This has the advantage to operate in ***QRM*** for an extended power range at low line maintaining high efficiency.

3.1.7 Peak Current Limitation

The peak current through the switching MOSFET is sensed via the ***PFC*** shunt resistor $R_{CS,PFC}$ to limit the maximum current through the MOSFET, the choke, and freewheeling diode.

Overcurrent Protection Level 1 (OCP1) is implemented by hardware. If the voltage $V_{CS,PFC}$ across the shunt resistor exceeds the over-current threshold $V_{CS,OCP1,\ PFC}$ for longer than the blanking time $t_{blank,OCP1,PFC}$, the MOSFET is turned off. The MOSFET is turned on when ZCD occurs or the PFC maximum period time-out signal triggers the start of the next switching cycle. ***Overcurrent Protection Level 2 (OCP2)*** is a second-level overcurrent protection implemented by hardware. The ***OCP2*** overcurrent threshold is fixed. The ***OCP2*** blanking time is $t_{blank,OCP2,PFC}$.

3.1.8 Protection Features

Protections features are triggered if fault conditions are present longer than the blanking times for each protection.

Attention**: **The controller may continue operation after exceeding protection thresholds because of blanking times as shown in Figure 12. All protection thresholds have to be set with respect to tolerances, blanking times and worst case transients.

Note: The blanking time as specified in the csv file does not include the protection notification time.

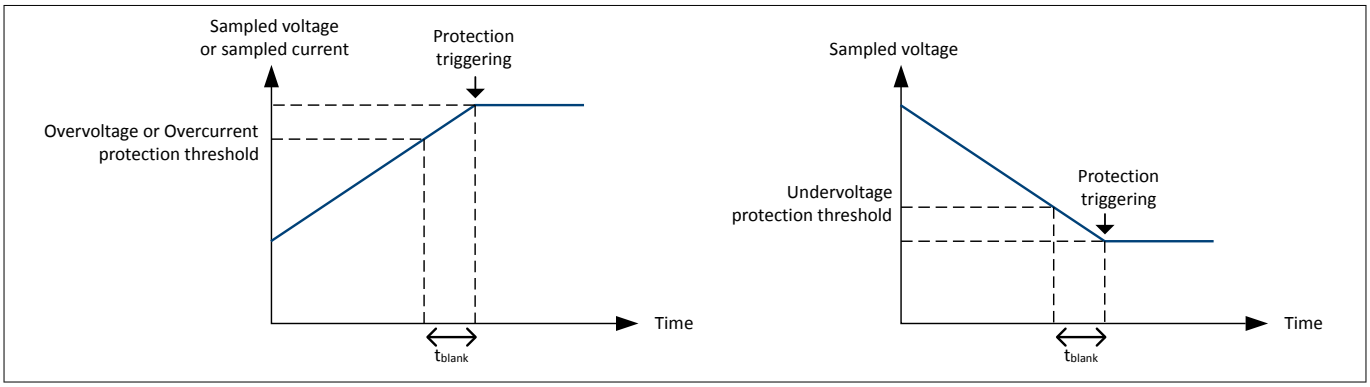


Figure 12 Blanking Times cause Excess of Threshold

3.1.8.1 Bus Under-voltage Protection

Under-voltage detection of the ***PFC*** bus voltage V_{bus} is sensed at the VS pin.

The ***PFC*** bus voltage is sensed and compared to a configurable under-voltage protection threshold $V_{bus,UV}$. If the bus voltage is below the threshold for longer than the blanking time $t_{blank,Vbus,UV}$, the protection will be triggered.

3.1.8.2 Bus Over-voltage Protection

Over-voltage detection of the ***PFC*** bus voltage V_{bus} is sensed at the VS pin.

The ***PFC*** bus voltage is sensed and compared to a configurable over-voltage protection threshold $V_{bus,OVP1}$ in ***Firmware (FW)***. If this threshold is exceeded for longer than the blanking time $t_{blank,Vbus,OVP1}$, the ***PFC*** stops switching. The ***PFC*** resumes operation when V_{bus} falls below $V_{bus,stdy,entr,OV}$.

$V_{bus,OVP2}$ is implemented in ***Hardware (HW)*** and it is fixed at a voltage which is represented as 7/6 V_{REF} at the bus voltage sensing pin (VS). The HW permits a blanking time $t_{blank,Vbus,OVP2}$ to be programmed.

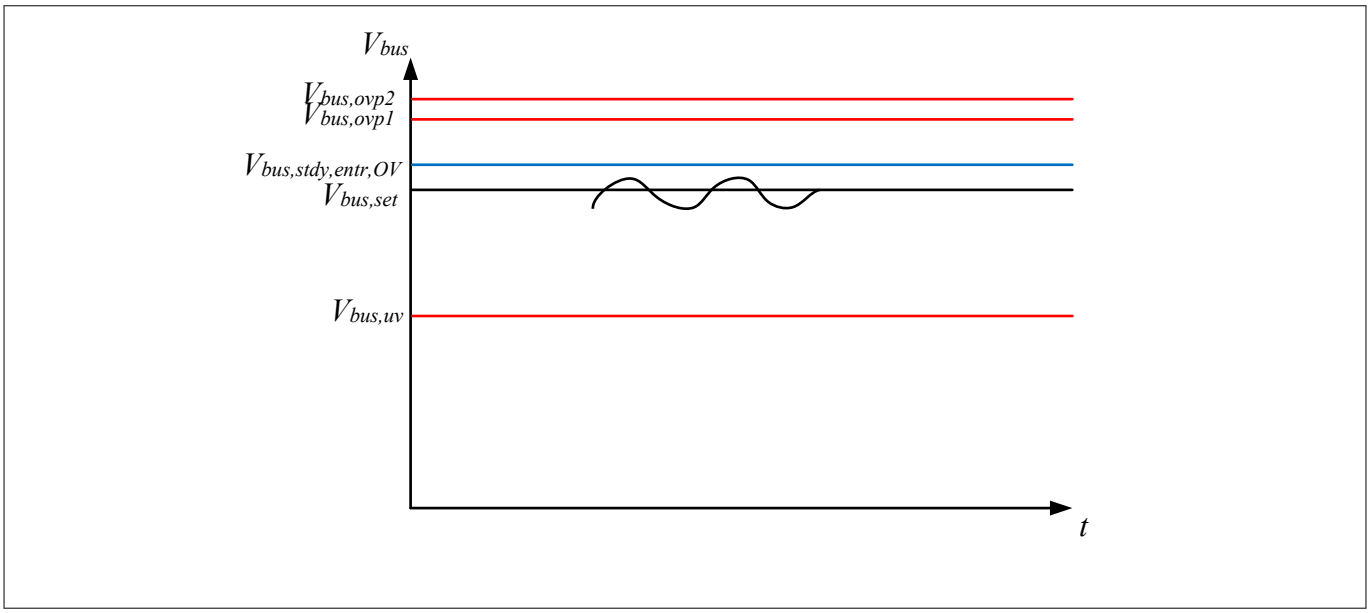


Figure 13 V_{bus} protections

3.1.8.3 Input Under-voltage Protection

Under-voltage detection of the input voltage V_{in} is sensed at the HV pin.

Values of $V_{in,rms}$ are compared to a configurable input undervoltage protection threshold $V_{in,UV}$. If the input voltage is below the threshold for longer than the blanking time $t_{blank,Vin,UV}$, the protection will be triggered. XDPL8221 features a configurable start-up threshold $V_{in,start,min}$ to create hysteresis for flicker-free operation before the second stage starts switching.

3.1.8.4 Input Over-voltage Protection

Over-voltage detection of the input voltage V_{in} is sensed at the HV pin.

Values of $V_{in,rms}$ are compared to a configurable input over-voltage protection threshold $V_{in,OV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,Vin,OV}$, the protection will be triggered. XDPL8221 features a configurable start-up threshold $V_{in,start,max}$ to create hysteresis for flicker-free operation before the second stage starts switching.

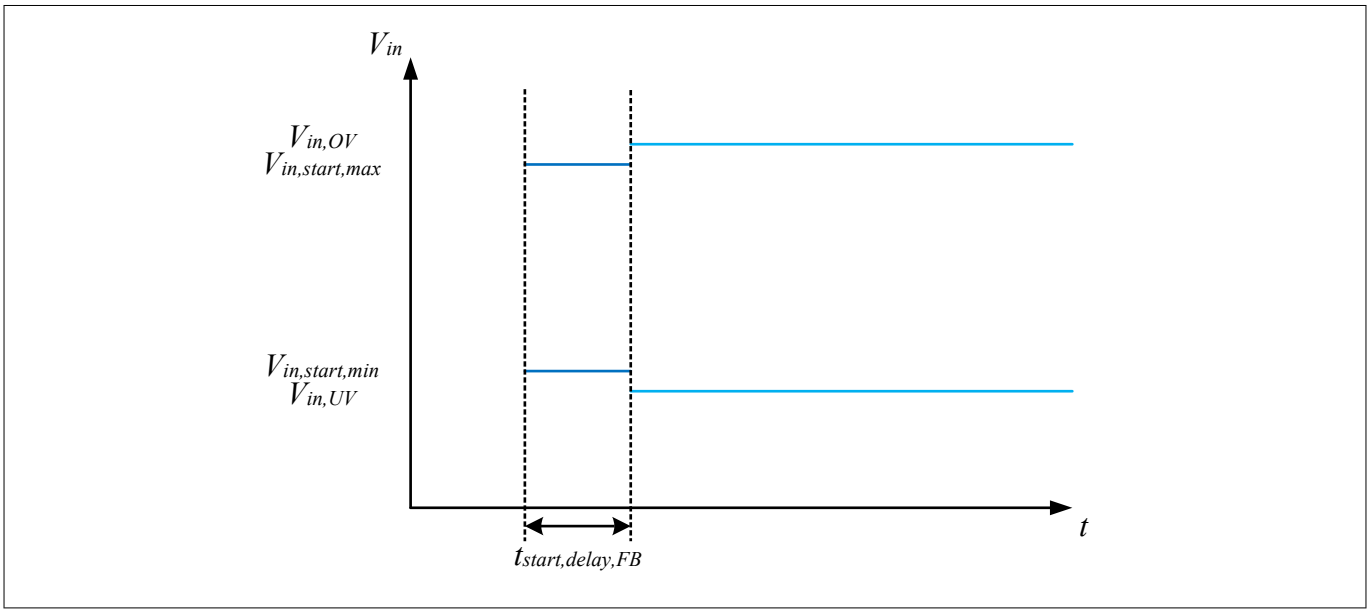


Figure 14 V_{in} protections

3.1.8.5 Other PFC Protections

Current Sense (CS) Resistor Short Protection

The input fuse should be chosen appropriately to protect converter if current-sense resistor is shorted.

Current Sense (CS) Resistor Open Protection

CS/ZCD external circuitry pulls the CSPFC pin high when CS resistor is open, OCP2 protection is triggered.

CSPFC Pin Short to GND Protection

In case of CSPFC pin short to ground the missing of quasi-resonant oscillations will trigger the CCM Protection.

CCM Protection

Continuous conduction mode (CCM) operation may occur during ***PFC*** startup for a limited time and is allowed. In normal operation, extended CCM operation in the ***PFC*** converter is considered a failure.

Circumstances where the ***PFC*** converter may experience CCM operation:

- Shorted PFC bypass diode
- Heavy load step which is out of specification
- Low input voltage outside the normal operating range

During CCM operation, the magnetizing current in the ***PFC*** choke does not decay to zero prior to MOSFET turn-on. Quasi-resonant oscillation is missing in the ZCD signal before the maximum switching period time-out is reached that turns the MOSFET on. This turn-on event without ZCD oscillation is monitored to protect the ***PFC*** converter from continuous CCM operation. Extended CCM operation protection is implemented within ***FW***.

If quasi-resonant oscillation is missing in the ZCD signal for longer than the blanking time $t_{blank,CCM,PFC}$, the protection is triggered.

Soft Start Failure

PFC start-up time maybe extended due to abnormally heavy loads or a low input voltages. ***PFC*** steady state operation may not be reached if $t_{start,PFC}$ reaches $t_{start,max,PFC}$ before the soft start has ended, and the protection is triggered.

3.2 Flyback Controller Features

The Flyback converter stage provides isolation and primary side control of the output current. Primary side regulation of the output current eliminates secondary side control feedback loop circuitry usually needed in isolated power converters. This feature reduces part count to reduce costs.

The Flyback stage features multi-mode operation (***QRM***, ***DCM*** and ***ABM***) which ensures efficiency and performance is optimized.

3.2.1 Primary Side Regulation

The XDPL8221 ***FB*** stage provides primary side control of output current and output voltage. No external feedback components are necessary for the current control.

Figure 15 shows typical current and voltage waveforms of the ***FB*** application operating in ***QRM1***.

In ***DCM***, the MOSFET will not turn on at the first valley of the resonant oscillation seen at V_{AUX}, but instead delayed.

Primary side regulation of the average output current is accomplished by sensing the primary peak current $I_{p,pk}$, the period of conduction of the output diode t_{demag} and the switching period $t_{sw,FB}$.

The voltage signal V_{AUX} of the auxiliary winding of the transformer contains information on the reflected output voltage V_{out}. The reflected output voltage is measured at the *ZCD* pin using a resistor divider.

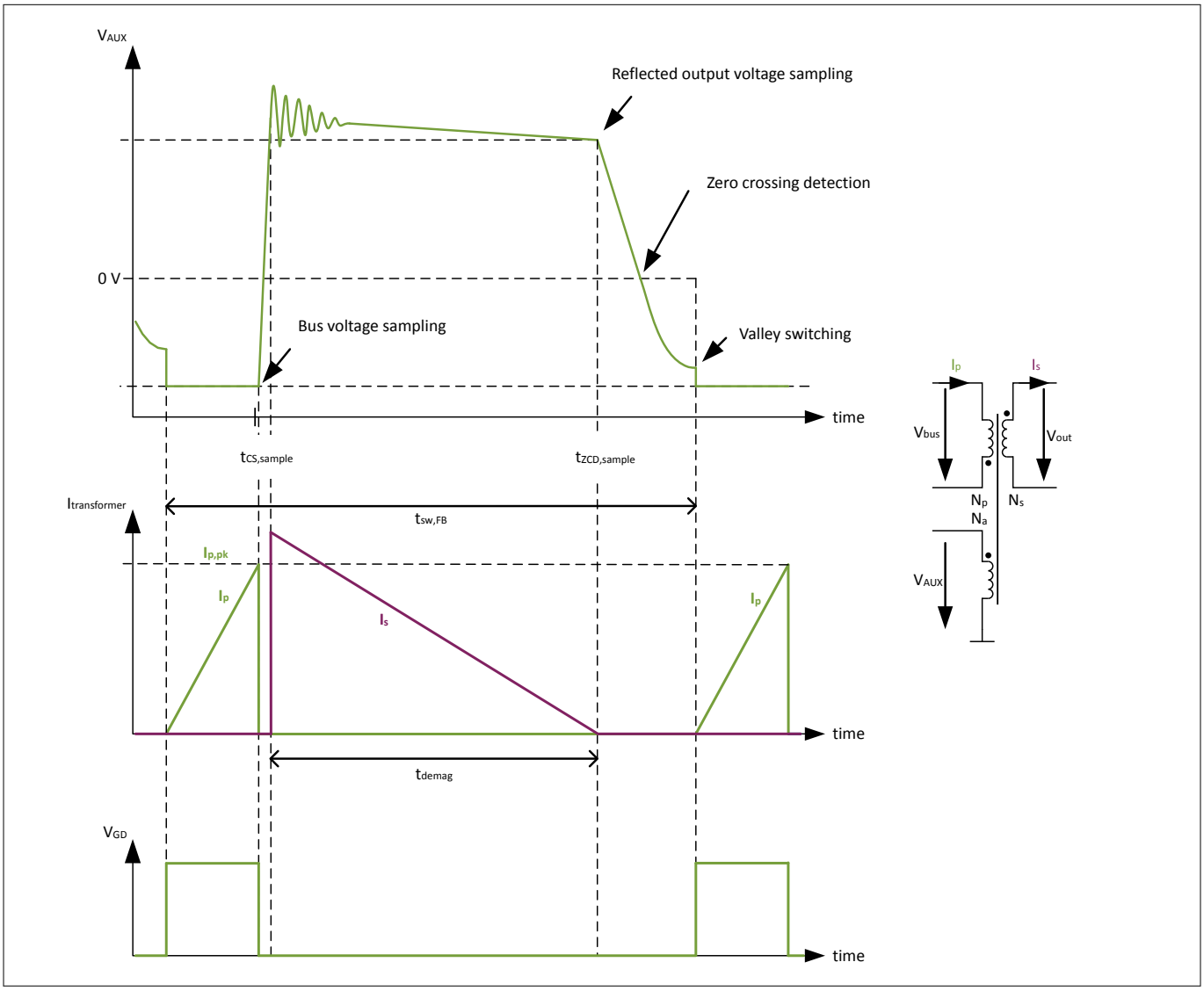


Figure 15 Typical Waveforms of a Flyback Converter

3.2.1.1 Primary Side Current Sensing

The primary side peak current $I_{p,pk}$ is controlled by the control loop using the $V_{CS,OCP1}$ level at the *CSFB* pin. This control scheme ensures suppression of any variation in the bus voltage.

Several delays exist from the time at which the ***OCP1*** level $V_{CS,OCP1}$ is exceeded at the *CSFB* pin until the gate switches off and the transformer current finally reaches its peak value. For a higher accuracy, the primary peak current $V_{CS,SH}$ is sampled a fixed time before turn-off of the gate. The primary side peak current is used to calculate the secondary side current and for protection. The propagation delay compensation parameter t_{PDC} allows optimization of the accuracy of the primary side peak current:

$$I_{p,pk} = \frac{V_{CS,SH}}{R_{CS,FB}} \cdot \frac{t_{on,FB} + t_{PDC}}{t_{on,FB} - t_{CSFB,offset}}$$

Equation 2

Note: If an RC low pass filter is added in front of the CSFB pin, the related low pass filter delay has to be included in t_{PDC}.

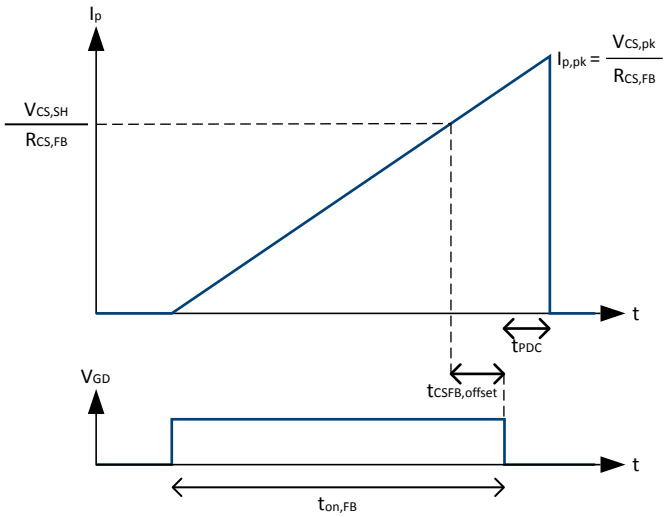


Figure 16 Propagation Delay Compensation for accurate Primary Peak Current Calculation

3.2.1.2 Primary Side Output Voltage Sensing

The output voltage is determined by measuring the reflected output voltage on the auxiliary winding. A resistor divider adapts the voltage to the operating range of the *ZCD* pin.

The output voltage is measured at the *ZCD* pin using the voltage $V_{ZCD,SH}$ at the end of the demagnetization time at the time $t_{ZCD,sample}$. The voltage measured at the *ZCD* pin, the dimensioning of the resistor dividers $R_{ZCD,FB,1}$ and $R_{ZCD,FB,2}$, transformer turns N_s and N_a as well as an offset $V_{out,offset}$ (caused by the secondary diode, for example) are used to calculate the output voltage V_{out} as follows:

$$V_{out} = V_{ZCD,SH} \frac{R_{ZCD,FB,1} + R_{ZCD,FB,2}}{R_{ZCD,FB,2}} \frac{N_s}{N_a} + V_{out,offset}$$

Equation 3

V_{out} is used for ***Primary Side Regulated (PSR)*** control loops in ***CV*** and ***LP*** modes as well as for output over- and undervoltage protections.

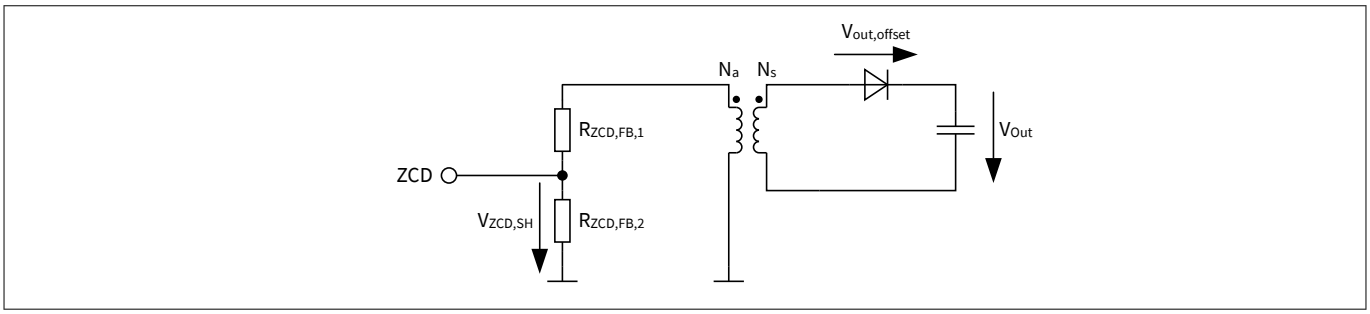


Figure 17 Primary Side Output Voltage Sensing using *ZCD* S&H

Note: Any relation between VCC and ZCD in self-supplied applications can be decoupled – e.g. by adding a linear regulator for VCC.

***Attention*: Please note that the time (t_{demag}) has to be longer than 2.0 µs to ensure that the reflected output voltage can be sensed correctly at the ZCD pin.**

3.2.1.3 Output Current Calculation

The output current is calculated based on the primary side peak current and the timing of the switching cycle.

The output current I_{out} is calculated using the duration of conduction of the output diode t_{demag}, the switching period $t_{sw,FB}$ as well as the number of transformer turns N_p, N_s and the transformer coupling $K_{coupling}$. The following equation is valid in ***QRM1*** and ***DCM***:

$$I_{out} = \frac{1}{2} I_{p,pk} \cdot \frac{N_p}{N_s} \cdot K_{coupling} \cdot \frac{t_{demag}}{t_{sw,FB}}$$

Equation 4

In ***ABM*** the average output current depends on the number of pulses $N_{ABM,PI}$ and the burst period $t_{burst,FB}$:

$$I_{out} = \frac{1}{2} I_{p,pk} \cdot \frac{N_p}{N_s} \cdot K_{coupling} \cdot \frac{t_{demag} \cdot N_{ABM,PI}}{t_{burst,FB}}$$

Equation 5

The coupling of the transformer can be approximated using the transformer primary inductance L_p and the transformer primary leakage inductance $L_{p,lk}$ as follows:

$$K_{coupling} \approx \frac{L_p}{L_p + L_{p,lk}}$$

Equation 6

The calculated current I_{out} is used for the control loop in the modes ***CC*** and ***LP***. The calculated current is also used for output overcurrent protection.

3.2.1.4 Output control scheme

The XDPL8221 includes three different control schemes for a ***CC***, ***CV*** or ***LP*** output.

Different use cases require the controller to operate according to different operation schemes:

- In the case of typical LED strings, the forward voltage of the LED string determines the output voltage of the driver. XDPL8221 operates in ***CC*** and drives a constant output current $I_{out,full}$ to the load. The forward voltage of the connected LED string has to be below a configurable maximum value $V_{out,set}$.

- In the case of LED loads including a power stage (e.g. Infineon BCR linear regulators or Infineon DC/DC buck ILD2111), XDPL8221 operates in ***CV***, ensuring a constant voltage $V_{out,set}$ to the load. The total output current drawn by the load has to be below a configurable maximum value $I_{out,full}$.
- In the case of a high output current setpoint $I_{out,full}$ and an overly long LED string which exceeds the configurable power limit $P_{out,set}$, XDPL8221 operates in ***LP*** to ensure that the power limit of the driver is not exceeded. The controller reduces the output current automatically, ensuring light output without any interruption even for overly long LED strings. The forward voltage of the connected LED string has to be below a configurable maximum value $V_{out,set}$.

For every update of the control loop, the control scheme is selected on the basis of the current operation conditions (output voltage V_{out} and output current I_{out}) and their distance to the three limiting setpoints ($V_{out,set}$, $P_{out,set}$ and $I_{out,full}$):

- For ***CC*** schemes, the internal reference current $I_{out,full}$ is weighted according to thermal management and a dimming curve to yield $I_{out,set}$. The calculated output current I_{out} is compared with the weighted reference current $I_{out,set}$ to generate an error signal for the output current.
- For ***CV*** schemes, the sensed output voltage V_{out} at the *ZCD* pin is compared to a reference voltage $V_{out,set}$ to generate an error signal for the output voltage.
- For ***LP*** schemes, the output current is limited to a maximum of $I_{out,set} = P_{out,set} / V_{out}$.

Out of these three schemes, for each step the most critical error is selected (see ***Figure 18***):

1. If any setpoint is exceeded, the largest error for power decrease is selected to bring the controller back to the desired operating point as quickly as possible.

2. If the current operating conditions are below all three setpoints, the smallest error for power increase is selected to avoid overshooting any setpoint.

The selected error signal is fed into a compensator to control the gate driver switching parameters (i.e. duty cycle and frequency) for the power MOSFET of the ***FB***.

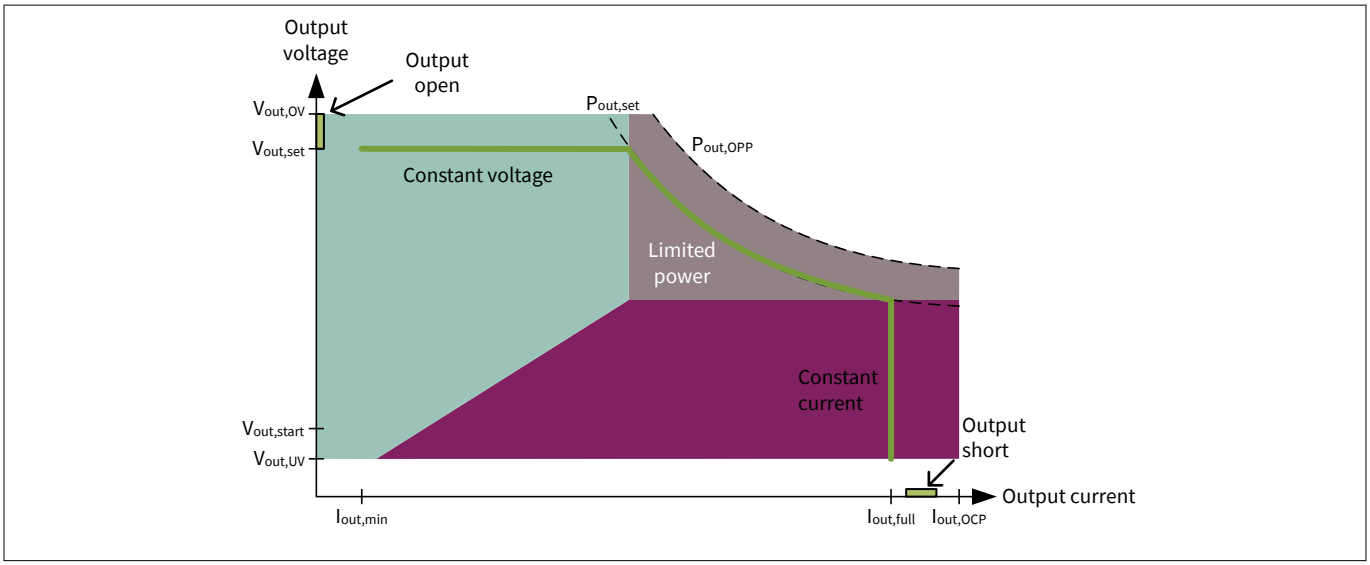


Figure 18 Control scheme for CC/CV/LP modes (non-dimmed)

In dimming cases, the output current setpoint $I_{out,set}$ is located between $I_{out,min}$ and $I_{out,full}$ and varies according to the sensed ***PWM*** duty cycle D_{DIM}. Dimming can be visualized by moving the vertical line for the output current setpoint in ***Figure 19*** from right to left.

Note: In the limited power mode, the maximum output current is limited to $I_{out,set} = P_{out,set} / V_{out}$. which is smaller than $I_{out,full}$. It can be selected through parameter, whether $I_{out,set}$ or $I_{out,full}$ should be mapped to 100% dimming level. If the $I_{out,full}$ is mapped to 100% dimming level in the limited power mode, the dimmer will experience the dead-travel between $I_{out,set}$ and $I_{out,full}$ (no current change while the dimming level is changing).

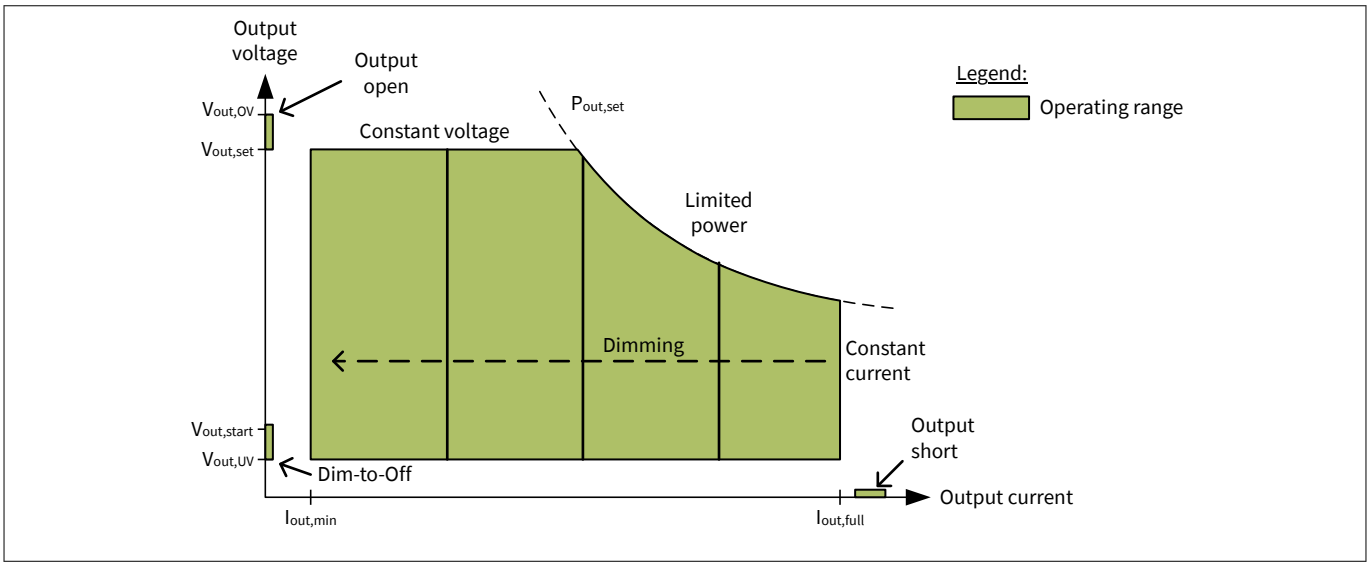


Figure 19 Control scheme for CC/CV/LP modes (including dimming)

One or more of the output control schemes can be deactivated by configuration of the setpoints. Some examples are given below:

- The ***LP*** scheme is not active for $P_{out,set} > V_{out,set} * I_{out,full}$. For such a configuration, the controller will only select between a ***CC*** and ***CV*** scheme.
- The ***CV*** scheme is not active for $V_{out,set} = V_{out,OV}$ as the output overvoltage protection will be triggered.
- The ***CC*** scheme is not active for $I_{out,full} = I_{out,OC}$ as the output overcurrent protection will be triggered.

Compensation of output losses

In case any output of flyback windings is not only supplying a current to LEDs, but also supplying other consumers (e.g. bleeders, CDM10VD, etc.), the primary side regulation of the output current will not be accurate. Parameter G_{loss} allows to compensate ohmic losses on the secondary side:

$I_{out,corrected} = I_{out,uncorrected} + G_{loss} * V_{out}$

Output current slew rate limitation

As the transient response of the ***PFC*** stage is rather slow (especially if the PFC is in low power mode), a fast increase of the flyback power can cause a significant undershoot of the bus voltage. To limit this undershoot, the rising slew rate of the flyback output current can be limited using parameter $I_{out,slew,rate,step}$ as shown in ***Figure 20***.

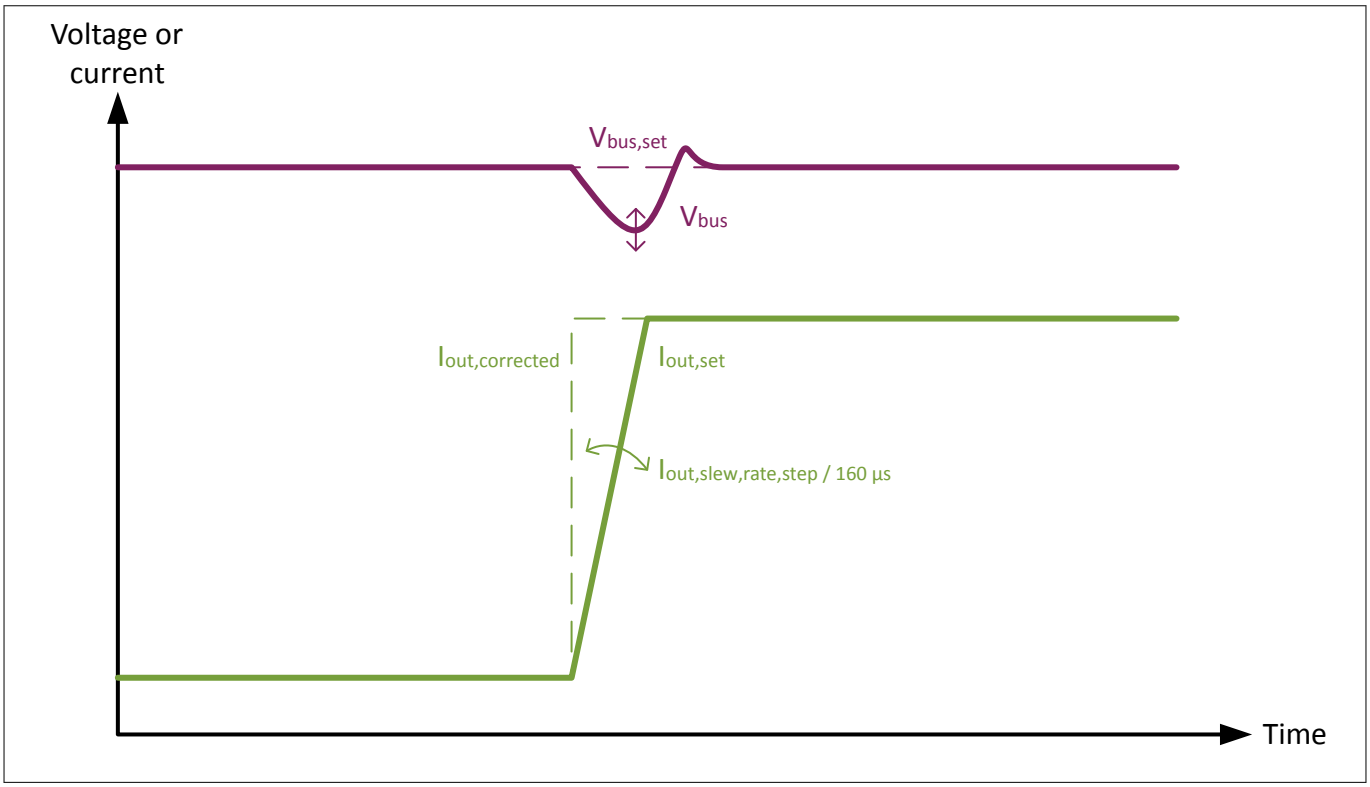


Figure 20 Output slew rate limitation

3.2.1.5 Multimode Scheme

The control loop of XDPL8221 uses three different switching modes: ***QRM1*** is optimized for high efficiency at high loads, ***DCM*** is used for medium loads and ***ABM*** is used for very light load conditions.

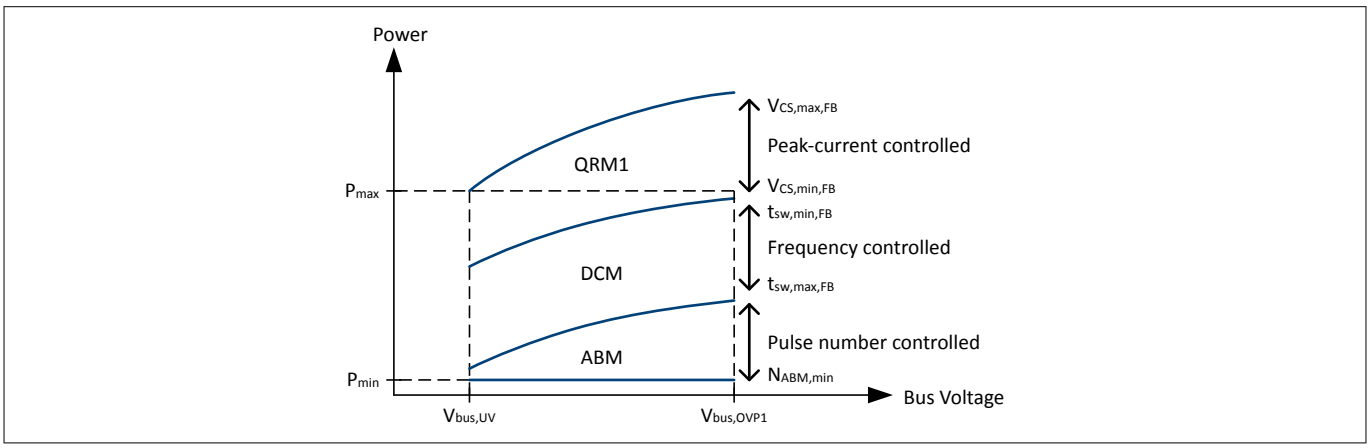


Figure 21 Flyback Multimode Operation Scheme

- ***QRM1***: This mode maximizes the efficiency by switching on the 1st valley of the V_{AUX} signal. This ensures zero current switching with a minimum of switching losses. The power is controlled by regulating the primary peak current using $V_{CS,OCP1}$:

$$P_{out} = \frac{1}{2} \cdot L_p \cdot \left(\frac{V_{CS,OCP1}}{R_{CS,FB}}\right)^2 \cdot \frac{1}{\frac{L_p \cdot V_{CS,OCP1}}{R_{CS,FB} \cdot V_{bus}}\left(1 + \frac{N_s}{N_p}\frac{V_{bus}}{V_{out}}\right) + \frac{t_{OSC,FB}}{2}}$$

Equation 7

- ***DCM***: This mode is used if $V_{CS,OCP1}$has reached its minimum value $V_{CS,min,FB}$. To allow lower output power, the controller extends the switching period $t_{sw,FB}$ later than the 1st valley:

$$P_{out} = \frac{1}{2} \cdot L_p \cdot \left(\frac{V_{CS,min,FB}}{R_{CS,FB}} \right)^2 \cdot \frac{1}{t_{sw,FB}}$$

Equation 8

- ***ABM***: This mode is used if $V_{CS,OCP1}$ cannot be reduced and $t_{sw,FB}$ cannot be increased anymore. To reduce power transfer, the controller will stop switching for some time, causing bursts of pulses:

$$P_{out} = \frac{1}{2} \cdot L_p \cdot \left(\frac{V_{CS,min,FB}}{R_{CS,FB}} \right)^2 \cdot \frac{N_{ABM,PI}}{t_{burst,FB}}$$

Equation 9

  The frequency of the bursts is defined by $1/t_{burst,FB}$. The pulses of each burst have a peak current of $V_{CS,min,FB}$ and a switching frequency of $1/t_{sw,max,FB}$. The number of pulses $N_{ABM,PI}$ is regulated to control the average power transfer during one burst period $t_{burst,FB}$.

The minimum power in DCM is limited by the transformer primary inductance L_p, maximum switching period $t_{sw,max,FB}$, minimum primary peak voltage $V_{CS,min,FB}$, maximum bus voltage $V_{bus,OVP1}$ and two timing parameters:

$$P_{min} = \frac{1}{2} \frac{V_{bus,OVP1}^2}{L_p} \left(\frac{V_{CS,min,FB}}{R_{CS,FB}} \frac{L_p}{V_{bus,OVP1}} + t_{OCP1,FB} + t_{PDC} \right)^2 \frac{1}{t_{sw,max,FB}}$$

Equation 10

The minimum power in ABM is limited by the transformer primary inductance L_p, burst period $t_{burst,FB}$, minimum number of pulses $N_{ABM,min}$, minimum primary peak voltage $V_{CS,min,FB}$, maximum bus voltage $V_{bus,OVP1}$ and two timing parameters:

$$P_{min} = \frac{1}{2} \frac{V_{bus,OVP1}^2}{L_p} \left(\frac{V_{CS,min,FB}}{R_{CS,FB}} \frac{L_p}{V_{bus,OVP1}} + t_{OCP1,FB} + t_{PDC} \right)^2 \frac{N_{ABM,min}}{t_{burst,FB}}$$

Equation 11

Note: If the load drops below the minimum load of P_{min}, the output voltage will rise up to the output overvoltage threshold $V_{out,OV}$ and trigger the protection. An auto-restart can be used to keep the output voltage close to $V_{out,OV}$ until the load increases again.

3.2.1.6 Active Burst Mode

The sense and control scheme for the active burst mode of the ***FB*** is described.

The typical waveform for the gate drivers, the secondary side flyback transformer current, the output voltage and the bus voltage are shown in the figure. The bursts are repeated with a configurable burst period $t_{burst,FB}$. It is advised to choose a burst frequency faster than 200 Hz to ensure a sufficient light quality and reduce output ripple. On the other hand, the burst frequency should not be too high as the human ear is more sensitive to higher frequencies.

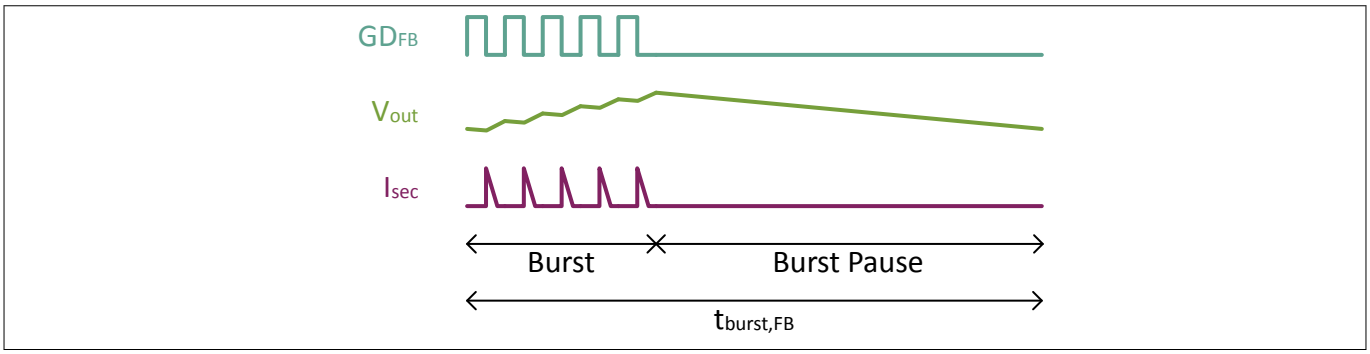


Figure 22 Example Waveforms in Active Burst Mode (not drawn to scale)

The ***FB*** switching pulses of each burst will boost the output voltage to a higher level. During the burst pause, the output voltage drops due to the load of the power converter.

To control the average output current or the average output voltage, the ***FB*** controller calculates the average secondary current and measures the output voltage once at the beginning and once at the end of each burst. These measurements are used to calculate the average output current and average output voltage for the complete burst. Based on these average values, the control loop updates the number of pulses per burst.

3.2.2 Flyback Startup

After startup, the ***FB*** of the XDPL8221 initiates a soft start to minimize the switching stress for the power MOSFET and secondary diode.

The controller switches with a configurable switching frequency of $f_{sw,start,FB}$ and increases the cycle-by-cycle current limit in steps of $V_{CS,step}$ with a configurable duration $t_{softstart}$ for each step. After the final $V_{CS,OCP1,start}$ limit level has been reached, the output will be charged until the minimum output voltage $V_{out,start}$, which ensures self-supply has been reached. At this condition, ***Continuous Conduction Mode (CCM)*** protection as well as output undervoltage protection are activated and the control loop takes over. The starting point for the control loop is to operate in ***ABM*** at lowest number of pulses, lowest switching frequency and lowest primary peak-current. These switching parameters avoid an overshoot of output current for a LED string with low forward voltage when dimmed down to a low output current.

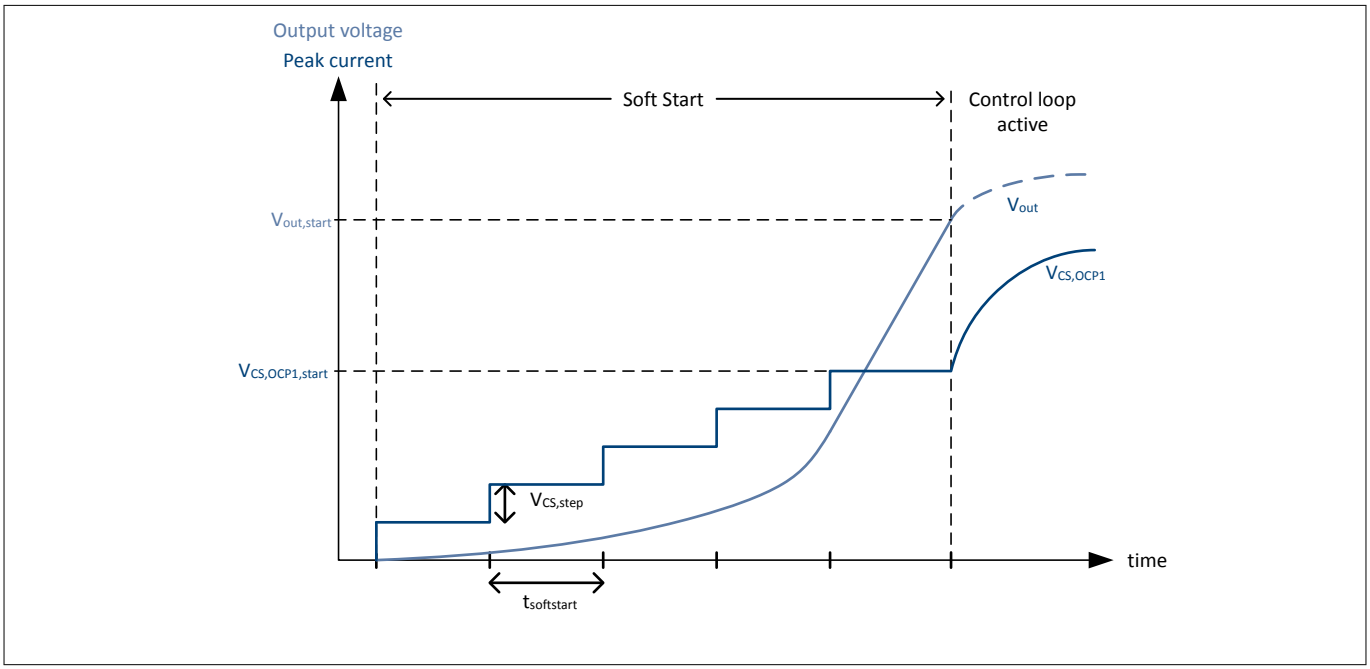


Figure 23 Flyback Startup Sequence

3.2.3 Protection features

Protections ensure the operation of the controller under restricted conditions. The protection monitoring signal(s) sampling rate, protection triggering condition(s) and protection reaction are described in this section.

Attention**: **The sampled protection monitoring signal accuracy is subjective to the digital quantization, tolerances of components (including Integrated Circuit (IC)) and estimations with indirect sensing (e.g. input and output voltage estimations based on ZCD, CS pin signals), while the protection level triggering accuracy is subjective to the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. reflected output voltage signal cannot be sensed by ZCD pin near AC input phase angle of 0° and 180°) and blanking time.

3.2.3.1 Primary Over-current Protection

The primary side over-current protection implemented in hardware covers fault conditions like a short in the transformer primary winding or an open *CS* pin.

The primary side current is compared to an over-current protection threshold $V_{CS,OCP2}$. If the threshold is exceeded for longer than the blanking time $t_{OCP2,FB}$, the protection will be triggered.

3.2.3.2 Output Under-voltage Protection

In case of a short of the output or an overload, the output voltage may drop to a low level. Detection of under-voltage in the output voltage V_{out} is enabled by measurement of the reflected voltage at the *ZCD* pin.

During operation, the output voltage is compared to a configurable under-voltage protection threshold $V_{out,UV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,out,UV}$, the protection will be triggered.

During startup,a shorted output or a strong capacitive loading may not allow the controller charging the output voltage to $V_{out,UV,start}$ within a timeout of $t_{start,max,FB}$. If this timeout expires the protection will be triggered. The timeout starts when the controller starts switching.

Note: The startup under-voltage threshold $V_{out,UV,start}$ has to be configured sufficiently above the under-voltage threshold $V_{out,UV}$ to allow undershoots at start-up which may occur, especially for resistive loads which already consume power from the beginning.

Attention**: **Output under-voltage protection is not available while the controller operates in ABM.

3.2.3.3 Output Over-voltage Protection

In case of a open output, the output voltage may rise to a high level. Over-voltage detection of the output voltage V_{out} is provided by measurement at the *ZCD* pin.

The output voltage is compared to an over-voltage protection threshold $V_{out,OV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,out,OV}$, the protection will be triggered.

Note: The blanking time $t_{blank,Vout,OV}$ must be taken into account because overshoots of the output voltage above the protection threshold can occur due to this time.

Note: This protection is usually triggered if the output is open or the output load drops below the minimum load P_{min}.

Attention**: **Output over-voltage protection is not available while the controller operates in ABM.

3.2.3.4 Output Over-current Protection

Over-current detection in the output current I_{out} is provided on the basis of the calculated output current.

The calculated output current is compared to a configurable over-current protection threshold $I_{out,OC}$. If the threshold is exceeded for longer than the blanking time $t_{blank,out,OC}$, the protection will be triggered.

3.2.3.5 Output Over-power Protection

Over-power detection in the output power P_{out} is provided on the basis of the calculated output power.

The calculated output power is compared to a configurable over-power protection threshold $P_{out,OP}$. If the threshold is exceeded for longer than the blanking time $t_{blank,out,OP}$, the protection will be triggered.

3.2.3.6 Other Flyback Protections

XDPL8221 includes additional protections to ensure the integrity and correct flow of the firmware.

- A hardware weak pull-up protects against an open *CSFB* pin. The *CSFB* OCP2 will be triggered for an open *CSFB* pin.
- A firmware watchdog protects against the *CSFB* pin becoming shorted to *GND*. The protection triggers if the sampled *CSFB* voltage is less than 97.6 mV for longer than the blanking time of $t_{softstart}$.
- A firmware state monitor supervises correct operation of the flyback in ***QRM1***, ***DCM*** or ***ABM***. A protection is triggered if the flyback enters ***CCM***.
- A firmware plausibility check ensures that both bus voltage measurements using the *ZCD* and*VS* pins are consistent.
- A firmware watchdog supervises correct data handling of the flyback.

3.2.3.6.1 Flyback Bus Voltage Sensing

The ***FB*** can sense the bus voltage using the reflection of bus voltage on the auxiliary winding while the gate is turned on. A resistor divider adapts the negative voltage to the operating range of the *ZCD* pin. This second measurement path is required to protect against component failures in the *VS* measurement path (open loop protection for the ***PFC*** stage).

The reflected bus voltage appears as a negative voltage at V_{AUX}. This negative voltage is internally clamped at the *ZCD* pin to the negative voltage V_{INPCLN}. The internal clamping current I_{ZCD} is measured at the end of the on-time at the time $t_{CS,sample}$. The measured clamping current of the *ZCD* pin, the dimensioning of the resistor dividers $R_{ZCD,FB,1}$ and $R_{ZCD,FB,2}$ as well as the number of transformer turns N_a and N_p are used to calculate the bus voltage $V_{bus,FB}$ as follows:

$$V_{bus,FB} = \left(\left(I_{ZCD} + \frac{V_{INPCLN}}{R_{ZCD,FB,2}}\right)R_{ZCD,FB,1} + V_{INPCLN}\right)\frac{N_p}{N_a}$$

Equation 12

$V_{bus,FB}$ is used for a plausibility check with the bus voltage V_{bus} as measured using the *VS* pin.

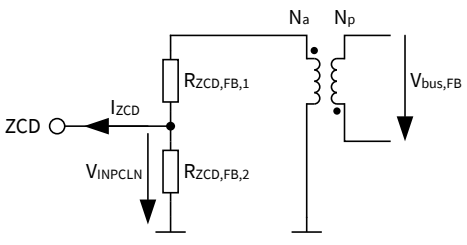


Figure 24 Bus Voltage Sensing using ZCD Clamp Current

3.3 General Controller Features

XDPL8221 provides general features using device level measurements (DLM) for firmware task scheduling, VCC control and temperature control which are independent of the target application.

3.3.1 Configurable Gate Driver Strengths

The gate driver output signals can be configured with respect to their rising slopes for switching on the power MOSFET and with respect to their high voltage levels.

This feature can save BOM components (1 diode & 1 resistor per gate driver) which are conventionally added to achieve the same purpose to lower any ***Electro-Magnetic Interference (EMI)***.

3.3.2 External Temperature Sensing

The external temperature is measured by measuring the voltage of an ***NTC*** with respect to the internal V_{REF} voltage.

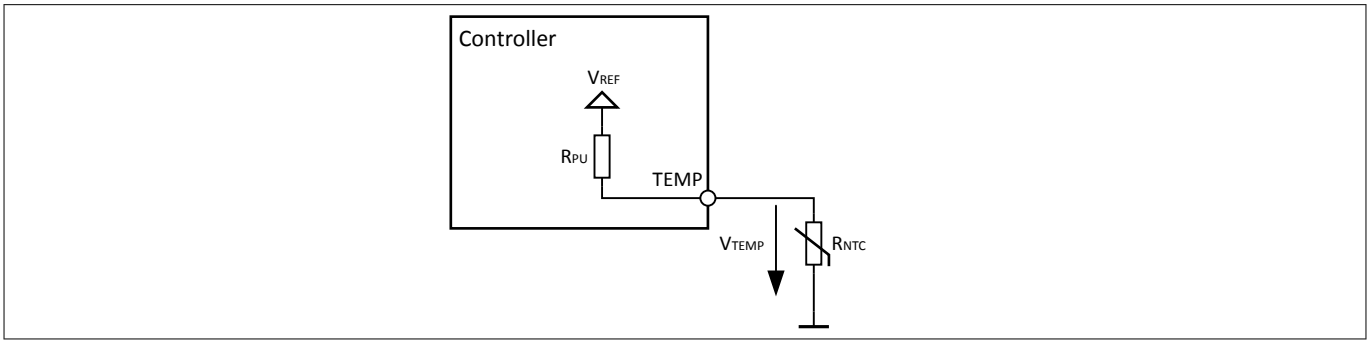


Figure 25 External Temperature Sensing using NTC

The controller calculates the resistance of the ***NTC*** based on the measured voltage V_{Temp}, the internal reference voltage V_{REF} and the internal pull-up resistance R_{PU}:

$$R_{NTC} = \frac{V_{Temp} \cdot R_{PU}}{V_{REF} - V_{Temp}}$$

Equation 13

3.3.3 Adaptive temperature protection

XDPL8221 offers adaptive temperature protection using the external temperature sensor. This feature reduces the output current according to temperature to protect the load and/or driver against overtemperature.

As long as the resistance of the NTC is lower than the temperature threshold $R_{NTC,hot}$ of the NTC, the current is gradually reduced from the maximum current $I_{out,set}$, as shown in ***Figure 26***. If the resistance of the NTC is higher than threshold $R_{NTC,hot}$, the output current is gradually increased again. This allows the controller to ensure operation at or below a temperature matching to $R_{NTC,hot}$.

If a reduction down to a minimum current $I_{out,red}$ is not able to compensate for any continued increase in temperature (causing a continuing reduction of NTC resistance), XDPL8221 will trigger external overtemperature protection if the external sensor exceeds $R_{NTC,critical}$.

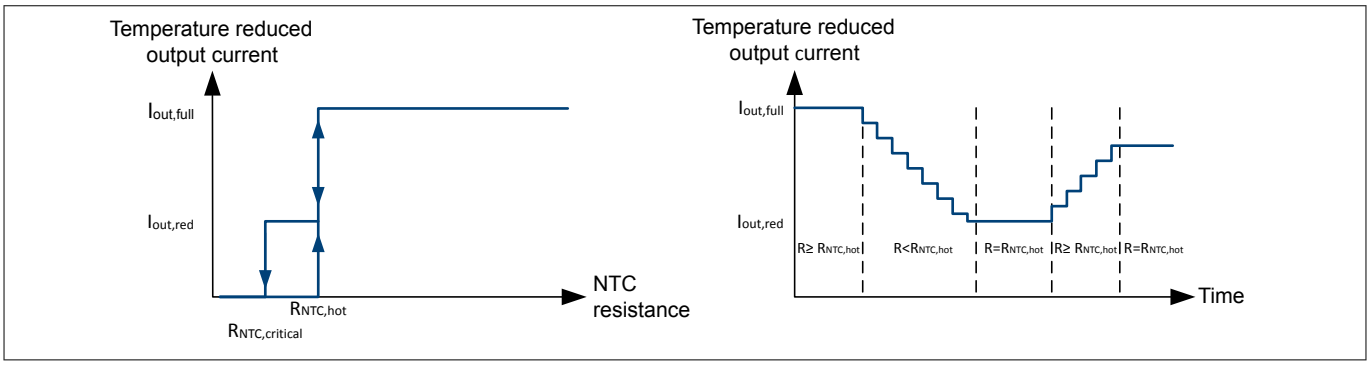


Figure 26 Adaptive temperature protection for external sensors

3.3.4 PWM Dimming Interface

The duty cycle sensed at the *PWM* pin is used to determine the output current level. The XDPL8221 can be configured to use either a linear or a quadratic dimming curve. Either normal or inverted dimming curves can be selected.

Figure 27 shows the relationship of the ***PWM*** duty cycle to the output current target value. Configurable levels $D_{DIM,min}$ and $D_{DIM,max}$ ensure that the minimum current $I_{out,min}$ and maximum current $I_{out,set}$ can always be achieved, thereby making the application robust against component tolerances. The dimming curve can be mirrored by changing its direction from normal to inverted ***PWM*** duty cycle.

An optional hysteresis can be enabled for the sensing of the ***PWM*** signal. This hysteresis can suppress jitter in the ***PWM*** signal. Any change of the ***PWM*** duty cycle within the hysteresis will not affect the output current.

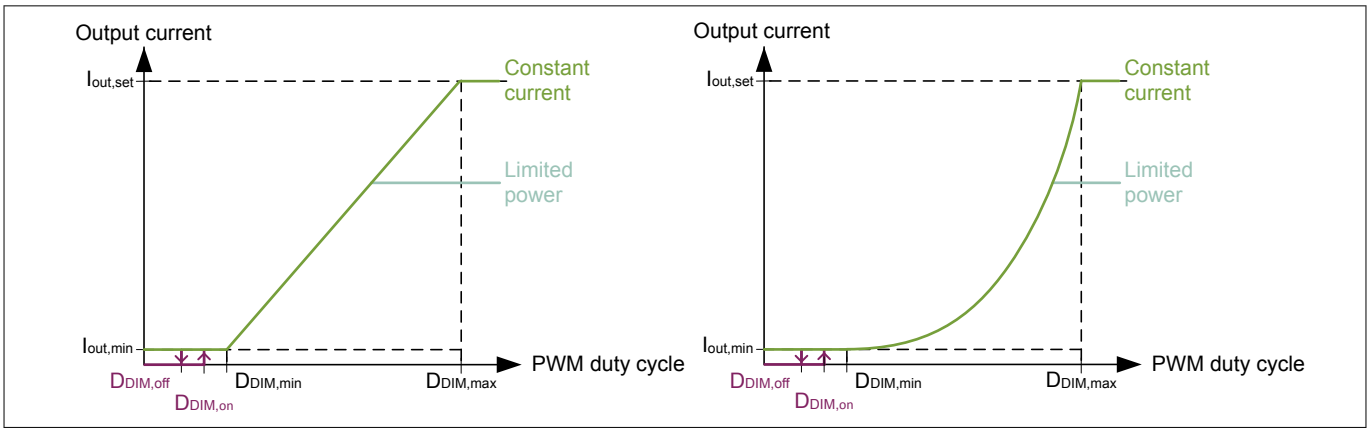


Figure 27 Selectable Dimming Curves

Using the optional Dim-to-Off feature, the light output can be stopped without removal of input voltage. In Dim-to-Off, the controller will enter auto-restart operation to minimize power consumption. The auto-restart recharges the output voltage to a minimum output voltage of $V_{out,start}$ to measure the ***PWM*** duty cycle during a time of $t_{blank,DIM,off}$. After $t_{blank,DIM,off}$, the controller decides if it stays in Dim-to-off by triggering an auto-restart or if it starts the control loop. With the Dim-to-Off feature, the output voltage can be maintained in a specific range by configuration of the startup voltage $V_{out,start}$ and auto-restart time t_{AR}, and by dimensioning of an active or passive output bleeder. If $V_{out,start}$ is configured to be low enough below the minimum forward voltage of the ***LED*** string, the ***LED***s will show no light in this state.

Note: A sufficient output bleeder is required to allow the controller to maintain the output voltage if the Dim-to-Off feature is enabled.

Dim-to-Off is entered if the ***PWM*** duty cycle exceeds the configurable threshold $D_{DIM,off}$ (see purple line in ***Figure 27***). As soon as the duty cycle exceeds $D_{DIM,on}$, the controller will start to continuously regulate output voltage or output current again.

In case the product of output current and output voltage would exceed the power limit, the controller will automatically enter the ***LP*** mode by reducing the output current to achieve the configured power limit (see light blue curve in ***Figure 27***). As a consequence, the dimmer may show extended dead travel at the highest output level. When dimming down, as soon as the product of dimmed output current and output voltage drops below the power limit, the output current will follow the regular dimming curve (green curve).

3.3.5 UART Command Interface

The ***UART*** command interface allows to control the operation of the ***LED*** driver as well as reading out status information from the controller. The electrical ***UART*** interface and the protocol are described.

XDPL8221 uses a common half-duplex ***UART*** interface with a baudrate of 57.600 baud. In half-duplex mode, both communication partners share one line to exchange data with a wired-AND structure. Therefore, both data transmit outputs (driver type: open-drain) are connected together to a common pull-up resistor to maximum 3.3 V. The value of the resistor define the rise time of the data signal at a 0-1 transition. The data receivers are connected to the same line and are always active to detect data collision. Each device also reads the data it is currently transmitting and checks the read data against the data that was intended to be written. In case of a mismatch, a data collision has occurred.

The ***UART*** communication is based on data bytes with 8 bit width, LSB first as shown in ***Figure 28***. Each data transfer starts with a start bit at low level and stops with two stop bits at high level (STOP). The idle level of the transmit and receive signals is the high level.

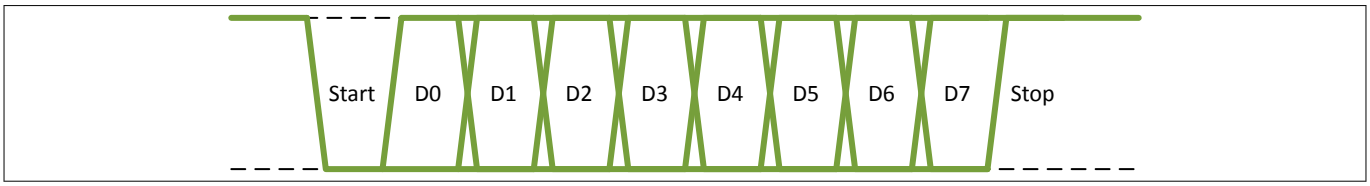


Figure 28 UART Byte Frame

Before a command is send, sending one or multiple SYNC commands (0x7F) is recommended. If a ***UART*** sync request occurs during a power saving state, the XDPL8221 will first recharge it's *VCC* voltage before responding with an ACK (0x00). After the XDPL8221 answered one or more sync requests with ACK, the external master can send subsequent GET or SET commands. The ***UART*** communication has to finish within a configurable timeout, otherwise a *VCC* undervoltage can occur.

In case ***UART*** communication is requested while the XDPL8221 is in power-saving state, a SYNC command will trigger a wakeup. In preparation of the communication, the XDPL8221 will first charge up the *VCC*. This ensures a wakeup with full *VCC* to be ready for communication. The XDPL8221 will be available for communication for a timeout of t_{UART} which can be adjusted based on the *VCC* capacitance. After the timeout, the XDPL8221 will continue with the protection reaction which was interrupted by the communication.

*Note: The **UART** line is pulled low for typically 500 µs during an auto-restart of the XDPL8221. This must not be misinterpret as **UART** frame error by other **UART** devices.*

A GET or SET command frame consists of 9 bytes as listed in ***Table 2***. The time between each byte must not exceed $t_{UART,intra\text{-}byte}$. The checksum at the end of the command ensures that XDPL8221 does not react to any disturbed communication. The checksum is the XOR combination of the previous bytes of the command.

Table 2 UART Commands

Command	Class	Command	ARG0	ARG1	ARG2	ARG3	ARG4	ARG5	Checksum
SYNC	0x7F	-	-	-	-	-	-	-	-
GET status	0x7C	0x04	0x41	ID	0x00	0x00	0x00	0x00	0xXX
GET internal temperature	0x7C	0x04	0x44	ID	0x00	0x00	0x00	0x00	0xXX
GET external NTC resistance	0x7C	0x04	0x45	ID	0x00	0x00	0x00	0x00	0xXX

Table 2 UART Commands (continued)

Command	Class	Command	ARG0	ARG1	ARG2	ARG3	ARG4	ARG5	Checksum
GET output voltage	0x7C	0x04	0x64	ID	0x00	0x00	0x00	0x00	0xXX
GET RMS input voltage	0x7C	0x04	0x65	ID	0x00	0x00	0x00	0x00	0xXX
GET bus voltage	0x7C	0x04	0x66	ID	0x00	0x00	0x00	0x00	0xXX
GET output current	0x7C	0x04	0x6A	ID	0x00	0x00	0x00	0x00	0xXX
SET non-dimmed current	0x7C	0x84	0x68	ID	Current		0x00	0x00	0xXX
GET non-dimmed current	0x7C	0x04	0x68	ID	0x00	0x00	0x00	0x00	0xXX
SET dimming level	0x7C	0x84	0x84	ID	Dimming Level		0x00	0x00	0xXX
GET dimming level	0x7C	0x04	0x84	ID	0x00	0x00	0x00	0x00	0xXX
START	0x7C	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x7C
STOP[1)]	0x7C	0x01	0x00	0x00	0x00	0x00	0x00	0x00	0x7D
SET sleep[2)]	0x7C	0x84	0x4F	0x00	0x00	0x00	0x00	0x00	0xB7

Restrictions apply to the non-dimmed current which can be set via ***UART*** SET command:

- $I_{out,min}$ < current set via ***UART*** < $I_{out,full}$:
  This is the normal operation range. The current will be regulated according to the ***UART*** command.
- Current set via ***UART*** > $I_{out,full}$:
  This case would overload the design. The controller will limit the output current to $I_{out,full}$.
- Current set via ***UART*** < $I_{out,min}$:
  This configuration is not allowed as it causes an invalid dimming curve. The ***UART*** master must not program a current in this range.

A response frame can consist of either 1 byte or 9 bytes. As the power stage is a noisy environment, the ***UART*** communication may occasionally be disturbed. In case of a mismatching checksum of the request or an incomplete frame, XDPL8221 will not provide any response. If a response to a command is missing, the ***UART*** master must not send any new request within $t_{UART,error}$.

Table 3 UART responses to commands

Response	ACK/NACK	ARG0	ARG1	ARG2	ARG3	ARG4	ARG5	ARG6	Checksum
Successful answer to SYNC or SET command	0x00 (ACK)	-	-	-	-	-	-	-	-
Successful response to a GET command	0x00 (ACK)	Value (see coding below)		00	00	00	00	00	0xXX
Generic Error Code for general protocol purposes or used as a non-contextualized generic NACK	0x01	-	-	-	-	-	-	-	-
One of the arguments in the given command is not valid	0x02	-	-	-	-	-	-	-	-
The command is not known	0x03	-	-	-	-	-	-	-	-

1 This command requires external VCC supply. Without external VCC supply, a VCC undervoltage protection will occur.

2 To wakeup from sleep by UART, the "UART during Latch" feature needs to be enabled.

Functional Description

The ID field allows to address one out of multiple XDPL8221s on a shared ***UART*** bus. Only devices with a matching ID will react to a ***UART*** command. Commands can use the broadcast ID 0x00 to address any XDPL8221 on a shared bus. A broadcast GET command will cause a collision on the shared bus in case multiple devices are connected. It is advised to use only GET commands with a device ID to ensure a response from a single, unique device.

*Note: All IDs of any XDPL8221s on a shared **UART** bus must be unique!*

The coding of the electrical values to their digital number representation is listed in ***Table 4***. For all 16 bit values the lower byte is transferred first.

Table 4 Number Representation of Values

Value	Conversion Factor	Offset	Minimum decimal value	Maximum decimal value
Current	4096 LSB / A	0	1 (≡ 244 µA)	40960 (≡ 10 A)
Dimming Level	81.92 LSB / %	0	0 (≡ 0 %[3])	8192 (≡ 100%)
Voltage	16 LSB / V	0	1 (≡ 62.5 mV)	8000 (≡ 500 V)
NTC resistance	1 LSB / Ω	0	0 (≡ 0 Ω)	32768 (≡ 32.768 kΩ)
Temperature	1 LSB / °C	40	0 (≡ -40°C)	190 (≡ 150°C)

The status value of the controller answered to a "GET status" command is coded as listed in ***Table 5***.

Table 5 Coding of Status

Bit	Description
15 to 14	The output current is determined by: • 00: Dimming • 01: Advanced temperature protection • 10: Limited power
13	The flyback regulates in • 0: CC or Limited Power mode • 1: CV mode
12	The dimming level is determined by: • 0: PWM • 1: UART
11	AC or DC input voltage: • 0: AC input voltage • 1: DC input voltage
10 to 9	Current protection reaction is • 00: Auto-restart • 01: Fast Auto-restart • 10: Latch • 11: Stop Mode
8	The on-going protection requires a VCC charging for the restart (1) or not (0)
7	A protection reaction is on-going (1) or not (0)

3 A UART dimming level of 0% triggers dim-to-off if it is enabled.

Table 5 Coding of Status (continued)

Bit	Description
6	A DLM protection was triggered (*Protection*$_{DLM}$ > 0)
5	A FB protection was triggered (*Protection*$_{FB}$ > 0)
4	A PFC protection was triggered (*Protection*$_{PFC}$ > 0)
3 to 0	Bit number of any bit set in either *Protection*$_{PFC}$, *Protection*$_{FB}$ or *Protection*$_{DLM}$ [4)]

The coding of system protections indicated by the value of the lowest 7 bits (bit 0-6) in the ***Table 5*** is given in the following table :

Table 6 Coding of System Protections

Value (bit 6-0)	System Protections
000 0000	No Protection
001 0001	Bus Over-voltage Protection Level 2
001 0010	Input Under-voltage Protection
001 0011	Input Over-voltage Protection
001 0100	PFC CCM Protection
001 0101	PFC Soft-start Failure Protection
001 0110	Bus Under-voltage Protection
001 0111	PFC Over-current Protection Level 2
010 0000	Flyback CS Pin Short to GND Protection
010 0001	Flyback Output Under-voltage Protection at Start-up
010 0010	Flyback Output Under-voltage Protection during Operation
010 0011	Flyback Output Over-voltage Protection
010 0100	Flyback Output Over-current Protection
010 0101	Flyback Over-current Protection Level 2
010 0110	Flyback CCM Protection
010 0111	Flyback Maximum T_{OSC} Exceeding Protection
010 1000	Dim-to-off at Start-up
010 1001	Dim-to-off during Operation
010 1010	Flyback Output Over-power Protection
010 1011	Flyback V_{bus} Plausibility Check Failure Protection
010 1100	Flyback Data Missing Protection
100 0000	External Over-Temperature Protection
100 0001	Internal Over-Temperature Protection
100 0010	Task scheduler protection
100 0011	VCC Under-voltage Lock Out Protection
100 0100	VCC Out of Range Protection

4 This assumes only one bit will be set in all three signals at a time. If multiple bits would be present, only the first error found will be chosen.

Table 6 Coding of System Protections (continued)

Value (bit 6-0)	System Protections
100 0101	RAM Parity Error Protection
100 0110	Watch Dog Error Protection
100 0111	Clock Check Error Protection

3.3.6 Protection features

Protections ensure the operation of the controller under restricted conditions. The protection monitoring signal(s) sampling rate, protection triggering condition(s) and protection reaction are described in this section.

Attention: ***The sampled protection monitoring signal accuracy is subjective to the digital quantization, tolerances of components (including IC) and estimations with indirect sensing (e.g. input and output voltage estimations based on ZCD, CS pin signals), while the protection level triggering accuracy is subjective to the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. reflected output voltage signal cannot be sensed by ZCD pin near AC input phase angle of 0° and 180°) and blanking time.***

3.3.6.1 Overtemperature Protection

Overtemperature protection initiates a shutdown once the critical temperature level $T_{critical}$ or the critical NTC resistance $R_{NTC,critical}$ is exceeded.

If the internal temperature sensor exceeds $T_{critical}$ or the external resistance drops below $R_{NTC,critical}$, XDPL8221 will trigger internal or external overtemperature protection.

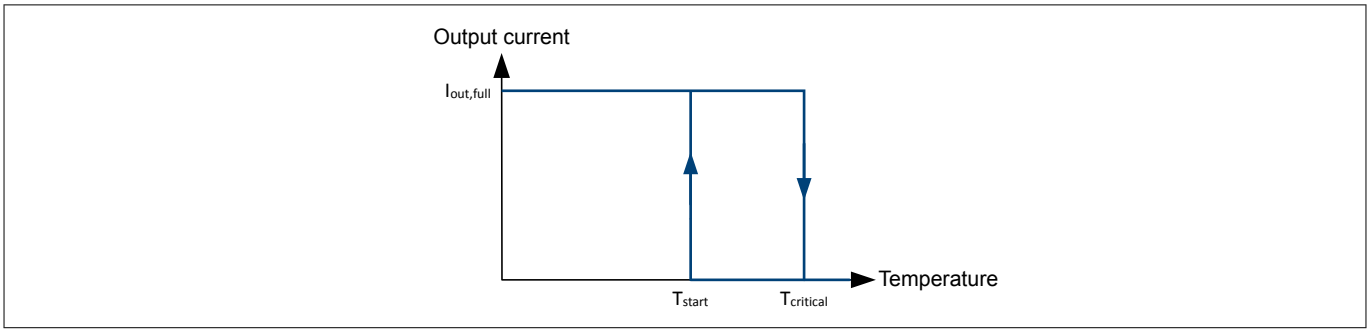


Figure 29 Temperature protection

If the controller is configured to react with auto-restart to internal or external overtemperature protection, it will only restart after the temperature drops below T_{start} and the NTC resistance exceeds $R_{NTC,hot}$.

If latch mode is selected instead, the IC will turn off and only restart after recycling of input power with a temperature below $T_{critical}$.

Note: Please note that the internal temperature sensor can only protect external components which have sufficient thermal coupling to XDPL8221. The external temperature sensor can be used to protect the temperature of external components (e.g. transformer, power MOSFETs or linear regulators).

3.3.6.2 VCC Undervoltage Lockout

A ***Undervoltage Lockout (UVLO)*** is implemented in hardware. It ensures defined enabling and disabling of the ***IC*** operation depending on the supply voltage V_{VCC} at the *VCC* pin in accordance with defined thresholds.

The ***UVLO*** contains a hysteresis with the voltage thresholds V_{VCCon} for enabling the controller and V_{UVoff} for disabling the controller. Once the mains input voltage is applied, current flows through an external resistor into the *HV* pin via the integrated depletion cell and diode to the *VCC* pin. The controller is enabled once V_{VCC}

exceeds the threshold V_{VCCon} and enters normal operation if no fault condition is detected. In this phase, V_{VCC} will drop until either external supply or the self-supply via the auxiliary winding takes over the supply at the *VCC* pin.

Note: The self-supply via the auxiliary winding must be in place before V_{VCC} falls below the V_{UVoff} threshold. Otherwise, the system will perform a fast restart.

Note: It is possible to supply VCC externally from an auxiliary power supply. In this case, the VCC also needs initially to ramp to V_{VCCon} to enable the IC.

3.3.6.3 VCC Overvoltage Protection

Overvoltage protection ensures that the voltage at the VCC pin is not exceeded.

The VCC voltage is compared to a configurable overvoltage protection threshold $V_{VCC,OV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,VCC}$, the protection will be triggered.

Note: The reaction to this protection is fixed to stop mode to ensure a discharge of VCC.

3.3.6.4 VCC Undervoltage Protection

The *VCC* voltage is compared to a configurable undervoltage protection threshold $V_{VCC,UV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,VCC}$, the protection will be triggered.

3.3.6.5 Other General Controller Protections

XDPL8221 includes several protections to ensure the integrity and correct flow of the firmware.

- A hardware watchdog checks correct execution of firmware. A protection is triggered in the event that the firmware does not service the watchdog within a defined period.
- A hardware ***Random Access Memory (RAM)*** parity check triggers a protection if a bit in the memory changes unintentionally.
- A hardware clock check watchdog checks that no clock oscillator is failing.
- A firmware ***Cyclic Redundancy Check (CRC)*** at each startup verifies the integrity of firmware code and its parameters.
- A firmware task execution watchdog triggers a protection if the firmware tasks are not executed as expected.

3.3.7 Protection Reactions

The reaction to each protection can be separately selected. Available reactions may include auto restart, fast auto restart, latch or stop mode.

Figure 30 depicts the timing of an auto-restart reaction:

1. If a protection threshold is exceeded for longer than the related blanking time t_{blank}, the protection is triggered.
2. Within a maximum $t_1 = 4 * 40$ µs, the gate driver of the power stage related to the protection is disabled.
3. Within a maximum $t_2 = 4 * 40$ µs, the gate drivers of other stages are disabled.
4. The reaction depends on the configuration of the protection:
   - In case of latch mode, the application will enter latch mode at this time. No further steps are done, the reaction ends here.
   - In case of stop mode, the application will stop and enter UART parametrization mode which allows to read out the error code. No further steps are done, the reaction ends here.
   - In case of a (fast) auto-restart reaction, the controller will enter a power saving mode for the auto-restart time t_{AR} or $t_{AR,fast}$ respectively.

5. The auto restart may include a new *VCC* charging cycle. The time t_3 typically depends on the input voltage.
6. The first power stage will enable its gate driver according to its startup sequence (soft start) again.
7. The second power stage will enable its gate driver according to its startup sequence (soft start) again. The startup of a subsequent power stage may be delayed by a time t_4 depending on any startup condition for the subsequent stage.

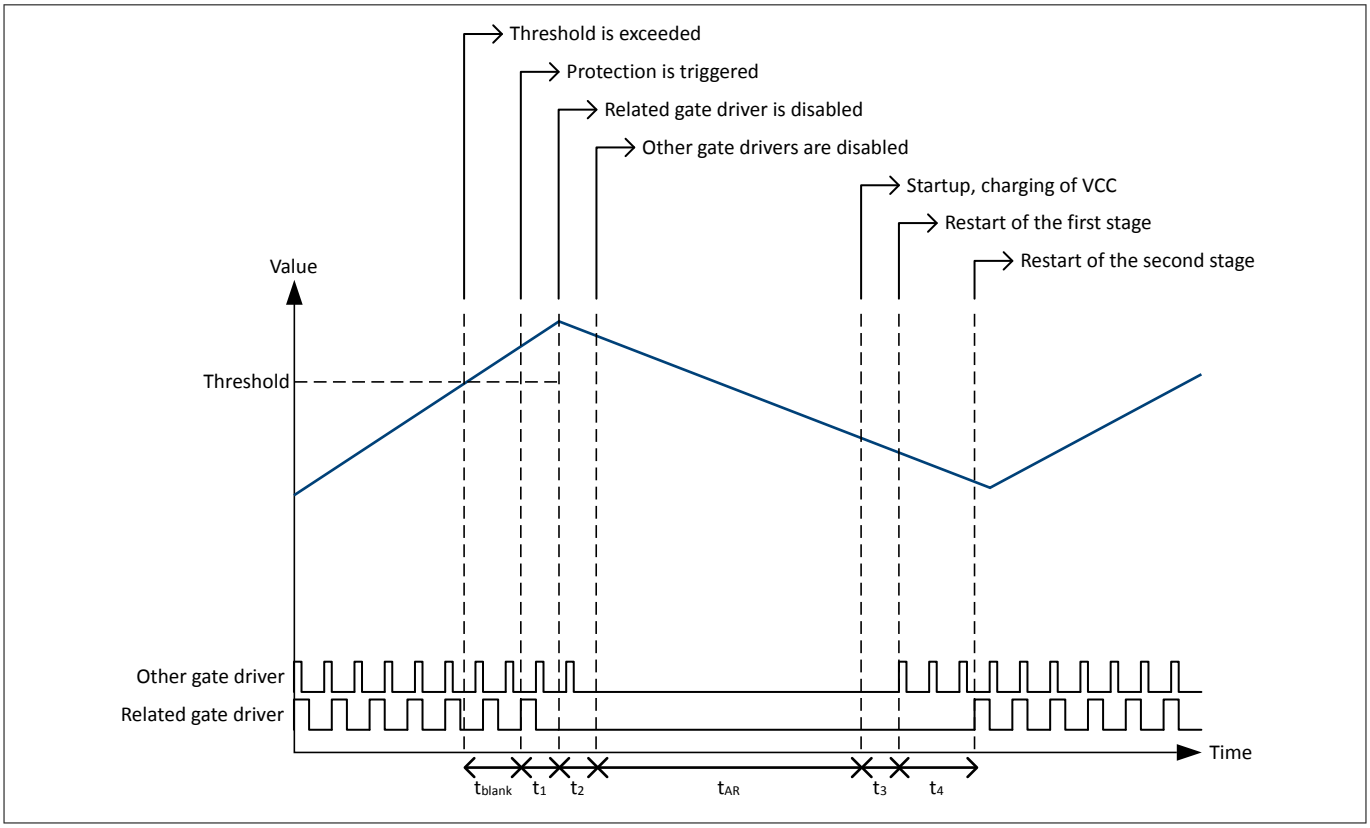


Figure 30 Protection Reaction for auto-restart

For some failures the system may eventually not be able to recover. These failures include:

- PFC OVP2
- PFC OCP2
- Bus voltage plausibility check
- Flyback *CSFB* short to *GND*
- Flyback OCP2
- Flyback oscillation period too long
- Flyback CCM protection
- Flyback output overcurrent protection
- RAM parity
- Watchdog
- Clock check protection
- *VCC* out-of-range protection
- Task Execution protection

For these cases, the controller features a limitation of auto-restarts. The controller will only restart a limited number of times $N_{AR,max}$. Afterward, the controller will latch. The counter for the limited number of restarts is reset whenever a restart due to a protection without limitation occurs.

3.3.7.1 Auto restart

When auto restart mode is activated, XDPL8221 stops switching at the GD pins. After a configurable auto restart time t_{AR}, XDPL8221 initiates a new startup including recharging of VCC and a soft start.

During the time in which the gate is not switching, the internal HV startup cell is automatically enabled and disabled to keep the VCC voltage between the V_{UVLO} and V_{OVLO} thresholds for the supply of XDPL8221. Due to the recharging of VCC for a restart, the time between stopping and starting gate driver pulses is longer than t_{AR}.

3.3.7.2 Fast Auto Restart

When fast auto restart mode is activated, XDPL8221 stops switching at the GD pins. After a configurable fast auto restart time $t_{AR,fast}$, XDPL8221 initiates a new startup including recharging of VCC and a soft start.

During the time in which the gate is not switching, the internal HV startup cell is automatically enabled and disabled to keep the VCC voltage between the V_{UVLO} and V_{OVLO} thresholds for the supply of XDPL8221. Due to the recharging of VCC for a restart, the time between stopping and starting gate driver pulses is longer than $t_{AR,fast}$.

3.3.7.3 Latch Mode

When latch mode is activated, XDPL8221 stops switching at the GD pins. The device stays in this state until input voltage is completely removed and the VCC voltage drops below the V_{UVLO} threshold. Only then can XDPL8221 be restarted by applying input voltage.

To maintain this state, the internal HV startup cell is automatically enabled and disabled to keep the VCC voltage between the V_{UVLO} and V_{OVLO} thresholds for the supply of XDPL8221. The current consumption is reduced to a minimum.

3.3.7.4 Stop Mode

When stop mode is activated, XDPL8221 stops switching at the GD pins. XDPL8221 enters ***UART*** communication mode to allow debugging of the system state.

Note: The VCC for XDPL8221 needs to be supplied by an external source. Without an external supply, VCC will drain to V_{UVLO} and XDPL8221 performs a restart.

4 Electrical Characteristics and Parameters

All signals are measured with respect to the ground pin, GND. The voltage levels are valid provided other ratings are not violated.

4.1 Package Characteristics

Table 7 Package Characteristics

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Thermal resistance for PG-DSO-16	R_{thJA}	—	119	K/W	

4.2 Absolute Maximum Ratings

Attention: ***Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.***

Table 8 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Voltage externally supplied to pin VCC	V_{VCCEXT}	–0.5	26	V	voltage that can be applied to pin VCC by an external voltage source
Voltage at pin GDx	V_{GDx}	–0.5	V_{VCC} + 0.3	V	if gate driver is not configured for digital I/O
Junction temperature	T_J	–40	125	°C	max. operating frequency 66 MHz f_{MCLK}
Storage temperature	T_S	–55	150	°C	
Soldering temperature	T_{SOLD}	—	260	°C	Wave Soldering [5]
Latch-up capability	I_{LU}	—	150	mA	[6] Pin voltages acc. to abs. max. ratings
ESD capability HBM	V_{HBM}	—	2000	V	[7]
ESD capability CDM	V_{CDM}	—	500	V	[8]
Input Voltage Limit	V_{IN}	–0.5	3.6	V	Voltage externally supplied to pins GPIO, MFIO, CS, ZCD, GPIO, VS, GDx (if GDx is configured as digital I/O). (If not stated different)

5 According to JESD22-A111 Rev A.
6 Latch-up capability according to JEDEC JESD78D, T_A= 85°C.
7 ESD-HBM according to ANSI/ESDA/JEDEC JS-001-2012.
8 ESD-CDM according to JESD22-C101F.

Table 8 Absolute Maximum Ratings (continued)

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Maximum permanent negative clamping current for ZCD and CS	$-I_{CLN_DC}$	—	2.5	mA	RMS
Maximum transient negative clamping current for ZCD and CS	$-I_{CLN_TR}$	—	10	mA	pulse < 500ns
Maximum negative transient input voltage for ZCD	$-V_{IN_ZCD}$	—	1.5	V	pulse < 500ns
Maximum negative transient input voltage for CS	$-V_{IN_CS}$	—	3.0	V	pulse < 500ns
Maximum permanent positive clamping current for CS	I_{CLP_DC}	—	2.5	mA	RMS
Maximum transient positive clamping current for CS	I_{CLP_TR}	—	10	mA	pulse < 500ns
Maximum current into pin VIN	I_{AC}	—	10	mA	for charging operation
Maximum sum of input clamping high currents for digital input stages of device	I_{CLH_sum}	—	300	µA	limits for each individual digital input stage have to be respected
Voltage at HV pin	V_{HV}	-0.5	600	V	

4.3 Operating Conditions

The recommended operating conditions are shown for which the DC Electrical Characteristics are valid.

Table 9 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Junction Temperature	T_J	–40	125	°C	max. 66 MHz f_{MCLK}
Lower VCC limit	V_{VCC}	V_{UVOFF}	—	V	device is held in reset when $V_{VCC} < V_{UVOFF}$
Voltage externally supplied to VCC pin	V_{VCCEXT}	—	24	V	maximum voltage that can be applied to pin VCC by an external voltage source
Gate driver pin voltage	V_{GD}	–0.5	V_{VCC} + 0.3	V	

4.4 DC Electrical Characteristics

The electrical characteristics provide the spread of values applicable within the specified supply voltage and junction temperature range, T_J from -40 °C to +125 °C.

Devices are tested in production at T_A = 25 °C. Values have been verified either with simulation models or by device characterization up to 125 °C.

Typical values represent the median values related to T_A = 25 °C. All voltages refer to GND, and the assumed supply voltage is V_{VCC} = 18 V if not otherwise specified.

Note: Not all values given in the tables are tested during production testing. Values not tested are explicitly marked.

Attention: The Vcc pin voltage must be higher than 3.4V before the voltage of any other pins (except GND and HV pins) exceeds 1.2V.

Table 10 Power Supply Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC_ON threshold	V_{VCCon}	—	V_{SELF}	—	V	Self-powered startup (default)
VCC_ON_SELF threshold	V_{SELF}	19	20.5	22	V	dV_{VCC}/dt = 0.2 V/ms
VCC_ON_SELF delay	t_{SELF}	—	—	2.1	µs	Reaction time of V_{VCC} monitor
VCC_UVOFF current	$I_{VCCUVOFF}$	5	20	40	µA	$V_{VCC} < V_{SELF}$(min) - 0.3 V or $V_{VCC} < V_{EXT}$(min) - 0.3 V [9]
UVOFF threshold	V_{UVOFF}	—	6.0	—	V	SYS_CFG0.SELUVTHR = 0_B
UVOFF threshold tolerance	Δ_{UVOFF}	—	—	±5	%	This value defines the tolerance of V_{UVOFF}
UVOFF filter constant	t_{UVOFF}	600	—	—	ns	1V overdrive
UVLO (UVWAKE) threshold	V_{UVLO}	—	V_{UVOFF} · 1.25	—	V	
UVWAKE threshold tolerance	Δ_{UVLO}	—	—	±5	%	This value defines the tolerance of V_{UVLO}
UVLO (UVWAKE) filter constant	t_{UVLO}	0.6	—	2.2	µs	1 V overdrive
OVLO (OVWAKE) threshold	V_{OVLO}	—	V_{SELF}	—	V	
OVLO (OVWAKE) filter constant	t_{OVLO}	0.6	—	2.4	µs	1 V overdrive
Nominal range 0% to 100%	V_{ADCVCC}	0	—	V_{REF}	V	$V_{ADCVCC} = 0.09 \cdot V_{VCC}$ [10]
Reduced VCC range for ADC measurement	R_{ADCVCC}	8	—	92	%	[11][12]

9 Tested at V_{VCC} = 5.5 V
10 Theoretical minimum value, real minimum value is related to V_{UVOFF} threshold.
11 Operational values.
12 Note that the system is turned off if $V_{VCC} < V_{UFOFF}$.

Table 10 Power Supply Characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum error for ADC measurement (8-bit result)	$TET0_{VCC}$	—	—	3.8	LSB_8	
Maximum error for ADC measurement (8-bit result)	$TET256_{VCC}$	—	—	5.2	LSB_8	
Gate driver current consumption excl. gate charge current	I_{VCCGD}	—	0.26	0.35	mA	$T_j \leq 125°C$
VCC quiescent current in PMD0	$I_{VCCPMD0}$	—	11	13	mA	All registers have reset values, clock is active at 66 MHz, CPU is stopped, $T_j \leq 85$ °C
VCC quiescent current in PMD0	$I_{VCCPMD0}$	—	—	14.5	mA	All registers have reset values, clock is active at 66 MHz, CPU is stopped, $T_j \leq 125$ °C
VCC quiescent current in power saving mode PSDM3 with standby logic active	$I_{VCCPSMD3}$	—	0.25	0.45	mA	$T_j \leq 125$ °C WU_PWD_CFG = 28_H
VCC quiescent current in power saving mode PSDM4 with standby logic active	$I_{VCCPSMD4}$	—	0.14	0.23	mA	$T_j \leq 125$ °C WU_PWD_CFG = 00_H

Table 11 Electrical Characteristics of the GDFB Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	V_{APD}	—	—	1.6	V	$I_{GD} = 5$ mA
R_{PPD} value	R_{PPD}	—	600	—	kΩ	Permanent pull-down resistor inside gate driver
R_{PPD} tolerance	Δ_{PPD}	—	—	±25	%	Permanent pull-down resistor inside gate driver
Driver output low impedance for GD0	R_{GDL}	—	—	4.4	Ω	$T_J \leq 125$ °C, $I_{GD} = 0.1$ A

Table 11 Electrical Characteristics of the GDFB Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Nominal output high voltage in PWM mode	V_{GDH}	—	10.5	—	V	GDx_CFG.VOL = 3, I_{GDH} = –1 mA
Output voltage tolerance	Δ_{VGDH}	—	—	±5	%	Tolerance of programming options if V_{GDH} > 10 V, I_{GDH} = –1 mA
Rail-to-rail output high voltage	V_{GDHRR}	V_{VCC}– 0.5	—	V_{VCC}	V	If V_{VCC} < programmed V_{GDH} and output at high state
Output high current in PWM mode for GD0	$-I_{GDH}$	—	100	—	mA	GDx_CFG.CUR = 8
Output high current tolerance in PWM mode	Δ_{IGDH}	—		±15	%	Calibrated [13]
Discharge current for GD0	I_{GDDIS}	800	—	—	mA	V_{GD} = 4 V and driver at low state
Output low reverse current	$-I_{GDREVL}$	—	—	100	mA	Applies if V_{GD} < 0 V and driver at low state
Output high reverse current in PWM mode	I_{GDREVH}	—	1/6 of I_{GDH}	—		Applies if V_{GD} > V_{GDH} + 0.5 V (typ) and driver at high state

Table 12 Electrical Characteristics of the CSFB Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.0	V	
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming V_{VDDA} = $V_{VDDA,typ}$	V_{OCP2}	—	1.6	—	V	SYS_CFG0.OCP2 = 00_B
Threshold voltage tolerance	Δ_{VOCP2}	—	—	±5	%	Voltage divider tolerance
Comparator propagation delay	t_{OCP2PD}	15	—	35	ns	
Minimum comparator input pulse width	t_{OCP2PW}	—	—	30	ns	
OCP2F comparator propagation delay	$t_{OCP2FPD}$	70	—	170	ns	dV_{CS}/dt = 100 V/µs

13 referred to GDx_CFG.CUR = 16

Table 12 Electrical Characteristics of the CSFB Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Delay from V_{CS} crossing V_{CSOCP2} to begin of GDx turn-off (I_{GD0} > 2mA)	$t_{CSGDxOCP2}$	125	135	190	ns	dV_{CS}/dt = 100 V/µs; f_{MCLK} = 66 MHz. GDx driven by QR_GATE FIL_OCP2.STABLE = 3
OCP1 operating range	V_{OCP1}	0	—	$V_{REF}/2$	V	RANGE =00_B
OCP1 threshold at full scale setting (CS_OCP1LVL=FF_H) for CS0	V_{OCP1FS}	1192	1229	1266	mV	RANGE =00_B
Delay from V_{CS} crossing V_{CSOCP1} to CS_OCP1 rising edge, 1.2 V range	t_{CSOCP1}	90	170	250	ns	Input signal slope dV_{CS}/dt = 150 mV/µs. This slope represents a use case of a switch-mode power supply with minimum input voltage.
Delay from CS_OCP1 rising edge to QR_GATE falling edge	$t_{OCP1GATE}$	—	—	12	ns	STB_RET31. OCP_ASM_SEL=0
Delay from QR_GATE falling edge to start of GDx turn-off	$t_{GATEGDx}$	1	3	5	ns	GDx driven by QR_GATE. Measured up to I_{GDx} > 2 mA
OCP1 comparator input single pulse width filter	t_{OCP1PW}	60	—	95	ns	Shorter pulses than min. are suppressed, longer pulses than max. are passed
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/2$	V	CS_ICR.RANGE =00_B
Reduced S&H operating range	RR_{CVSH}	8	—	92	%	CS_ICR.RANGE =00_B Operational values
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET0_{CS0S}$	—	—	4.7	LSB	CS_ICR.RANGE =00_B
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET256_{CS0S}$	—	—	6.0	LSB	CS_ICR.RANGE =00_B
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/6$	V	CS_ICR.RANGE =11_B
Reduced S&H operating range	RR_{CVSH}	20	—	80	%	CS_ICR.RANGE =11_B Operational values

Table 12 Electrical Characteristics of the CSFB Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET0_{CS0S}$	—	—	8.0	LSB	CS_ICR.RANGE =11_B
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET256_{CS0S}$	—	—	8.7	LSB	CS_ICR.RANGE =11_B
S&H delay of input buffer	t_{CSHST}	—	—	510	ns	Referring to jump in input voltage. Limits the minimum gate driver T_{on} time.

Table 13 Electrical Characteristics of the ZCD Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.3	V	
Input clamping current, high	I_{CLH}	—	—	100	µA	
Zero-crossing threshold	V_{ZCTHR}	15	40	70	mV	
Comparator propagation delay	t_{ZCPD}	30	50	70	ns	dV_{ZCD}/dt = 4 V/µs
Input voltage negative clamping level	$-V_{INPCLN}$	140	180	220	mV	Analog clamp activated
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	4	mA	CRNG =00_B Gain = 600 mV/mA
Reduced I/V-conversion operating range	RR_{IV}	5	—	80	%	
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{IV}$	—	—	4.1	LSB_8	CRNG =00_B
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{IV}$	—	—	9.7	LSB_8	CRNG =00_B

Table 13 Electrical Characteristics of the ZCD Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum deviation between ZCD clamp voltage and trim result stored in OTP	E_{ZCDClp}	—	—	±5	%	$-I_{IV} > 0.25$ mA
IV-conversion delay of input buffer	t_{IVST}	—	—	900	ns	Refers to jump in input current[14]
Nominal S&H input voltage range 0% to 100%	V_{ZSH}	0	—	$2/3 \cdot V_{REF}$	V	SHRNG $=0_B$
Nominal S&H input voltage range 0% to 100%	V_{ZSH}	$V_{REF}/2$	—	$7/6 \cdot V_{REF}$	V	SHRNG $=1_B$
Reduced S&H input voltage range	RR_{ZVSH}	4	—	95	%	
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{ZVS0}$	—	—	3.7	LSB_8	SHRNG $=0_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{ZVS0}$	—	—	4.9	LSB_8	SHRNG $=0_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{ZVS1}$	—	—	4.2	LSB_8	SHRNG $=1_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{ZVS1}$	—	—	5.8	LSB_8	SHRNG $=1_B$
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.0	µs	SHRNG $=0_B$ $T_j \le 125$ °C
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.6	µs	SHRNG $=1_B$ $T_j \le 125$ °C

14 Limits the minimum gate driver T_{on} time.

Table 14 Electrical Characteristics of the VS Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Nominal measurement range 0% to 100%	V_{VS}	0	—	V_{REF}	V	Gain 1, no offset
Nominal measurement range 0% to 100%	V_{VS}	$5/6 \cdot V_{REF}$	—	$7/6 \cdot V_{REF}$	V	Gain 3, with offset
Reduced operating range	RR_{VVS}	5	—	95	%	Gain 1, no offset
Reduced operating range	RR_{VVS}	10	—	90	%	Gain 3, with offset
Maximum error for corrected measurement (8-bit result)	$TET0_{VS}$	—	—	4.1	LSB_8	Range 1, no offset
Maximum error for corrected measurement (8-bit result)	$TET256_{VS}$	—	—	5.6	LSB_8	Range 1, no offset
Maximum error for corrected measurement (8-bit result)	$TET0_{VS}$	—	—	12.0	LSB_8	Range 2, with offset
Maximum error for corrected measurement (8-bit result)	$TET256_{VS}$	—	—	12.9	LSB_8	Range 2, with offset
Overvoltage comparator threshold	THR_{OV}	2.70	2.8	2.90	V	
Overvoltage comparator propagation delay	t_{PDOV}	—	—	300	µs	Step at input

Table 15 Electrical Characteristics of the HV Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Leakage current at HV pin	I_{HVleak}	—	—	10	µA	V_{HV} = 600 V HV startup cell disabled
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	9.6	mA	CURRNG = 11_B
Reduced measurement range for current path	RR_{IMEAS}	5	—	78	%	CURRNG = 11_B. Operational values.
Maximum error for corrected ADC measurement (8-bit result, temperature gain correction applied)	$TET0_{DP}$	—	—	5.7	LSB_8	CURRNG = 11_B

Table 15 Electrical Characteristics of the HV Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum error for corrected ADC measurement (8-bit result, temperature gain correction applied)	$TET256_{DP}$	—	—	6.3	LSB_8	CURRNG = 11_B

Table 16 Electrical Characteristics of the PWM Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{INPUT}	—	—	10	pF	
Input low voltage	V_{IL}	—	—	1.0	V	
Input high voltage	V_{IH}	2.0	—	—	V	
Input leakage current, no pull device	I_{LK}	–5	—	+1	µA	V_{MFIO} = 0 V / 3 V
Input low current with active weak pull-up WPU	$-I_{LPU}$	30	—	90	µA	Measured at max. V_{IL}
Input high current with active weak pull-down WPD	I_{HPD}	90	—	300	µA	Measured at min. V_{IH}
Pull-up resistor value	R_{PU}	—	2.25	—	kΩ	RPU=1111_B
Pull-up resistor tolerance	Δ_{RPU}	—	—	±20	%	Overall tolerance
PWM input frequency	f_{PWM}	500	—	2000	Hz	
PWM duty cycle	D_{PWM}	5	—	95	%	

Table 17 Electrical Characteristics of the TEMP Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
MFIO reference voltage	$V_{MFIOREF}$	—	V_{REF}	—	V	Selection = V_{REF}
Nominal range 0% to 100%	V_{MFIO}	0	—	V_{REF}	V	Gain = 1
Reduced operating range	RR_{VMFIO}	4	—	96	%	Gain = 1. Operational values.
Maximum error for corrected measurement (8-bit result)	$TET0_{MFI0}$	—	—	4.0	LSB_8	Gain = 1
Maximum error for corrected measurement (8-bit result)	$TET256_{MFI0}$	—	—	4.8	LSB_8	Gain = 1

Table 17 Electrical Characteristics of the TEMP Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Offset calibration voltage	V_{CAL}	—	$V_{MFIOREF}/8$	—	V	
Offset calibration voltage absolute tolerance	Δ_{VCAL}	—	—	±3	LSB	Ref. to $V_{MFIOREF}$ =V_{REF}, Gain = 1
Offset calibration voltage variation over temperature	Δ_{VCAL_TMP}	—	—	±1	LSB	Ref. to $V_{MFIOREF}$ =V_{REF}, Gain = 1
Pull-up resistor value	R_{PU}	—	11	—	kΩ	RPU=0110_B
Pull-up resistor tolerance	Δ_{RPU}	—	—	±20	%	Overall tolerance

Table 18 Electrical Characteristics of the CSPFC Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.0	V	
OCP1 operating range	V_{OCP1}	0	—	$V_{REF}/2$	V	RANGE =00_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	1.6	—	V	SYS_CFG0.OCP2 = 00_B
Threshold voltage tolerance	Δ_{VOCP2}	—	—	±5	%	Voltage divider tolerance
Comparator propagation delay	t_{OCP2PD}	15	—	35	ns	
Minimum comparator input pulse width	t_{OCP2PW}	—	—	30	ns	
OCP2F comparator propagation delay	$t_{OCP2FPD}$	70	—	170	ns	dV_{CS}/dt = 100 V/µs
Delay from V_{CS} crossing V_{CSOCP2} to begin of GDx turn-off (I_{GD0} > 2mA)	$t_{CSGDxOCP2}$	125	135	190	ns	dV_{CS}/dt = 100 V/µs; f_{MCLK} = 66 MHz. GDx driven by QR_GATE FIL_OCP2.STABLE = 3
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/2$	V	CS_ICR.RANGE =00_B
Reduced S&H operating range	RR_{CVSH}	4	—	90	%	Operational values
Hysteretic comparator threshold	THR_{HYS}	—	0.54	—	V	1 → 0 transition

Table 18 Electrical Characteristics of the CSPFC Pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Hysteretic comparator threshold	THR_{HYS}	—	1.53	—	V	0 → 1 transition
Hysteretic comparator threshold tolerance	Δ_{THRHYS}	—	—	±120	mV	
Hysteretic comparator propagation delay	t_{PDHYS}	—	90	—	ns	Rising edge
Hysteretic comparator propagation delay	t_{PDHYS}	—	40	—	ns	Falling edge
Hysteretic comparator minimum input pulse width	t_{PWHYS}	—	—	300	ns	

Table 19 Electrical Characteristics of the UART Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	µA	only digital input
Input clamping current, high	I_{CLH}	—	—	100	µA	only digital input
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	V_{APD}	—	—	1.6	V	I_{GD} = 5 mA
Input capacitance	C_{INPUT}	—	—	25	pF	
Input low voltage	V_{IL}	—	—	1.0	V	
Input high voltage	V_{IH}	2.1	—	—	V	
Input low current with active weak pull-up WPU	$-I_{LPU}$	30	—	90	µA	Measured at max. V_{IL}
UART baudrate	f_{UART}	-5%	57600	+5%	baud	
Time between bytes within a UART frame	$t_{UART,intra-byte}$	—	—	500	µs	
Waiting time after a missing response	$t_{UART,error}$	15	—	—	ms	

Table 20 Electrical Characteristics of the GDPFC Pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	V_{APD}	—	—	1.6	V	I_{GD} = 5 mA
R_{PPD} value	R_{PPD}	—	600	—	kΩ	Permanent pull-down resistor inside gate driver
R_{PPD} tolerance	Δ_{PPD}	—	—	±25	%	Permanent pull-down resistor inside gate driver
Driver output low impedance for GD1/2	R_{GDL}	—	—	7.0	Ω	$T_J \leq 125$ °C, I_{GD} = 0.1 A
Nominal output high voltage in PWM mode	V_{GDH}	—	10.5	—	V	GDx_CFG.VOL = 3, I_{GDH} = –1 mA
Output voltage tolerance	Δ_{VGDH}	—	—	±5	%	Tolerance of programming options if V_{GDH} > 10 V, I_{GDH} = –1 mA
Rail-to-rail output high voltage	V_{GDHRR}	V_{VCC}– 0.5	—	V_{VCC}	V	If V_{VCC} < programmed V_{GDH} and output at high state
Output high current in PWM mode for GD1/2	$-I_{GDH}$	—	104	—	mA	GDx_CFG.CUR = 24
Output high current tolerance in PWM mode	Δ_{IGDH}	—		±15	%	Calibrated [15]
Discharge current for GD1/2	I_{GDDIS}	500	—	—	mA	V_{GD} = 4 V and driver at low state
Output low reverse current	$-I_{GDREVL}$	—	—	100	mA	Applies if V_{GD} < 0 V and driver at low state
Output high reverse current in PWM mode	I_{GDREVH}	—	1/6 of I_{GDH}	—		Applies if V_{GD} > V_{GDH} + 0.5 V (typ) and driver at high state

15 referred to GDx_CFG.CUR = 16

Table 21 Electrical Characteristics of the A/D Converter

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Integral non-linearity	INL	—	—	1	LSB_8	16)

Table 22 Electrical Characteristics of the Reference Voltage

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Reference voltage	V_{REF}	—	2.428	—	V	
VREF overall tolerance	Δ_{VREF}	—	—	±1.5	%	Trimmed, $T_j \leq 125$ °C and aging

Table 23 Electrical Characteristics of the OTP Programming

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OTP programming voltage at the VCC pin for range $C000_H$ to $CFFF_H$	V_{PP}	7.35	7.5	7.65	V	Operational values
OTP programming voltage at the VCC pin for range $D000_H$ to $DFFF_H$	V_{PP}	9.0	—	V_{VCC}	V	Operational values
OTP programming current	I_{PP}	—	1.6	—	mA	Programming of 4 bits in parallel

Table 24 Electrical Characteristics of the Clock Oscillators

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Master clock oscillation period including all variations	t_{MCLK}	19.2	20.0	21.1	ns	In reference to 50 MHz f_{MCLK}
Main clock oscillator frequency variation of stored DPARAM frequency	Δ_{MCLK}	–3.2	—	+2.0	%	Temperature drift and aging only, 50 MHz f_{MCLK}
Standby clock oscillator frequency	f_{STBCLK}	96	100	104	kHz	Trimming tolerance at $T_A = 25$ °C
Standby clock oscillator frequency	f_{STBCLK}	90	100	110	kHz	Overall tolerance

16 ADC capability measured via channel MFIO without errors due to switching of neighbouring pins, e.g. gate drivers, measured with STC = 5. MFIO buffer non-linearity masked out by taking ADC output values ≥ 30 only.

Table 25 Electrical Characteristics of the Temperature Sensor

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Temperature sensor ADC output operating range	ADC_{TEMP}	0	—	190	LSB	ADC_{TEMP} = 40 + temperature / °C)
Temperature sensor tolerance	Δ_{TEMP}	—	—	±6	K	Incl. ADC conversion accuracy at 3 σ

5 Package Dimensions

The package dimensions of PG-DSO-16 are provided.

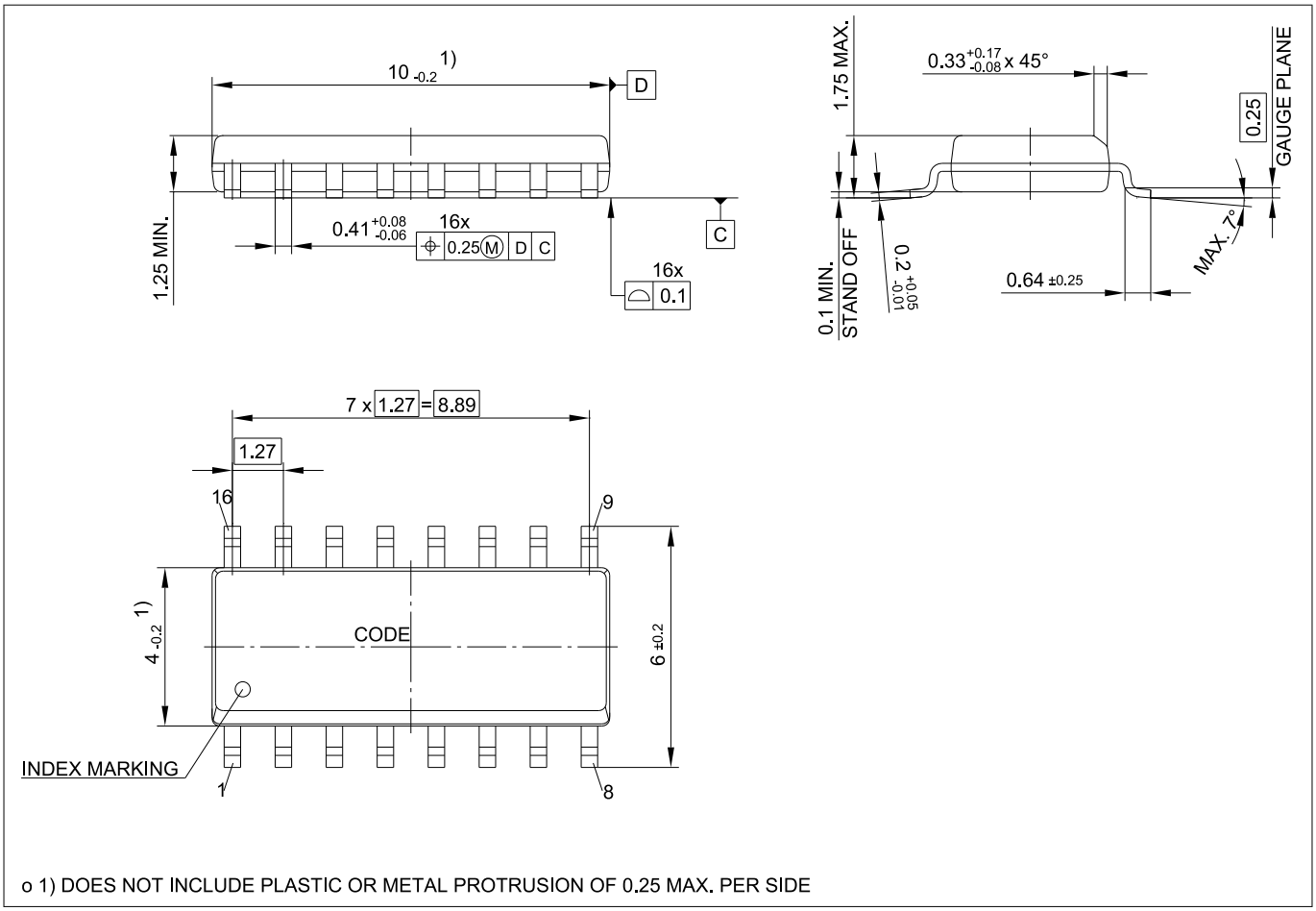


Figure 31 Package Dimensions for PG-DSO-16

Note: Dimensions in mm.

Note: You can find all of our packages, packing types and other package information on our Infineon Internet page “Products”: http://www.infineon.com/products.

6 References

1. Infineon Technologies AG: *XDPL8221 Design Guide*
2. Infineon Technologies AG: *XDPL8221 Reference Board Test Report*
3. Infineon Technologies AG: *CoolMOS P7 power MOSFETs*, ***http://www.infineon.com/P7***
4. Infineon Technologies AG: *.dp Vision User Manual*
5. Infineon Technologies AG: *.dp Interface Gen2* which can be ordered at ***http://ehitex.com/programmer/486/.dp-interface-board-gen2***
6. Infineon Technologies AG: *.dp Interface Gen2 User Manual*
7. Infineon Technologies AG: *XDP Programming Manual*

Revision History

Major changes since previous revision

Revision History

Revision	Description
1.1	• Indication of ambient temperature for IC is deleted. • UART dimming changed from duty cycle to dimming level. • Minor Change of wording
1.0	• Minor change of wording

Glossary

ABM
Active Burst Mode (ABM)

Active Burst Mode is an operating mode of a switched-mode power supply for very light load conditions. The controller switches in bursts of pulses with a pause between bursts in which no switching is done.

AC
Alternating Current (AC)

An Alternating Current is a form of power supply in which the flow of electric charge periodically reverses direction.

ADC
Analog-to-Digital Converter (ADC)

An analog-to-digital converter is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

BOM
Bill of Materials (BOM)

A bill of materials is a list of the raw materials, sub-assemblies, intermediate assemblies, sub-components, parts and the quantities of each needed to manufacture an end product.

CC
Constant Current (CC)

Constant Current is a mode of a power supply in which the output current is kept constant regardless of the load.

Glossary

CCM
Continuous Conduction Mode (CCM)

Continuous Conduction Mode is an operational mode of a switching power supply in which the current is continuously flowing and does not return to zero.

CRC
Cyclic Redundancy Check (CRC)

A cyclic redundancy check is an error-detecting code commonly used to detect accidental changes to raw data.

CV
Constant Voltage (CV)

Constant Voltage is a mode of a power supply in which the output voltage is kept constant regardless of the load.

DAC
Digital-to-Analog Converter (DAC)

A digital-to-analog converter is a device that converts digital data into an analog signal (typically voltage).

DC
Direct Current (DC)

A Direct Current is a form of power supply in which the flow of electric charge is only into one direction.

DCM
Discontinuous Conduction Mode (DCM)

Discontinuous Conduction Mode is an operational mode of a switching power supply in which the current starts and returns to zero.

ECG
Electronic Control Gear (ECG)

An electronic control gear is a power supply which provides one or more light module(s) with the appropriate voltage or current.

EMI
Electro-Magnetic Interference (EMI)

Also called Radio Frequency Interference (RFI), this is a (usually undesirable) disturbance that affects an electrical circuit due to electromagnetic radiation emitted from an external source. The disturbance may interrupt, obstruct, or otherwise degrade or limit the effective performance of the circuit.

FB
Flyback (FB)

A flyback converter is a power converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of galvanic isolation between the input and any outputs.

FW
Firmware (FW)

A proprietary software exploiting a set of functions.

GUI
Graphic User Interface (GUI)

A graphical user interface is a type of interface that allows users to interact with electronic devices through graphical icons and visual indicators.

HW
Hardware (HW)

The collection of physical elements that comprise a computer system.

Glossary

IC
Integrated Circuit (IC)

A miniaturized electronic circuit that has been manufactured in the surface of a thin substrate of semiconductor material. An IC may also be referred to as micro-circuit, microchip, silicon chip, or chip.

IIR
Infinite Impulse Response (IIR)

Infinite impulse response is a property applying to many linear time-invariant systems. Common examples of linear time-invariant systems are most electronic and digital filters. Systems with this property have an impulse response which does not become exactly zero past a certain point, but continues indefinitely.

LED
Light Emitting Diode (LED)

A light-emitting diode is a two-lead semiconductor light source which emits light when activated.

LP
Limited Power (LP)

Limited Power is a mode of a power supply in which the output power is limited regardless of the load.

NTC
Negative Temperature Coefficient Thermistor (NTC)

A negative temperature coefficient thermistor is a type of resistor whose resistance declines over temperature.

OCP1
Overcurrent Protection Level 1 (OCP1)

The Overcurrent Protection Level 1 is limiting the current in a switched-mode power supply to limit the power delivered to the output of the power supply.

OCP2
Overcurrent Protection Level 2 (OCP2)

The Overcurrent Protection Level 2 is protecting the current in a switched-mode power supply from exceeding a maximum threshold.

OTP
One Time Programmable Memory (OTP)

A One-Time Programmable memory is a form of memory to which data can be written once. After writing, the data is stored permanently and cannot be further changed.

PF
Power Factor (PF)

Power factor is the ratio between the real power and the apparent power.

PFC
Power Factor Correction (PFC)

Power factor correction increases the power factor of an AC power circuit closer to 1 which corresponds to minimizing the reactive power of the power circuit.

PSR
Primary Side Regulated (PSR)

A Primary Side Regulated power supply controls its operation based on a property sensed on primary side of an isolated power supply.

PWM
Pulse Width Modulation (PWM)

Pulse-width modulation is a technique to encode an analog value into the duty cycle of a pulsing signal with arbitrary amplitude.

Glossary

QRM
Quasi-Resonant Mode (QRM)

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by only switching at preferred times when switching losses are low.

QRM1
Quasi-Resonant Mode, switching in first valley (QRM1)

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by switching at the occurrence of the first valley of a signal which corresponds to a time when switching losses are low.

QRMn
Quasi-Resonant Mode, switching in valley n (QRMn)

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by switching at the occurence of an nth valley of a signal which corresponds to a time when switching losses are low.

RAM
Random Access Memory (RAM)

Random-access memory is a form of computer data storage which allows data items to be read and written regardless of the order in which data items are accessed.

THD
Total Harmonic Distortion (THD)

The total harmonic distortion of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

UART
Universal Asynchronous Receiver Transmitter (UART)

A universal asynchronous receiver transmitter is used for serial communications over a peripheral device serial port by translating data between parallel and serial forms.

USB
Universal Serial Bus (USB)

Universal Serial Bus is an industry standard that defines cables, connectors and communications protocols used in a bus for connection, communication, and power supply between computers and electronic devices.

UVLO
Undervoltage Lockout (UVLO)

The Undervoltage-Lockout is an electronic circuit used to turn off the power of an electronic device in the event of the voltage dropping below the operational value.

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