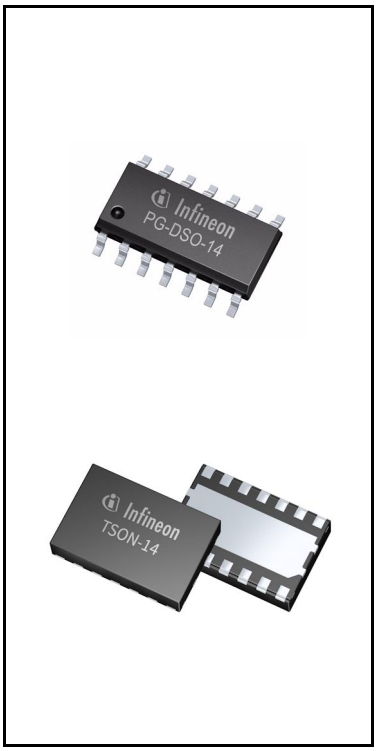
TLE7268

Dual LIN 2.2 / SAE J2602 Transceiver



1 Overview

Quality Requirement Category: Automotive

Features

- Two independent single-wire LIN transceivers in one device
- Transmission rate up to 20 kbps
- Compliant to ISO 17987-4, LIN Specification 2.2 A and SAE J2602
- Very low current consumption in Sleep mode with wake-up capability
- Very low leakage current on the BUSx pins
- Digital I/O levels compatible for 3.3 V and 5 V microcontrollers
- TxD protected with dominant time-out function and state check after mode change to Normal Operation mode
- bus_x short to V_{BAT} protection
- bus_x short to GND handling
- Overtemperature protection
- Undervoltage detection
- Very high ESD robustness: +/- 10 kV (IEC61000-4-2), +/-8 kV (HBM)
- Optimized for high electromagnetic compliance (EMC)
- Very low electromagnetic emission and high immunity to interference
- Available in PG-DSO-14 and PG-TSON-14 package
- Automated Optical Inspection (AOI) support with PG-TSON-14 package
- Pin and footprint compatible with single LIN transceivers such as TLE7257, TLE7258, and TLE7259-3GE
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Body Control Modules (BCM)
- Gateway

Description

The TLE7268 is a dual transceiver for the Local Interconnect Network (LIN) with integrated wake-up and protection features. The TLE7268 is designed for in-vehicle networks using data transmission rates up to

Overview

20 kbps. The TLE7268 includes two independent transceivers that operate as bus drivers between the protocol controller and physical LIN networks.

The TLE7268 supports different modes of operation of the two transceivers for minimizing ECU current consumption in low power modes. When both transceivers are in Sleep mode, the TLE7268 typically draws a quiescent current of less than 10 µA, while they still can wake up on detecting LIN bus traffic on either bus channel. A common INH output can be used for controlling external circuitry, for example voltage regulators.

Based on the Infineon BiCMOS technology the TLE7268 provides excellent ESD robustness together with very high electromagnetic compliance (EMC). The TLE7268 reaches a very low level of electromagnetic emission (EME) within a broad frequency range and independent from the battery voltage. The TLE7268 is AEC qualified and tailored to withstand the harsh conditions of automotive environment.

Type	Package	Marking
TLE7268SK	PG-DSO-14	7268
TLE7268LC	PG-TSON-14	7268

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2 Block diagram

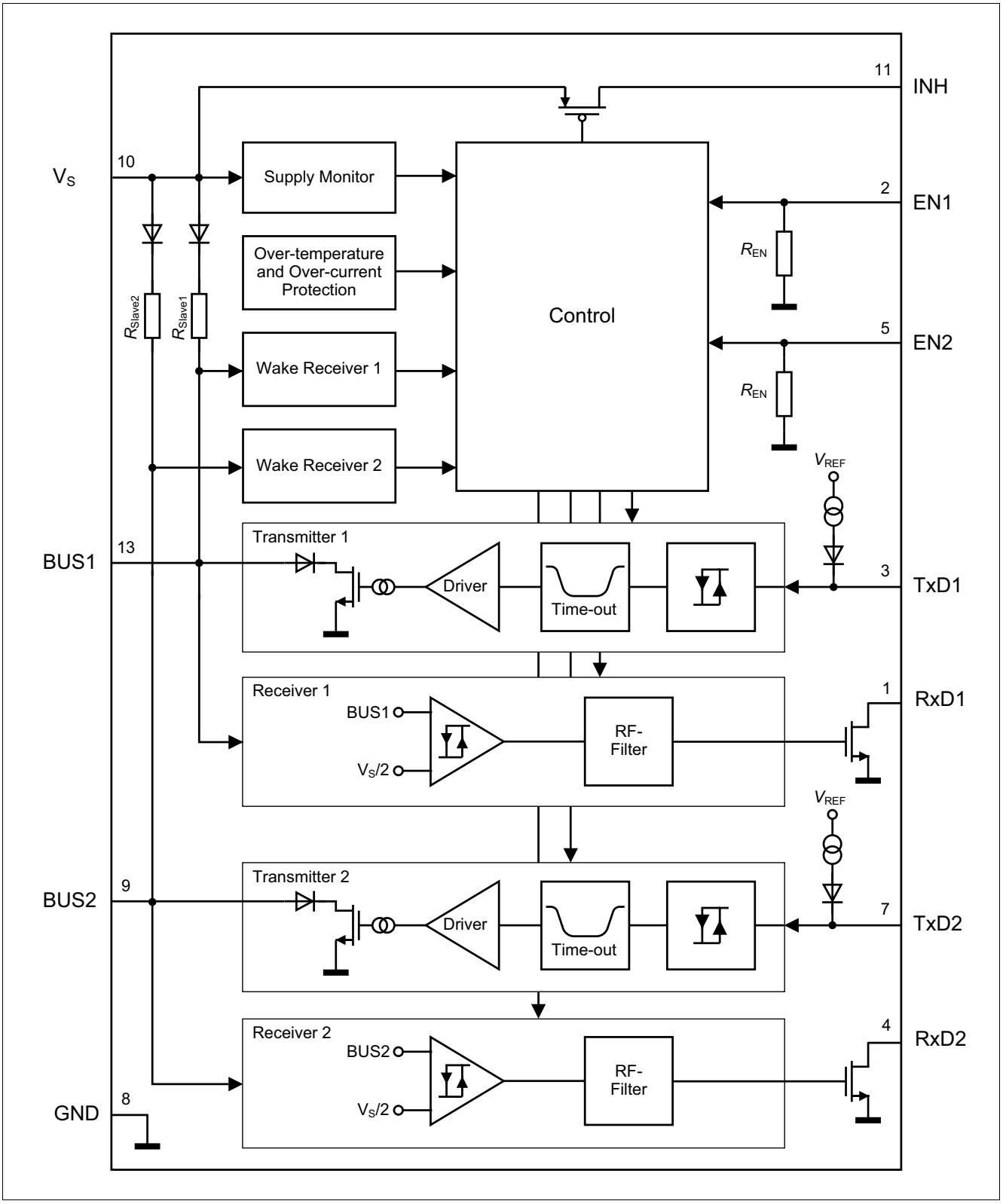


Figure 1 Block diagram

3 Pin configuration

3.1 Pin assignment

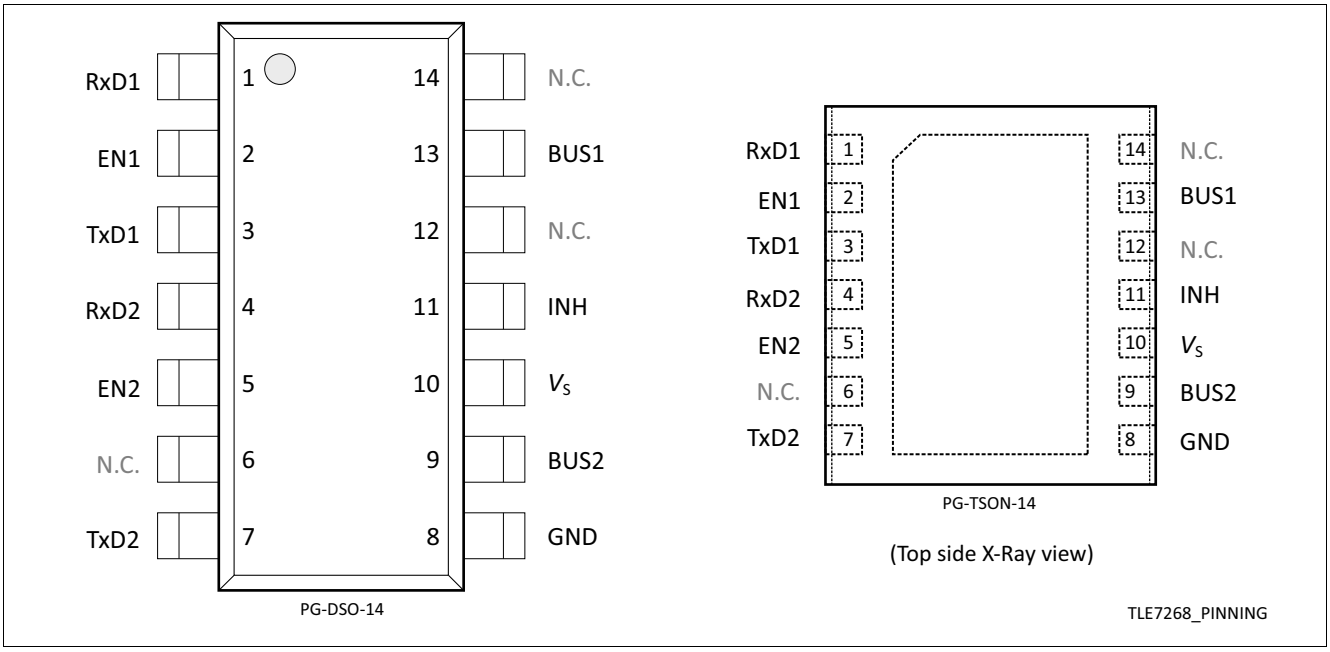


Figure 2 Pin configuration

3.2 Pin definitions and Functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	RxD1	**Receive data output 1;** • requires an external pull-up resistor • monitors the LIN bus_1 signal in Normal Operation mode • Indicates a wake-up event on BUS1 in Standby mode
2	EN1	**Enable input 1;** • has an integrated pull-down resistor • set this pin to “high” to select Normal Operation mode for transceiver_1
3	TxD1	**Transmit data input 1;** • has an integrated pull-up current source • set this pin to “low” to drive a dominant signal on LIN bus_1
4	RxD2	**Receive data output 2;** • requires an external pull-up resistor • monitors the LIN bus_2 signal in Normal Operation mode • Indicates a wake-up event on BUS2 in Standby mode

Pin configuration

Table 1 Pin definitions and functions

Pin	Symbol	Function
5	EN2	**Enable input 2;** • has an integrated pull-down resistor • set this pin to “high” to select Normal Operation mode for transceiver_1
6	*N.C.*	**Not connected**
7	TxD2	**Transmit data input 2;** • has an integrated pull-up current source • set this pin to “low” to drive a dominant signal on LIN bus_2
8	GND	**Ground**
9	BUS2	**BUS Input / Output 2;** • has an integrated LIN slave termination
10	V_S	**Battery supply input;** • requires decoupling capacitor of 100 nF
11	INH	**Inhibit output;** • Battery supply related output • “high” when transceiver_1 OR transceiver_2 is in Normal Operation mode OR in Standby mode
12	N.C.	**Not connected**
13	BUS1	**BUS Input / Output 1;** • has an integrated LIN slave termination
14	*N.C.*	**Not connected**

4 Functional description

The LIN interface is a single wire, bidirectional bus, used for in-vehicle networks. The TLE7268 Dual LIN transceiver is the interface between the microcontroller and physical LIN bus (see Figure 15). The TLE7268 drives data from the microcontroller to the LIN bus via the TxD1/TxD2 inputs. The TLE7268 converts the transmit data streams on the TxD1/TxD2 inputs to LIN signals with optimized slew rates in order to minimize the level of electromagnetic emission on the LIN networks. The RxD1/RxD2 outputs read back the information from the LIN bus to the microcontroller. The integrated filter networks of the receivers suppress noise from the LIN bus and increase the electromagnetic immunity level of the transceivers.

The LIN specification defines two valid bus states (see Figure 3):

- dominant: LIN bus voltage level close to GND level
- recessive: LIN bus voltage level pulled up to the supply voltage V_S by bus termination

By setting the TxD1/TxD2 input of the TLE7268 to a “low” signal, the transceiver generates a dominant level on the corresponding BUS1/BUS2 pin. The RxD1/RxD2 outputs read the signal on the corresponding LIN bus pin and indicate the dominant LIN bus signal with a “low” signal to the microcontroller. Setting the TxD1/TxD2 pins to “high”, the TLE7268 sets the corresponding LIN interface pin BUS1/BUS2 to the recessive level. At the same time a “high” signal on the RxD1/RxD2 outputs indicates the recessive level on the LIN bus.

Every LIN network consists of a master node and one or more slave nodes. To configure a transceiver for master node applications, a termination resistor of 1 kΩ and a diode must be connected between LIN bus and power supply V_S (see Figure 15).

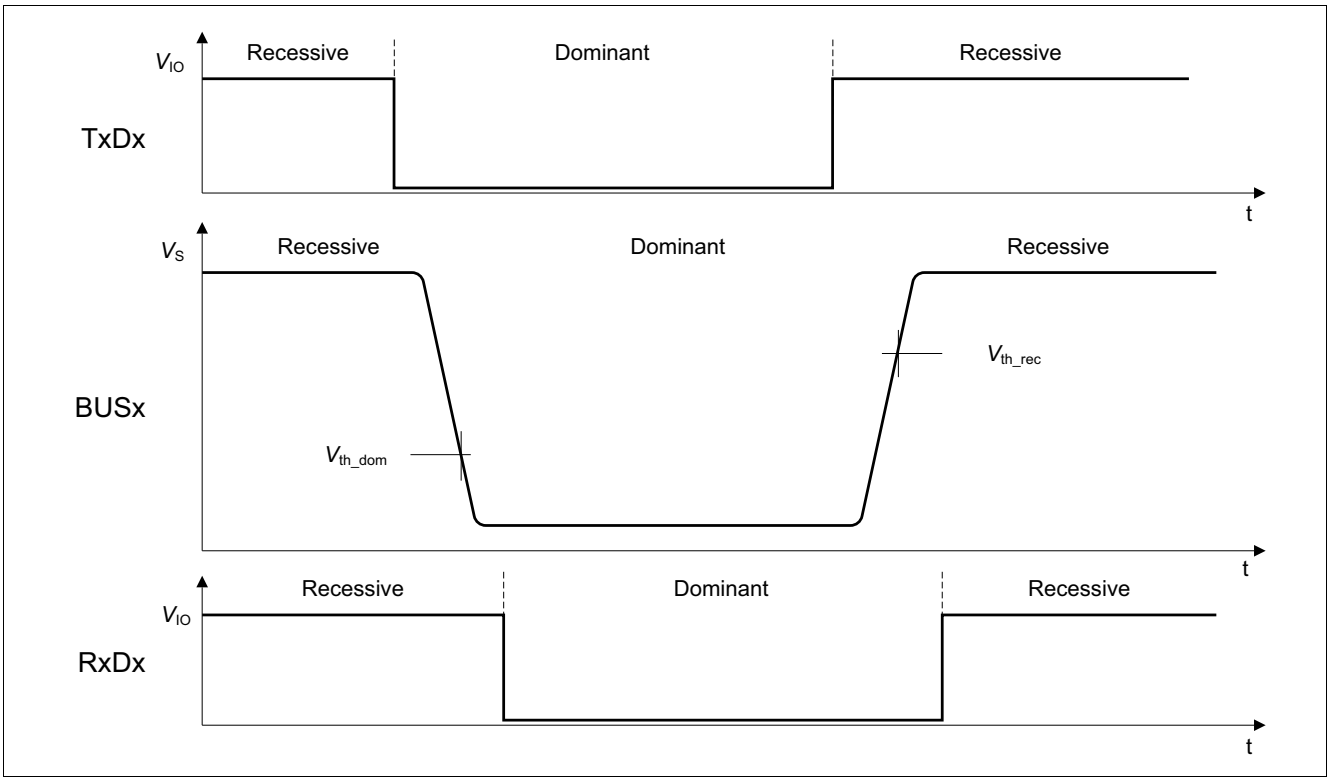


Figure 3 LIN bus signals

4.1 Operating modes

The transceivers of the TLE7268 have the following major operation modes (see Figure 4):

- Normal Operation mode
- Standby mode
- Sleep mode

The transceivers can operate independently of each other regarding operational mode, for example one transceiver can be in Normal Operation mode while the other is in Sleep mode or in Standby mode. The only feature that introduces a dependency between the two transceivers is the voltage regulator control output, the INH pin. INH is floating only when both transceivers are in Sleep mode. INH “high” immediately indicates a mode change of any transceiver, which has been triggered by bus wake-up or by a “high” signal on either ENx input.

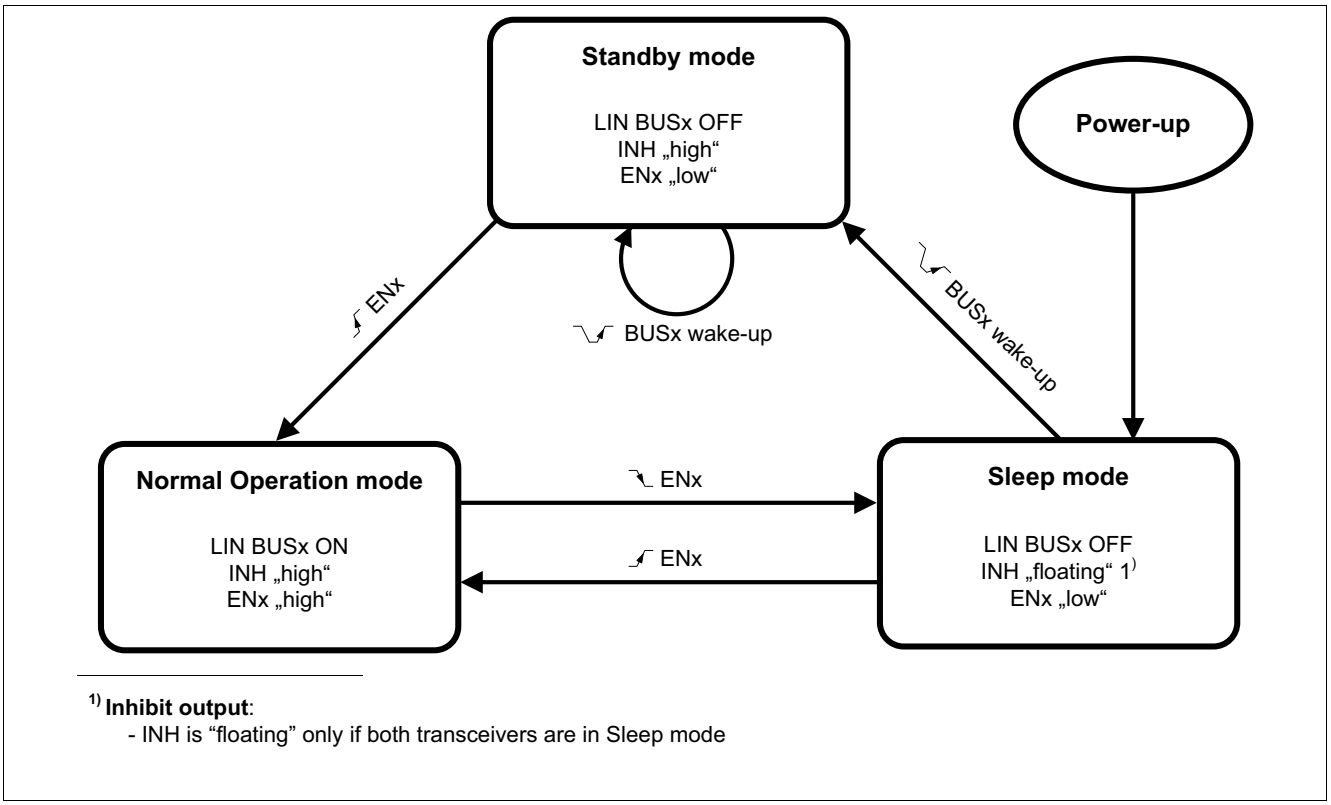


Figure 4 Operation mode state diagram

4.2 Normal Operation mode

In Normal Operation mode all functions of the TLE7268 are available and the device is fully functional. Data can be received from the LIN Bus as well as transmitted to the LIN Bus. The following functions are available in the Normal Operation mode:

- The transmitter_x is turned on, data on the TxDx input pin is driven on the LIN bus_x.
- The receiver_x is turned on, data on the LIN bus_x is monitored on the RxDx output.
- The TxDx pin is pulled up to the internal power supply by an internal current source of the TLE7268.
- The INH output is switched on.
- The LIN bus is not continuously monitored after a LIN Bus Wake Up (Chapter 4.5)
- The undervoltage detection is enabled (see Chapter 5.2).

Conditions for entering the Normal Operation mode:

- The Normal Operation mode can be entered from all modes of Operation by setting the ENx input pin to “high”.

After a mode change for a transceiver_x of the TLE7268to Normal Operation mode, a “high” signal for at least t_{to_rec} on the TxDx input is required before releasing data communication on the corresponding transceiver (see Figure 5). After a mode change to Normal Operation mode while the TxDx is “low”, the Transmitter_x remains inactive until there is a transition from “low” to “high” at the TxDx pin. This behavior excludes possible bus communication disturbance during a mode change.

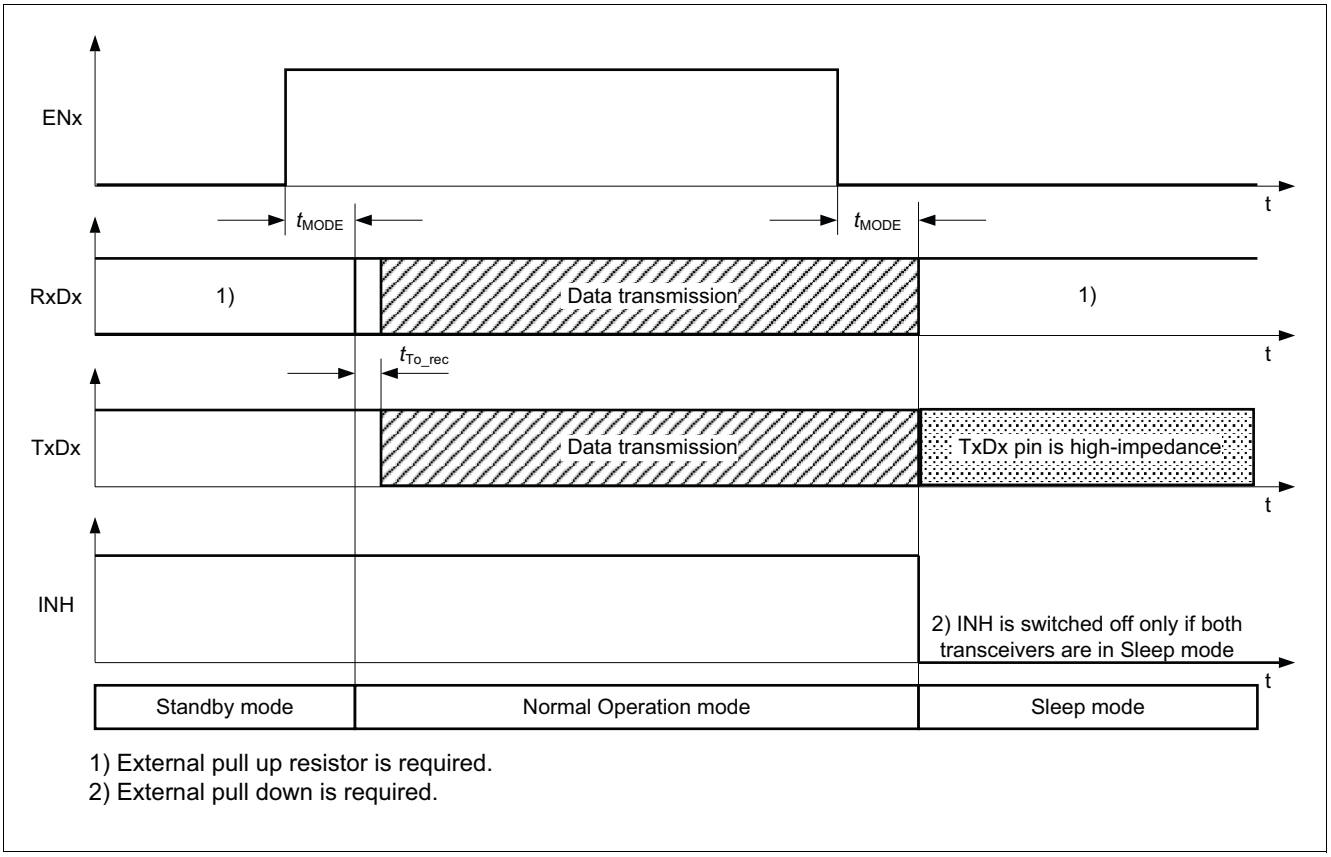


Figure 5 Transition from Standby mode to Normal Operation mode

4.3 Standby mode

In Standby mode no communication with the LIN Bus is possible. The following functions are available:

- The transmitter_x is turned off, the TxD_x input is inactive and the BUSx output is permanent recessive.
- The receiver_x is turned off.
- The RxDx output indicates a wake-up event (see Figure 4).
- The TxDx pin is pulled up to the internal power supply by an internal current source of the TLE7268.
- The INH output is switched on.
- The LIN Bus x is continuously monitored for a valid Bus Wake up (Chapter 4.5) and indicates a wake-up event on the RxDx pin.
- The undervoltage detection is disabled if the second transceiver is not in Normal Operation mode (see Chapter 5.2).

Conditions for entering the Standby mode:

- A bus wake-up event on the BUSx pin, while the ENx input pin remains “low”.

4.4 Sleep mode

Sleep mode is a low power mode with quiescent current consumption reduced to a minimum while a transceiver_x is still able to wake-up by a message on the LIN bus_x. The following functions are available:

- The transmitter_x is turned off.
- The receiver_x is turned off.
- RxDx output is “high” if a pull-up resistor is connected to the external microcontroller supply.
- The TxDx input is disabled and the internal pull-up current source is switched off.
- The INH output is switched off and is “floating” if both transceivers of the TLE7268 are in Sleep mode.
- The LIN Bus x is continuously monitored for a valid Bus Wake up (Chapter 4.5).
- The undervoltage detection is disabled if the second transceiver is not in Normal Operation mode (Chapter 5.2).

Conditions for entering the Sleep mode:

- The Sleep mode will be entered, if the transceiver_x is in Normal Operation mode AND the ENx pin has been set to “low” (see Figure 6).
- The Sleep mode will be entered, if V_S exceeds the $V_{S_UV_PON}$ threshold, while the ENx input pin remains “low” (see Figure 7).

Figure 6 shows the behavior of the RxDx, TxDx and INH pin when the transceivers enter Sleep mode from Normal Operation mode.

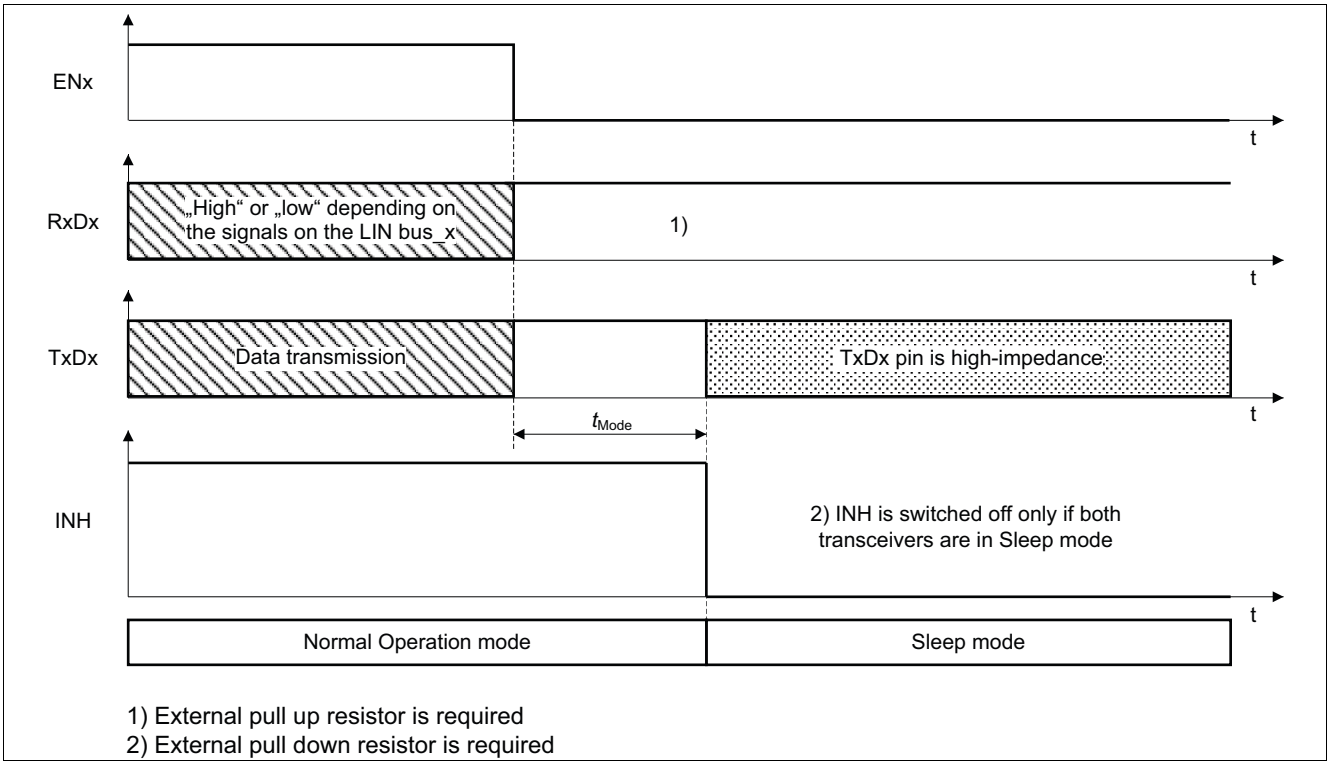
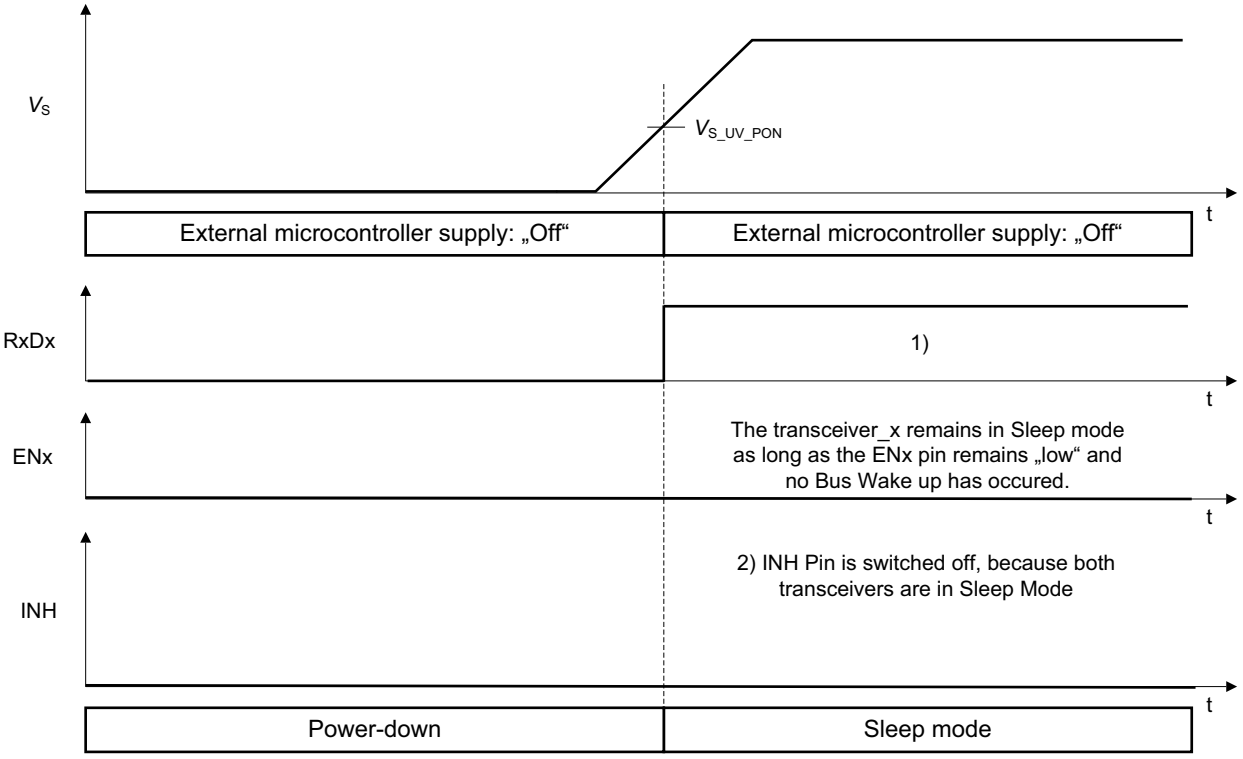


Figure 6 Transition from Normal Operation mode to Sleep mode



1) External pull up resistor is required.

2) External pull down resistor is required.

Figure 7 Transition from Power-down to Sleep mode

4.5 Wake-up events

A wake-up event on the LIN Bus changes the operation mode for transceiver_x of the TLE7268 from Sleep mode to Standby mode. There are two different ways to exit Sleep mode:

- Bus wake-up via a dominant signal on the pin BUSx for at least the time t_{WK_bus}.
  The TLE7268 changes into Standby mode.
- Mode change by setting the ENx input “high”.
  The TLE7268 changes into Normal Operation mode.

4.5.1 Bus wake-up via LIN bus

The bus wake-up, also called remote wake-up, changes the transceivers’ operation mode from Sleep mode to Standby mode. A falling edge on the LIN Bus, followed by a dominant bus signal for t > $t_{WK,bus}$ results in a bus wake-up event. The mode change to Standby mode is performed with the subsequent rising edge on the LIN bus. The transceiver_x of TLE7268 remains in Sleep mode until it detects a change from dominant to recessive on the LIN bus_x (see Figure 8).
In Standby mode a “low” signal on the RxDx output indicates a bus wake-up event of transceiver_x.

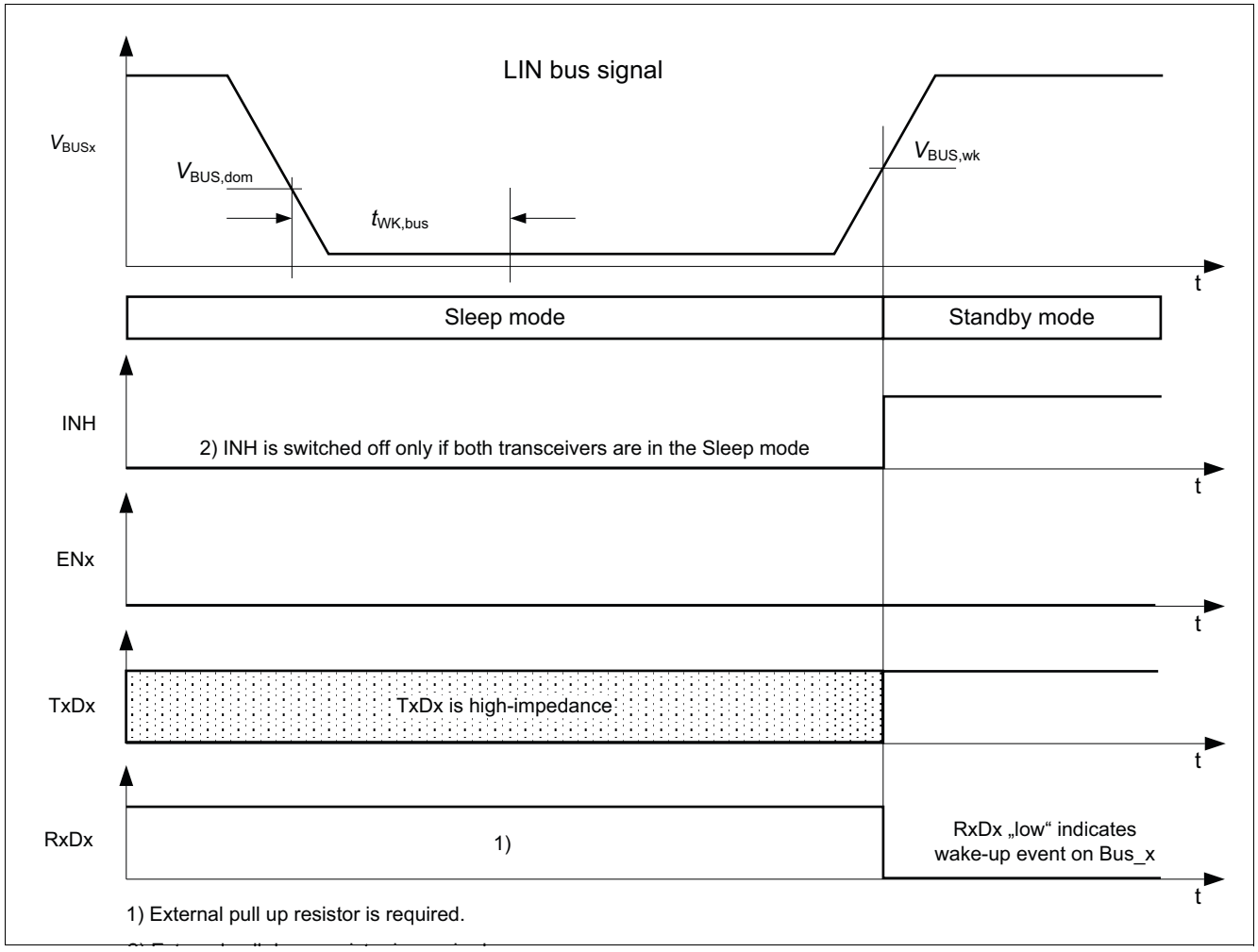


Figure 8 Bus wake-up behavior

4.5.2 Mode transition via EN pin

It is possible to change a transceiver_x's mode from Sleep mode to Normal Operation mode by setting the corresponding ENx input "high". This feature is useful with an external microcontroller that is continuously powered (instead of being controlled by the INH output). The EN1/EN2 pins have integrated pull-down resistors to ensure the transceivers remain in Sleep mode or in Standby mode, even if the voltage at each ENx pin is floating. The EN1/EN2 inputs have integrated hysteresis (see Figure 9).

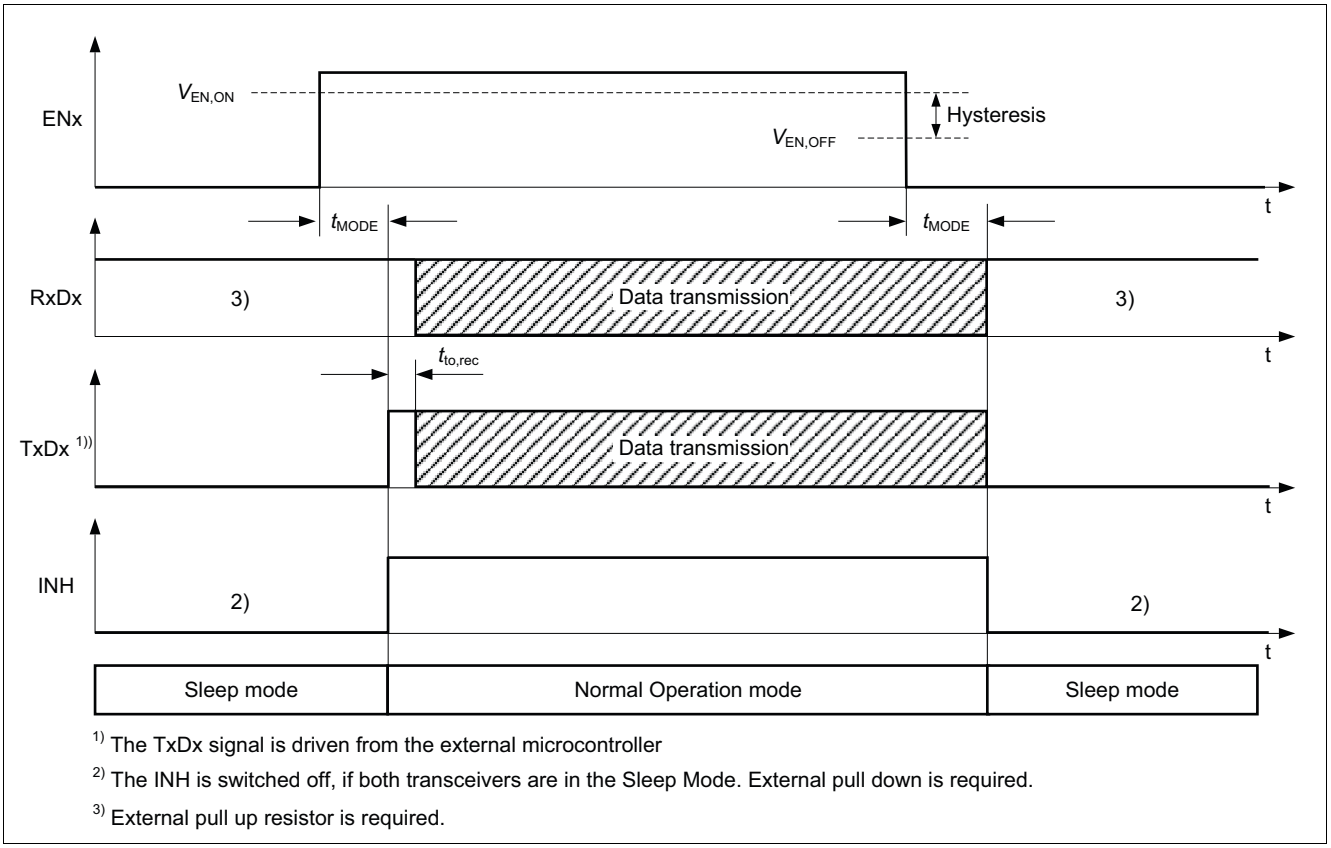


Figure 9 Transition from Sleep mode to Normal Operation mode

A transition from "high" to "low" on the ENx pin changes the operation mode of transceiver_x from Normal Operation mode to Sleep mode. If transceiver_x is already in Sleep mode, changing the ENx from "low" to "high" results in a mode change from Sleep mode to Normal Operation mode. If the transceiver_x is in Standby mode, then a change from "low" to "high" on the ENx pin changes the mode to Normal Operation mode (see Figure 5).

The transceivers of the TLE7268 change operation modes regardless of the signal on the BUS1 and BUS2 pins. In case of a short circuit from LIN bus_x to GND, which results in a permanent dominant signal, the transceiver_x can be put to Sleep mode by setting the ENx input to "low".

After the mode change to Normal Operation mode, a "high" signal for the time t_{to_rec} on the TxDx input is required to release the data communication of transceiver_x.

5 Fail safe functions

5.1 Overtemperature protection

The integrated overtemperature sensors protect the TLE7268 from thermal overstress on the transmitters. In case of an overtemperature event $T_J > T_{JSD}$, the temperature sensors disable the transmitters (see **Figure 10**). An overtemperature event does not cause any mode change. The TLE7268 does not indicate an overtemperature event to the microcontroller.

If the junction temperature drops below the thermal shutdown level $T_J < T_{JSD}$, then the transmitters are switched on again. A signal change from “high” to “low” on the TxDx input restarts data communication of transceivers after a “high” signal with a duration of at least $t_{to,rec}$.

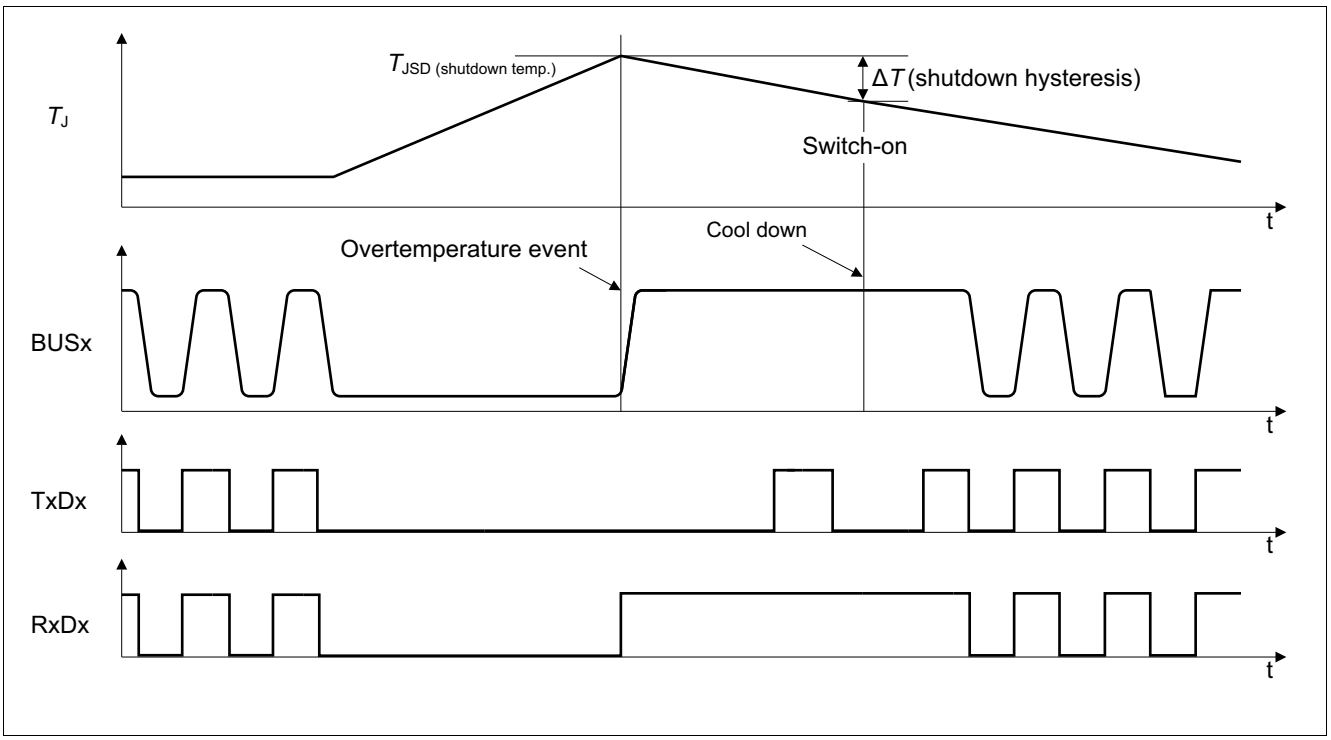


Figure 10 Overtemperature shutdown

A temperature hysteresis is implemented for avoiding toggling during temperature shutdown.

5.2 Undervoltage detection

If $V_S < V_{S_UV}$, then the TLE7268 detects an undervoltage event. During an undervoltage event the transmitters and the receivers are disabled and no mode change is performed. If $V_S > V_{S_UV}$ the transmitter will be enabled after t_{blank_UV}. Figure 11 shows this scenario.

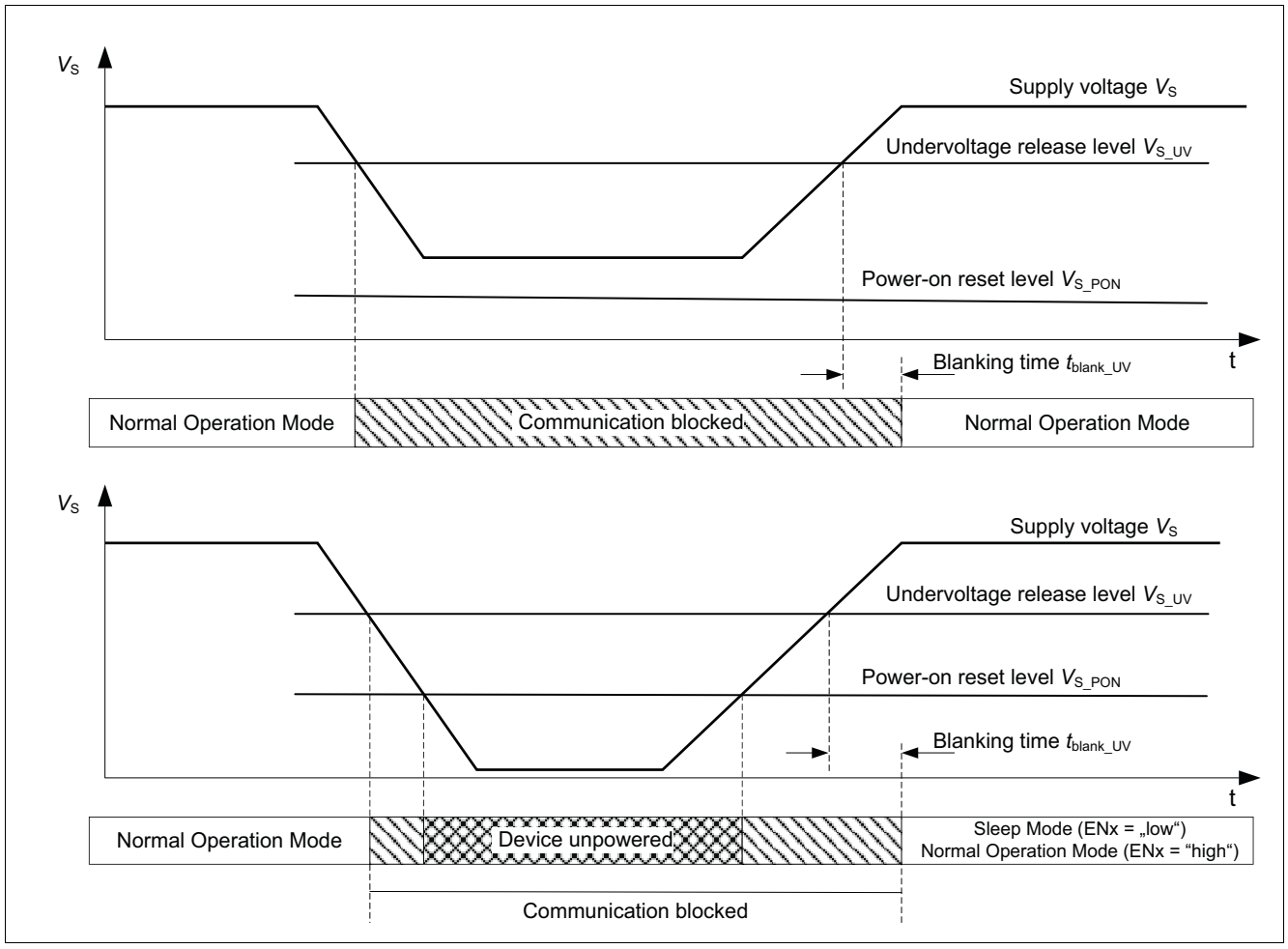


Figure 11 Undervoltage detection

5.3 TxD time-out

The TxD time-out feature protects the LIN BUSx from blocking permanently in case the signal on the TxDx pin is continuously “low”, for example due to a malfunctioning microcontroller or a short circuit on the printed circuit board. In Normal Operation mode, a continuous “low” signal at the TxDx input for time $t > t_{TxD}$ enables the TxD time-out feature and the TLE7268 disables the transceivers's output driver stage (see Figure 12). The receiver_x remains active and data on the LIN BUSx is still monitored on the RxDx output.

The TLE7268 releases the output stage after a TxD time-out event when it detects a “high” signal on the corresponding TxDx input for the time $t_{to,rec}$.

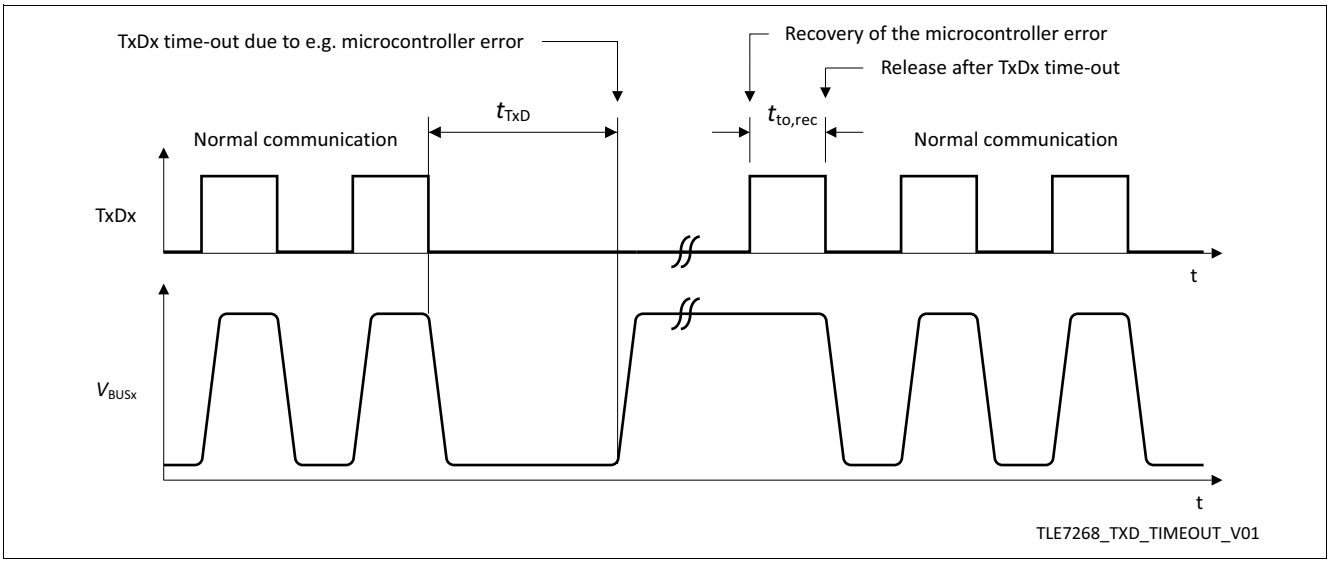


Figure 12 TxD time-out

5.4 3.3 V and 5 V logic capability

The TLE7268 can be used for 3.3 V and 5 V microcontrollers. The inputs and the outputs can operate at both voltage levels. The RxD1/RxD2 outputs require external pull-up resistors to the microcontroller supply to define the voltage level (see Figure 15).

5.5 Short circuit

The BUS1/BUS2 pins of TLE7268 can withstand short circuit to GND and short circuit to the power supply V_S. The integrated overtemperature protection may disable the transmitters in case of a permanent short circuit on the bus pins causing overheating.

5.6 Unconnected logic pins

If the input pins are not connected and floating (see Table 2), then the integrated pull-up resistors and pull-down resistors at the digital input pins force the TLE7268 into fail safe behavior.

Table 2 Unconnected logical inputs

Input signal	Default state	Comment
TxD1, TxD2	“high”	pull-up current source to V_{Ref} disabled in Sleep mode
EN1, EN2	“low”	pull-down resistor R_{EN}

6 General product characteristics

6.1 Absolute maximum ratings

Table 3 Absolute maximum ratings [1)]

All voltages with respect to ground; positive current flowing into pin; unless otherwise specified

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Battery supply voltage	V_S	-0.3	–	40	V	ISO 17987 Param. 11	P_5.1.1
input voltage at BUS1, BUS2	V_{BUS}	-27	–	40	V	–	P_5.1.2
Difference voltage between BUS1 and BUS2	$\lvert V_{BUS1-BUS2}\rvert$	-	–	40	V	–	P_5.1.14
Logic voltage at EN1, EN2, TxD1, TxD2, RxD1, RxD2	V_{logic}	-0.3	–	6.0	V	–	P_5.1.3
INH voltage	V_{INH}	-0.3	–	V_S + 0.3	V	–	P_5.1.4
Currents							
Output current at RxD1, RxD2	I_{RxD}	0	–	15	mA	–	P_5.1.5
Output current at INH	I_{INH}	-5	–	5	mA	–	P_5.1.6
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_5.1.7
Storage temperature	T_s	-55	–	150	°C	–	P_5.1.8
ESD Resistivity							
Electrostatic discharge voltage at V_S, BUS1, BUS2	$V_{ESD_HBM_BUS}$	-8	–	8	kV	Human Body Model (100pF via 1.5 kΩ)[2)]	P_5.1.9
Electrostatic discharge voltage all other pins	$V_{ESD_HBM_ALL}$	-2	–	2	kV	Human Body Model (100pF via 1.5 kΩ)[2)]	P_5.1.10
Electrostatic discharge voltage corner pins	$V_{ESD_CDM_CP}$	-750	–	750	V	Charged Device Model[3)]	P_5.1.11
Electrostatic discharge voltage all other pins	V_{ESDCDM_OP}	-500	–	500	V	Charged Device Model[3)]	P_5.1.12

1) Not subject to production test, specified by design
2) ESD susceptibility HBM according to ANSI / ESDA / JEDEC JS-001
3) ESD susceptibility, Charged Device Model “CDM” EIA / JESD 22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

6.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltages							
Extended supply voltage range for operation	$V_{S(ext)}$	18	–	40	V	Parameter deviations possible	P_5.2.1
Supply voltage range for normal operation	$V_{S(nor)}$	5.5	–	18	V	ISO 17987 Param. 10	P_5.2.2
Thermal parameters							
Junction temperature	T_j	-40	–	150	°C	–	P_5.2.3

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

6.3 Thermal characteristics

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 5 Thermal resistance [1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance							
Junction to ambient PG-DSO-14	R_{thJA}	–	-	110	K/W	[2)]	P_5.3.1
Junction to ambient PG-TSON-14	R_{thJA}	–	-	120	K/W	[3)]	P_5.3.1
Thermal shutdown junction temperature							
Thermal shutdown temperature	T_{JSD}	150	175	200	°C	–	P_5.3.2
Thermal shutdown hysteresis	ΔT	–	10	–	K	–	P_5.3.3

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (TLE7268) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu).

3) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (TLE7268) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu).

7 Electrical characteristics

7.1 Functional device characteristics

7.1.1 General timing parameters

Table 6 General Timing Parameters

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay time for mode change	t_{MODE_x}	–	–	50	µs	1)	P_7.1.1
TxD time-out	t_{TxD_x}	8	18	28	ms		P_7.1.2
TxD recessive time to release transmitter	$t_{to,}$	–	–	10	µs	1)	P_7.1.3

1) Delay time specified for a load of 10 kΩ, 20 pF on the INH output

7.1.2 Power supply interface

7.1.2.1 Current consumption

Table 7 Current consumption

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption at V_S, Normal Operation mode, recessive state (both transceivers)	$I_{S,rec}$	0.1	0.8	2.0	mA	INH open, without R_L; V_{TxD1} = V_{TxD2} = “high”	P_7.1.4
Current consumption at V_S, Normal Operation mode, dominant state (both transceivers)	$I_{S,dom}$	0.2	2.2	4.5	mA	INH open, without R_L; V_{TxD1} = V_{TxD2} = 0 V	P_7.1.5
Current consumption at V_S, Standby mode (both transceivers)	$I_{S,standby}$	100	400	900	µA	Standby mode, V_S = V_{BUS1} = V_{BUS2}	P_7.1.6
Current consumption at V_S, Sleep mode (both transceivers)	$I_{S,sleep,typ}$	1	8	15	µA	Sleep mode, T_j < 40 °C; V_S = 13.5 V; V_S = V_{BUS1} = V_{BUS2}	P_7.1.7

Table 7 Current consumption (cont'd)

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption at V_S, Sleep mode (both transceivers)	$I_{S,sleep}$	1	12	20	µA	Sleep mode, $V_S = V_{BUS1} = V_{BUS2}$	P_7.1.8
Current consumption at V_S, Sleep mode (both transceivers), BUS1 and BUS2 shorted to GND	I_{S,SC_GND}	200	–	1600	µA	Sleep mode, V_S = 13.5 V; $V_{BUS1} = V_{BUS2}$ = 0 V	P_7.1.9

7.1.2.2 Undervoltage detection

Table 8 Undervoltage detection

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power-on reset level on V_S	$V_{S,PON}$	–	–	4.3	V	Reset level for mode change	P_7.1.10
Undervoltage detection threshold	$V_{S,UV}$	4.4	5.0	5.5	V		P_7.1.11
Undervoltage detection hysteresis	$V_{S,UV,HYS}$	–	300	–	mV	1)	P_7.1.12
Undervoltage blanking time	$t_{BLANK,UV}$	–	10	–	µs	1)	P_7.1.13

1) Not subject to production test, specified by design

7.1.2.3 INH output

Table 9 INH output

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Inhibit output: INH							
Inhibit voltage drop	ΔV_{INH}	–	–	1.0	V	I_{INH} = -2.0 mA	P_7.1.14
Leakage current	$I_{INH,lk}$	-5.0	–	–	µA	Sleep mode; V_{INH} = 0 V	P_7.1.15

7.1.3 LIN controller interface

Table 10 LIN controller interface

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver outputs: RxD1, RxD2							
"High" level leakage current	$I_{RD,H,leak_x}$	–	–	5	µA	V_{RxD1} = V_{RxD2} = 5 V; V_{BUS1} = V_{BUS2} = V_S	P_7.1.16
"Low" level output current	I_{RD,L_x}	2	–	–	mA	V_{RxD1} = V_{RxD2} = 0.4 V; V_{BUS1} = V_{BUS2} = 0 V	P_7.1.17
Transmitter inputs: TxD1, TxD2							
"High" level input voltage range	V_{TD,H_x}	2	–	6.0	V	Recessive state	P_7.1.18
"Low" level input voltage range	V_{TD,L_x}	-0.3	–	0.8	V	Dominant state	P_7.1.19
Input hysteresis	V_{TD,hys_x}	–	200	–	mV	1)	P_7.1.20
Pull-up current	I_{TD_x}	-60	–	-20	µA	V_{TxD1} = V_{TxD2} = 0 V; Normal Operation or Standby mode	P_7.1.21
Enable inputs: EN1, EN2							
"High" level input voltage range	V_{EN,H_x}	2	–	6.0	V	Normal Operation mode	P_7.1.23
"Low" level input voltage range	V_{EN,L_x}	-0.3	–	0.8	V	Sleep or Standby mode	P_7.1.24
Input hysteresis	V_{EN,hys_x}	–	200	–	mV	1)	P_7.1.25
Pull-down resistance	R_{EN_x}	15	30	60	kΩ	–	P_7.1.26

1) Not subject to production test, specified by design

7.1.4 Bus transmitter and receiver

7.1.4.1 Bus receiver

Table 11 Bus receiver

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver threshold voltage, recessive to dominant edge	$V_{th_dom_x}$	0.4 × V_S	0.44 × V_S	–	V	–	P_7.1.28
Receiver dominant state	V_{BUSdom_x}	- 27	–	0.4 × V_S	V	ISO 17987 (Par. 17)	P_7.1.29
Receiver threshold voltage, dominant to recessive edge	$V_{th_rec_x}$	–	0.56 × V_S	0.6 × V_S	V	–	P_7.1.30
Receiver recessive state	V_{BUSrec_x}	0.6 × V_S	–	40	V	ISO 17987 (Par. 18)	P_7.1.31
Receiver center voltage	$V_{BUS_CNT_x}$	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	ISO 17987 (Par. 19)[1]	P_7.1.32
Receiver hysteresis	V_{HYS_x}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	ISO 17987 (Par. 20)[2]	P_7.1.33
Wake-up threshold voltage	V_{BUS,wk_x}	0.40 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_7.1.34
Dominant time for bus wake-up	t_{WK,bus_x}	30	–	150	µs	–	P_7.1.35

1) $V_{BUS_CNT} = (V_{th_dom} + V_{th\ rec}) / 2$;
2) $V_{HYS} = V_{th_rec} - V_{th_dom}$

7.1.4.2 Bus transmitter

Table 12 Bus transmitter

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus recessive output voltage	V_{BUS,ro_x}	0.8 × V_S	–	V_S	V	V_{TxDx1} = V_{TxDx2}= “high”; Open load	P_7.1.36
Bus short circuit current	$I_{BUSx_SC_x}$	40	85	125	mA	V_{BUS1} = V_{BUS2} = 18 V; ISO 17987 (Par. 12);	P_7.1.37
Leakage current loss of ground	$I_{BUS_NO_GND_x}$	-1	-0.5	–	mA	V_S = 0 V; V_{BUS1}= V_{BUS2}= -12 V; ISO 17987 (Par. 15)	P_7.1.38
Leakage current loss of battery	$I_{BUS_NO_BAT_x}$	–	1	5	µA	V_S = 0 V; V_{BUS1} = V_{BUS2} = 18 V ISO 17987 (Par. 16)	P_7.1.39
Leakage current driver off and bus dominant	$I_{BUS_PAS_dom_x}$	-1	-0.5	–	mA	V_S = 18 V; V_{BUS1} = V_{BUS2} = 0 V ISO 17987 (Par. 13)	P_7.1.40
Leakage current driver off and bus recessive	$I_{BUSx_PAS_rec_x}$	–	1	5	µA	V_S = 8 V, V_{BUS1} = V_{BUS2} = 18 V, ISO 17987 (Par. 14)	P_7.1.41
Forward voltage serial diode	$V_{SerDiode_x}$	0.4	–	1.0	V	$I_{SerDiodex}$ = 75 µA[1] ISO 17987 (Par.21)	P_7.1.42
Bus pull-up resistance	R_{slave_x}	20	40	60	kΩ	Normal Operation mode; ISO 17987 (Par. 26)	P_7.1.43
Input capacitance	C_{i,BUS_x}	–	–	30	pF	[2]	P_7.1.46

1) ΔV_{BUSx} = voltage difference between V_S and BUSx. $V_{SerDiodex}$ = ΔV_{BUSx} - $I_{SerDiodex}$ * $R_{Slave\ x}$
2) Not subject to production test, specified by design

7.1.4.3 Dynamic transceiver parameters

Table 13 Dynamic transceiver parameters

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Propagation delay BUSx to RxDx (“dominant” to “low”)	$t_{rx_pdf_x}$	1	3.5	6	µs	R_{RxD1} = R_{RxD2} = 2.4 kΩ; C_{RxD1} = C_{RxD2} = 20 pF; ISO 17987 (Par. 31)	P_7.1.47
Propagation delay BUSx to RxDx (“recessive” to “high”)	$t_{rx_pdr_x}$	1	3.5	6	µs	R_{RxD1} = R_{RxD2} = 2.4 kΩ; C_{RxD1} = C_{RxD2} = 20 pF; ISO 17987 (Par. 31)	P_7.1.48
Receiver delay symmetry	$t_{rx_sym_x}$	-2	–	2	µs	t_{rx_sym} = t_{rx_pdf} - t_{rx_pdr}; R_{RxD1} = R_{RxD2} = 2.4 kΩ; C_{RxD1} = C_{RxD2} = 20 pF; ISO 17987 (Par. 32)	P_7.1.49
Duty cycle D1 (for worst case at 20 kBit/s)	*D1*	0.396	–	–		Duty cycle 1 [1] $TH_{Rec(max)}$ = 0.744 × V_S; $TH_{Dom(max)}$ = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$ / 2 × t_{bit}; ISO 17987 (Par. 27)	P_7.1.50
Duty cycle D1 for V_S supply 5.5 V to 7.0 V (for worst case at 20 kBit/s)	*D1*	0.396	–	–		Duty cycle 1 [1] $TH_{Rec(max)}$ = 0.760 × V_S; $TH_{Dom(max)}$ = 0.593 × V_S; V_S = 5.5 … 7.0 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$ / 2 × t_{bit};	P_7.1.51
Duty cycle D2 (for worst case at 20 kBit/s)	*D2*	–	–	0.581		Duty cycle 2 [1] $TH_{Rec(min)}$ = 0.422 × V_S; $TH_{Dom(min)}$ = 0.284 × V_S; V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$ / 2 × t_{bit} ; ISO 17987 (Par. 28)	P_7.1.52
Duty cycle D2 for V_S supply 6.1 V to 7.6 V (for worst case at 20 kBit/s)	*D2*	–	–	0.581		Duty cycle 2 [1] $TH_{Rec(min)}$ = 0.410 × V_S; $TH_{Dom(min)}$ = .275 × V_S; V_S = 6.1 … 7.6 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$ / 2 × t_{bit} ;	P_7.1.53

Table 13 Dynamic transceiver parameters (cont'd)

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_J < 150 °C
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D3 (for worst case at 10.4 kBit/s)	*D3*	0.417	–	–		Duty cycle 3 [1] $TH_{Rec(max)}$ = 0.778 × V_S; $TH_{Dom(max)}$ = 0.616 × V_S; V_S = 7.0 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus_rec(min)}$ / 2 × t_{bit}; ISO 17987 (Par. 29)	P_7.1.54
Duty cycle D3 for V_S supply 5.5 V to 7.0 V (for worst case at 10.4 kBit/s)	*D3*	0.417	–	–		Duty cycle 3 [1] $TH_{Rec(max)}$ = 0.797 × V_S; $TH_{Dom(max)}$ = 0.630 × V_S; V_S = 5.5 … 7.0 V; t_{bit} = 96 µs; D3 = $t_{bus_rec(min)}$ / 2 × t_{bit};	P_7.1.55
Duty cycle D4 (for worst case at 10.4 kBit/s)	*D4*	–	–	0.590		Duty cycle 4 [1] $TH_{Rec(min)}$ = 0.389 × V_S; $TH_{Dom(min)}$ = 0.251 × V_S; V_S = 7.6 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus_rec(max)}$ / 2 × t_{bit} ; ISO 17987 (Par. 30)	P_7.1.56
Duty cycle D4 for V_S supply 6.1 V to 7.6 V (for worst case at 10.4 kBit/s)	*D4*	–	–	0.590		Duty cycle 4 [1] $TH_{Rec(min)}$ = 0.378 × V_S; $TH_{Dom(min)}$ = 0.242 × V_S; V_S = 6.1 … 7.6 V; t_{bit} = 96 µs; D4 = $t_{bus_rec(max)}$ / 2 × t_{bit} ;	P_7.1.57

1) Bus load concerning LIN Spec 2.2:
Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_L
Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_L
Load 3 = 10 nF / 500 Ω = C_{BUS} / R_L

7.2 Diagrams

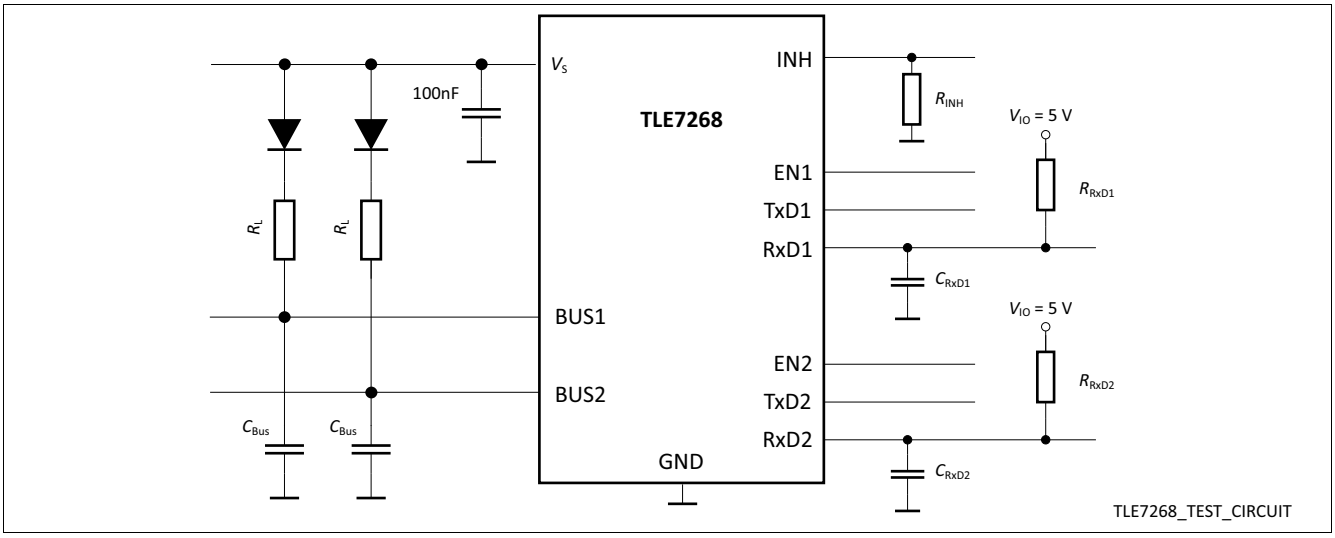


Figure 13 Simplified test circuit

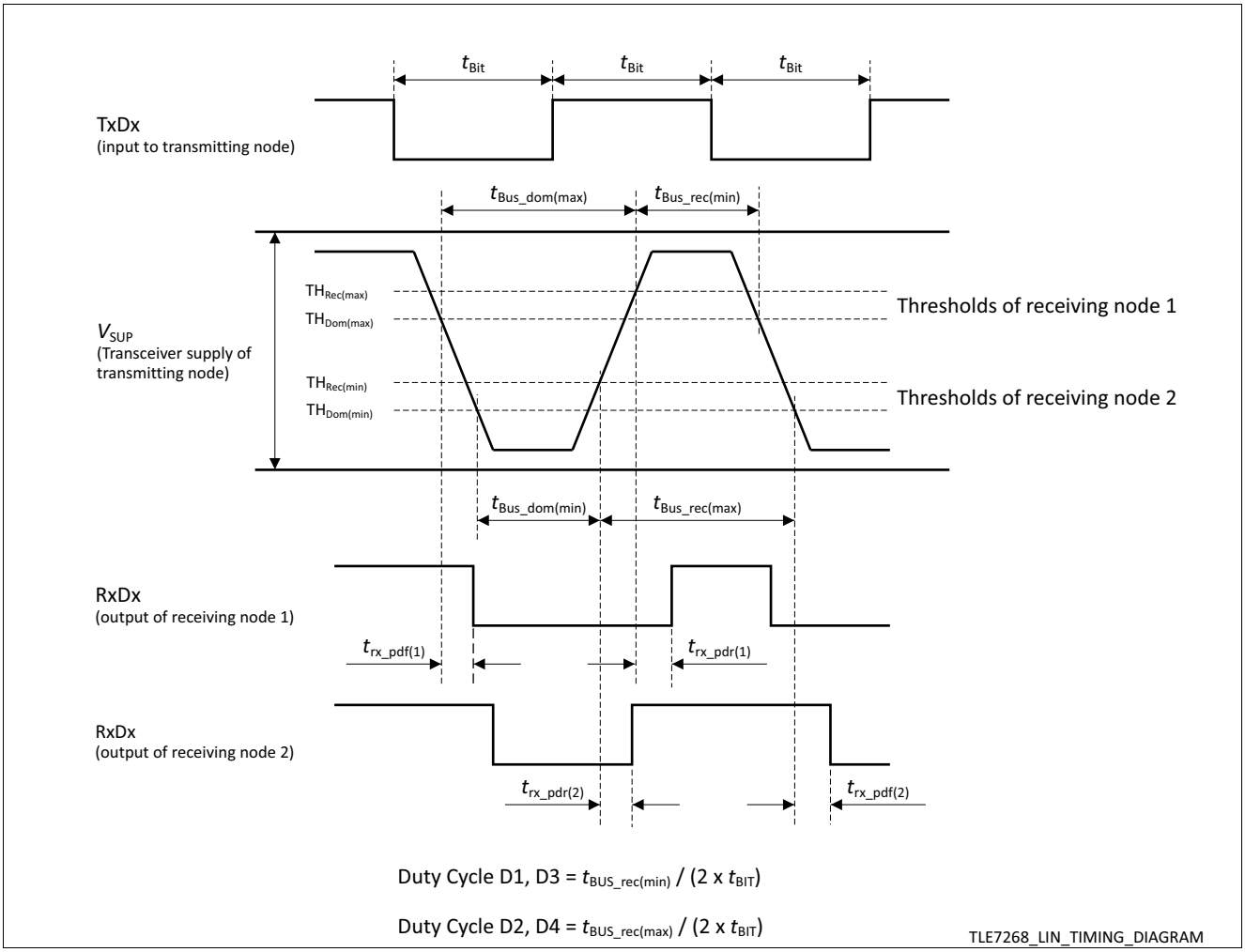


Figure 14 Timing diagram for dynamic characteristics

8 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

8.1 ESD robustness according to IEC61000-4-2

Tests for ESD robustness according to IEC61000-4-2 Gun test (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 14 ESD robustness according to IEC61000-4-2

Performed test	Result	Unit	Remarks
Electrostatic discharge voltage at pin V_S, BUS versus GND	≥ +10	kV	[1)]Positive pulse
Electrostatic discharge voltage at pin V_S, BUS versus GND	≤ -10	kV	[1)]Negative pulse

1) Not subject to production test. ESD susceptibility “ESD GUN” according IEC 61000-4-2, Tested by external test facility (IBEE Zwickau, EMC test report Nr. 04-05-17 and Nr. 14-06-17).

8.2 Physical layer compatibility

Since the LIN physical layer is independent from higher LIN layers (for example LIN protocol layer), all nodes with a LIN physical layer according to this revision can be mixed with LIN physical layer nodes according to older revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1 and LIN 2.2) without any restrictions.

8.3 TxD fail safe input

The TxD1/TxD2 inputs have internal pull-up structures for avoiding bus disturbance in case the TxDx input is open. In case of an unconnected TxDx input, the TxDx is pulled up to an internal voltage supply (see Figure 1) and the output to the LIN bus on the pin BUSx is always recessive. This ensures that the transceiver does not disturb communication on the LIN bus.

In Sleep mode the pull-up structure on each TxD1/TxD2 input is disabled in order to minimize quiescent current of the TLE7268. The logic at the TxDx input does not react to any signal change on the TxDx input and the transmitter_x is turned off. In Sleep mode the transceiver_x can not disturb or block the LIN BUSx.

Table 15 TxDx termination (TxDx inputs open)

Operation mode	Internal pull-up structure	TxDx input signal	Transmitter_x	BUSx output
Normal Operation mode	active	“high”	on	recessive
Standby mode	active	“high”	off	recessive
Sleep mode	inactive	floating	off	recessive

8.4 Application example

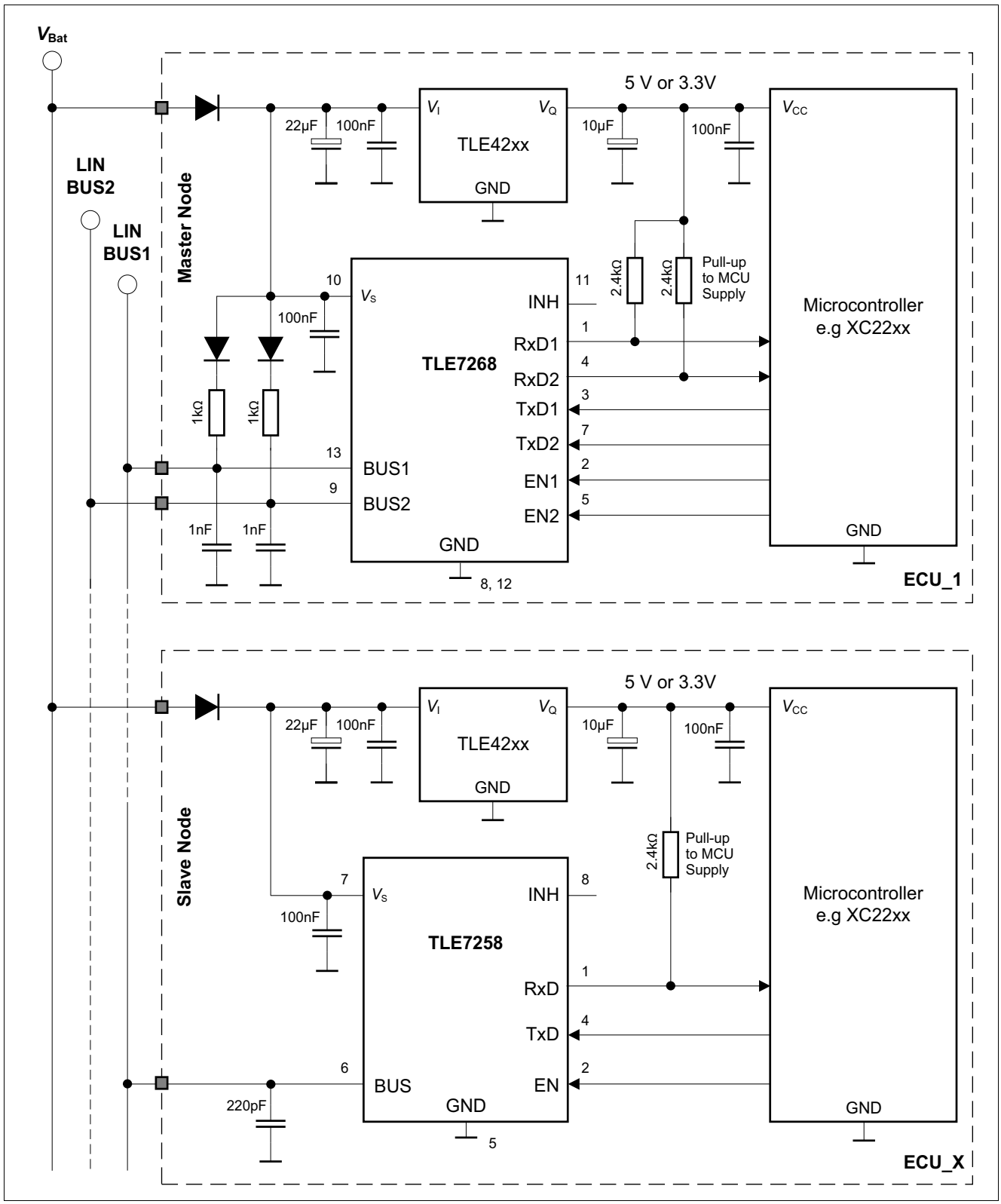


Figure 15 Simplified application circuit

8.5 RxDx pull-up resistor

The receive data outputs RxD1/RxD2 provide open drain behavior for allowing the output level to be adapted to the microcontroller supply voltage. Because of this, 3.3 V microcontroller derivatives without 5 V tolerant ports can be used. In case the microcontroller port pin does not provide integrated pull-up circuits, external pull-up resistors connected to the microcontroller logic supply voltage V_{IO} are required.

Figure 16 shows typical RxD1/RxD2 pin input current and input voltage characteristics across temperature. The RxDx pull-up resistors can be dimensioned according to the minimum “high”-level input voltage and the maximum “low”-level input voltage of the application’s microcontroller port pins’ (Rx). Typically pull-up resistors R_{RxD1}/R_{RxD2} of 2.4 kΩ are recommended.

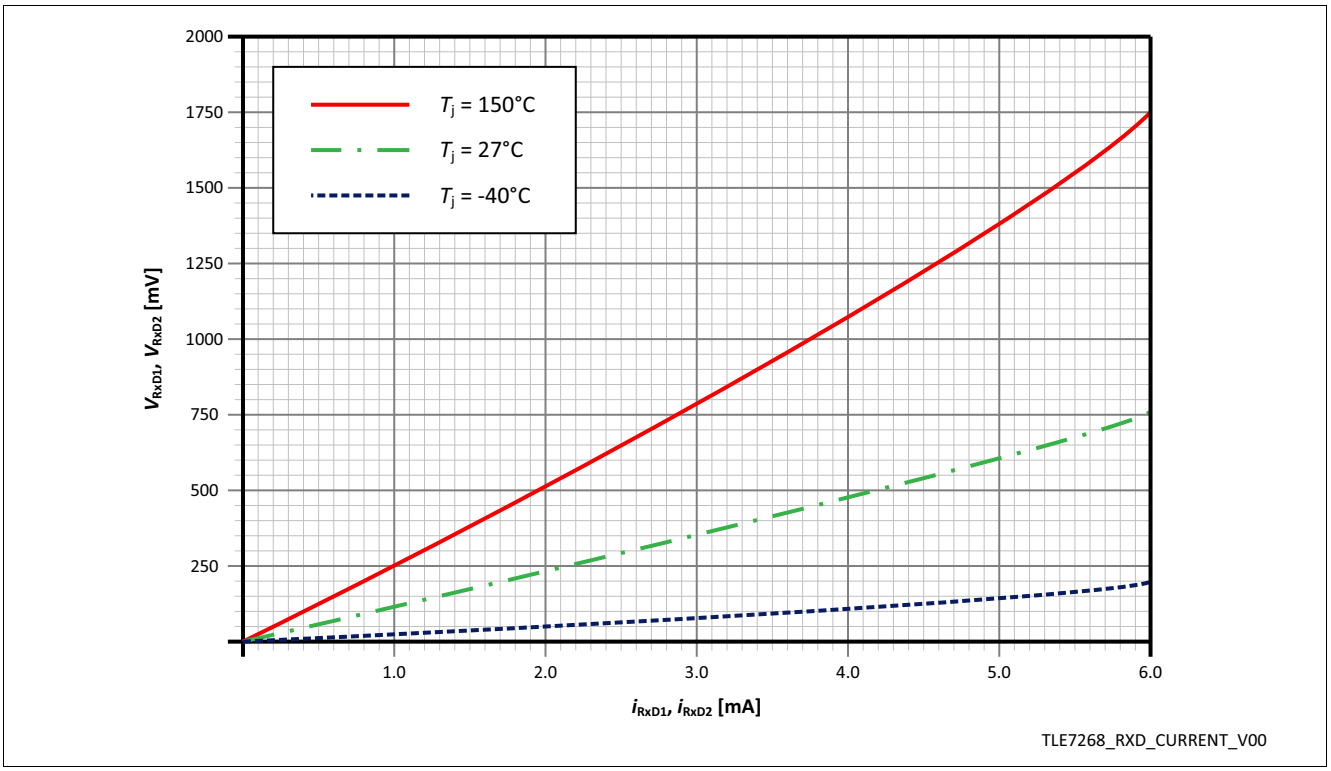
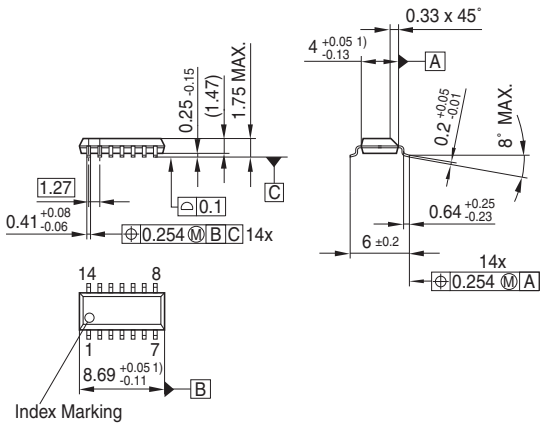


Figure 16 RxDx pin input typical current and voltage characteristics

8.6 Further application information

- Please contact Infineon for information regarding the FMEA pin
- For further information you may contact www.infineon.com/automotive-transceiver

9 Package outlines



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 17 PG-DSO-14

Package outlines

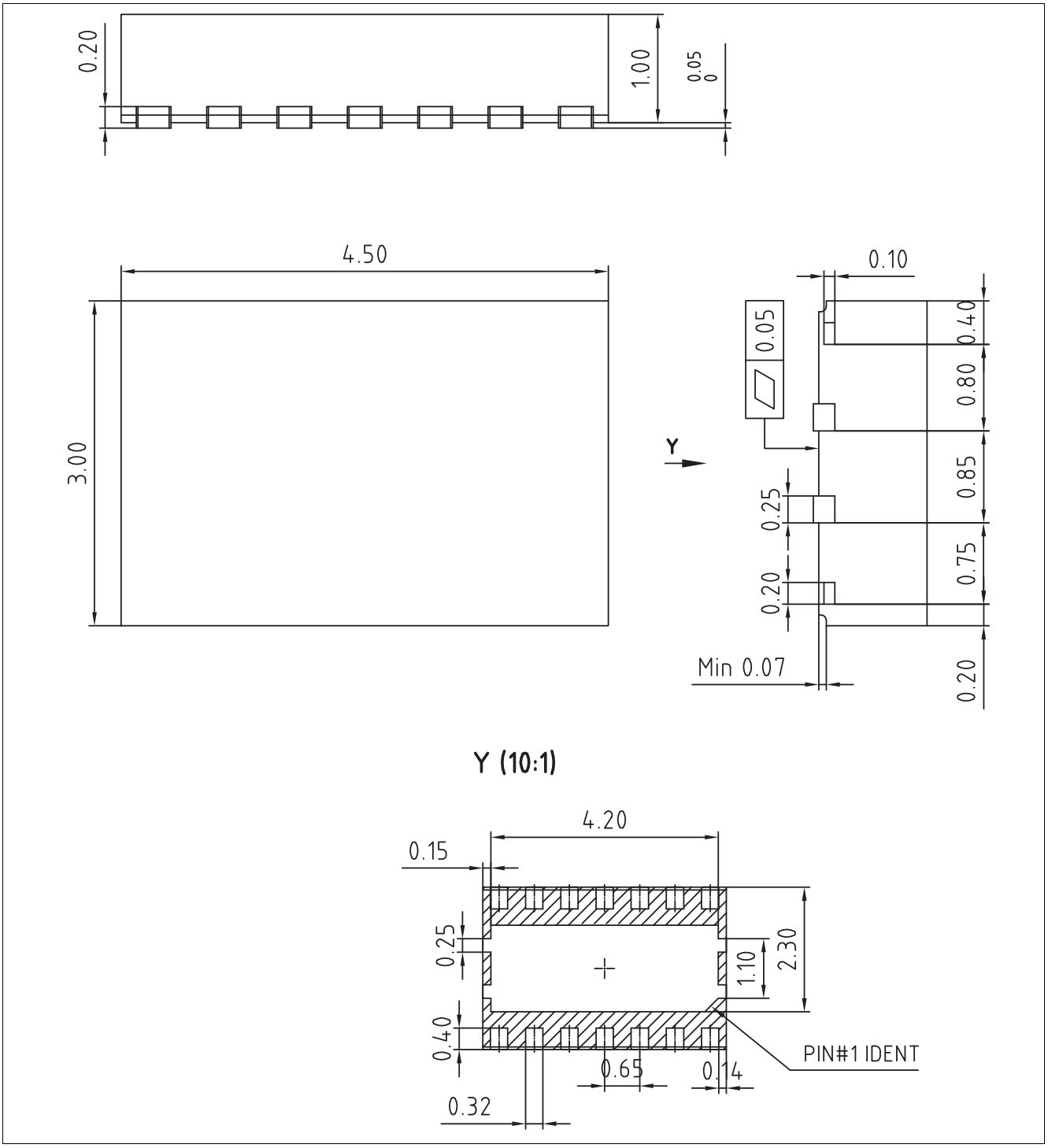


Figure 18 PG-TSON-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

10 Revision history

Table 16 Revision history

Revision	Date	Changes
1.0	2017-07-25	Data Sheet created

Trademarks of Infineon Technologies AG
µHVIC™, µIPM™, µPFC™, AU-ConvertIR™, AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolDP™, CoolGaN™, COOLiR™, CoolMOS™, CoolSET™, CoolSiC™, DAVE™, DI-POL™, DirectFET™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, GaNpowIR™, HEXFET™, HITFET™, HybridPACK™, iMOTION™, IRAM™, ISOFACE™, IsoPACK™, LEDrivIR™, LITIX™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OPTIGA™, OptiMOS™, ORIGA™, PowIRaudio™, PowIRStage™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, SmartLEWIS™, SOLID FLASH™, SPOC™, StrongIRFET™, SupIRBuck™, TEMPFET™, TRENCHSTOP™, TriCore™, UHVIC™, XHP™, XMC™.

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