500 W ultra-low-profile CoolGaN™ LLC converter

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About this document

Scope and purpose

This engineering report explains how to set up and run the 500 W ultra-low-profile CoolGaN™ LLC converter board, intended as an evaluation board for TV power supply applications. This board features CoolGaN™ Transistor 100 V G3 IGC033S101, CoolGaN™ Transistor 650 V G5 IGLD65R110D2, and XDPP1148-100B digital controller as shown in Figure 1.

The board converts the high DC input voltage to a constant 22 V DC output. At full load, the average operating frequency of this unit varies from 400 kHz to 500 kHz depending on the input voltage level. To demonstrate the operation of the board, some test points are provided to observe the signals with proper test equipment. Finally, some of the unit's performance metrics, such as hardware thermal imaging, and efficiency vs. load, are evaluated.

Intended audience

This engineering report is intended for power electronics design engineers, applications engineers, and students who are familiar with power converters.

Infineon components featured

- IGC033S101
- IGLD65R110D2
- XDPP1148-100B
- 2EDS8265H
- 1EDN7136U

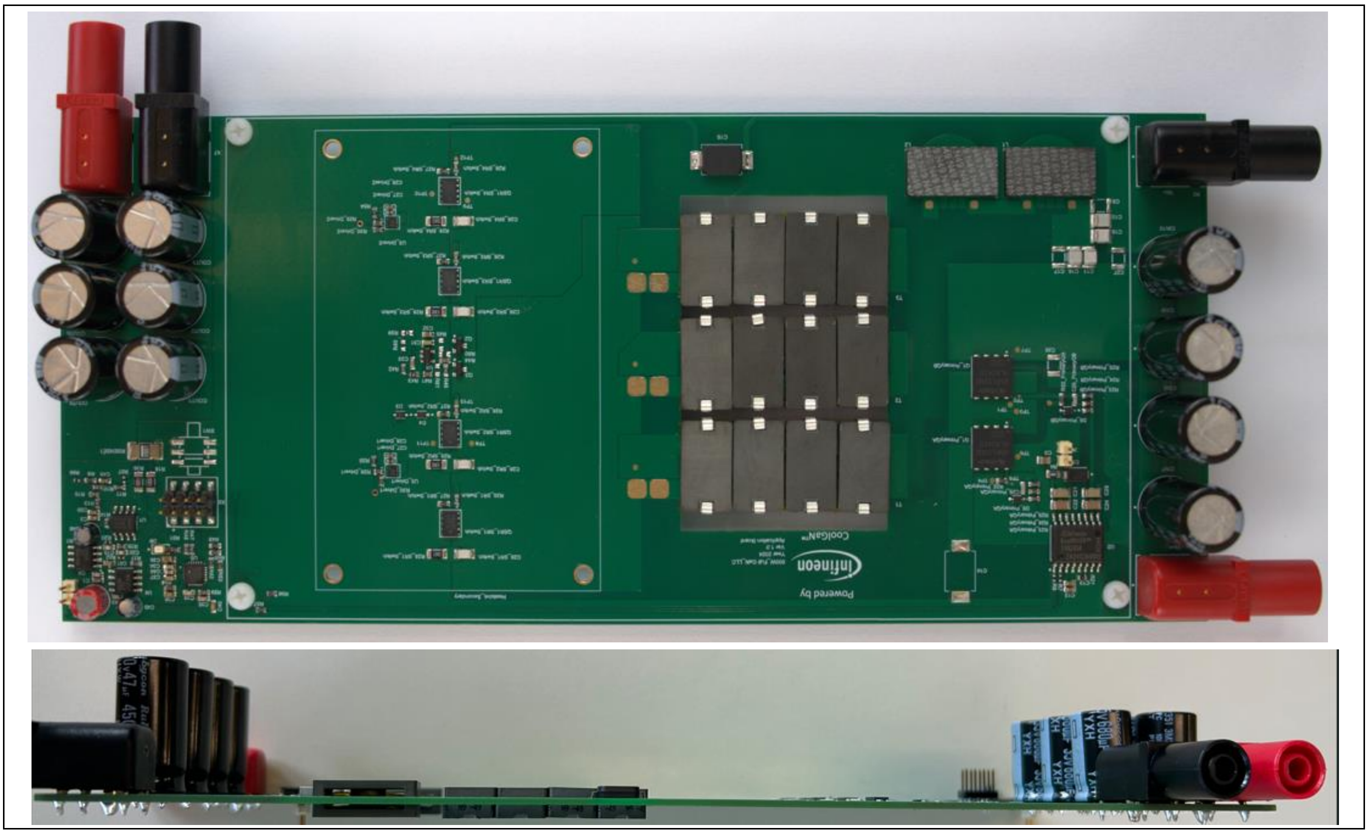

Figure 1 500 W ultra-low-profile evaluation board featuring CoolGaN™ IGC033S101

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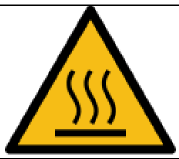
Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

The 500 W ultra-low-profile CoolGaN™ LLC converter board provides a quick way to evaluate the Infineon CoolGaN™ technology in both primary and secondary sides in TV power supply applications in a high-frequency, half-bridge LLC topology ([1],[2]). As shown in Figure 2, the main controller of the half-bridge LLC converter is the Infineon XDPP1148 digital power supply controller. The typical application diagram of XDPP1148 in half-bridge LLC is shown in Figure 3 ([3]).

To observe the thermal performance of the components installed on the PCB of the reference design, the PCB layout is designed in a non-compact form factor with least occupied space. In a practical end product design, you can optimize the PCB layout and reduce the hardware volume based on the designers' preference in manufacturing approach.

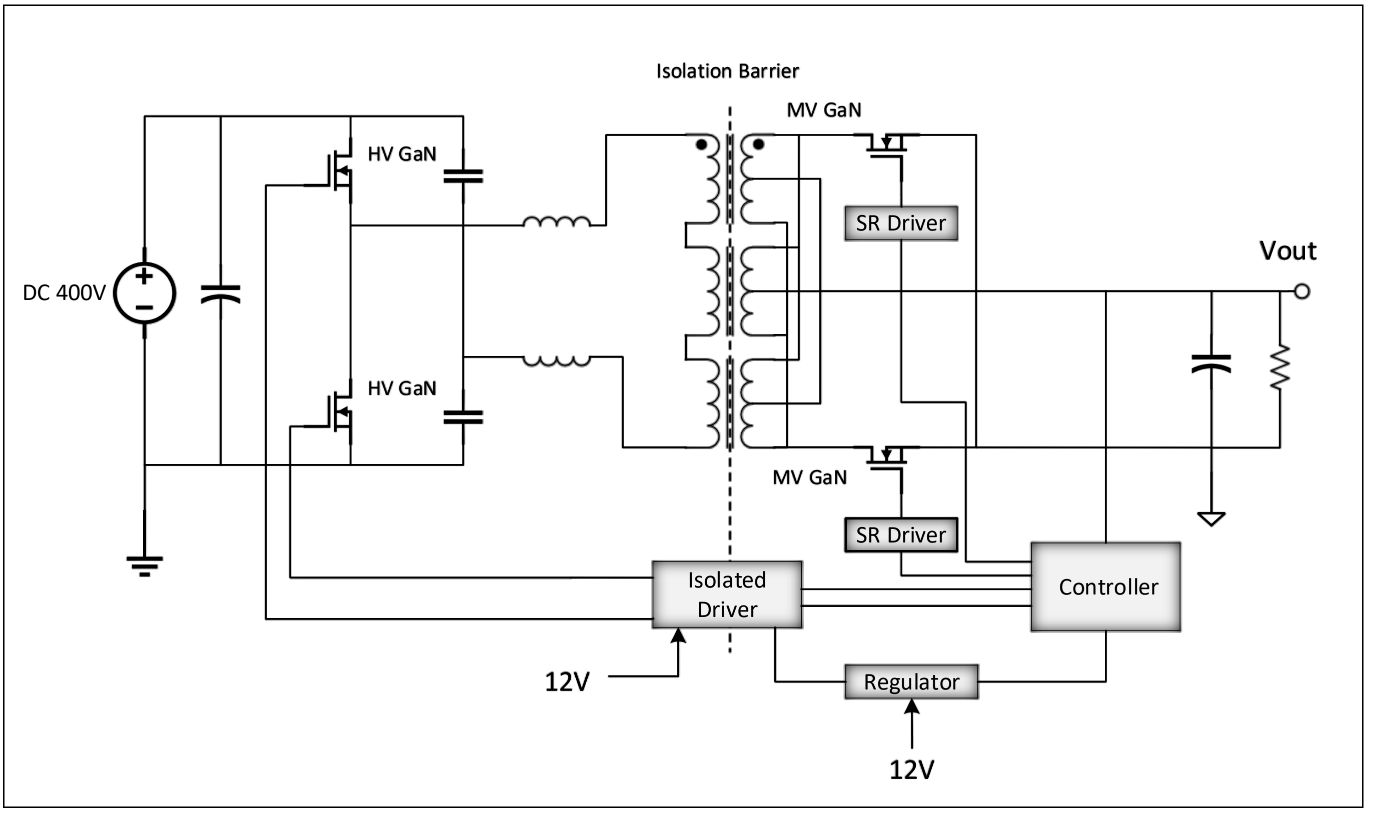


Figure 2 CoolGaN™ technology in half-bridge LLC topology

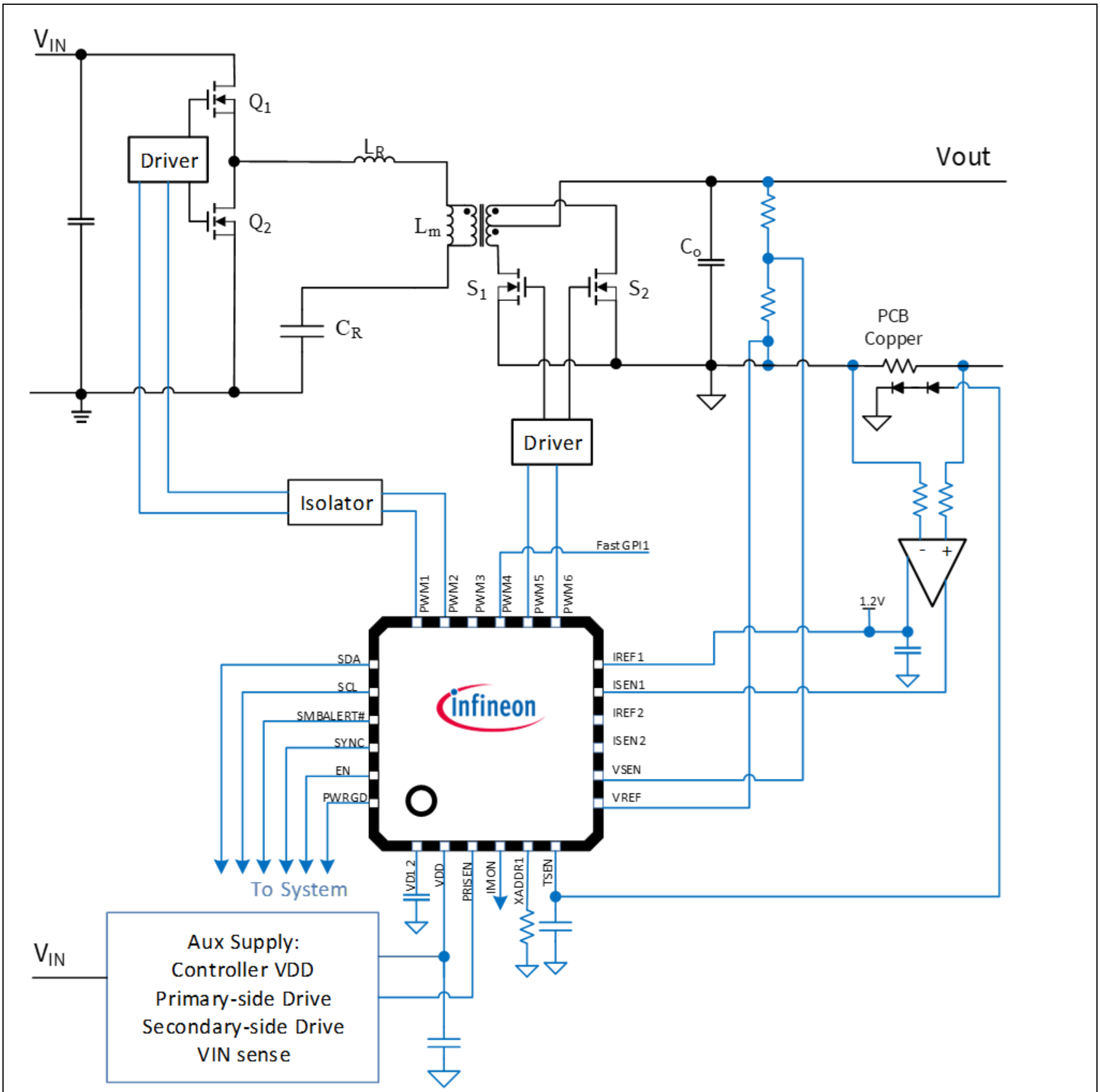


Figure 3 XDPP1148 digital power supply controller circuitry in half-bridge topology

1.1 Reference board specifications

Table 2 Reference board specifications and limits

Parameter	Values			Unit	Notes
	Min.	Typ.	Max.		
DC input voltage	375		410	V	
DC input current			2	A	
DC output voltage		22	24	V	
DC output current	0		20	A	
Efficiency (peak)			96	%	
Standby power consumption			< 300	mW	
Rated power			500	W	
Operating frequency at full power	350		550	kHz	Changes based on the input voltage
Operating ambient temperature		25	40	°C	

Note: The PCB dimensions are 100 x 180 mm (max.).

2 Functional description

The block diagram of the hardware and their functions is shown in Figure 4. The DC input stage includes the input DC source and electrolytic capacitors. The primary side mainly includes the CoolGaN™ Transistor 650 V G5 IGLD65R110D2, two adjacently placed resonant inductors, resonant capacitors, and transformer primary-side windings. The 2EDS8265H isolated gate driver drives the high-side and low-side HV GaN transistor on the primary side through the PWM signals generated from the XDPP1148-100B secondary-side digital controller. The feedback signals to the digital controller are provided by the current-sensing resistor and the output voltage resistor divider. The output voltage is regulated by the resistor divider, and it is set to regulate the output DC voltage at 22 V. The synchronous rectifier (SR) IGC033S101 MV GaN transistor is driven by the gate driver through the PWM signals generated from the same digital controller as the primary PWM. Figure 5 shows a different section of the reference board.

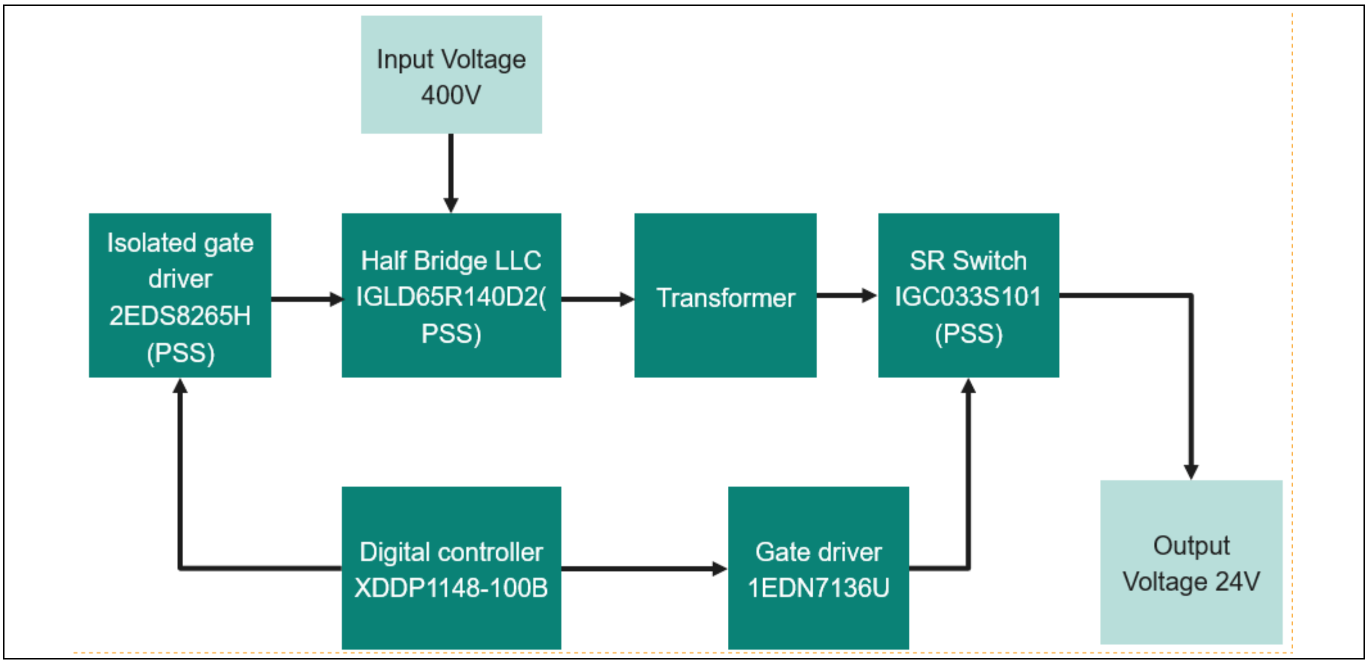


Figure 4 Block diagram of the CoolGaN™ IPS evaluation hardware in ACF topology [3]

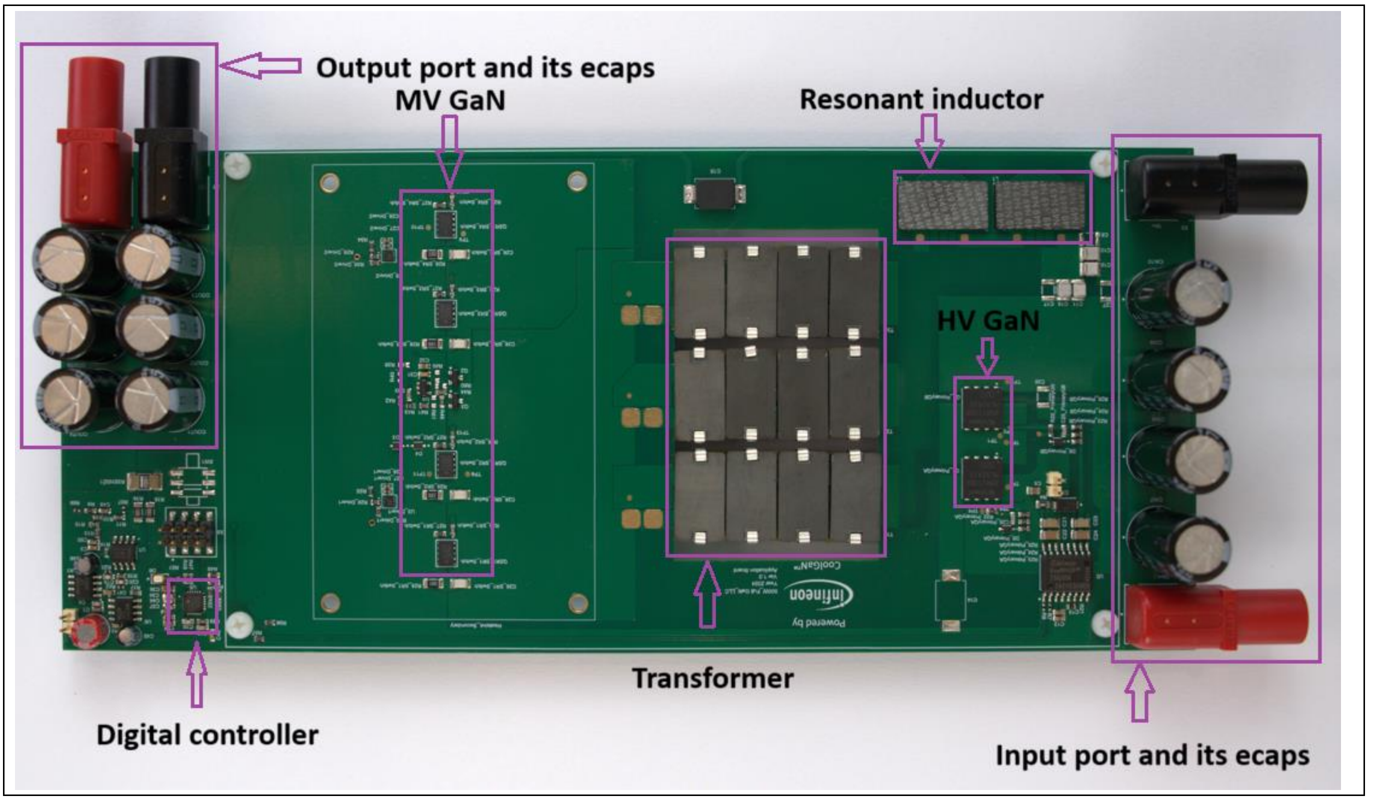


Figure 5 Evaluation board sections

The schematic is shown in Figure 6. The following sections explain each item in detail.

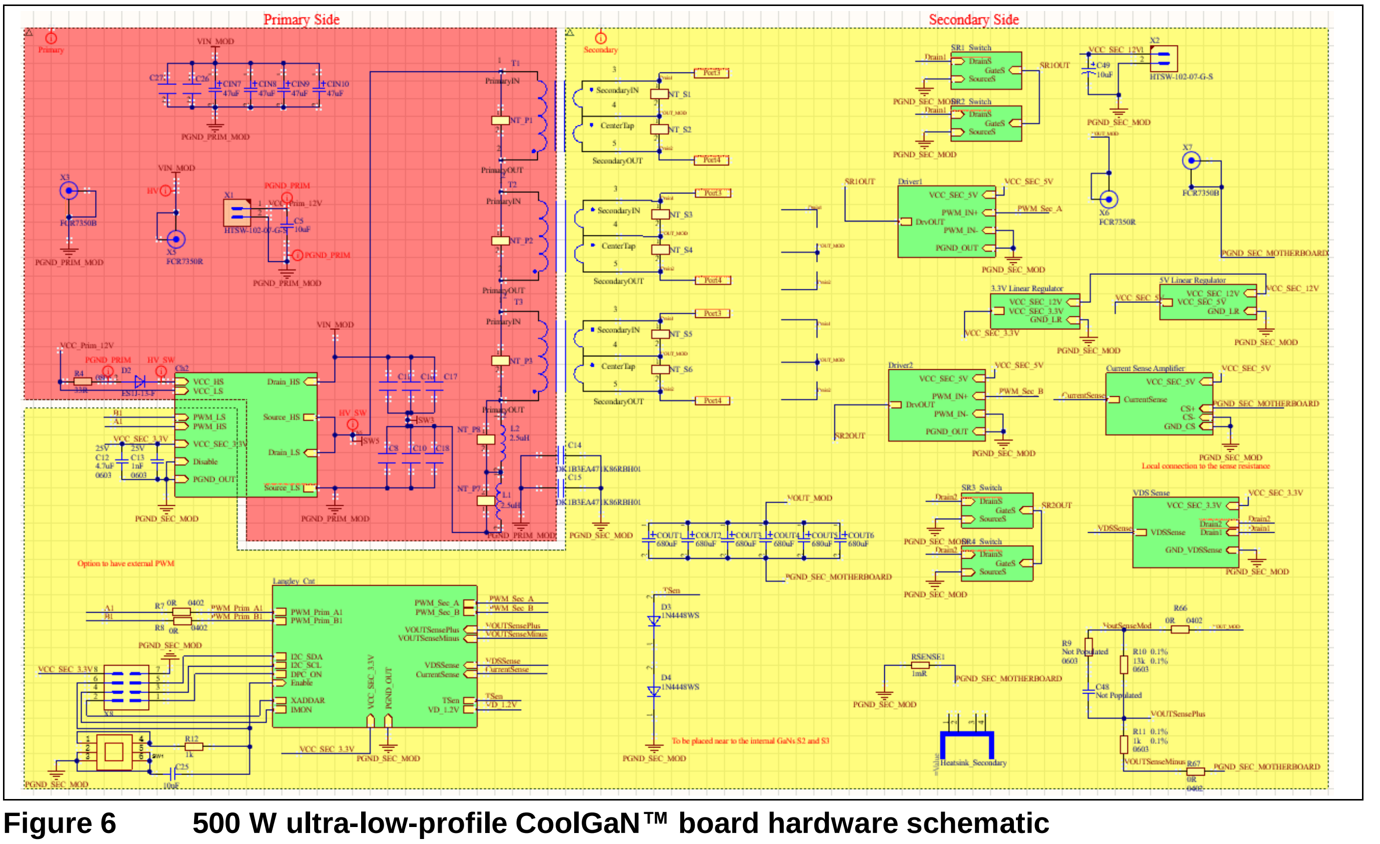


Figure 6 500 W ultra-low-profile CoolGaN™ board hardware schematic

2.1 HV CoolGaN™ circuitry

Figure 7 shows the circuitry around the primary-side CoolGaN™ Transistor 650 V G5 IGLD65R110D2 in this reference board. The XDPP1148 secondary-side digital controller sends the PWM signals to the primary-side HV GaN bridge through the 2EDS8265H isolated gate driver.

In this application, the CoolGaN™ Transistor 650 V G5 IGLD65R110D2's driving circuit should be current mode circuit, providing a constant driving current when the GaN transistor is on. In addition, to enhance the anti-interference ability of noise when the GaN transistor is off, the negative voltage turning off is adopted.

In Figure 7, when the GaN transistor is on, the value of R25 and gate voltage determines the constant driving current, while R24 determines the slew rate of the rising current at the beginning. At the turn-on stage, the driving current charges the capacitor C25, which makes the C25 voltage positive (left side "+", right side "-"). At the turn-off stage, the driving voltage becomes zero; Q1 turning off will become voltage negative. When turning off, the turning-off current will mainly pass through D5 and R23, so the value of R23 determines the turn-off speed [4].

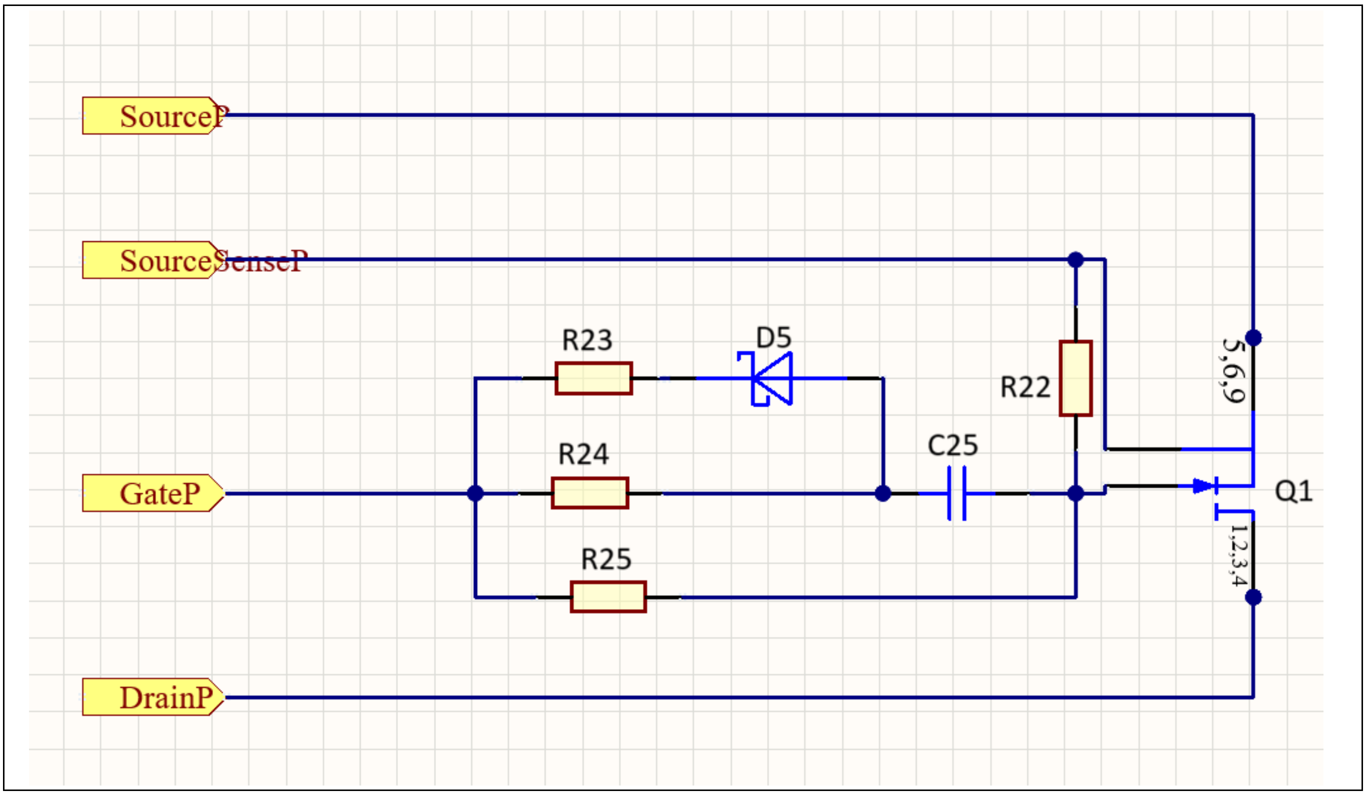


Figure 7 Primary HV CoolGaN™ circuitry in 500 W half-bridge topology

2.1.1 HV GaN gate driver

The output side of the 2EDS8265H HV GaN gate driver includes two supply power terminals [5]:

- Low-side V_{CC} directly supplied by the external 12 V DC voltage at the primary side
- High-side V_{CC} supplied by the bootstrap circuit having the same external 12 V DC voltage input as the low-side V_{CC}

The input side power is provided by the 3.3 V generated by the secondary-side LDO, whose input voltage is the external 12 V DC voltage at the secondary side.

2.1.2 SR gate driver

A 5 V V_{CC} generated from the secondary-side LDO is used to supply the two 1EDN7136 SR gate drivers. The RC network for this channel consists of R5, R6, and C3. As for the low-side, a standard 22 kΩ resistor is used to ensure pull-down of the high-side GaN gate during startup. One series 47 kΩ resistor is required on each of the two input pins (IN+ and IN-).

2.1.3 Enable circuit

Figure 8 shows the circuit which connects a mechanical switch to the enable pin. An RC filter is often added between them for improving the reliability and stability of the enable signal provided by the XDP114x digital controller. Normally, R = 1 kΩ and C=10 nF is recommended.

By connecting an external mechanical switch for the enabling function, you can manually change the power status. Also, the EN logic can be configured to be active HIGH or active LOW.

Note that the enable signal is asserted if ON_OFF_CONFIG is set to “response to EN”. It is recommended that EN be asserted only after VCC_Prim_12V, VCC_SEC_12V, and power supplies (VIN_MOD) for the power stages are ready.

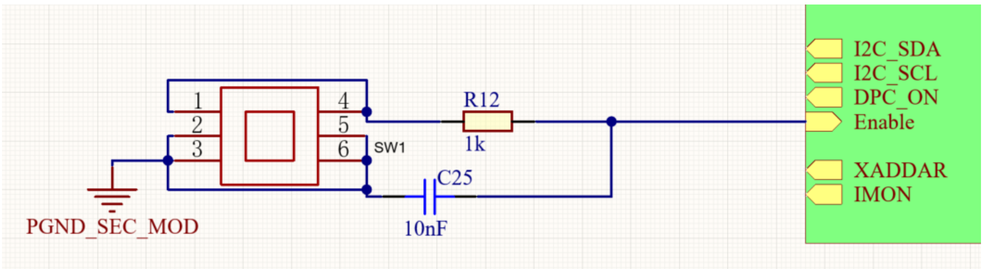


Figure 8 Enable circuit

2.1.4 Transformer design

For an ultra-thin power supply design, the highest components (normally, magnetic components such as the transformer and resonant inductor) should not exceed the maximum height of the application.

Since the target design is a 7-mm-tall DC-DC power supply, a planar transformer core is required. After considering the PCB dimensions and optional magnetic cores, three groups of four ELP 18/4/10 with I 18/2/10 cores in cascade are selected in series connection for the transformer cores. The primary side windings of the three groups cores are in series configuration and the secondary side windings is in parallel configuration. The transformer magnetic base unit cores’ dimension is shown in Figure 9. With such magnetic core selection, the transformer total height is lower than 6.1 mm. The calculated primary winding to secondary windings turns ratio is 9:1, and each group core has a 3:1 turns ratio.

For the transformer windings configuration, the top and bottom layers are placed with one turn of secondary winding, and middle layer 1 and middle layer 2 are placed with three turns of primary windings. To reduce the AC resistance of primary windings, the three turns of primary windings are in series configuration.

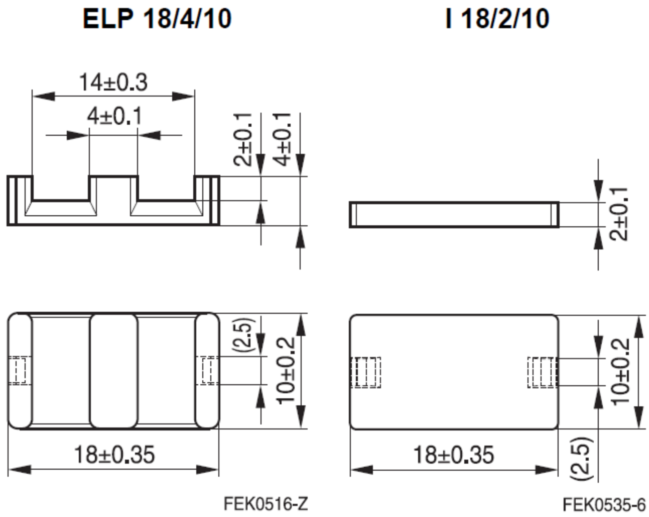


Figure 9 Transformer unit core dimensions

2.1.5 Resonant inductor design

Resonant inductor design has the same considerations as the transformer core. There are two resonant inductors in series. Two pairs of ER 18/3/10 cores are selected for the resonant inductor cores. The inductor magnetic cores' dimension is shown in Figure 10. This magnetic core selection allows for the inductor total height to be below 6.3 mm with the calculated inductor windings number as four for each (one turn windings on each layer).

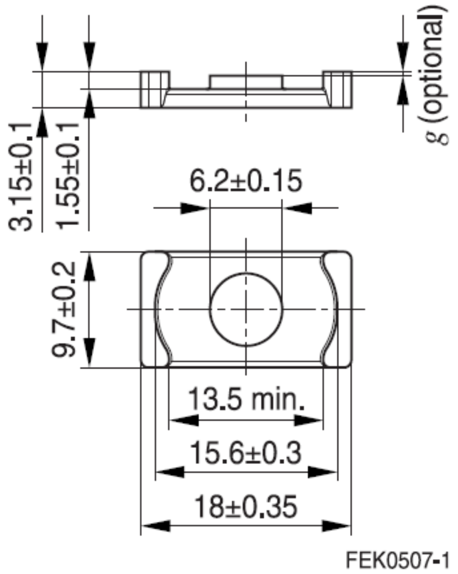


Figure 10 **Transformer unit core dimensions**

3 Setup and use

Figure 11 shows the interface ports on the board. It mainly consists of three parts:

1. Input voltage and output voltage ports (J1 and J2)
2. Primary and secondary VCC input voltage ports
3. I2C interface ports

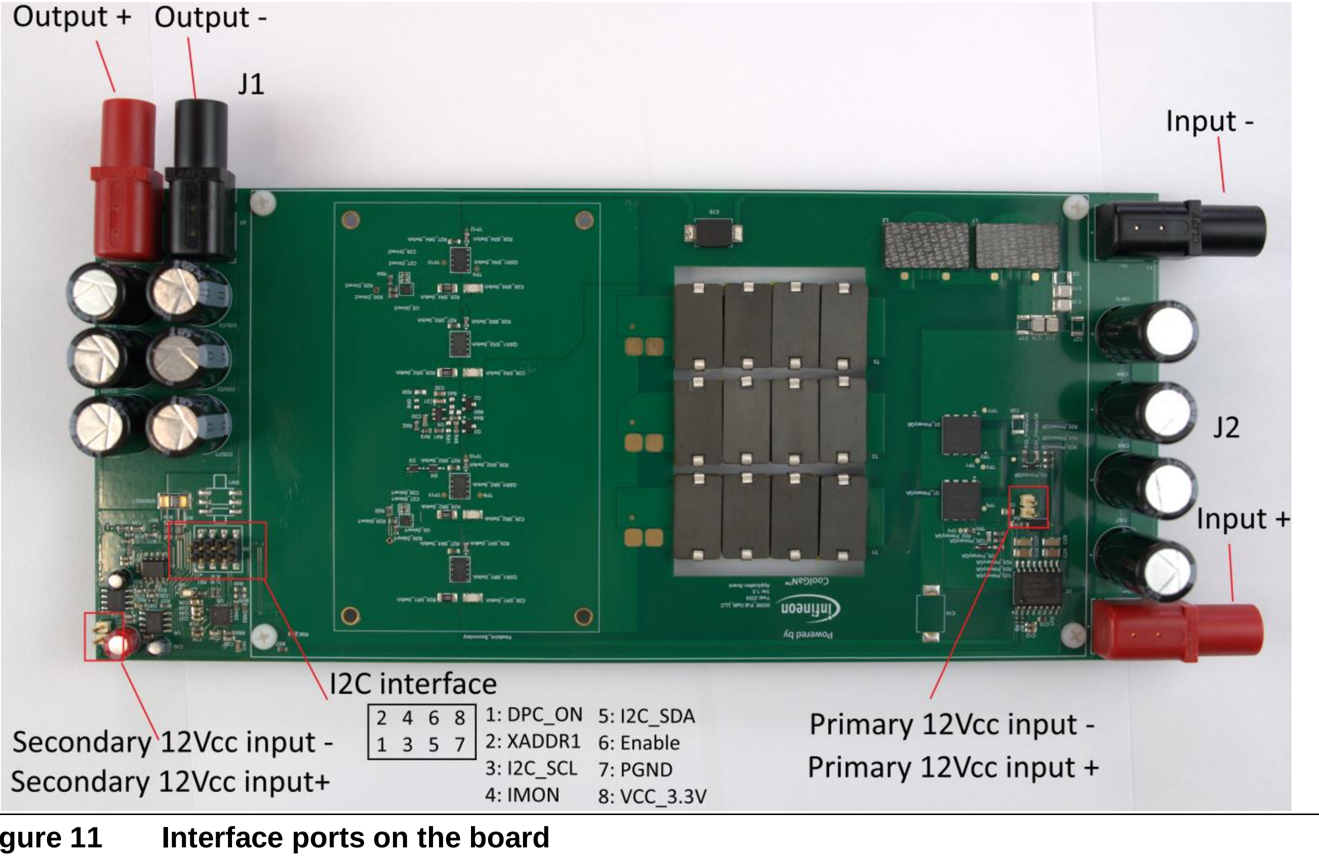


Figure 11 Interface ports on the board

Figure 12 shows the recommended configuration to measure the efficiency of the reference board using two channels of a power analyzer. If a power analyzer is not used, connect the DC source directly to the DC (in) terminal (J2) and the DC load to LV (+) and LV (-) on the J1 terminal. If the DC load is an electronic load, note the polarity to avoid damaging the load.

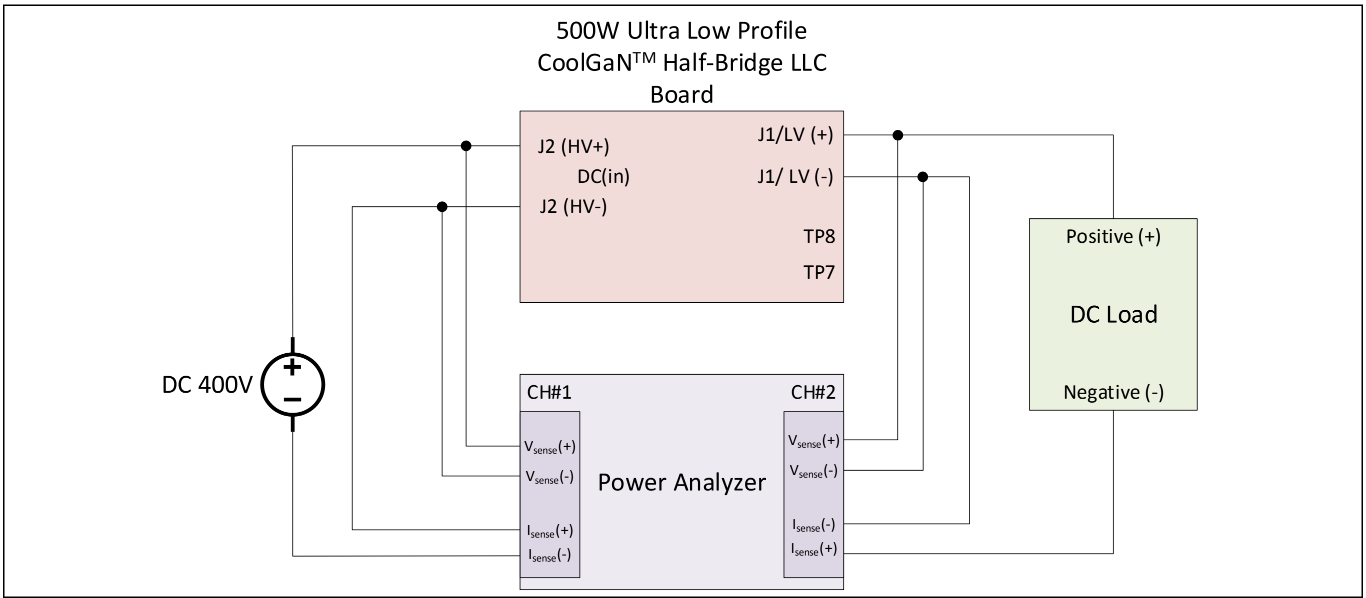


Figure 12 Recommended connections for efficiency measurements [3]

Attention: ***This evaluation hardware has high-voltage terminals and exposed areas. To avoid electric shock, take appropriate measures. The hardware does not have any overvoltage protection system. Use an appropriate protective epoxy shield or box to cover the hardware to prevent any possible injury.***

Attention: ***Always observe the input and output voltages. Do not operate the board above the specified input voltage (410 V DC). Use a lab test power supply with a current limit and set it to a proper value to avoid catastrophic damage to the board in case of any failure. Eye and ear protection are recommended for safety, because all power electronic labs employ it. Contact Infineon for any safety concerns and technical questions.***

3.1 Test equipment required

1. DC power supply up to 410 V with sufficient current (~2 A_{RMS}) and with proper high-voltage cables
2. Oscilloscope for measurements and observations with standard passive probes
3. Power analyzer (two channels) to measure efficiency
4. Isolated current probe (Rogowski type) to observe the resonant current
5. Voltmeter to measure the output DC voltage
6. DC electronic load

3.2 Setting up the XDPP1148 development environment

Projects based on the XDPP1148 digital controller are developed using the XDP™ Designer design tool, a multi-platform development toolset. This tool enables you to evaluate and configure the XDPP1148 controller, allowing for real-time modifications to fault thresholds, response setting, and other parameters, which are stored in RAM and can be modified an unlimited number of times. However, these changes will be lost when the input voltage and 3.3 V VDD are removed, unless you store the customized configuration in the one-time programmable (OTP) memory, ensuring that these settings are retained even when the power is cycled.

3.2.1 Download XDP™ Designer

Download and install XDP™ Designer through Infineon Developer Center Launcher (DCL).

After installing the tool, use the USB007A1 USB-to-I2C convertor device to connect the PC and the board.

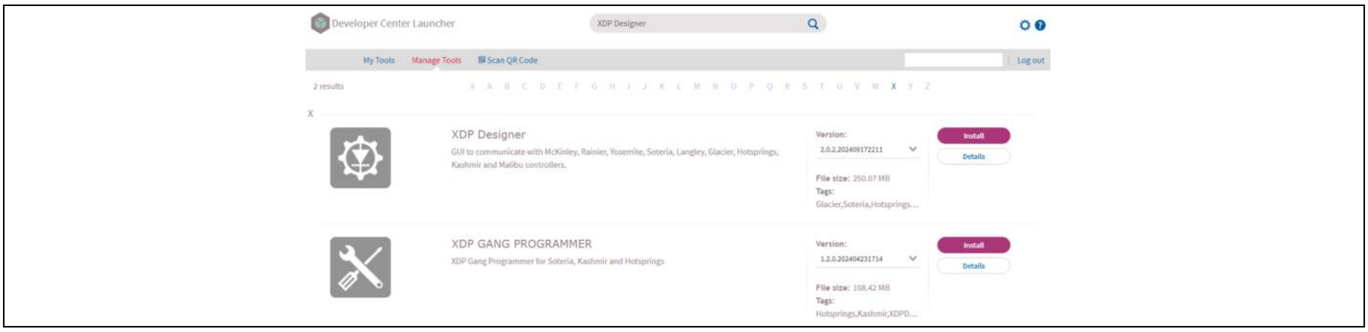


Figure 13 Downloading XDP™ Designer GUI

3.2.2 Topology selection and PWM mapping

In the XDP™ Designer tool, configure the topology to LLC Half bridge (Primary Side Type) with Center Tapped (Secondary Side Type), mapping the PWMs according to hardware pin connections.

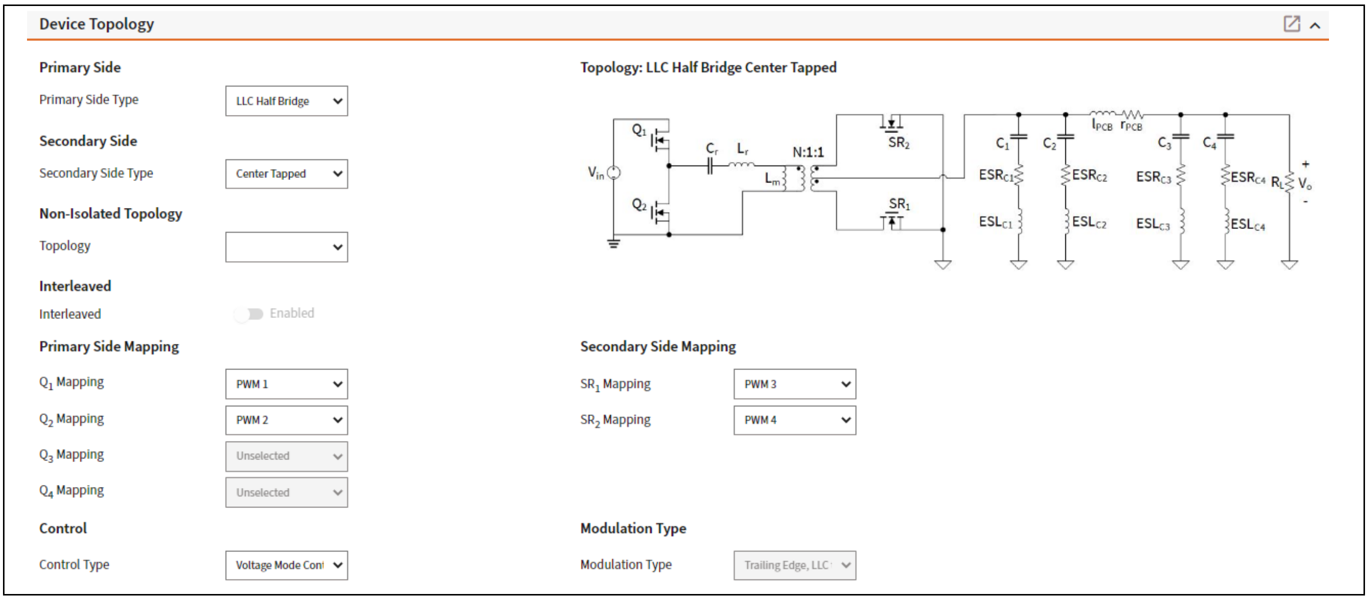
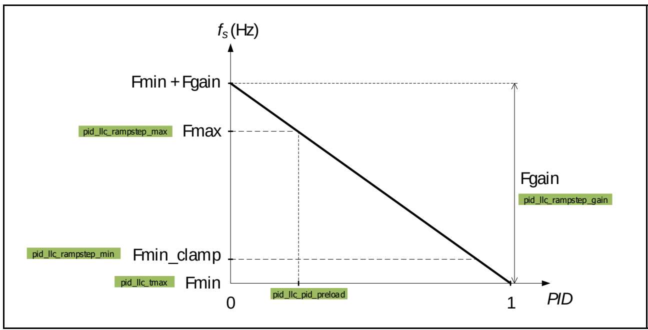


Figure 14 Topology selection and PWM mapping

3.2.3 Frequency setting

To configure the frequency setting in XDPP1148, refer to the following PID coefficient vs. frequency graph and related register settings. It includes setting the following and other register settings to ensure the proper operation of the device. These must be configured according to the specific application requirements:

- Resonant frequency (**llc_tres**)
- Minimum operating frequency (**pid_llc_rampstep_min**)
- Maximum operating frequency (**pid_llc_rampstep_max**)
- Gain frequency (**pid_llc_rampstep_gain**)



Register	Decimal value
llc_mode[1:0]	3 (LLC Close loop)
pid_llc_tmax[11:0]	570 (Fmin = 350kHz)
pid_llc_ramstep_min[10:1]	256 (Clamped Fmin=350kHz)
pid_llc_ramstep_gain[10:1]	203 (Fgain = 278kHz)
pid_llc_ramstep_max[10:1]	438 (Fmax = 600kHz)
pid_llc_pid_preload[10:1]	0.1(=Fmin+Fgain-Fmax)/Fgain)
llc_tres[11:0]	435 (Fres = 460kHz)

Figure 15 Frequency-related register configuration

3.2.4 Soft-start for LLC controller

The LLC converter soft-start process consists of two stages, with the first stage ramping up the duty cycle from a minimum value (**llc_ss_duty_start**) to a maximum value (**llc_ss_duty_max**) while switching at the initial soft-start frequency (**1/ llc_ss_tswitch_start**). The ramp-up speed can be configured by **llc_ss_duty_step** and **llc_ss_duty_steptime**, allowing for customization of the soft start process to meet specific application requirements.

Once the LLC duty cycle reaches its maximum value, the converter enters the second stage of the soft-start process, where the LLC duty cycle remains at its maximum value while the switching frequency modulates from the initial soft-start frequency to the steady-state frequency. The controller measures the output voltage and ramps it towards the target voltage at a transition rate defined by VOUT_TRANSITION_RATE (PMBus setting) as shown below:

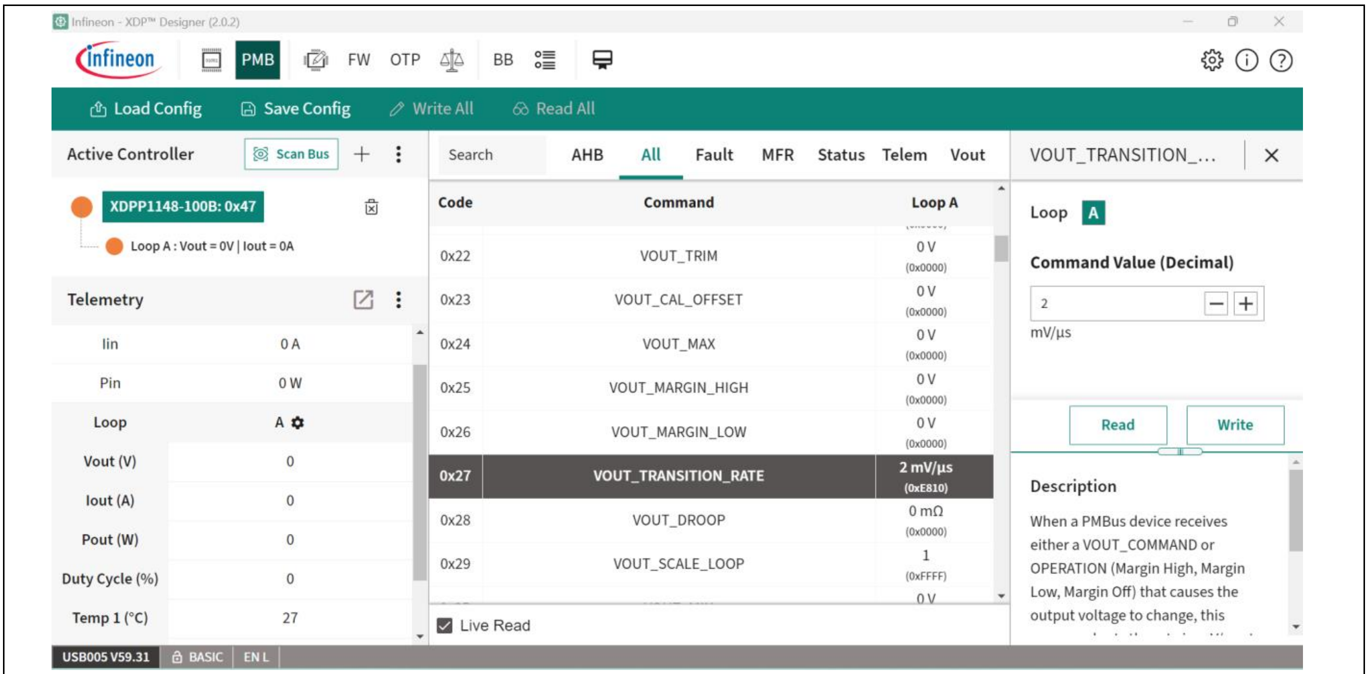
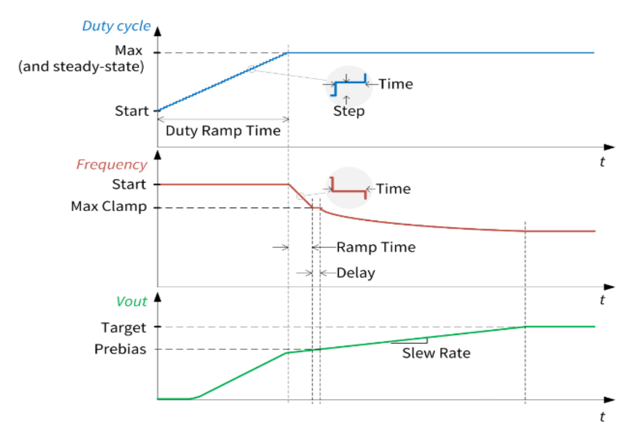


Figure 16 Configuring the soft-start of the LLC converter using Infineon XDP™ Designer



Register	Decimal Value
llc_ss_duty_start[11:0]	819 (20% duty)
llc_ss_duty_max[11:0]	4095 (99.99% duty)
llc_ss_duty_step[8:0]	5 (0.122% per step)
llc_ss_duty_steptime[15:0]	100 (2us)
vc_llc_rampstep_start[15:0]	2 (Fstart = 700kHz)
vc_llc_rampstep_time[15:0]	83 (1.66us)
llc_ss_ol_to_cl_dly[7:0]	78 (4.99us)
vc_llc_vramp_tstep[15:0]	512 (10.24us)
PMBus	
VOUT_TRANSITION_RATE	2 (2mV/us)

Figure 17 Soft-start of the LLC converter

3.2.5 Adaptive SR control

The adaptive SR timing control is achieved by sensing the SR V_{DS} voltage, which is clamped by a small-signal MOSFET (OptiMOS™ BSS123N) and sent to a comparator with a configurable threshold set by a resistor divider (R1 and R2) as shown in Figure 18.

The comparator measures the SR body diode conduction time, as shown in Figure 19, specifically the duration between the rising edge of the first body diode conduction pulse before SR PWM turns on and the falling edge of the second body diode conduction pulse after SR PWM turns off, which indicates half of the resonant period is below resonant operation. This signal is sent to the fast GPI1 input and processed by the device to adjust the maximum SR pulse width.

In Figure 18, R5 resistor can be designed as hysteresis function to the VDS threshold voltage if be needed.

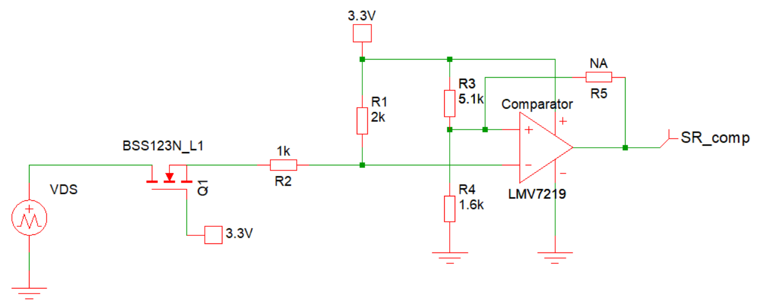


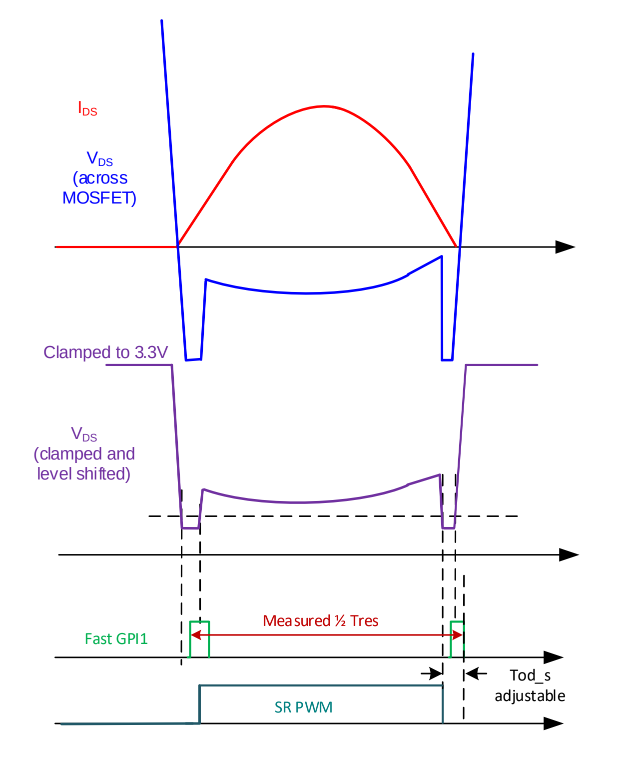
Figure 18 Topology selection and PWM mapping

The SR turn-on timing follows the primary switching turn-on sequence. The SR turn-off time is defined by the following formula.

$$t3 = 0.5 * llc_{tres} + llc\_tdtprim\_plus\_tiso - toff\_dly\_t3$$

Equation 1

Here, **llc_tres** is resonant frequency. **tdtprim_plus_tiso** and **toff_dly_t3** can be tuned for optimizing the SR turn-on timing.



Register	Decimal Value
sr_on_mode [1:0]	0 (Immediate turn on SR)
sr_timing_mode [2:0]	5 (mode2 +50ns)
sr_timing_cnt_max [7:0]	5 (No. of consecutive comparison)
sr_timing_cycle_sel [0]	0 (even half cycle)
sr_timing_ramp_sel [0]	0 (PWM ramp 0)
sr_trigger_select [0]	0 (External trigger 1)
llc_tdtprim_plus_tiso [8:0]	106 (132.5ns)
toff_dly_t3[5:0]	48 (220ns)
llc_tres_max [11:0]	483 (414kHz)
llc_tres_min [11:0]	395 (506kHz)
llc_auto_sr_tsw_range [1:0]	1 (Tswitch>max (tres au and tres)
llc_tres_mon_sel [0]	0 (Programmed Tres)
sr_meas1[7:0]	Read only register
sr_meas2[7:0]	Read only register
sr_meas3[11:0]	Read only register
sr_meas4[11:0]	Read only register
llc_tres_zone [1:0]	Read (current Tswitch)

Figure 19 VDS sensing for adaptive SR and related register setting

3.3 Measurement points

The following table lists the test points to connect the oscilloscope for observation (either through-hole pad-pair, or single-point access).

Table 3 Test point descriptions

Test point	Description
TP1	Primary-side high-side HV GaN driving ground point
TP2	Use this test point together with TP1 to observe the primary-side, high-side HV GaN Vgs signal
TP3	Primary-side half-bridge middle point/switching point
TP4	Primary-side low-side HV GaN driving ground point
TP5	Use this test point together with the primary-side low-side HV GaN gate point to observe the low-side HV GaN Vgs signal
TP6	Primary-side ground point
TP7	Primary-side input voltage test point
TP8	Secondary-side SR1 MV GaN Drain point
TP9	Secondary-side SR2 MV GaN Drain point
TP10	Secondary-side SR2 MV GaN Source point
TP11	Secondary-side SR1 MV GaN Source point
TP12	Secondary-side SR2 MV GaN Gate test point
TP13	Secondary-side SR1 MV GaN Gate test point

3.4 Sequence of power-up and power-down

3.4.1 Power up

1. Connect the I2C port near the digital controller with the GUI on the PC through the USB007A1 USB-to-I2C convertor box.
2. Power up the primary- and secondary-side external 12 V DC source.
   After that, the GUI should communicate with the digital controller. Because the DC bus of the converter is discharged at startup, to avoid the inrush current in powering up, the DC source must be programmed to ramp up its output voltage (1~5 V/ms) to the target input voltage (375 V–410 V).
3. Disconnect or turn off the DC load. Alternatively, reduce the load to be below the max load. The converter might not start up if the load exceeds the max load.
4. Set the soft-start register and output voltage values in the GUI to correct value, and then select **Output ON** at the **Operation** button in the GUI to generate the PWMs to soft-start.
   Figure 20 shows the soft startup of the converter with 400 V DC supply turn-on. Figure 21 shows the output voltage transient when a full load-step change is applied and when the load is turned off. Less than 1 V overshoot and undershoot is observed in a full load-step change.

3.4.2 Power down

To power off the converter, simply turn off the DC source. Because the DC bus has no bleeder resistor, the DC bus will remain energized if the converter is turned off in no-load condition; therefore, we suggest turning off the DC source while the load relates to less than 1 W load. This will de-energize the DC bus.

Attention: ***This evaluation hardware does not have bleeder resistors, so the DC bus might remain energized. To avoid electric shock and discharge the DC bus, always turn off the source when the DC load is applied.***

Do not touch any exposed area on the PCB even when the hardware is not operating.

If the LED (D6) is off, it does not indicate that the DC bus is discharged. The controller will be off when the secondary-side external 12 V DC voltage is powered off. Be aware that touching the hardware can cause electric shock.

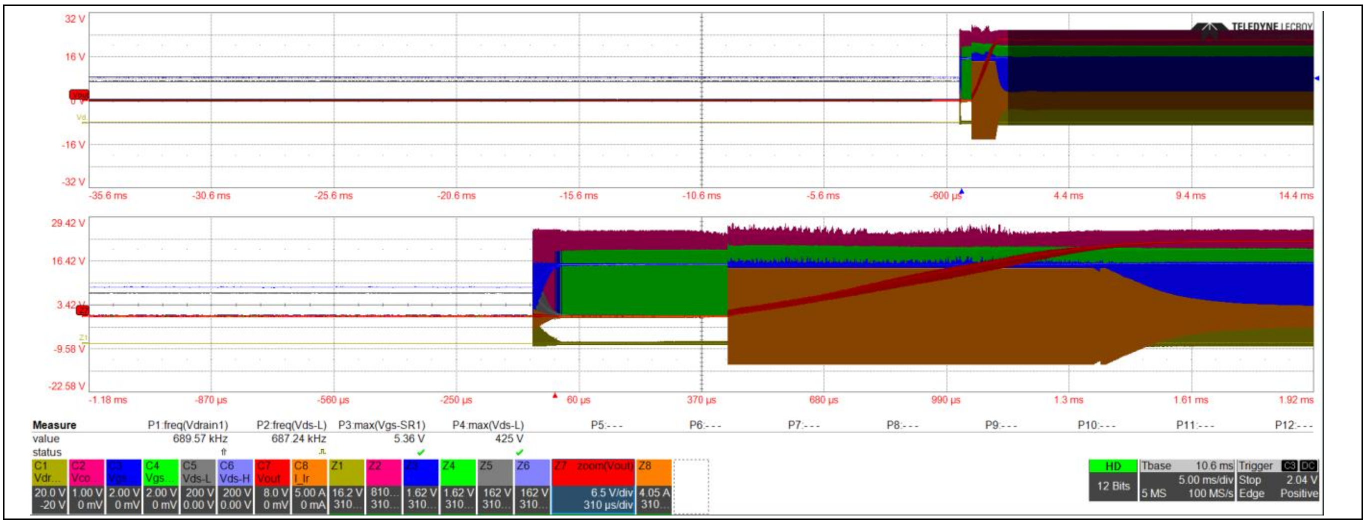


Figure 20 DC output startup transient with 400 V DC input (Ch7: DC output)

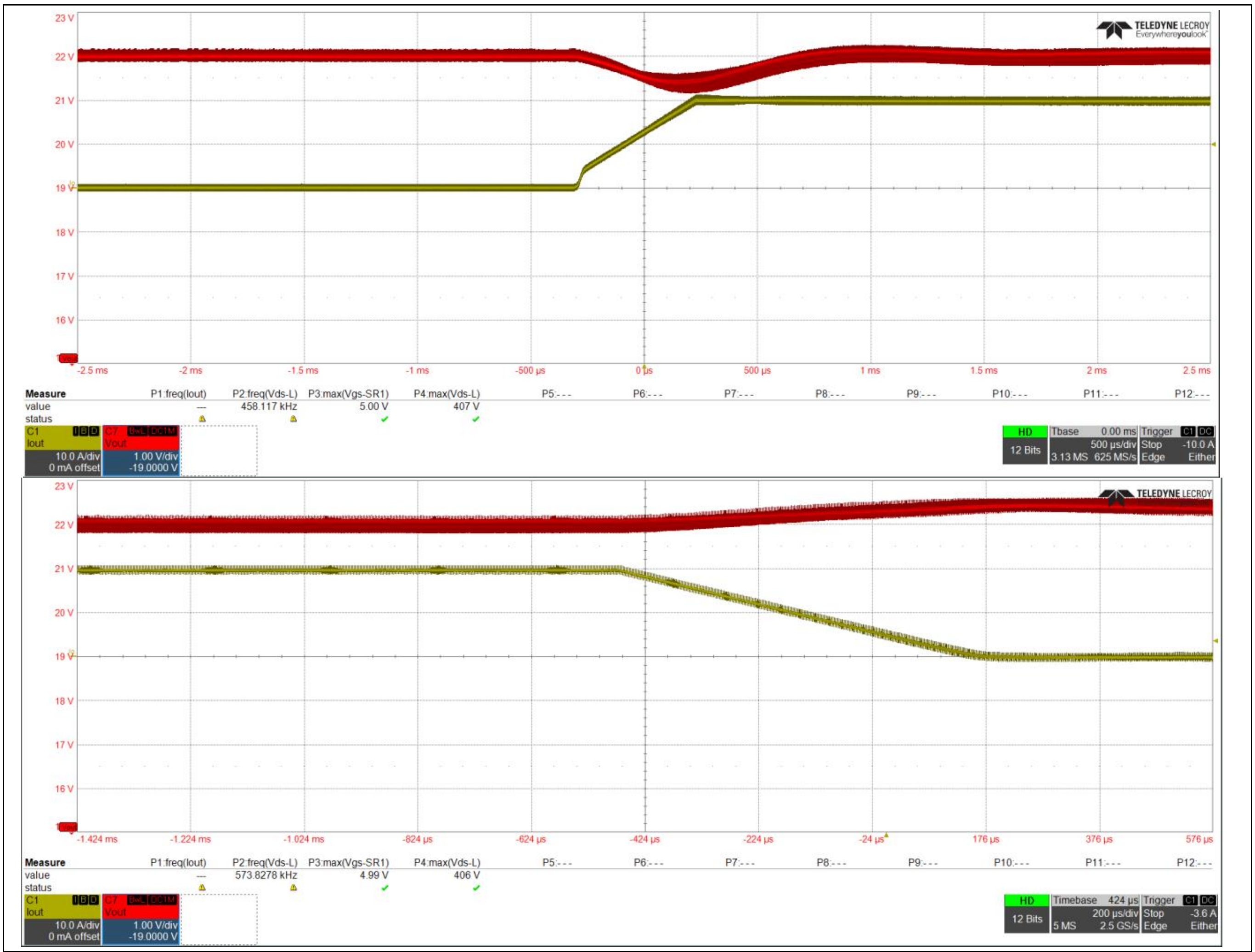


Figure 21 DC output transient with full load-step change under 400 V DC input (Ch1: DC output load current, Ch7: DC output with 19 V offset)

3.5 Full-power test

After power-up, different loads (0~20 A) can be applied. Note that the temperature of the setup will rise depending on the load. The efficiency measurement will be most accurate when the hardware has reached its steady-state thermal condition (transformer core has minimal loss at 70°C to 90°C). We suggest at least 30 minutes' running time to capture any efficiency data. The electrical signals can be observed immediately on the oscilloscope. Figure 22 shows some of the waveforms captured at full power with 400 V DC input voltage.

In this condition, the converter operates at full ZVS condition at around 485 kHz. The inductor resonant current is close to a sine wave and indicates that the LLC works above the resonant frequency. Also, the SR gate driving signal shows that before the SR turning on and after the SR turning off, there is approximately 50 ns body diode conduct time. This margin will ensure the safety of SR operation.

Note that the SR Vds voltage spike is approximately 10 V. Its peak SR Vds value reaches 55 V, which is far below the SR MV GaN max Vds voltage of 100 V.

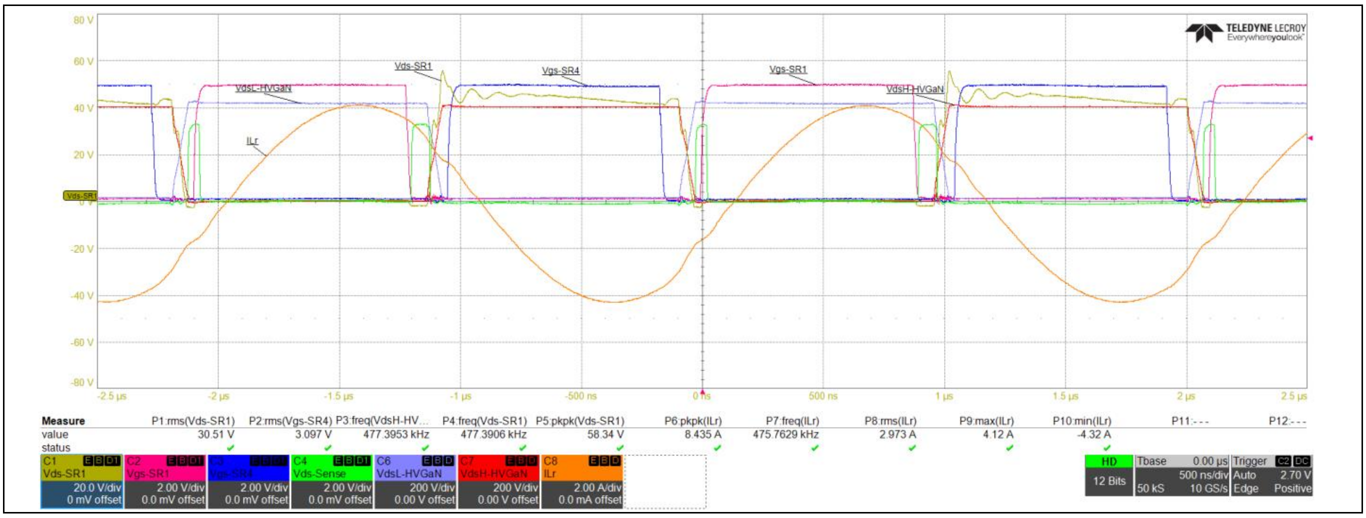


Figure 22 **Half-bridge LLC waveforms at full load and 400 V DC input (Ch1: SR1 drain-source voltage, Ch2: SR1 gate-source voltage, Ch3: SR4 gate-source voltage, Ch4: SR1 drain-source sense circuit comparator output voltage, Ch6: Primary low-side HV GaN drain-source voltage, Ch7: Primary high-side HV GaN drain-source voltage, Ch8: Primary resonant inductor current)**

Figure 23 shows the waveforms with 375 V DC input. Note that increasing the input voltage increases the frequency. Figure 24 shows the waveforms with 400 V DC input and different load conditions.

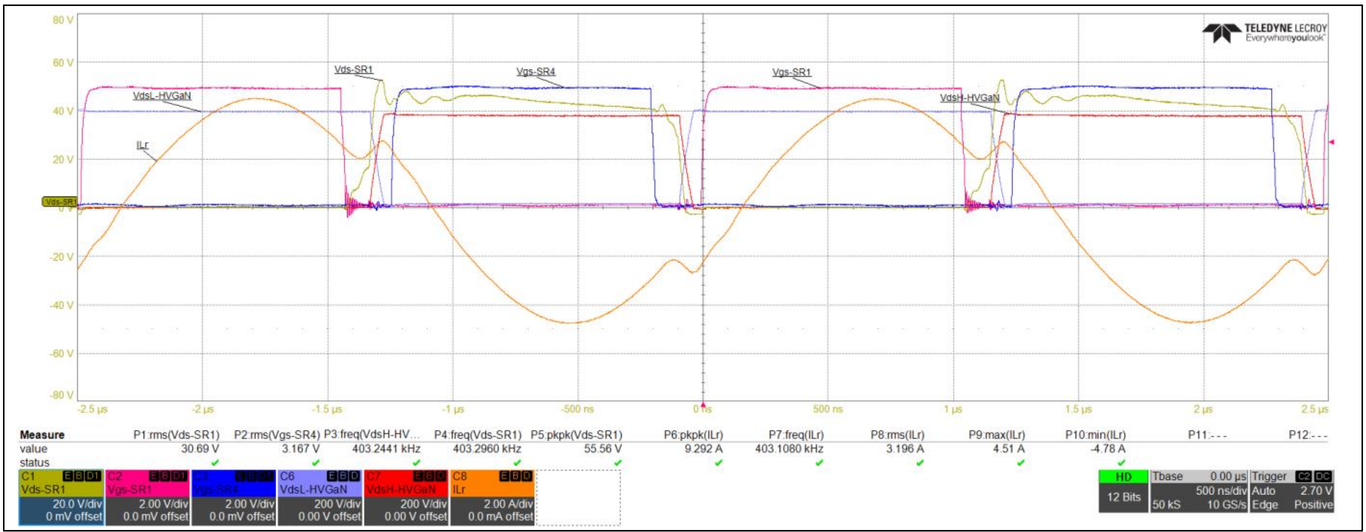
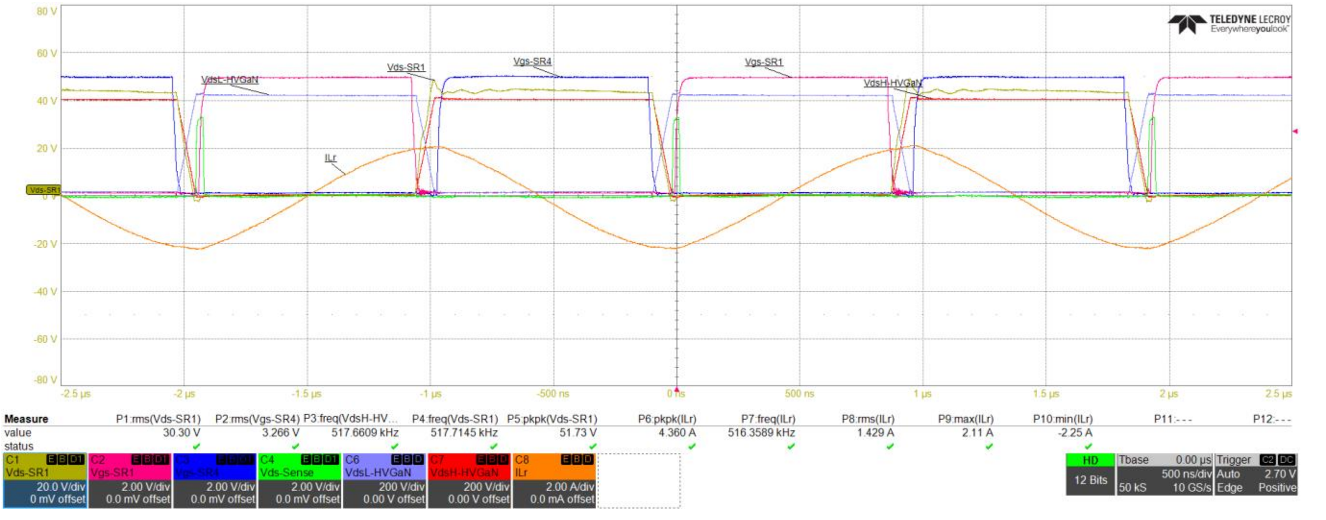
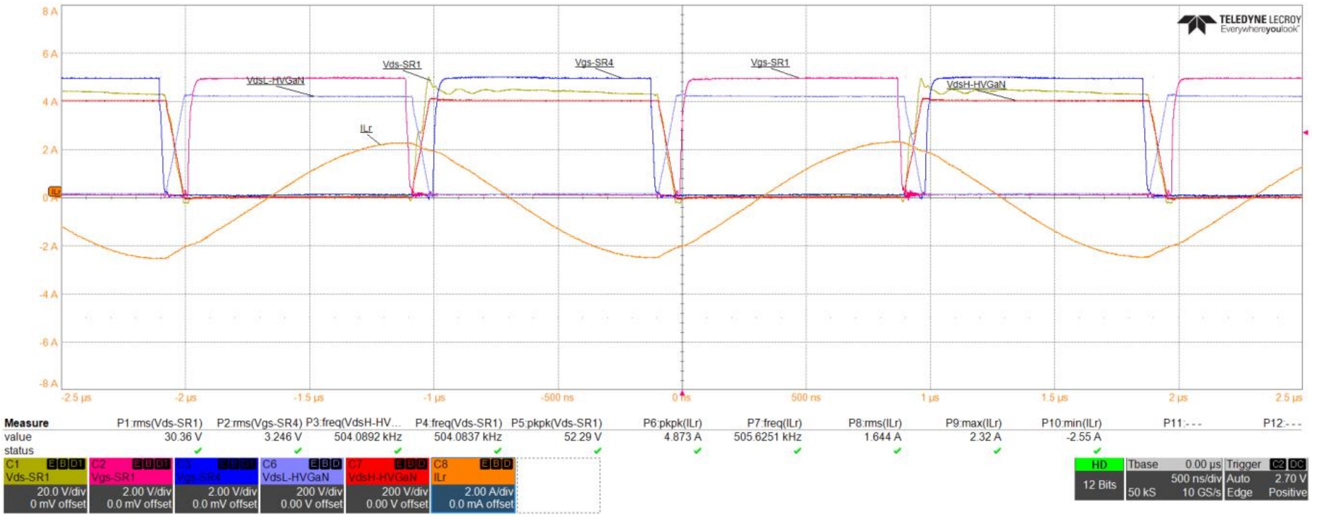


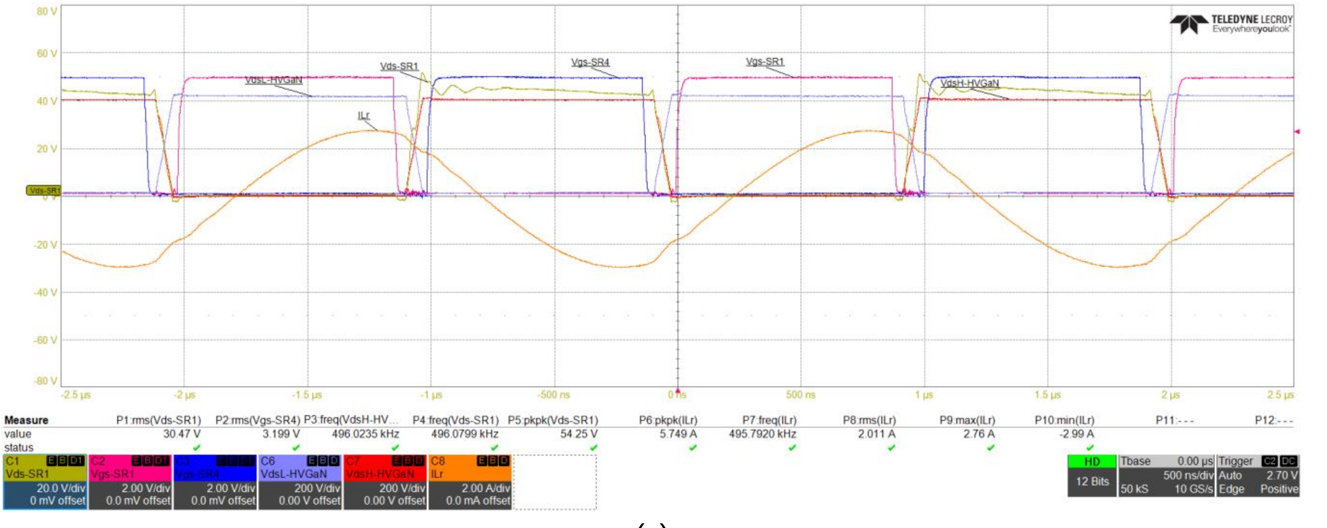
Figure 23 **Half-bridge LLC waveforms at full load with 375V DC (Ch1: SR1 drain-source voltage, Ch2: SR1 gate-source voltage, Ch3: SR4 gate-source voltage, Ch4: SR1 drain-source sense circuit comparator output voltage, Ch6: Primary low-side HV GaN drain-source voltage, Ch7: Primary high-side HV GaN drain-source voltage, Ch8: Primary resonant inductor current)**



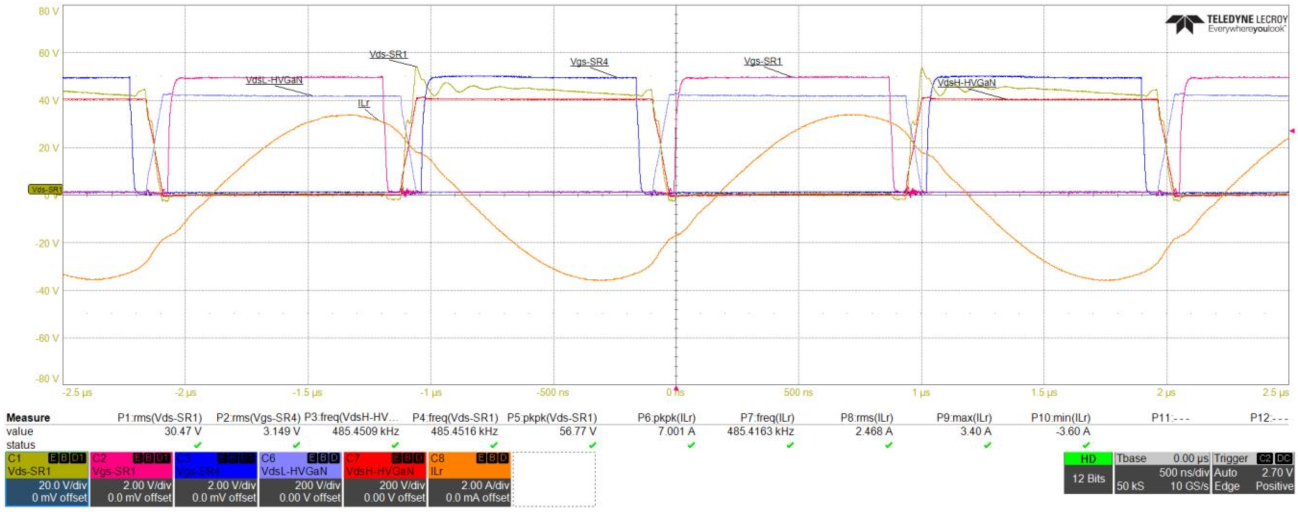
(a)



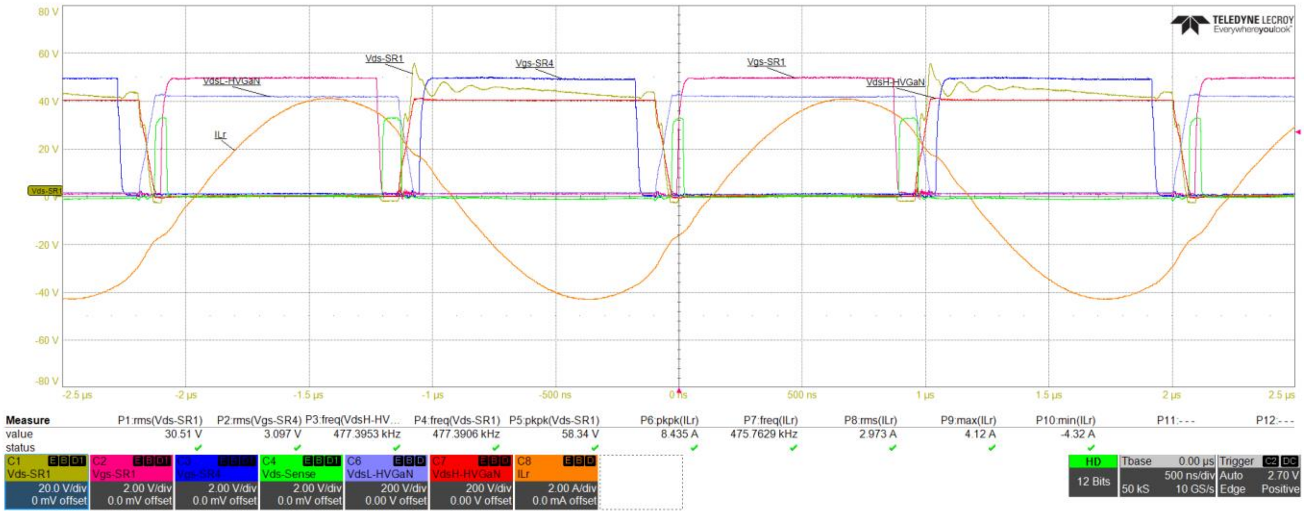
(b)



(c)



(d)



(e)

Figure 24 **Half-bridge LLC waveforms operating under 400V DC input and different load conditions: (a) no load, (b) 25% load, (c) 50% load, (d) 75% load and (e) 100% load (Ch1: SR1 drain-source voltage, Ch2: SR1 gate-source voltage , Ch3: SR4 gate-source voltage, Ch4: SR1 drain-source sense circuit comparator output voltage, Ch6: Primary low-side HV GaN drain-source voltage, Ch7: Primary high-side HV GaN drain-source voltage, Ch8: Primary resonant inductor current)**

3.6 Efficiency performance

Efficiency of the evaluation board is measured with various load and input voltage conditions:

- Table 4: Measurement results with 400 V DC input voltage
- Table 5: Measurement results with 390 V DC input voltage
- Table 6: Measurement results with 375 V DC input voltage

Figure 25 shows the efficiency curves. The measurements show that this evaluation board has a peak efficiency of close to 96% when the input voltage is 400 V.

Table 4 **Efficiency performance with 400 V DC supply**

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (%)	Efficiency (%)	Four-point average efficiency	Full load switching frequency
399.93	1.1481	21.922	20.03	100	95.63		485 kHz
399.96	0.8615	21.93	15.024	75	95.62		–
400.16	0.5777	21.93	10.01	50	94.98		–
400.17	0.2982	21.948	5.005	25	92.05		–

Table 5 Efficiency performance with 390 V DC supply

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (%)	Efficiency (%)	Four-point average efficiency	Full load switching frequency
390.05	1.1812	21.917	20.015	100	95.21		446 kHz
390.01	0.8924	21.935	15.112	75	95.24		–
390.04	0.5961	21.933	10.007	50	94.4		–
390.09	0.3097	21.947	5.001	25	90.85		–

Table 6 Efficiency performance with 375 V DC supply

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (%)	Efficiency (%)	Four-point average efficiency	Full load switching frequency
375.7	1.2587	21.928	20.03	100	92.88		403 kHz
375.64	0.948	21.933	15.028	75	92.56		–
375.5	0.6455	21.939	10.111	50	91.52		–
375.37	0.3352	21.943	5.006	25	87.3		–

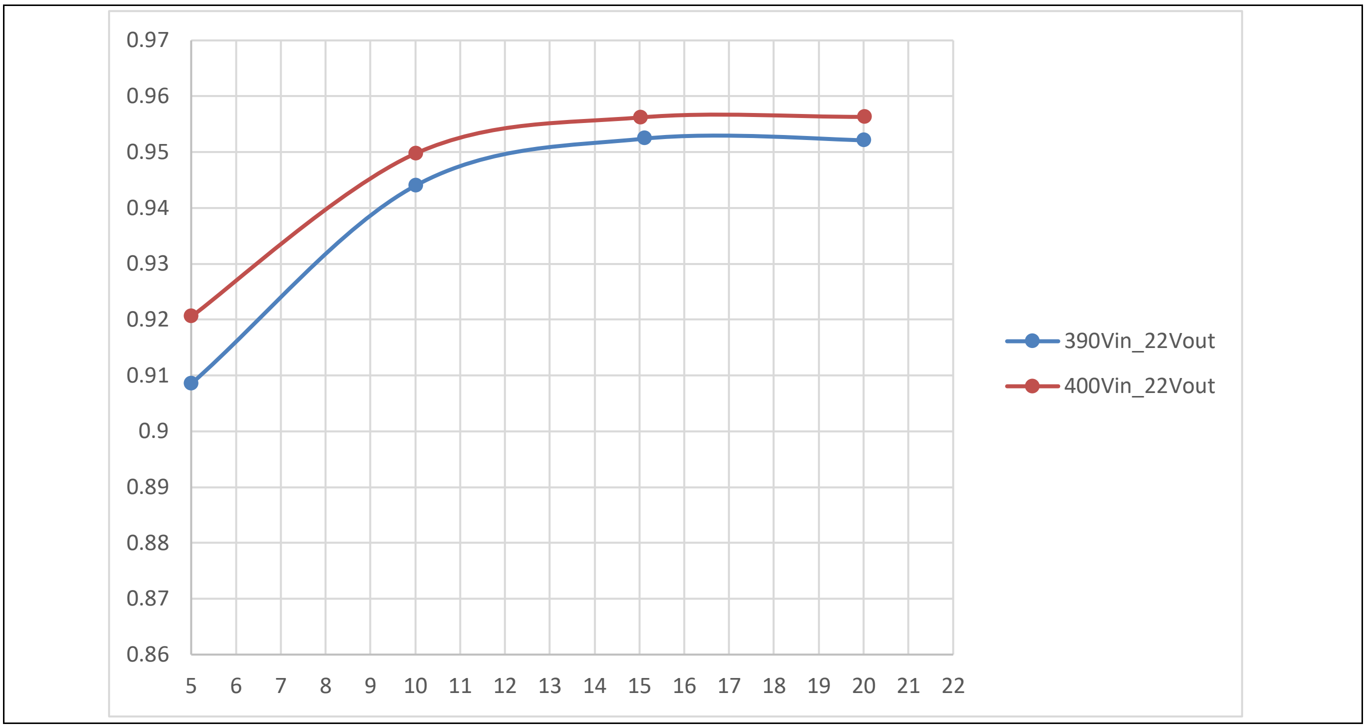


Figure 25 Half-bridge LLC board efficiency curve under different input voltage and load conditions

3.7 Thermal performance

Thermal images of this evaluation board are captured while operating at full load and different input DC voltages:

- Figure 26: Thermal image of the unit under test with 400 V DC input and operating at full power
- Figure 27: Thermal image with 390 V DC input voltage
- Figure 28: Thermal image with 375 V DC input voltage

In high-line condition (400 V DC), due to the higher switching frequency and high input voltage, the primary-side current and the inductor magnetic flux density are lower compared to the other two input voltage. Thus, the thermal temperature of the primary-side winding and inductor magnetic cores is lower than for the other two input voltages.

These thermal images show that the transformer magnetic core temperature runs at a relatively high level.

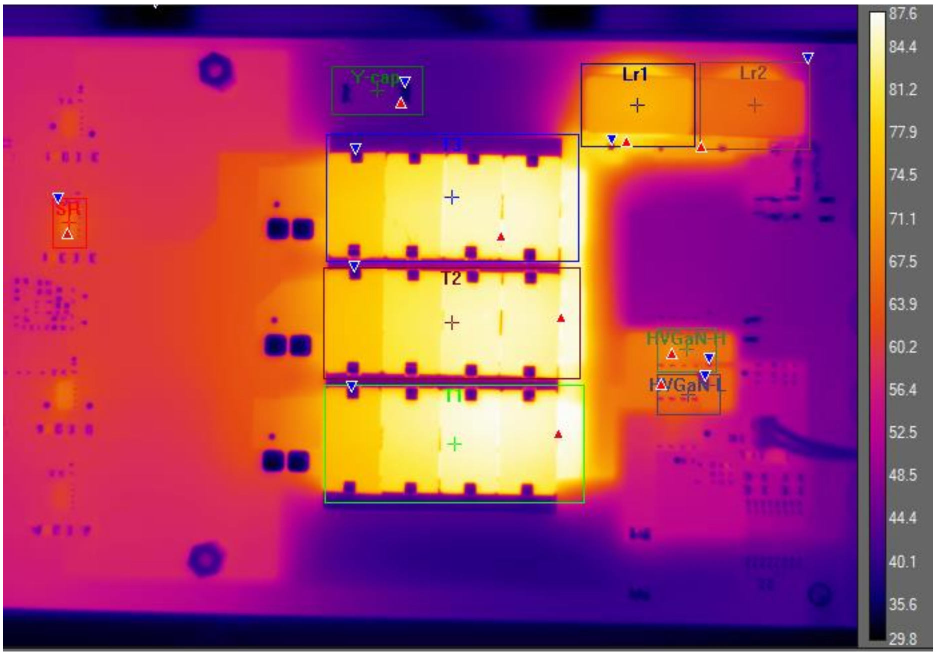


Figure 26 Thermal image of the half-bridge LLC board at full power with 400 V DC input voltage

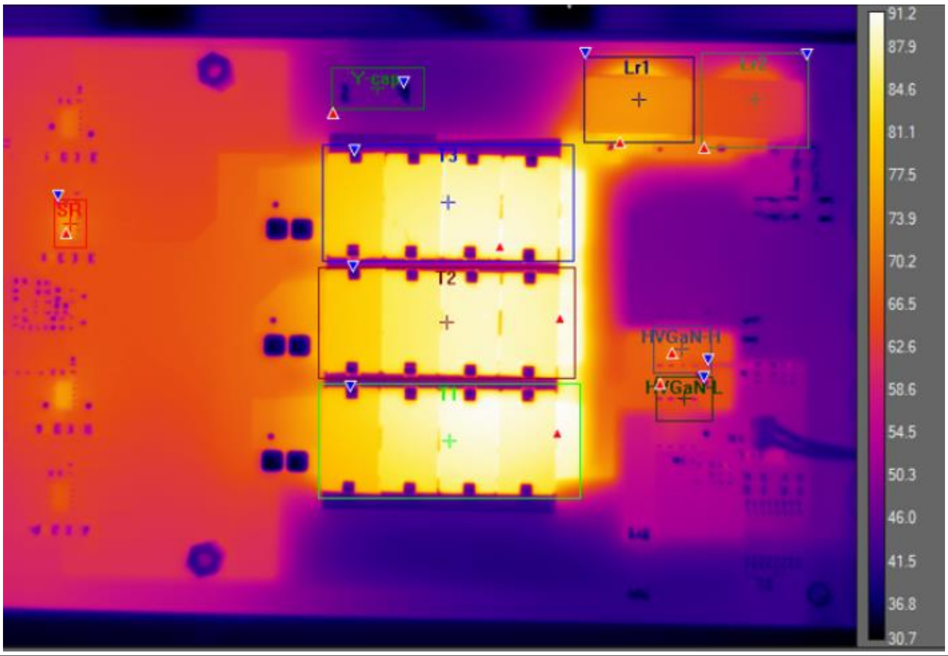


Figure 27 Thermal image of the half-bridge LLC board at full power with 390 V DC input voltage

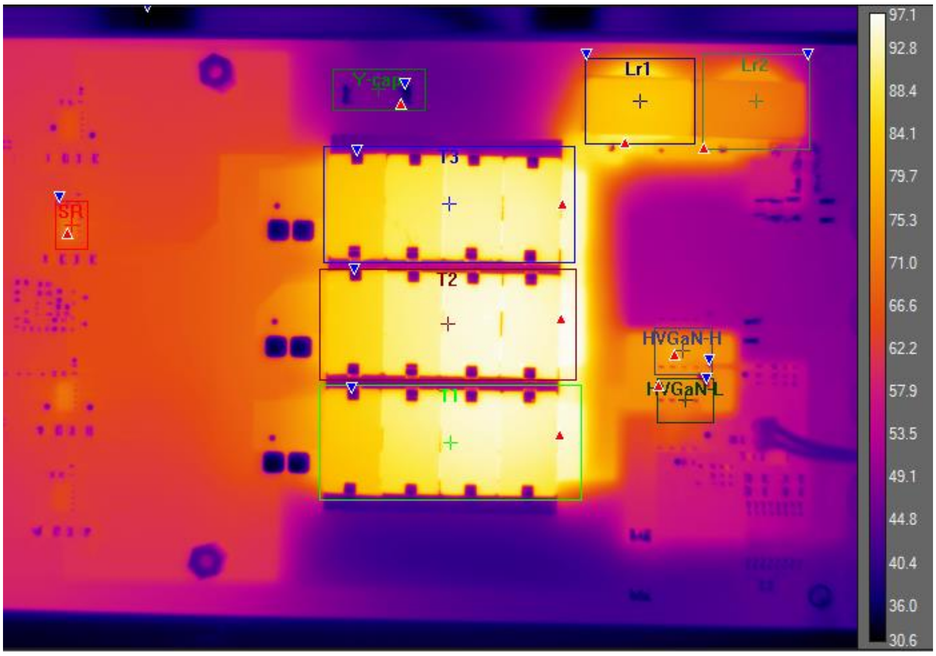


Figure 28 Thermal image of the half-bridge LLC board at full power with 375 V DC input voltage

To reduce the temperature of the transformer magnetic core, one set of heat spreader can be placed at the bottom of the transformer core with TIM between the core and the heat spreader, as showed in Figure 29. Figure 30, Figure 31, and Figure 32 show he thermal pictures of adding one piece of 2 mm heat spreader under the transformer core with 0.5 mm and 15 W/(m·K) TIM in between. It can be seen that the transformer magnetic core runs at a safe temperature after adding the heat spreader.

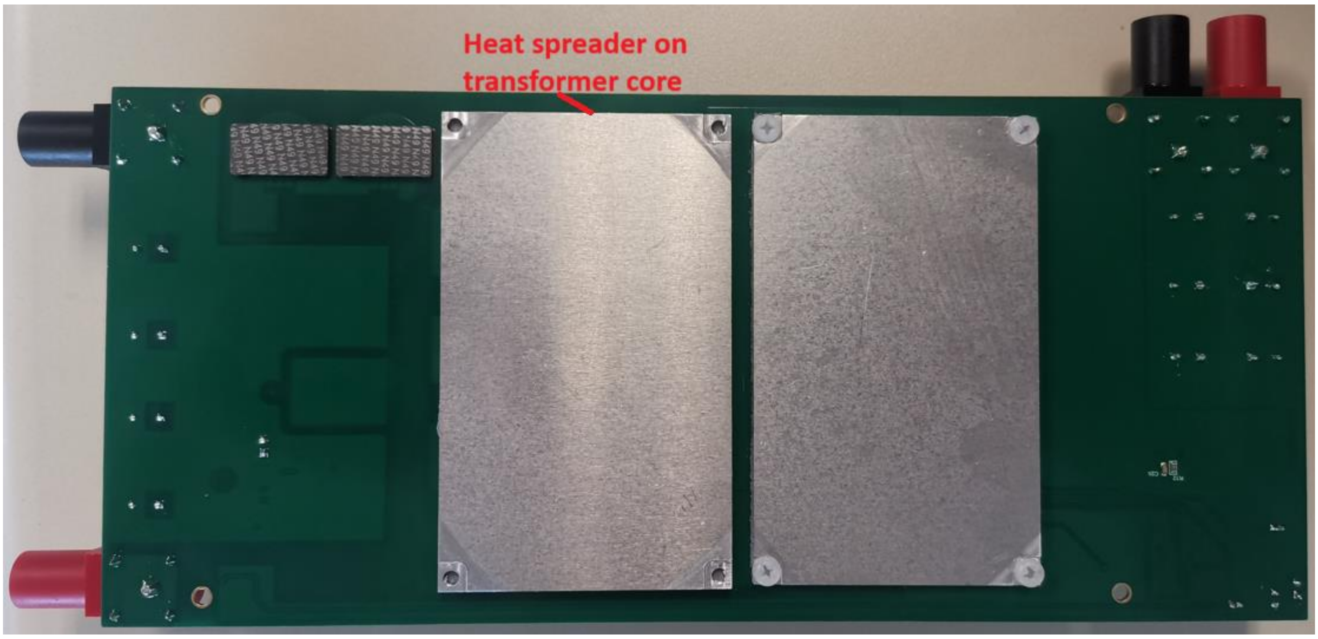


Figure 29 Heat spreader on transformer core on the bottom side of the board

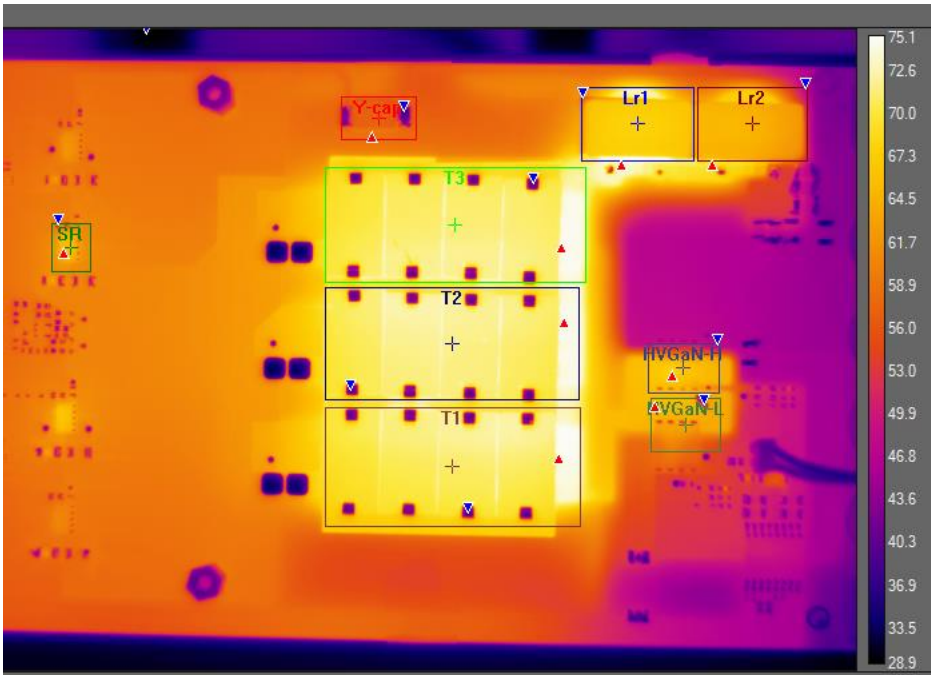


Figure 30 Thermal image of the half-bridge LLC board at full power with 400 V DC input voltage and heat spreader at transformer core bottom

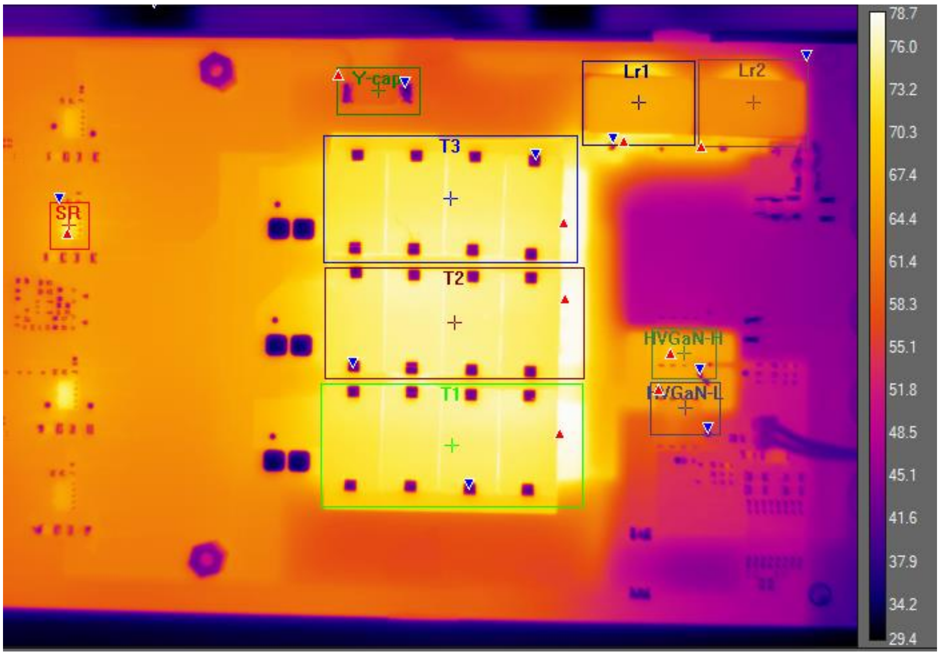


Figure 31 Thermal image of the half-bridge LLC board at full power with 390 V DC input voltage and heat spreader at transformer core bottom

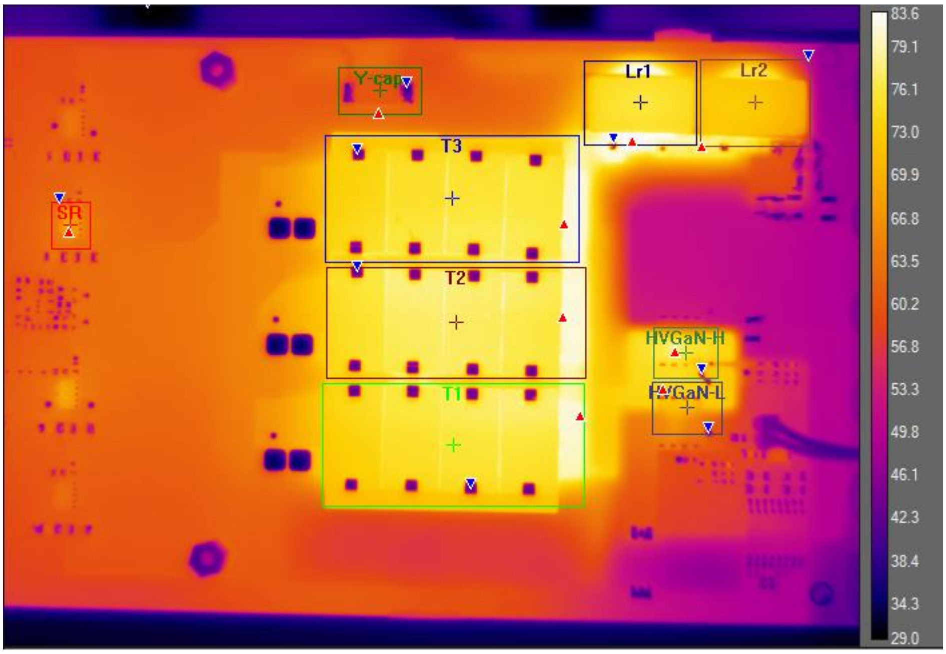


Figure 32 Thermal image of the half-bridge LLC board at full power with 375 V DC input voltage and heat spreader at transformer core bottom

4 PCB layout

The evaluation board is 1.44 mm thick, with four layers – 87.5 µm thick copper on the outer layers, and 70 µm on the middle layers. The layers are shown from Figure 33 to Figure 36.

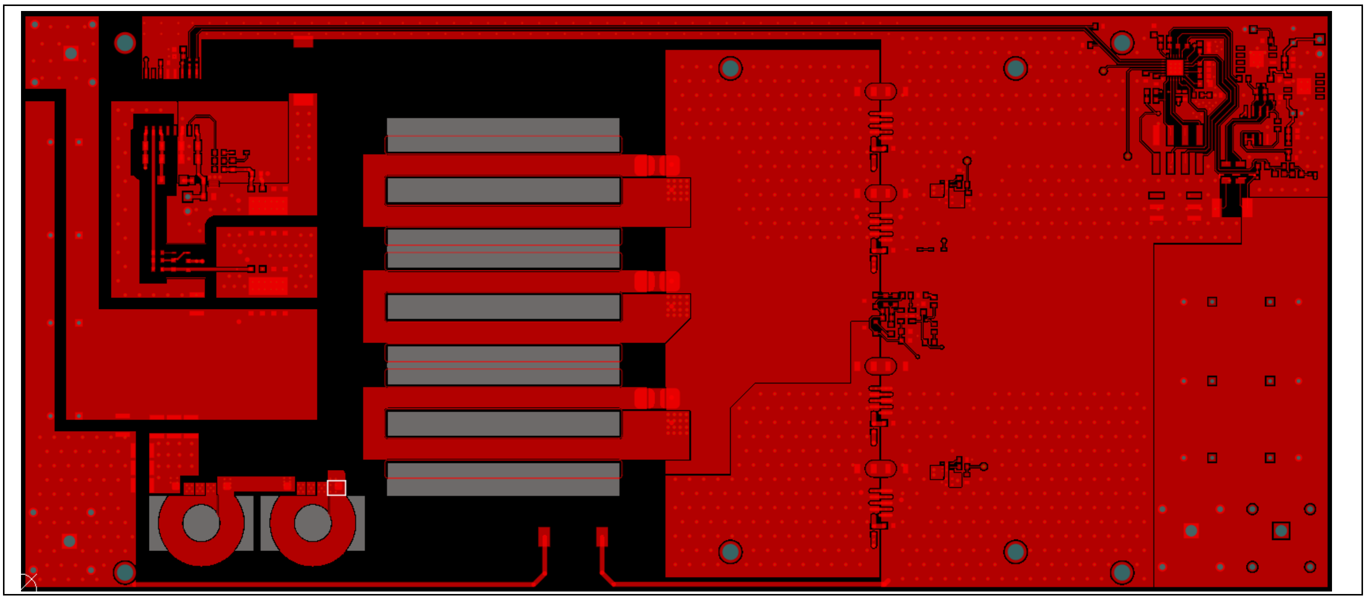


Figure 33 Top copper layer

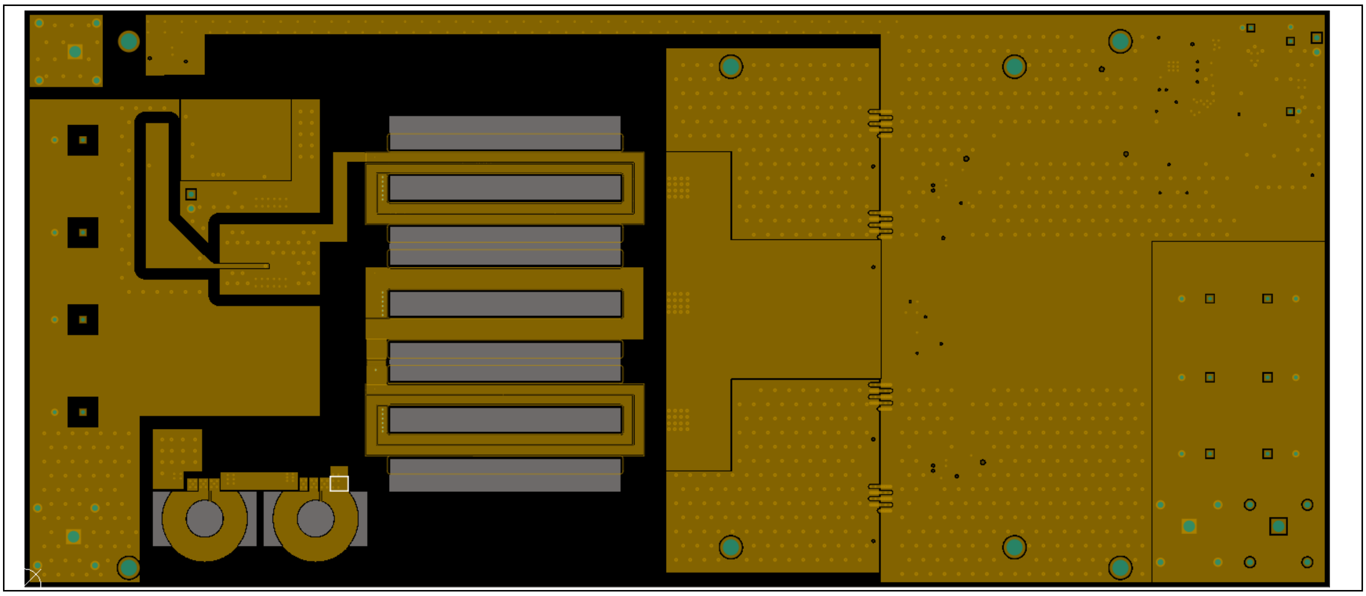


Figure 34 Upper middle copper layer

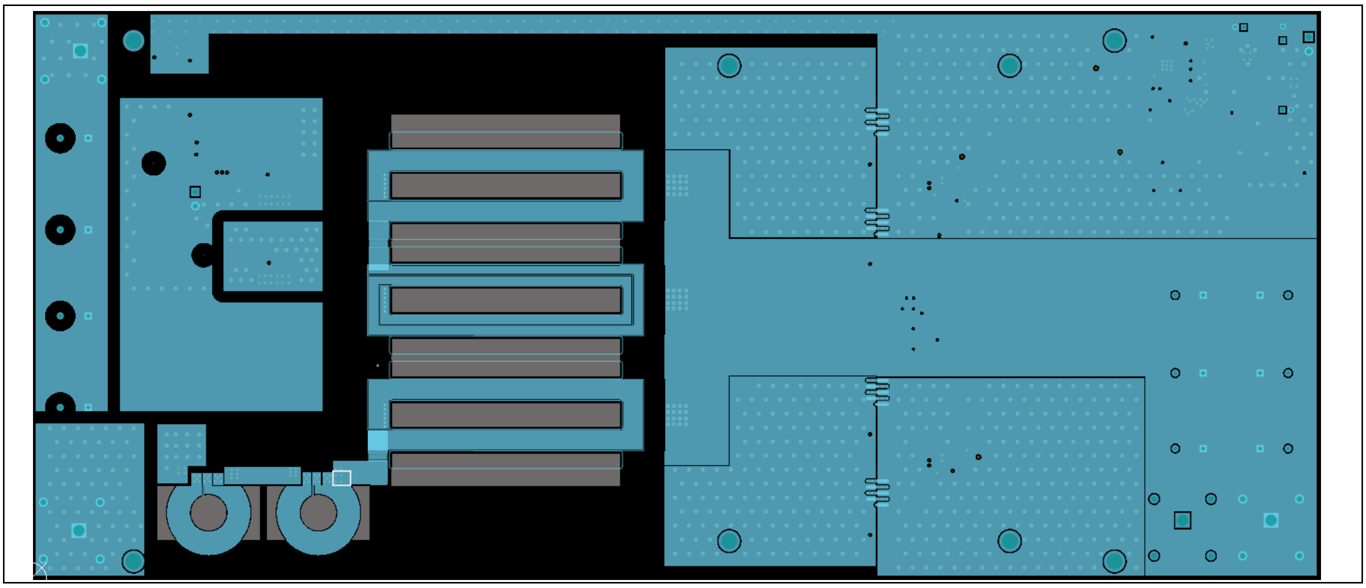


Figure 35 Lower middle copper layer

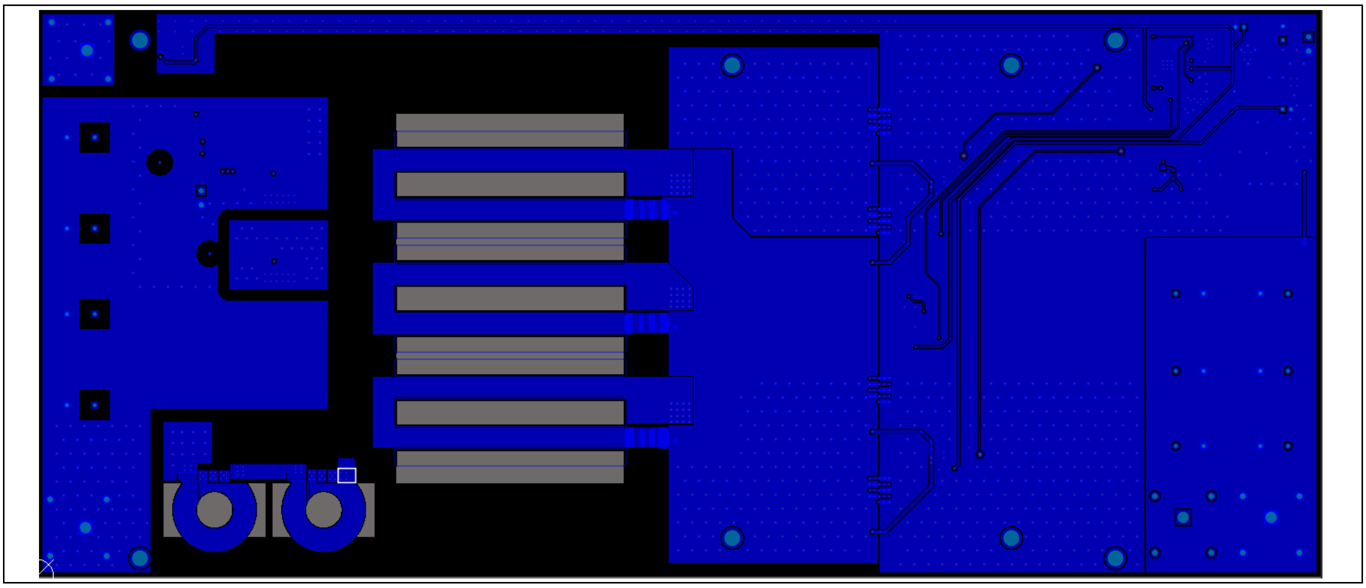


Figure 36 Bottom copper layer

5 Bill of materials

Table 7 PCB BOM

Designator	Description	Vendor	Quantity
C10, C11, C16, C18	Ceramic COG capacitor 4.7nF 630V	TDK	4
Heatsink_Secondary	Extruded 90mm L X 55mm W X 6mm H 1 fiin 2mm 2.2mm pitch		1
R7, R8, R66, R67	RES / STD / 0R / 63mW / 0R / 0ppm/K / -55°C to 155°C / 0402(1005) / SMD / -	Yageo	4
U3_Driver1, U3_Driver2	Single-channel TDI gate driver	Infineon	2
R11	RES / STD / 1k / 100mW / 0.1% / 25ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Yageo	1
R46	RES / - / 1k / 100mW / 1% / 100ppm/K / - / 0603(1608) / SMD / -	Panasonic	1
RSENSE1	RES / - / 1mR / 2W / 1% / 100ppm/K / - / 2512(6332) / SMD / -	Yageo	1
D3, D4	Small Signal Diode, 1V	ON Semiconductor	2
C35, C39	CAP / CERA / 1nF / 10V / 2% / C0G (EIA) / NP0 / -55°C to 125°C / 0603(1608) / SMD / -	Kemet	2
C4	CAP / CERA / 1nF / 50V / 5% / - / -55°C to 125°C / 0603(1608) / SMD / -	Wurth Elektronik	1
C13	CAP / CERA / 100nF / 25V / 10% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	Murata	1
R26_SR1_Switch, R26_SR2_Switch, R26_SR3_Switch, R26_SR4_Switch	RES / STD / 1R / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	4
C28_Driver1, C28_Driver2	CAP / CERA / 1uF / 10V / 10% / X7S (EIA) / -55°C to 125°C / 0402(1005) / SMD / -	Murata	2
C43	CAP / CERA / 1uF / 6.3V / 10% / X5R (EIA) / -55°C to 85°C / 0603(1608) / SMD / -	Murata	1
C44	CAP / CERA / 1uF / 10V / 10% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	Murata	1
C1	CAP / CERA / 1uF / 16V / 5% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	Kemet	1
C38	CAP / CERA / 2.2uF / 25V / 10% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	Murata	1
C22, C24	CAP / CERA / 1.5uF / 16V / 10% / X7R (EIA) / -55°C to 125°C / 1206(3216) / SMD / -	Murata	2
R48	RES / STD / 1.6k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	1
T1, T2, T3	ELP 18/4/10 Planar Transformer core small pad	TDK	3

Designator	Description	Vendor	Quantity
U2	2EDS8265H,Fast, Robust, Dual-Channel, Functional and Reinforced Isolated MOSFET Gate-Driver with Accurate and Stable Timing	Infineon Technologies	1
R14, R19, R44	RES / STD / 2k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay, Yageo	3
C32	CAP / CERA / 2.2uF / 6.3V / 10% / X5R (EIA) / -55°C to 85°C / 0603(1608) / SMD / -	Murata	1
C25_PrimaryQA, C25_PrimaryQB	CAP / CERA / 3nF / 25V / 5% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	Murata	2
R51	RES / STD / 3.01k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	1
R15	RES / STD / 3.9k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	1
C3	CAP / CERA / 4.7uF / 10V / 10% / X5R (EIA) / -55°C to 85°C / 0603(1608) / SMD / -	Murata	1
C12	CAP / CERA / 4.7uF / 25V / 10% / X5R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	Murata	1
R21	RES / STD / 5k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	1
R41	RES / STD / 5.1k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	1
R42	RES / STD / 1.6k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	1
R20, R62	RES / STD / 10k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0402(1005) / SMD / -	Panasonic	2
R13	RES / STD / 10k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	1
R22_PrimaryQA, R22_PrimaryQB, R27_SR1_Switch, R27_SR2_Switch, R27_SR3_Switch, R27_SR4_Switch, R49, R50, R52, R53, R54, R55, R56, R57, R58	RES / STD / 10k / 100mW / 0.1% / 50ppm/K / -55°C to 125°C / 0603(1608) / SMD / -	Vishay	15
R17, R23_PrimaryQA, R23_PrimaryQB, R24_PrimaryQA, R24_PrimaryQB	RES / STD / 10R / 100mW / 1% / 200ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Yageo	5
C41	CAP / CERA / 10uF / 10V / 10% / X5R (EIA) / -55°C to 85°C / 0603(1608) / SMD / -	Murata	1
C5	CAP / CERA / 10uF / 16V / 10% / X5R (EIA) / -55°C to 85°C / 0805(2012) / SMD / -	Murata	1

Designator	Description	Vendor	Quantity
C25	CAP / CERA / 10nF / 50V / 5% / - / -55°C to 125°C / 0603(1608) / SMD / -	Yageo	1
R10	RES / STD / 13k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Yageo	1
C33	CAP / CERA / 15pF / 10V / 5% / C0G (EIA) / NP0 / -55°C to 125°C / 0603(1608) / SMD / -	Wurth Elektronik	1
R4	RES / STD / 33R / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Vishay	1
R28_SR1_Switch, R28_SR2_Switch, R28_SR3_Switch, R28_SR4_Switch	RES / STD / 33R / 250mW / 0.1% / 25ppm/K / -55°C to 155°C / 1206(3216) / SMD / -	KOA Speer Electronics Inc.	4
R29_Driver1, R29_Driver2, R30_Driver1, R30_Driver2	RES / STD / 47k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603 (1608) / SMD / -	Vishay	4
CIN7, CIN8, CIN9, CIN10	CAP / ELCO / 47uF / 450V / 20% / Aluminium electrolytic / -40°C to 105°C / 5.00mm C X 0.60mm W 12.50mm Dia X 27.00mm H / THT / -	Rubycon	4
C27_Driver1, C27_Driver2	CAP / CERA / 100nF / 10V / 20% / X7S (EIA) / -55°C to 125°C / 0402(1005) / SMD / -	Taiyo Yuden	2
C18, C31, C40	CAP / CERA / 100nF / 10V / 5% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	Kemet	3
C34, C36, C37	CAP / CERA / 100nF / 6.3V / 10% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	Murata	3
C19, C20	CAP / CERA / 100pF / 10V / 1% / C0G (EIA) / NP0 / -55°C to 125°C / 0603(1608) / SMD / -	Kemet	2
R16, R18	RES / STD / 100R / 250mW / 1% / 100ppm/K / -55°C to 155°C / 1206(3216) / SMD / -	Vishay	2
C21, C23	CAP / CERA / 220nF / 25V / 5% / X7R (EIA) / -55°C to 125°C / 1206(3216) / SMD / -	Murata	2
C26_SR1_Switch, C26_SR2_Switch, C26_SR3_Switch, C26_SR4_Switch	CAP / CERA / 220pF / 100V / 5% / C0G (EIA) / NP0 / -55°C to 125°C / 1206(3216) / SMD / -	Murata	4
R43,R47	RES / STD / 0R / 100mW / 1% / 200ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	2
R25_PrimaryQA, R25_PrimaryQB	RES / STD / 470R / 100mW / 5% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Yageo	2
COUT1, COUT2, COUT3, COUT4, COUT5, COUT6	CAP / ELCO / 680uF / 35V / 20% / Aluminiumelectrolytic / -55°C to 105°C / 5.00mm C X 0.60mm W 12.75mm Dia X 22.00mm H / THT / -	Epcos	6
D5_PrimaryQA, D5_PrimaryQB	BAT54WS-7-F,Schottky Diodes & Rectifiers 30V 200mW	Diodes Incorporated	2
Q2, Q3	BSS123N,OptiMOS Small-Signal-Transistor VDS 100V	Infineon Technologies	2
C45, C46, C49	Polarized Capacitor (Radial)		3

Designator	Description	Vendor	Quantity
C15	Multilayer Ceramic Capacitors MLCC - SMD/SMT 100pF 300V 10% 11.4x6x2.5mm SMD		1
D2	ES1J-13-F,DIODE ES1JL 600V 1A Sub SMA	Diodes Incomrporated	1
X3, X7	Banana Test Connector, 4mm, Socket, PCB Mount, 24 A, 1 kV, Gold Plated Contacts, Black	Cliff ELectronics Component Limited	2
X5, X6	Banana Test Connector, 4mm, Socket, PCB Mount, 24 A, 1 kV, Gold Plated Contacts, Red	Cliff ELectronics Component Limited	2
D6	LEDM2214X140N, LED GREEN CLEAR SMD	OSRAM Opto Semiconductors	1
X8	SMT .025 SQ Post Header, 2.54mm pitch, 8 pins, vertical, double row	Samtec	1
X1, X2	Through hole .025 SQ Post Header, 2.54mm pitch, 2 pin, vertical, single row	Samtec	2
X4	Through hole .025 SQ Post Header, 2.54mm pitch, 2 pin, vertical, single row	Samtec	1
Q1_PrimaryQA, Q1_PrimaryQB	IGLD65R110D2, 650V CoolGaN™ enhancement-mode Power Transistor, Temp Range(-55°C to 150°C)	Infineon Technologies	2
L1, L2	Planar Inductor		4
QSR1_SR1_Switch, QSR1_SR2_Switch, QSR1_SR3_Switch, QSR1_SR4_Switch	IGC033S101, CoolGaN™ Power-Transistor, VDS 100V	Infineon Technologies	4
U4	LMV7219M5X-5-Pin-SOT23	TI	1
C48	CAP / CERA / 1nF / 25V / 10% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	Murata	1
R45, R59, R60, R61,R12	RES / - / 1k / 100mW / 1% / 100ppm/K / - / 0603(1608) / SMD / -	Panasonic	5
R9	RES / STD / 10k / 100mW / 0.1% / 15ppm/K / -55°C to 125°C / 0603(1608) / SMD / -	Vishay	1
U1	OPAx140 High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz, JFET Op Amp	TI	1
U6	TLF80511EJ V33 ,Low Dropout Linear Fixed Voltage Regulator, 3.3V, 400mA	Infineon Technologies	1
LR1	TLF80511EJ V50 , Low Dropout Linear Fixed Voltage Regulator, 3.3V, 400mA	Infineon Technologies	1
U5	Digital controller XDPP1148-100B	Infineon Technologies	1
SW1	TK-6580K8-1, Button switch	Yuandi Electronics Co,Ltd	1

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Revision history

Document version	Date of release	Description of changes
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