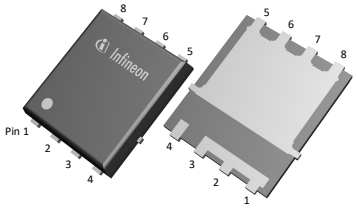
MOSFET

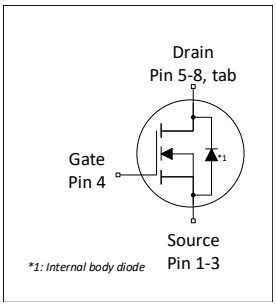
PG-TDSON-8

OptiMOS™ 5 Linear FET 2, 100 V



Features

- Ideal for hot-swap, battery protection and e-fuse applications
- Very low on-resistance $R_{DS(on)}$
- Wide safe operating area SOA
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	3.5	mΩ
I_D	164	A
$I(V_{DS}=50\ V, t_p=10\ ms)$	7.4	A

Type / Ordering code	Package	Marking	Related links
ISC035N10NM5LF2	PG-TDSON-8	35N10LF2	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	164 116 19	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	656	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	398	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	217 3	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagrams 3 and 4 for more detailed information

[4] See Diagram 14 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.7	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5]	R_{thJA}	-	-	50	°C/W	-

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.3	3.1	3.9	V	V_{DS}=V_{GS}, I_D=115 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	3.0	3.5	mΩ	V_{GS}=10 V, I_D=50 A
Gate resistance	R_G	-	1.5	2.3	Ω	-
Transconductance [6]	g_{fs}	26	52	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	5500	7200	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [7]	C_{oss}	-	780	1000	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance [7]	C_{rss}	-	19	33	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	11	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	10	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	35	-	nC	V_{DD}=50 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	17	-	nC	V_{DD}=50 V, I_D=50 A, V_{GS}=0 to 10 V
Gate to drain charge [9)]	Q_{gd}	-	12	18	nC	V_{DD}=50 V, I_D=50 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	30	-	nC	V_{DD}=50 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total [9)]	Q_g	-	70	88	nC	V_{DD}=50 V, I_D=50 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	6.4	-	V	V_{DD}=50 V, I_D=50 A, V_{GS}=0 to 10 V
Output charge [9)]	Q_{oss}	-	90	115	nC	V_{DS}=50 V, V_{GS}=0 V

8) See "Gate charge waveforms" for parameter definition

9) Defined by design. Not subject to production test.

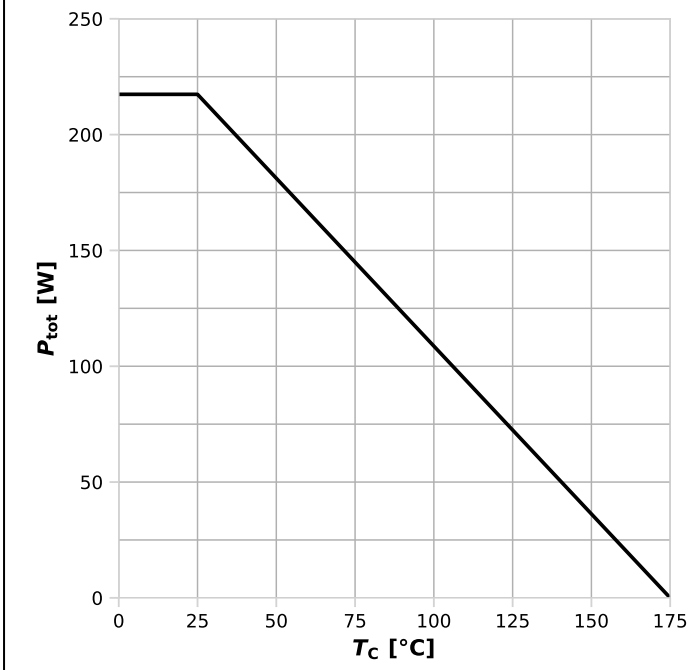
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	159	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	656	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.84	1.2	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [10)]	t_{rr}	-	49	98	ns	V_R=50 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [10)]	Q_{rr}	-	72	144	nC	V_R=50 V, I_F=50 A, di_F/dt=100 A/µs

10) Defined by design. Not subject to production test.

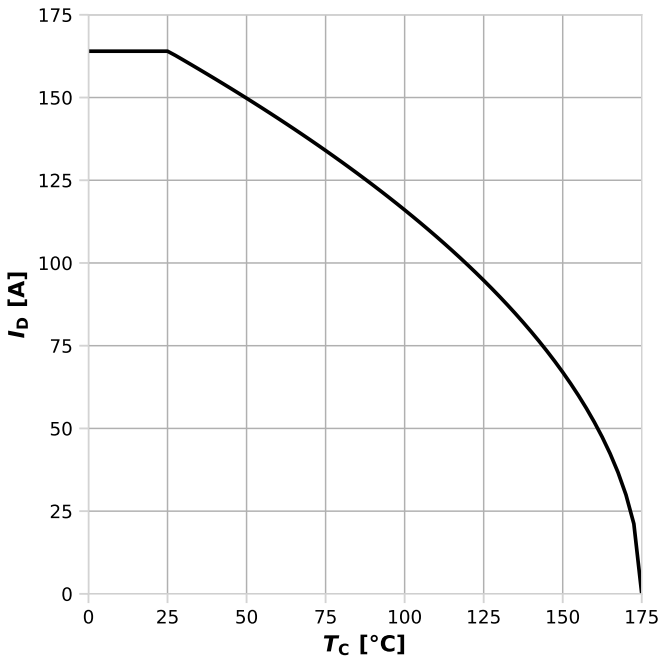
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



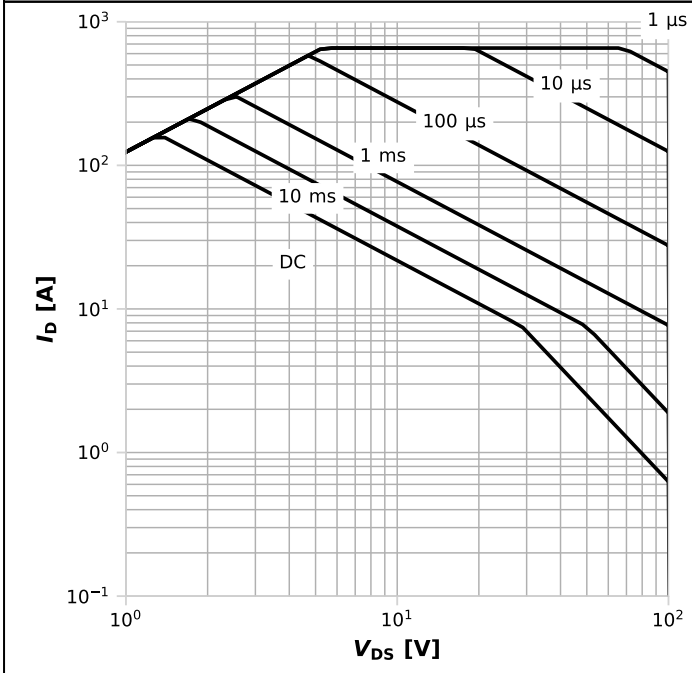
P_{tot}=f(T_C)

Diagram 2: Drain current



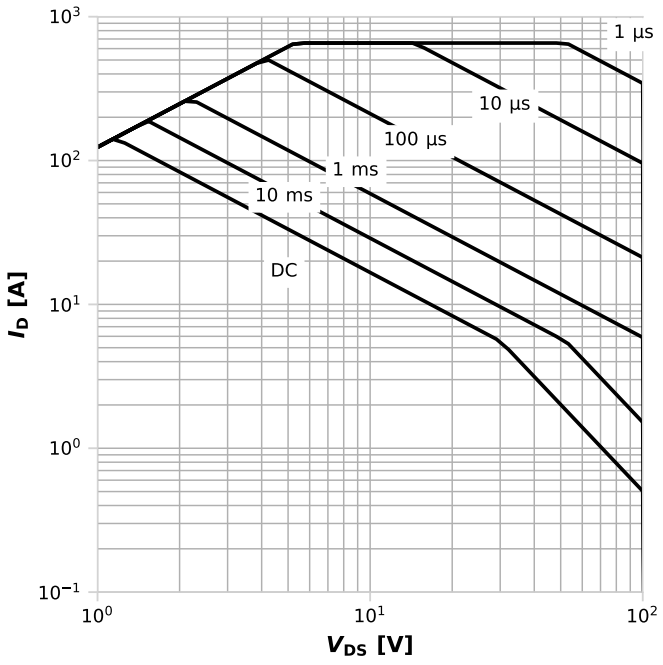
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



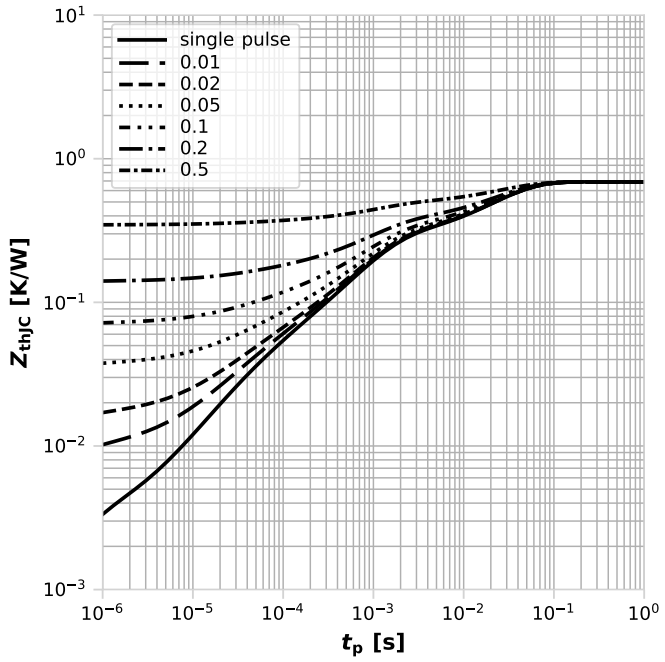
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Safe operating area



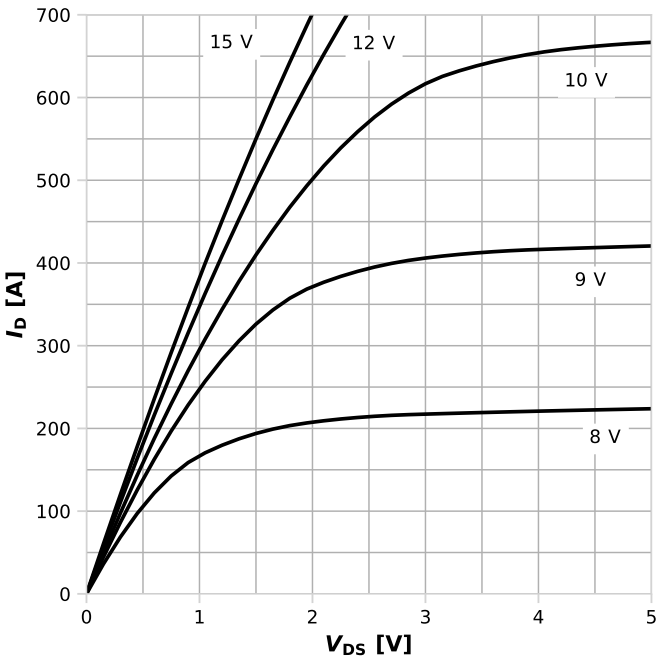
I_D=f(V_{DS}); T_C=125 °C; D=0; parameter: t_p

Diagram 5: Max. transient thermal impedance



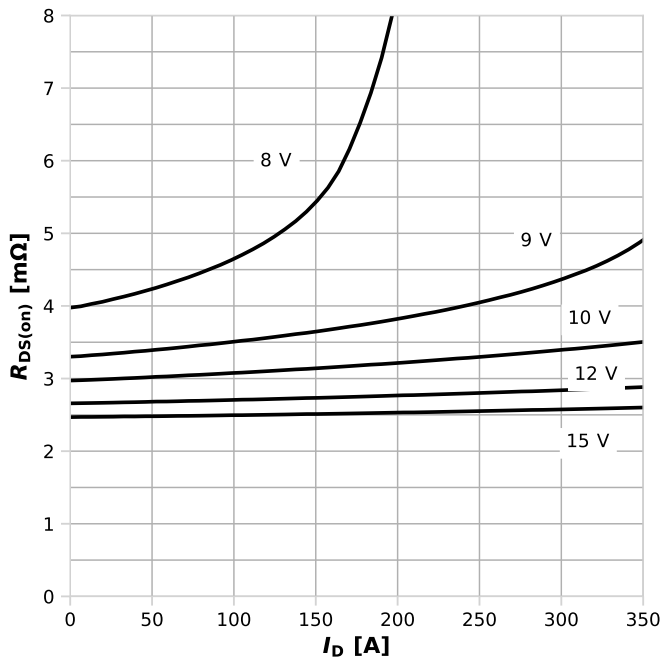
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 6: Typ. output characteristics



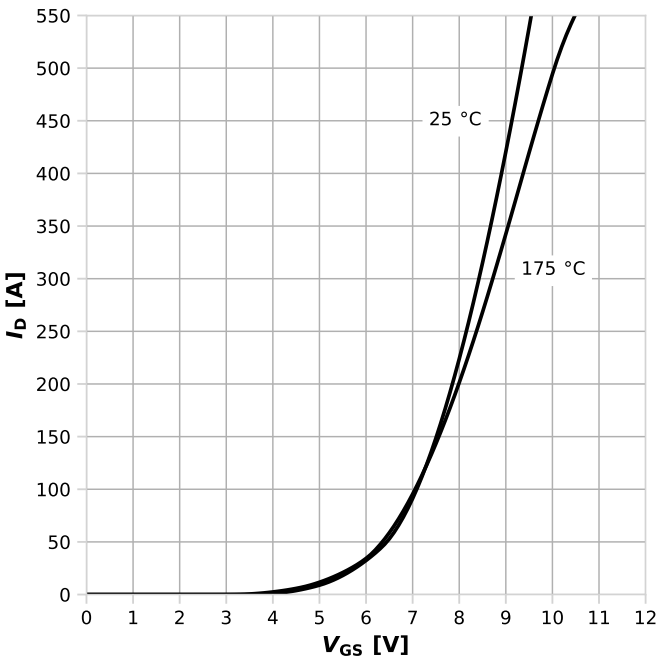
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on resistance



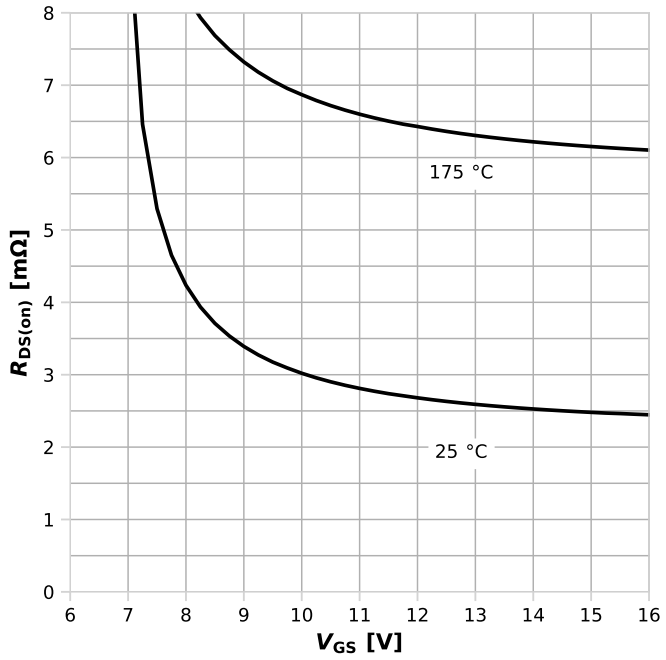
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 8: Typ. transfer characteristics



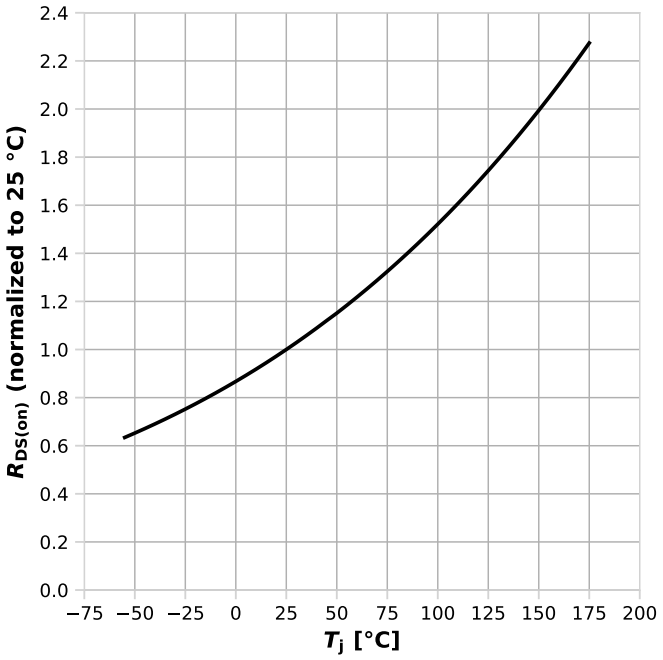
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 9: Typ. drain-source on resistance



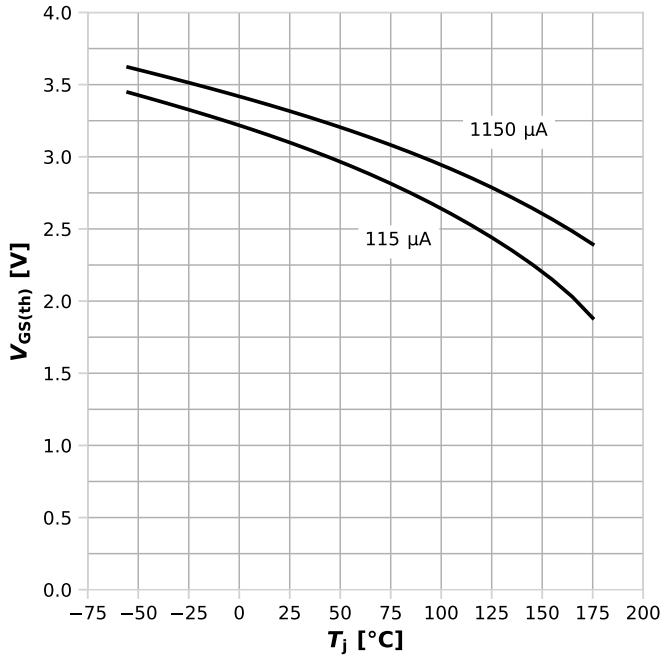
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 10: Normalized drain-source on resistance



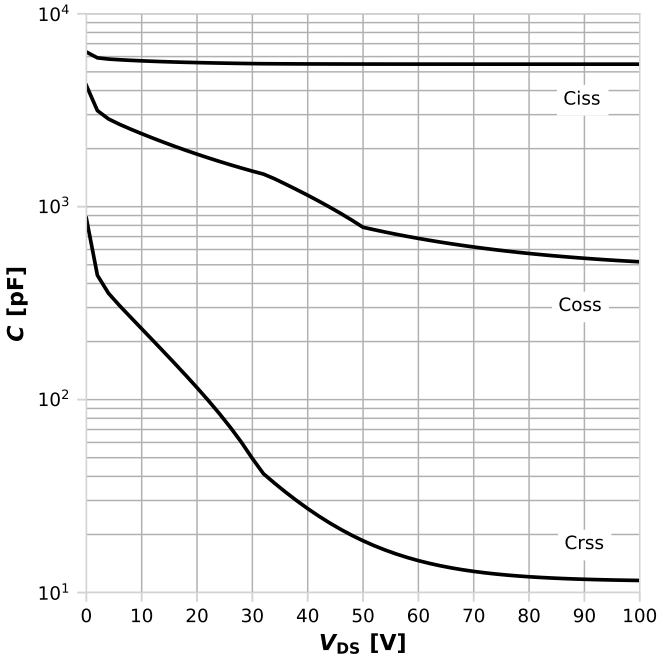
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 11: Typ. gate threshold voltage



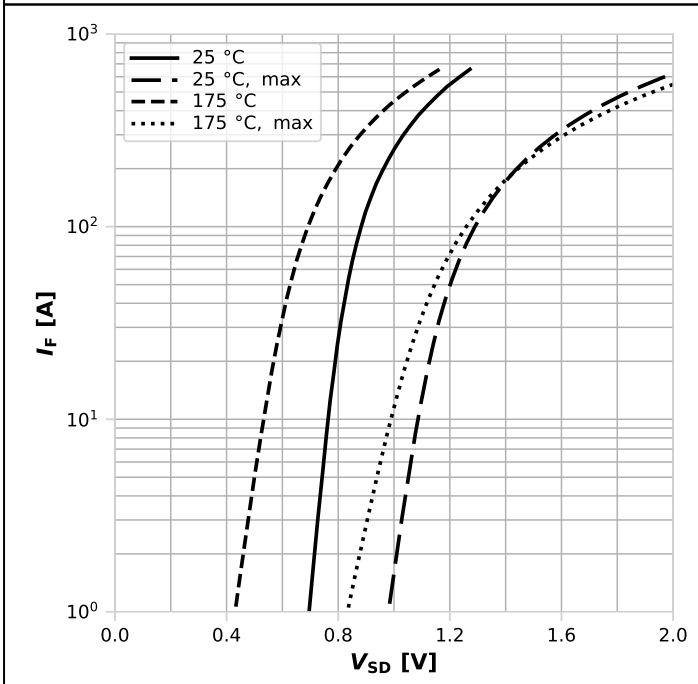
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 12: Typ. capacitances



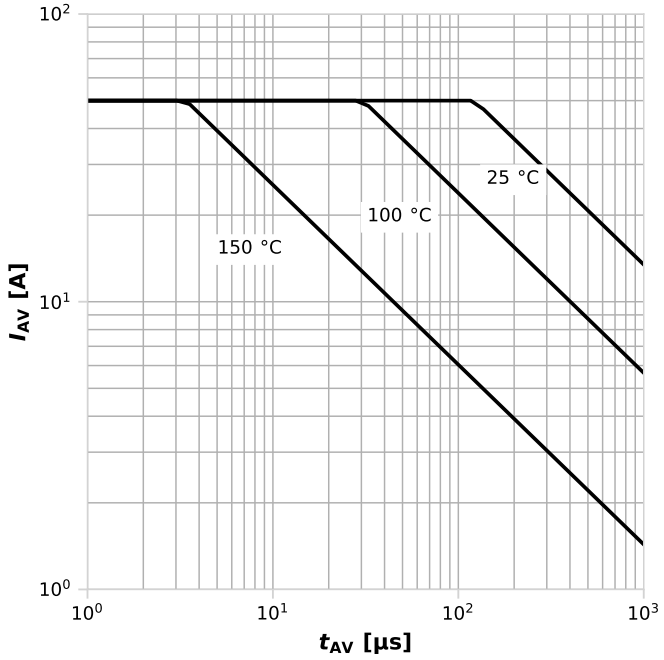
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 13: Forward characteristics of reverse diode



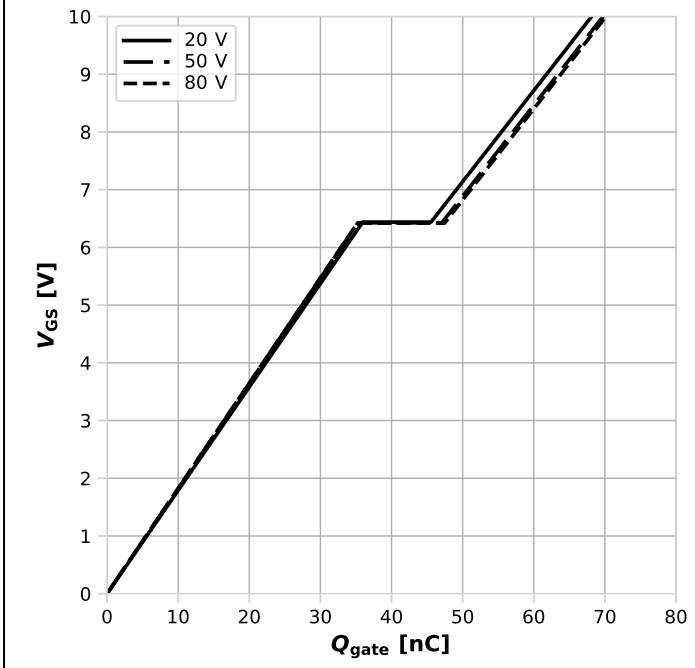
I_F=f(V_{SD}); parameter: T_j

Diagram 14: Avalanche characteristics



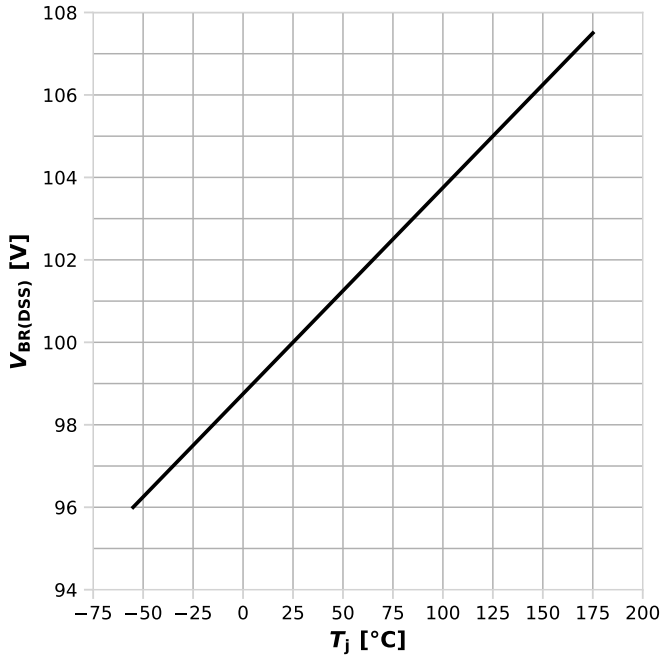
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 15: Typ. gate charge

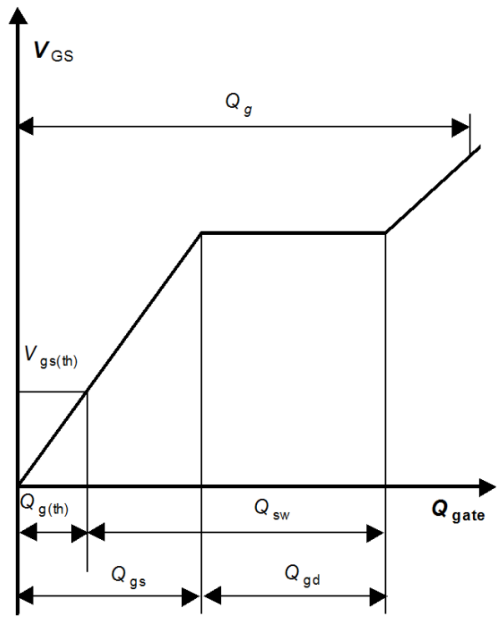


V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 16: Drain-source breakdown voltage



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms

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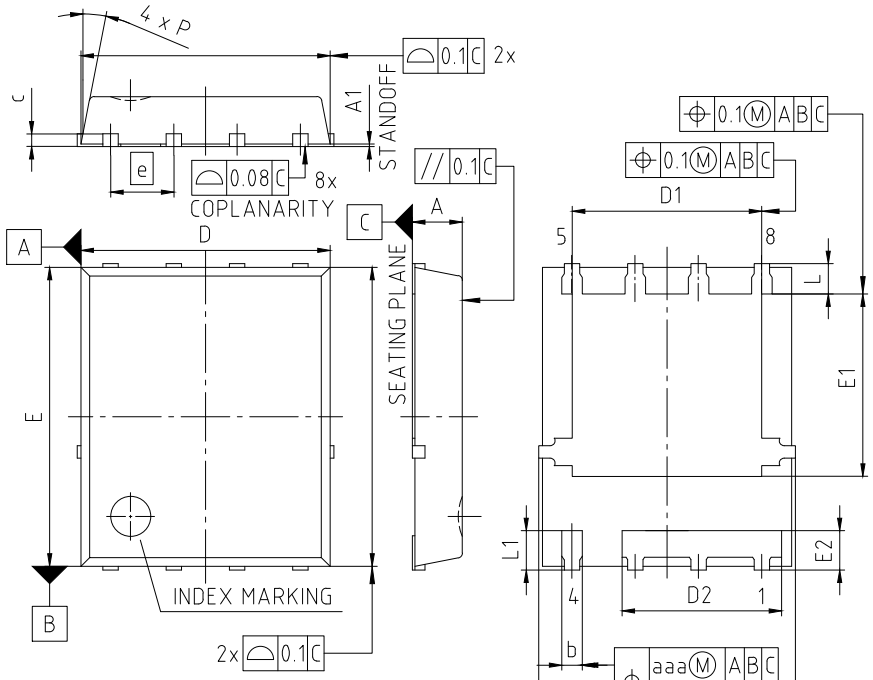
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TDSON-8-U04	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0	0.05
b	0.26	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.70	4.40
D2	2.94	3.25
D3	4.80	5.15
E	5.70	6.10
E1	3.40	3.76
E2	0.69	0.90
e	1.27	
L	0.45	0.72
L1	0.69	0.90
aaa	0.10	0.25
P	8°	12°

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
   INTRUSION 0.1 MM
   PROTRUSION 0.1 MM
3) LEAD LENGTH UP TO ANTI FLASH LINE
4) ALL METAL SURFACES ARE PLATED,
   EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

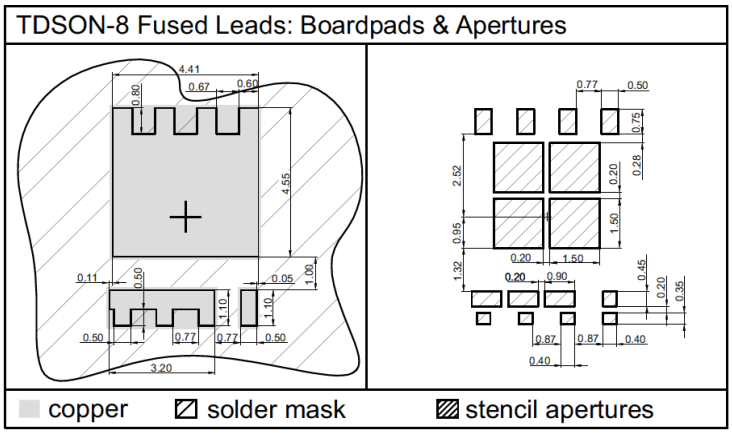


Figure 2 Footprint drawing PG-TDSON-8, dimensions in mm

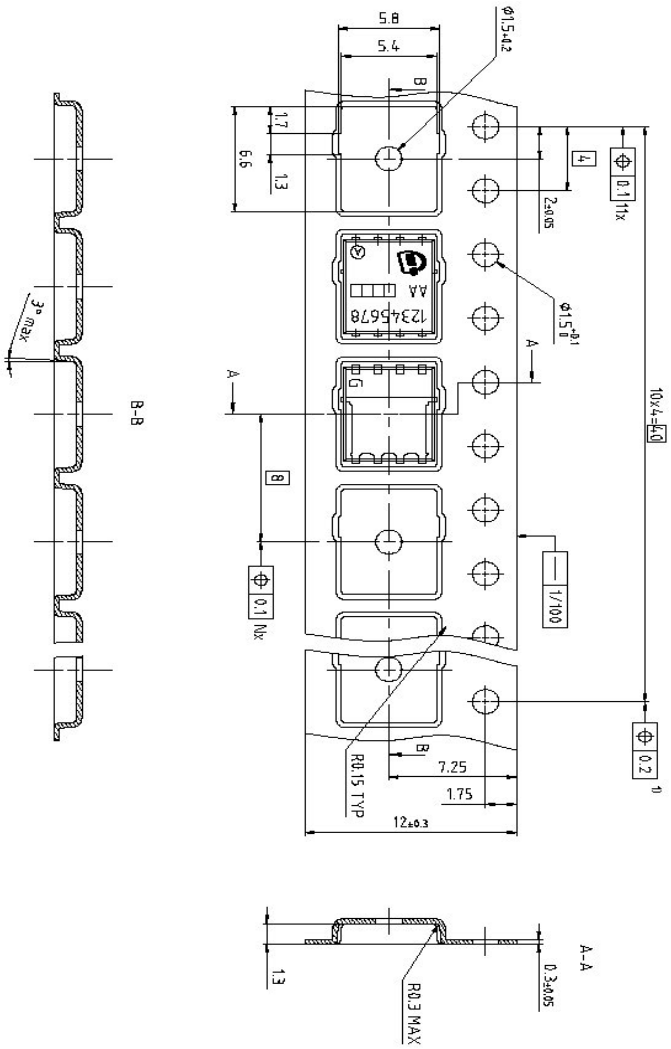


Figure 3 Packaging variant PG-TDSON-8, dimensions in mm

Revision history

ISC035N10NM5LF2

Revision 2024-10-22, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.1	2023-11-08	Update sales name and marking
2.2	2024-10-22	Update SOA and transient thermal impedance diagrams

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