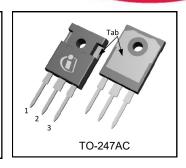
IRFP150NPbF



V _{(BR)DSS}	100V
R _{DS(on)} max.	0.036Ω
I _D	42A

Gate Pin 1 Source Pin 3



G	D	s
Gate	Drain	Source

Features

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- · Fully Avalanche Rated
- Lead-Free

Description

Fifth Generation HEXFET Power MOSFETs utilizes advanced processing techniques to achieve extremely low onresistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of other applications.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude th use of TO-220 devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

Paga part number	Bookaga Typa	Standard Pack		Orderable Part Number
Base part number	Package Type	Form	Quantity	Orderable Part Number
IRFP150NPbF	TO-247AC	Tube	25	IRFP150NPbF

Symbol	Symbol Parameter		Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	42	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	30	Α
I _{DM}	Pulsed Drain Current ①⑤	140	
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	160	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
Single Pulse Avalanche Energy ②⑤		420	mJ
I _{AR} Avalanche Current ①		22	А
E _{AR} Repetitive Avalanche Energy ①		16	mJ
dv/dt	Peak Diode Recovery dv/dt③⑤	5.0	V/ns
TJ	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units
$R_{ hetaJC}$	Junction-to-Case		0.95	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24		°C/W
$R_{\scriptscriptstyle{ hetaJA}}$	Junction-to-Ambient		40	



Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.11		V/°C	Reference to 25°C, I _D = 1mA ⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance			0.036	Ω	V _{GS} = 10V, I _D = 23A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
gfs	Forward Trans conductance				S	$V_{DS} = 25V, I_{D} = 22A$ (§
I	Drain-to-Source Leakage Current			25		$V_{DS} = 100V, V_{GS} = 0V$
I _{DSS} Drair	Jiani-lo-Source Leakage Current			250	μΛ	$V_{DS} = 80V, V_{GS} = 0V, T_{J} = 150$ °C
	Gate-to-Source Forward Leakage			100	۵,	$V_{GS} = 20V$
IGSS	Gate-to-Source Reverse Leakage			-100	nA	V _{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q_g	Total Gate Charge	 	110		I _D = 22A
Q_{gs}	Gate-to-Source Charge	 	15	nC	$V_{DS} = 80V$
Q_{gd}	Gate-to-Drain Charge	 	58		V _{GS} = 10V, See Fig.6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	 11			$V_{DD} = 50V$
t _r	Rise Time	 56		ns	I _D = 22A
$t_{d(off)}$	Turn-Off Delay Time	 45		115	$R_G = 3.6\Omega$
t _f	Fall Time	 40			R _D = 2.9Ω , See Fig.10⊕⑤
L_D	Internal Drain Inductance	 5.0			Between lead, 6mm (0.25in.)
Ls	Internal Source Inductance	 13			from package and center of die contact
C _{iss}	Input Capacitance	 1900			$V_{GS} = 0V$
C _{oss}	Output Capacitance	 450		рF	$V_{DS} = 25V$
C _{rss}	Reverse Transfer Capacitance	 230			f = 1.0MHz, See Fig.5®

Diode Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current (Body Diode)			42	l .	MOSFET symbol showing the
I _{SM}	Pulsed Source Current (Body Diode) ①			140	1	integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage			1.3	٧	$T_J = 25^{\circ}C, I_S = 23A, V_{GS} = 0V $ ④
t _{rr}	Reverse Recovery Time		180	270	ns	$T_J = 25^{\circ}C$, $I_F = 22A$
Q_{rr}	Reverse Recovery Charge		1.2	1.8	μC	di/dt = 100A/µs ④⑤

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② V_{DD} = 25V, T_{J} = 25°C, L = 1.7mH, R_{G} = 25Ω, I_{AS} = 22A.(See fig. 12).
- $\label{eq:local_local_local} \mbox{\Im} \quad I_{SD} \leq 22A, \ di/dt \leq 180A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \ T_J \leq 175^{\circ}C.$
- 4 Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRF1310N data and test conditions



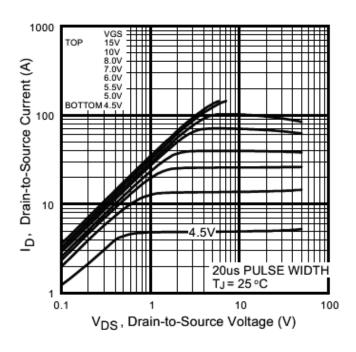


Fig. 1 Typical Output Characteristics

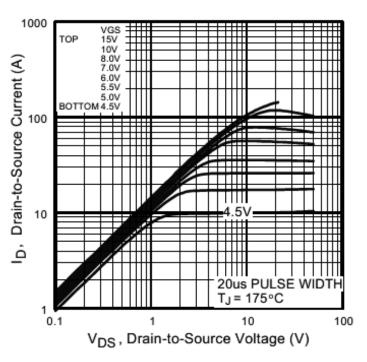


Fig. 2 Typical Output Characteristics

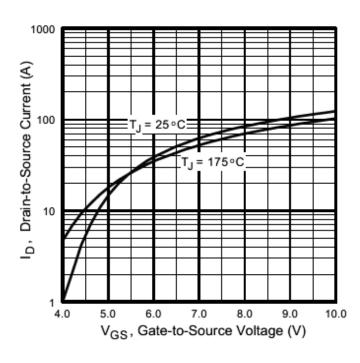


Fig. 3 Typical Transfer Characteristics

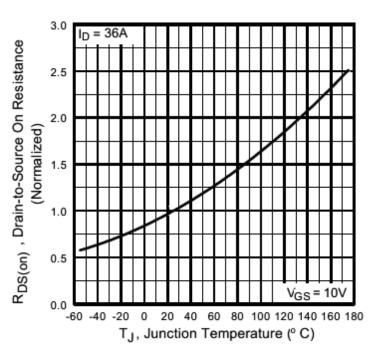


Fig. 4 Normalized On-Resistance vs. Temperature



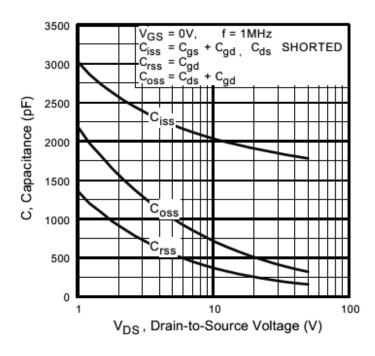


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

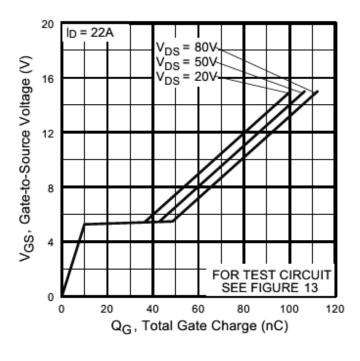


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

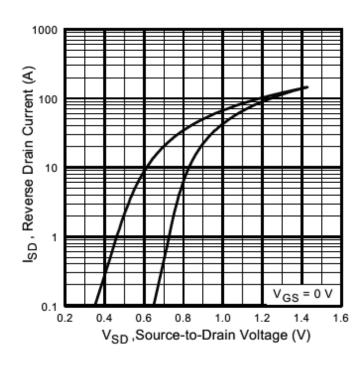


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

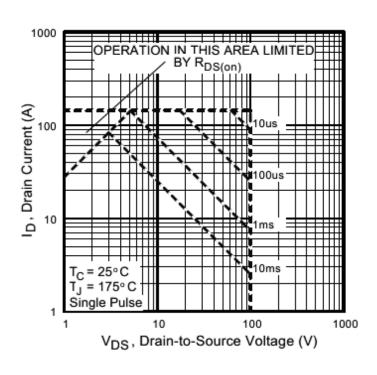


Fig 8. Maximum Safe Operating Area



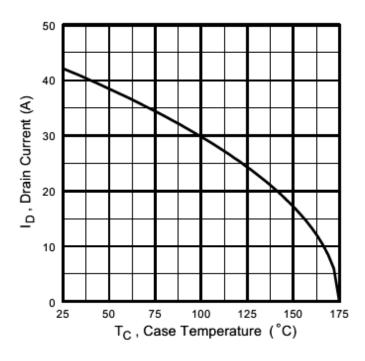


Fig 9. Maximum Drain Current vs. Case Temperature

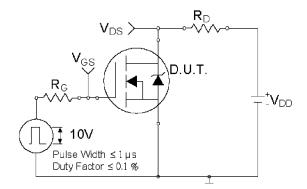


Fig 10a. Switching Time Test Circuit

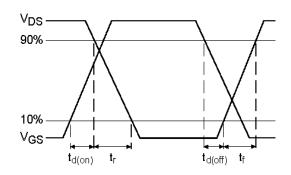


Fig 10a. Switching Time Waveforms

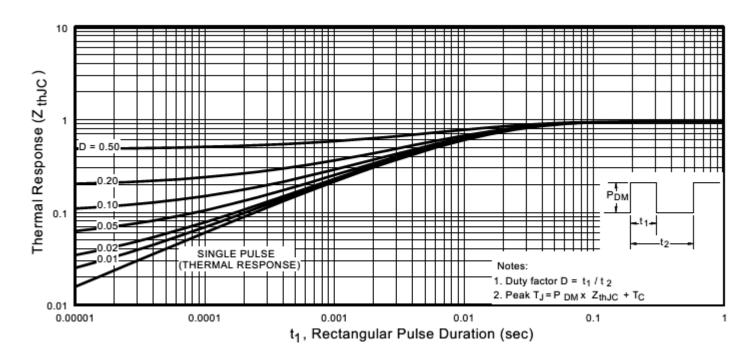


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



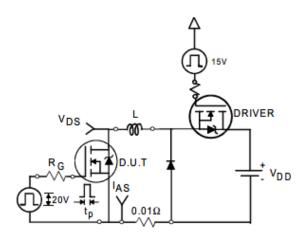


Fig. 12a. Unclamped Inductive Test Circuit

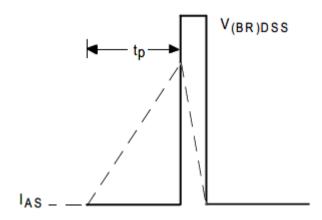


Fig. 12b. Unclamped Inductive Waveforms

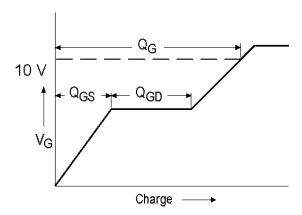


Fig 13a. Basic Gate Charge Waveform

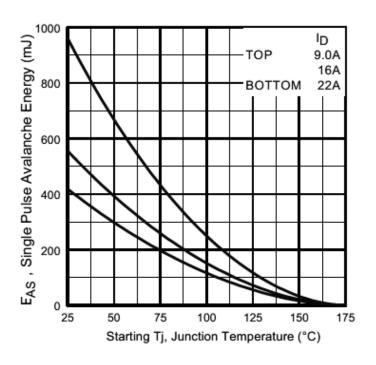


Fig 12c. Maximum Avalanche Energy vs. Drain Current

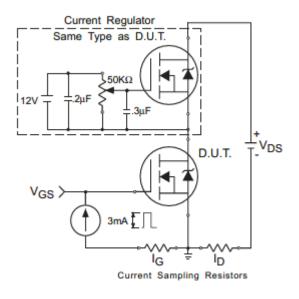
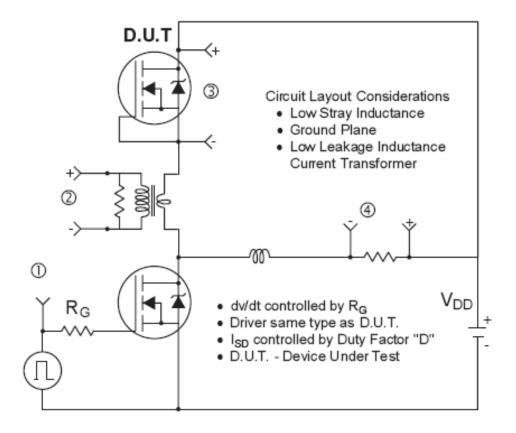


Fig 13b. Gate Charge Test Circuit





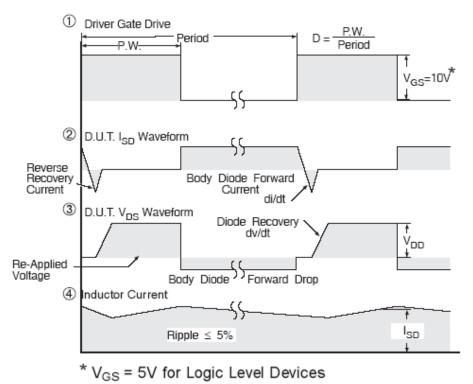
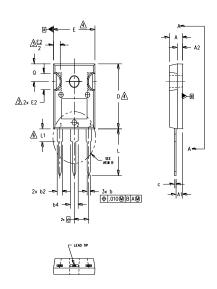
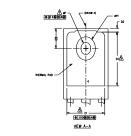


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

infineon

TO-247AC Package Outline (Dimensions are









NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.

2. DIMENSIONS ARE SHOWN IN INCHES.

<u>3</u>.

CONTOUR OF SLOT OPTIONAL.

DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127)
PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.

LEAD FINISH UNCONTROLLED IN L1.

OP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 * TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.

8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

		DIMEN	ISIONS		
SYMBOL	INC	HES	MILLIM	IETERS	
	MIN.	MAX.	MIN.	MAX.	NOTES
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
ь1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
С	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215	BSC	5.46 BSC		
Øk		.010 0.25		25	
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØΡ	.140	.144	3.56	3.66	
øP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217	BSC	5.51	BSC	
	1		ll .		I

LEAD ASSIGNMENTS

<u>HEXFET</u>

- 1.- GATE 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

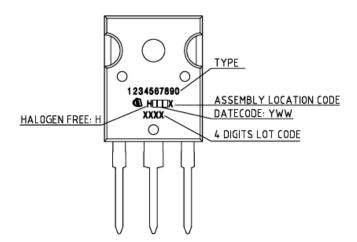
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR 3.- EMITTER
- 4.- COLLECTOR

<u>DIODES</u>

- 1.- ANODE/OPEN
- 2. CATHODE
- 3.- ANODE

TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.



Revision History

Date	Rev.	Comments		
2024-10-03	2.1	 Update datasheet to Infineon format Updated Part marking –page 8 		
		Added disclaimer on last page.		

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