International
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IRF7739L1TRPbF

DirectFET™ Power MOSFET ②

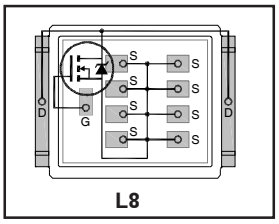
Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$
40V min	±20V max	0.70mΩ@ 10V
$Q_{g\ tot}$	Q_{gd}	$V_{gs(th)}$
220nC	81nC	2.8V

Applications

- RoHS Compliant, Halogen Free ②
- Lead-Free (Qualified up to 260°C Reflow)①
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①
- Industrial Qualified

Applicable DirectFET Outline and Substrate Outline ①



L8

DirectFET™ ISOMETRIC

SB	SC			M2	M4		L4	L6	L8	

Description

The IRF7739L1TRPbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has a footprint smaller than a D^2PAK and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems.

The IRF7739L1TRPbF is optimized for high frequency switching and synchronous rectification applications. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance power converters.

Ordering Information

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF7739L1TRPbF	DirectFET Large Can	Tape and Reel	4000	IRF7739L1TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)④	270	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)④	190	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)③	46	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited) ④	375	
I_{DM}	Pulsed Drain Current ⑤	1070	
E_{AS}	Single Pulse Avalanche Energy ⑥	270	mJ
I_{AR}	Avalanche Current ⑤	160	A

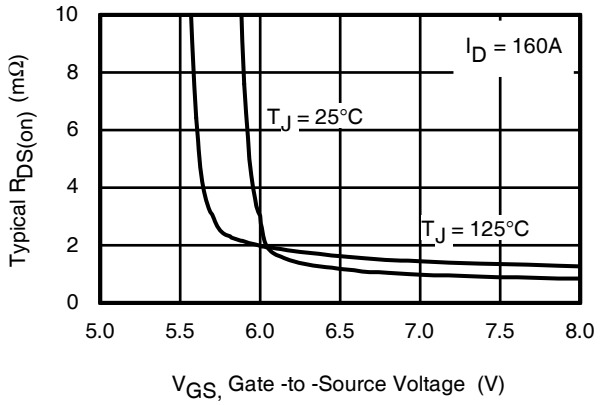


Fig 1. Typical On-Resistance vs. Gate Voltage

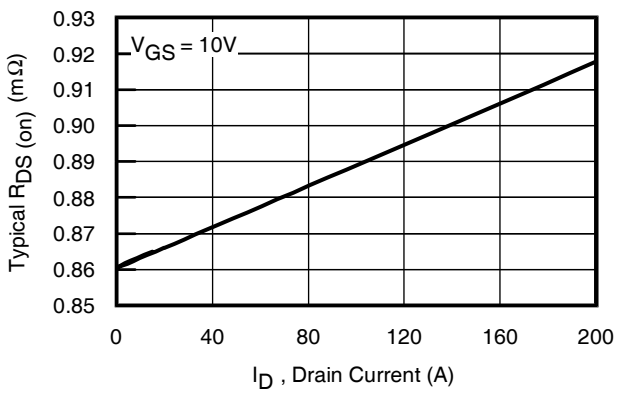


Fig 2. Typical On-Resistance vs. Drain Current

Notes:

① Click on the hyperlink (to the relevant technical document) for more details.

② Click on the hyperlink (to the DirectFET website) for more details

③ Surface mounted on 1 in. square Cu board, steady state.

④ T_C measured with thermocouple mounted to top (Drain) of part.

⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑥ Starting T_J = 25°C, L = 0.021mH, R_G = 25Ω, I_{AS} = 160A.

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.008	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.70	1.0	mΩ	V_{GS} = 10V, I_D = 160A ⑦
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.8	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-6.7	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	280	—	—	S	V_{DS} = 10V, I_D = 160A
Q_g	Total Gate Charge	—	220	330		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	46	—		V_{DS} = 20V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	19	—	nC	V_{GS} = 10V
Q_{gd}	Gate-to-Drain Charge	—	81	120		I_D = 160A
Q_{godr}	Gate Charge Overdrive	—	74	—		See Fig. 9
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	100	—		
Q_{oss}	Output Charge	—	83	—	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	—	1.5	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	21	—		V_{DD} = 20V, V_{GS} = 10V ⑦
t_r	Rise Time	—	71	—		I_D = 160A
$t_{d(off)}$	Turn-Off Delay Time	—	56	—	ns	R_G=1.8Ω
t_f	Fall Time	—	42	—		
C_{iss}	Input Capacitance	—	11880	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	2510	—	pF	V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	1240	—		ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	8610	—		V_{GS} = 0V, V_{DS} = 1.0V, f=1.0MHz
C_{oss}	Output Capacitance	—	2230	—		V_{GS} = 0V, V_{DS} = 32V, f=1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	110	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	1070		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 160A, V_{GS} = 0V ⑦
t_{rr}	Reverse Recovery Time	—	87	130	ns	T_J = 25°C, I_F = 160A, V_{DD} = 20V
Q_{rr}	Reverse Recovery Charge	—	250	380	nC	di/dt = 100A/µs ⑦

Notes:

⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑦ Pulse width ≤ 400µs; duty cycle ≤ 2%.

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Absolute Maximum Ratings

	Parameter	Max.	Units
P_D @T_C = 25°C	Power Dissipation ④	125	W
P_D @T_C = 100°C	Power Dissipation ④	63	
P_D @T_A = 25°C	Power Dissipation ①	3.8	
T_P	Peak Soldering Temperature	270	°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	40	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑧	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨	20	—	
$R_{\theta J\text{-}Can}$	Junction-to-Can ④⑩	—	1.2	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	—	0.4	

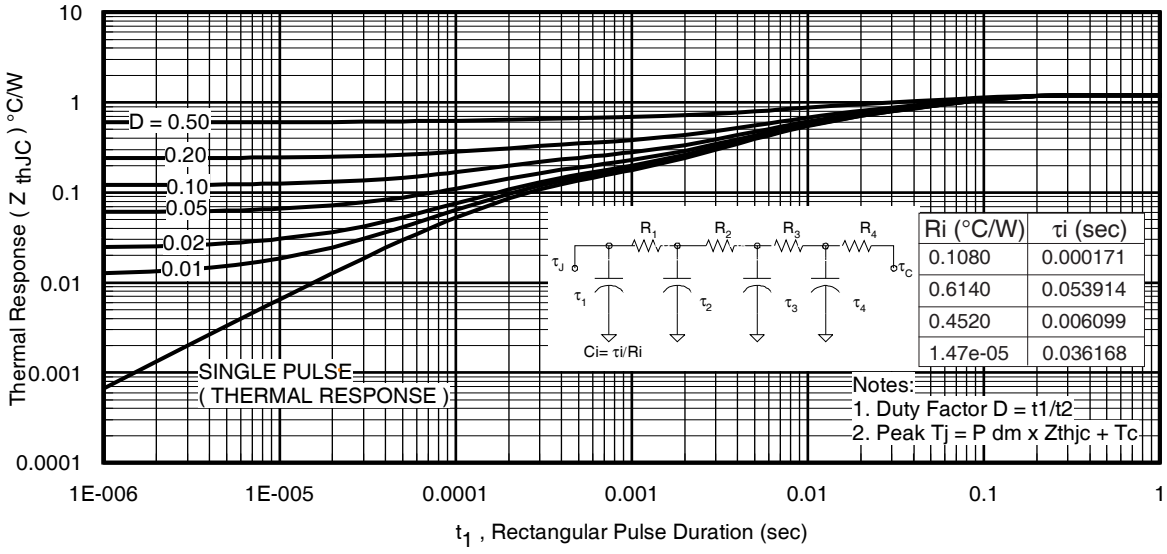


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Case ④

Notes:

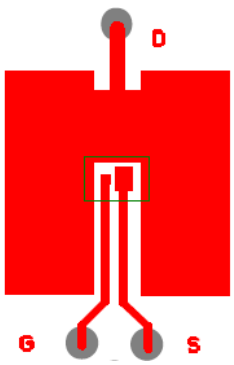
③ Surface mounted on 1 in. square Cu board, steady state.

④ T_C measured with thermocouple incontact with top (Drain) of part.

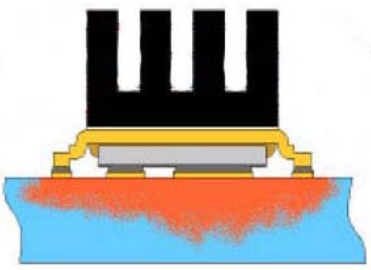
⑧ Used double sided cooling, mounting pad with large heatsink.

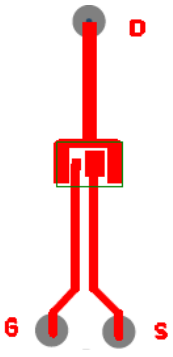
⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

⑩ R_θ is measured at T_J of approximately 90°C.



③ Surface mounted on 1 in. square Cu board (still air).





⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink. (still air)

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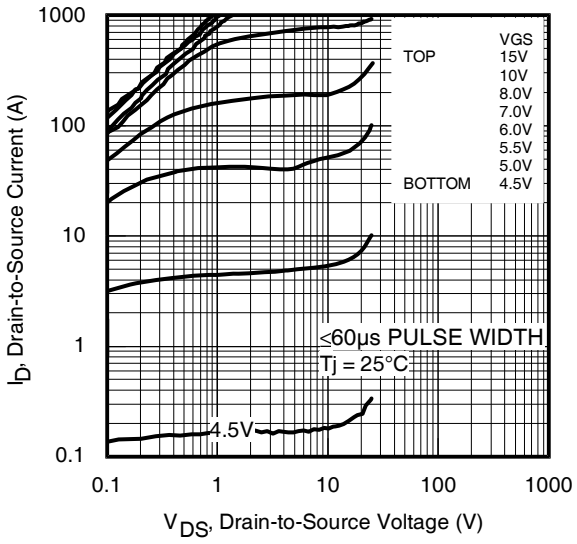

Fig 4. Typical Output Characteristics

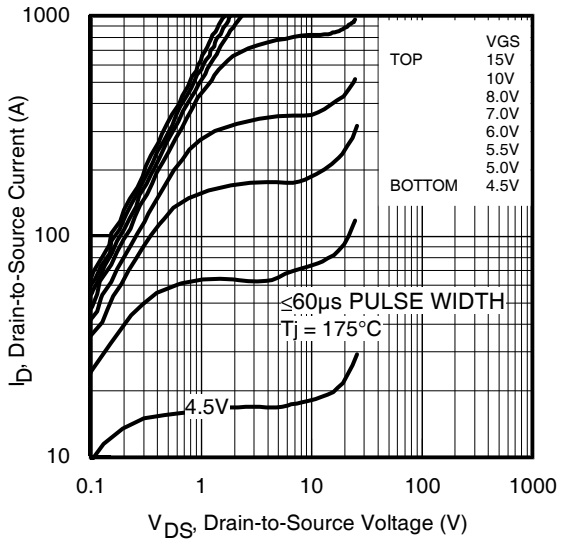

Fig 5. Typical Output Characteristics

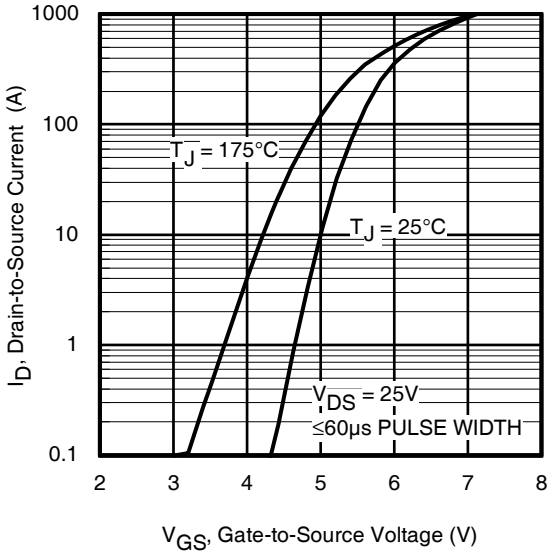

Fig 6. Typical Transfer Characteristics

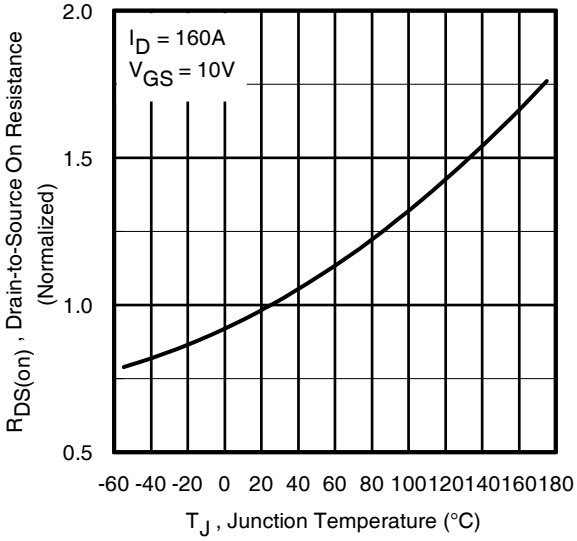

Fig 7. Normalized On-Resistance vs. Temperature

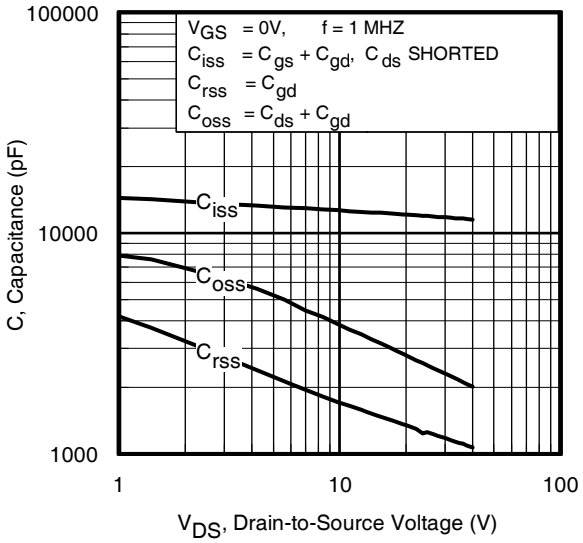

Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

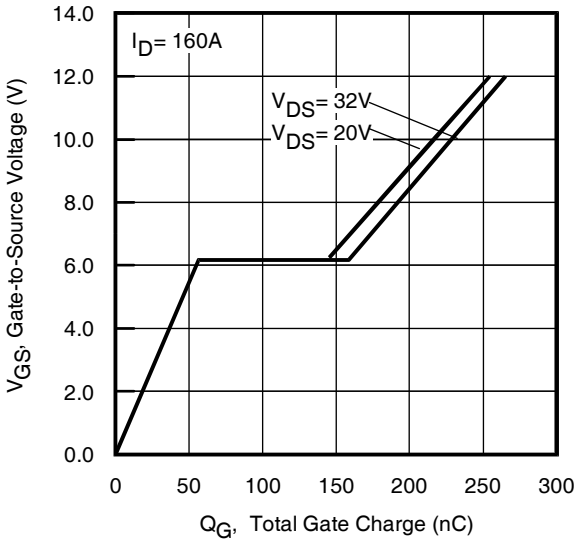

Fig 9. Typical Total Gate Charge vs. Gate-to-Source Voltage

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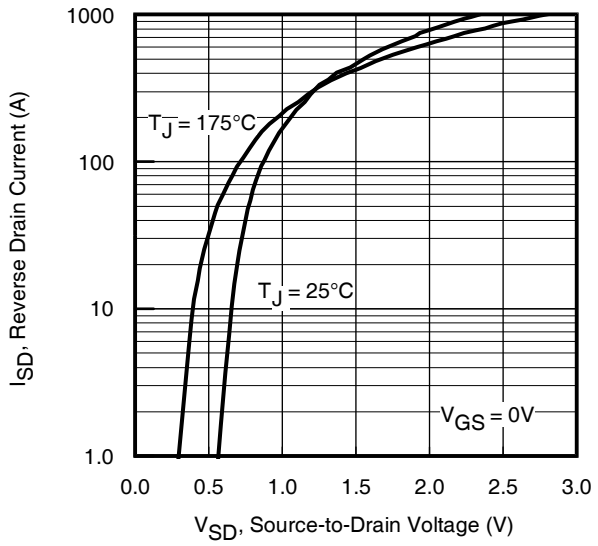

Fig 10. Typical Source-Drain Diode Forward Voltage

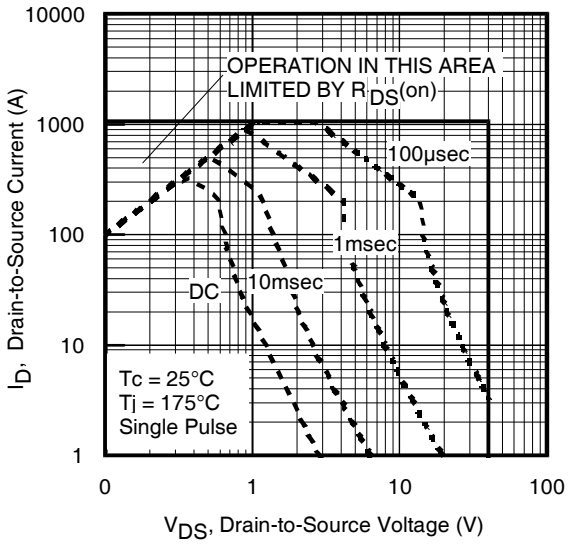

Fig11. Maximum Safe Operating Area

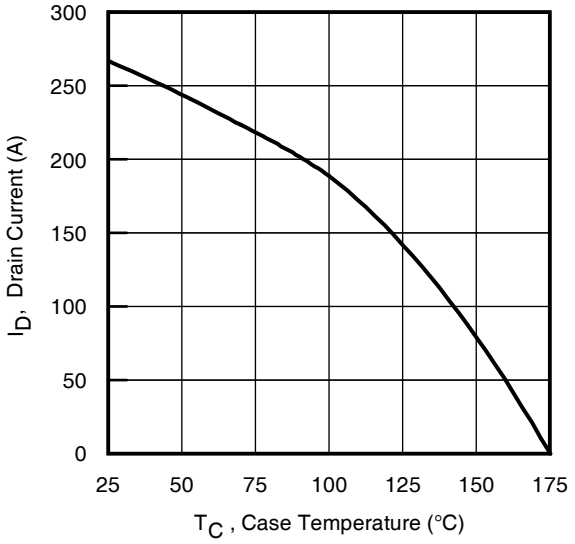

Fig 12. Maximum Drain Current vs. Case Temperature

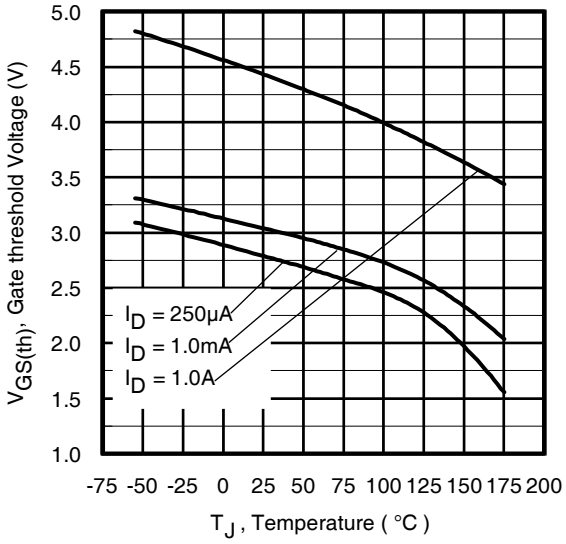

Fig 13. Typical Threshold Voltage vs. Junction Temperature

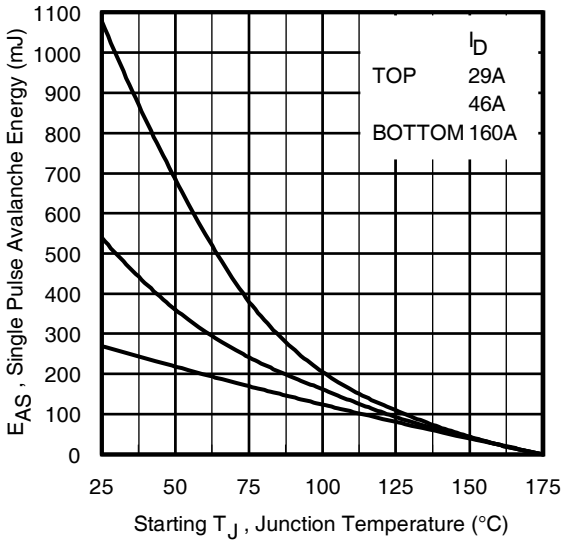

Fig 14. Maximum Avalanche Energy vs. Drain Current

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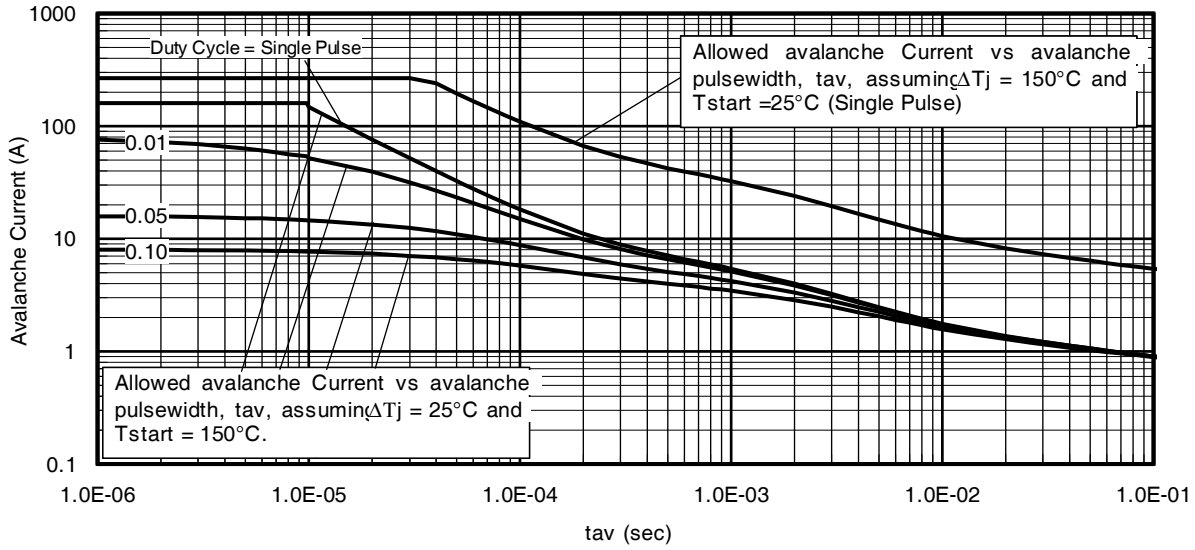


Fig 15. Typical Avalanche Current vs. Pulsewidth

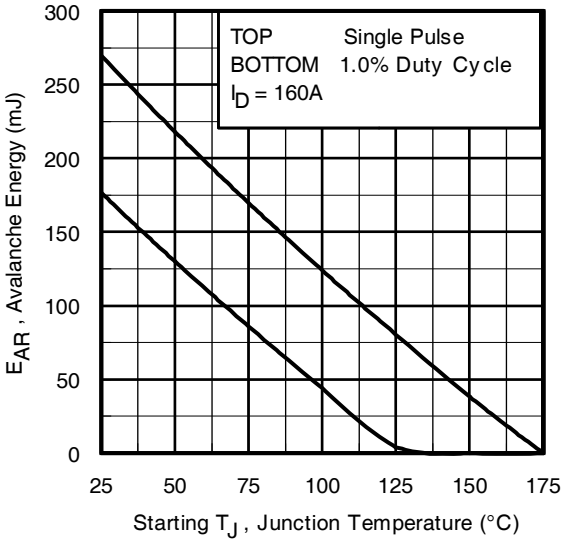
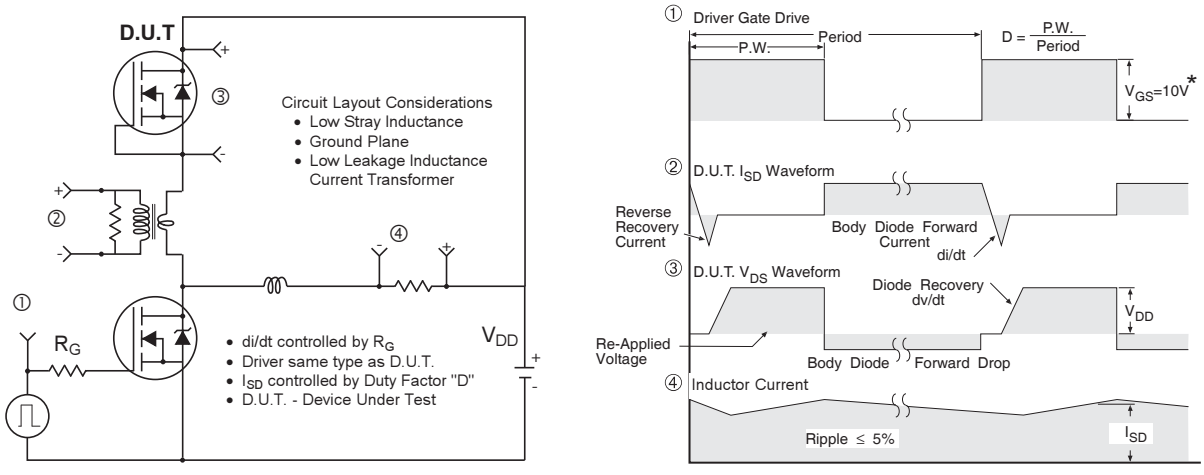


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 19a, 19b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_a$$



* V_{GS} = 5V for Logic Level Devices

Fig 17. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

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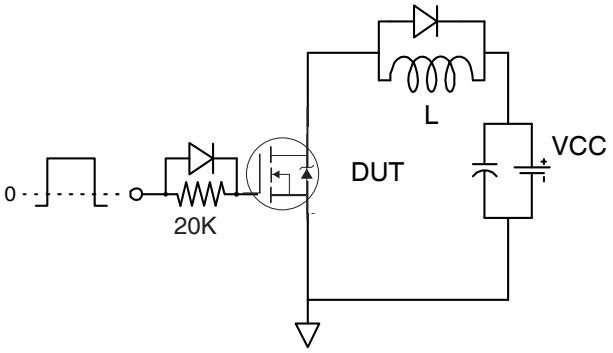

Fig 18a. Gate Charge Test Circuit

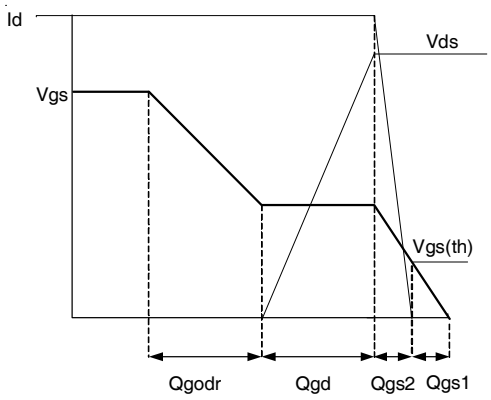

Fig 18b. Gate Charge Waveform

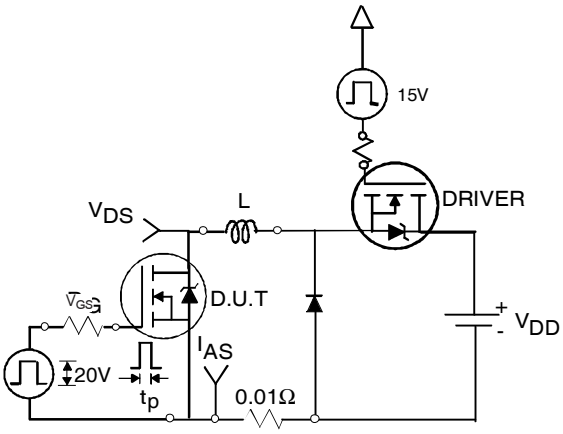

Fig 19a. Unclamped Inductive Test Circuit

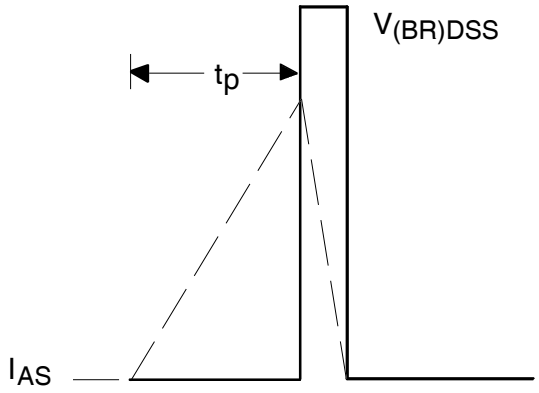

Fig 19b. Unclamped Inductive Waveforms

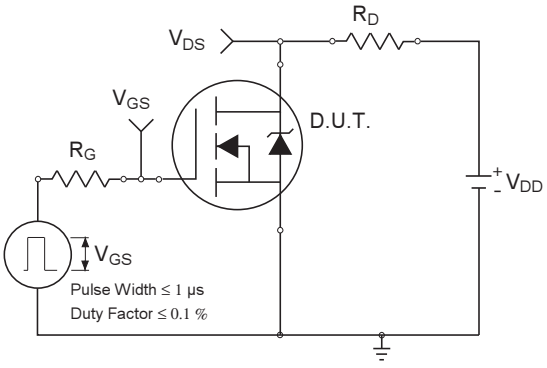

Fig 20a. Switching Time Test Circuit

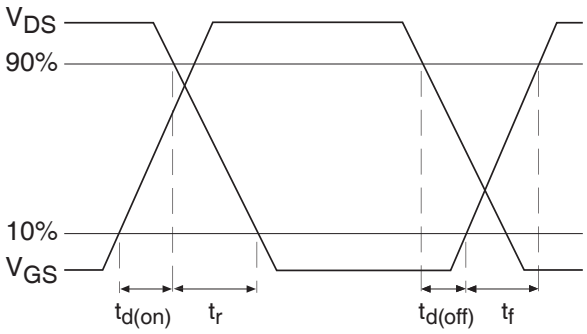

Fig 20b. Switching Time Waveforms

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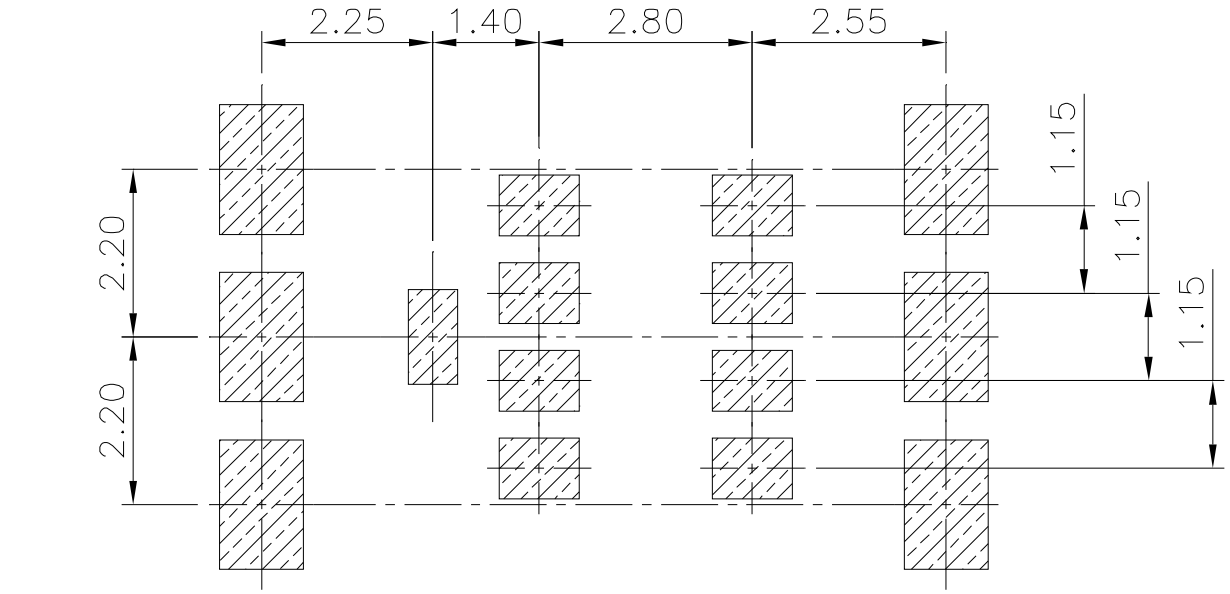
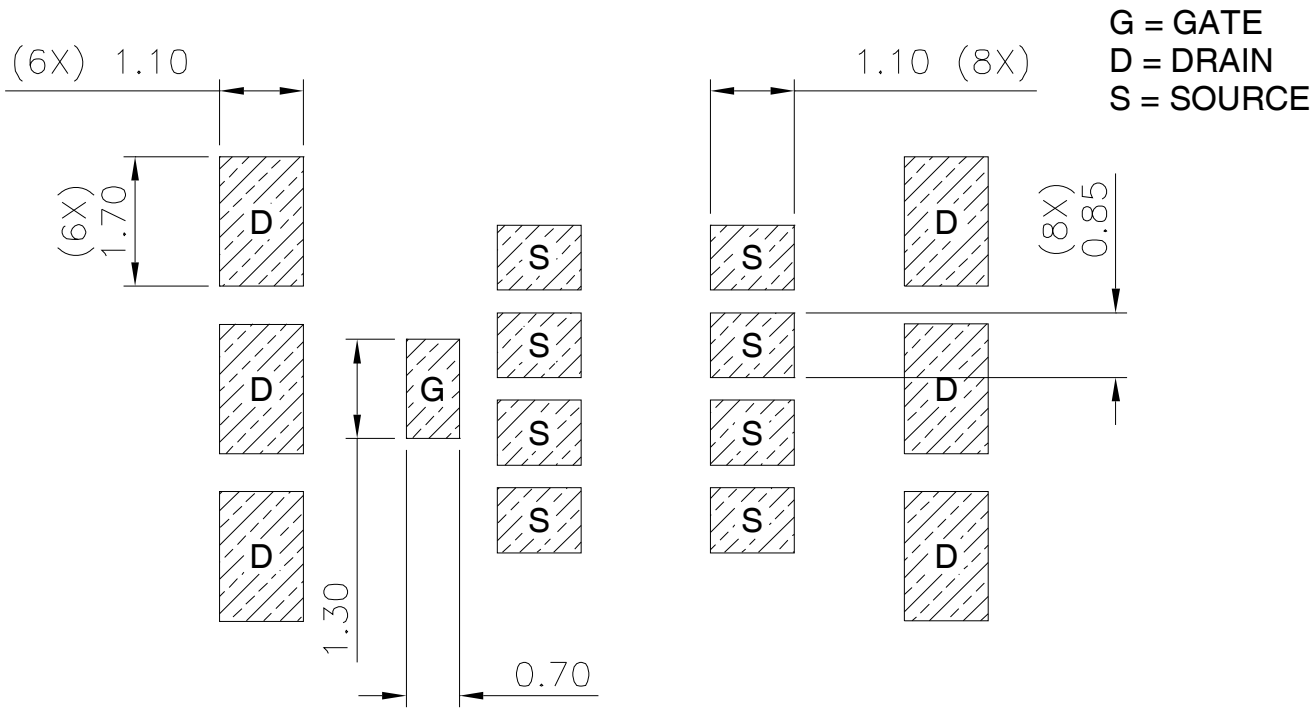
DirectFET™ Board Footprint, L8 (Large Size Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations





G = GATE
D = DRAIN
S = SOURCE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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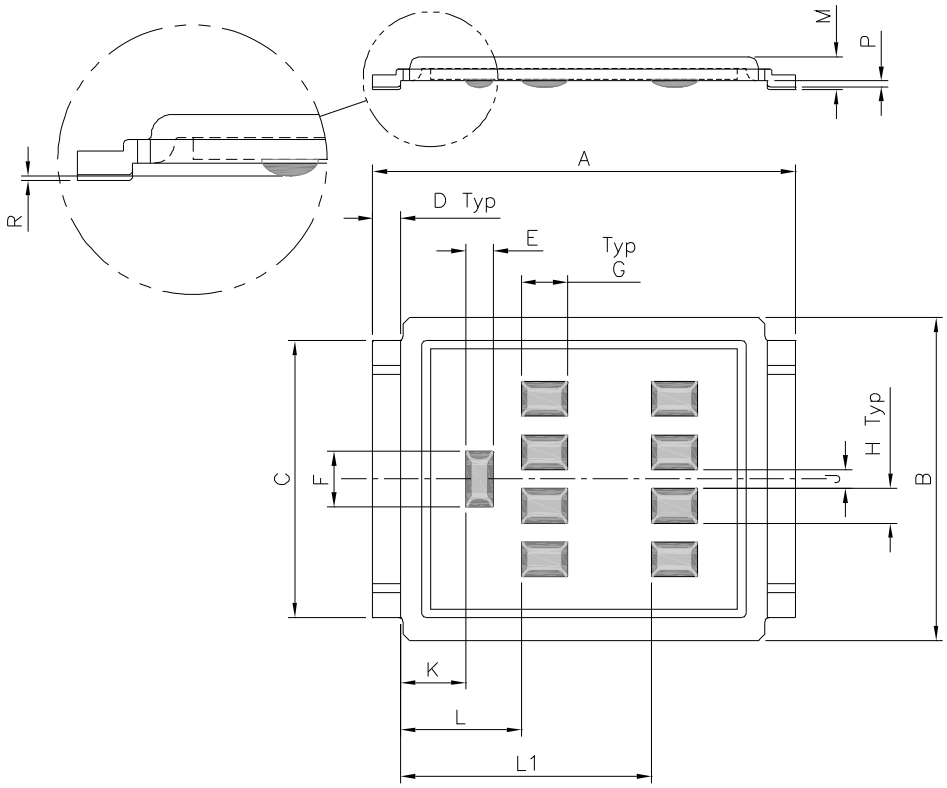
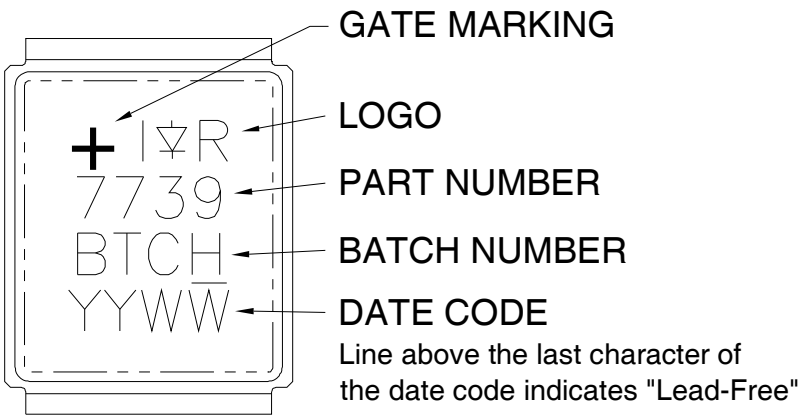
DirectFET™ Outline Dimension, L8 Outline (LargeSize Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations



DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	9.05	9.15	0.356	0.360
B	6.85	7.10	0.270	0.280
C	5.90	6.00	0.232	0.236
D	0.55	0.65	0.022	0.026
E	0.58	0.62	0.023	0.024
F	1.18	1.22	0.046	0.048
G	0.98	1.02	0.039	0.040
H	0.73	0.77	0.029	0.030
J	0.38	0.42	0.015	0.017
K	1.35	1.45	0.053	0.057
L	2.55	2.65	0.100	0.104
L1	5.35	5.45	0.211	0.215
M	0.68	0.74	0.027	0.029
P	0.09	0.17	0.003	0.007
R	0.02	0.08	0.001	0.003

DirectFET™ Part Marking



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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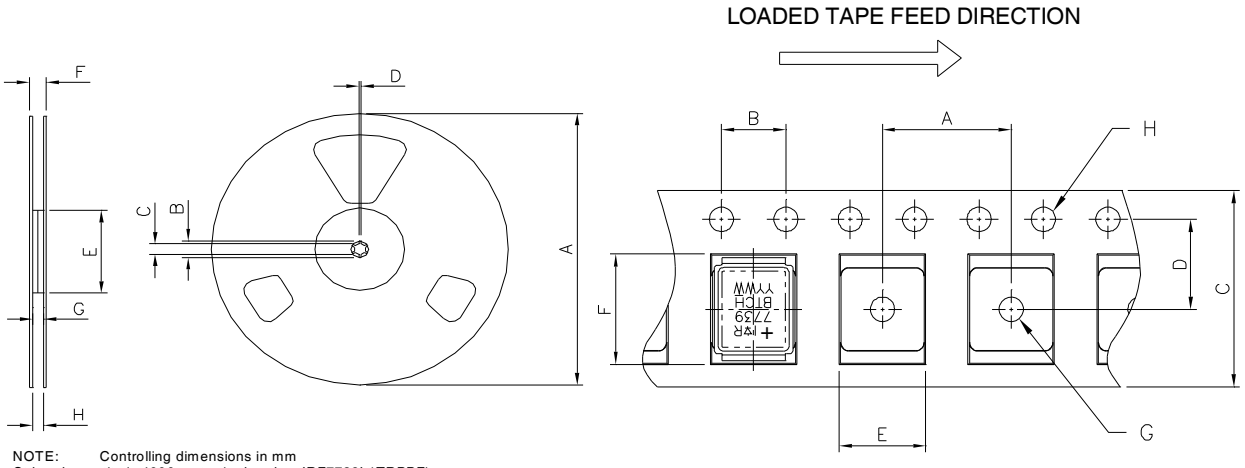
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4000 parts. (ordered as IRF7739L1TRPBF).

REEL DIMENSIONS				
STANDARD OPTION (QTY 4000)				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	330.00	N.C	12.992	N.C
B	20.20	N.C	0.795	N.C
C	12.80	13.20	0.504	0.520
D	1.50	N.C	0.059	N.C
E	99.00	100.00	3.900	3.940
F	N.C	22.40	N.C	0.880
G	16.40	18.40	0.650	0.720
H	15.90	19.40	0.630	0.760

NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	11.90	12.10	4.69	0.476
B	3.90	4.10	0.154	0.161
C	15.90	16.30	0.623	0.642
D	7.40	7.60	0.291	0.299
E	7.20	7.40	0.283	0.291
F	9.90	10.10	0.390	0.398
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification level	Industrial †† *	
Moisture Sensitivity Level	DirectFET	MSL1 (per JEDEC J-STD-020D†††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

* Industrial qualification standards except autoclave test conditions

Revision History

Date	Comments
2/12/2013	TR1 option removed and Tape & Reel Info updated accordingly. Hyperlinks added throw-out the document

International IOR Rectifier

IR WORLD HEADQUARTERS: 101N Sepulveda Blvd, El Segundo, California 90245, USA

To contact International Rectifier, please visit http://www.irf.com/whoto-call/

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