

IRF7307PbF

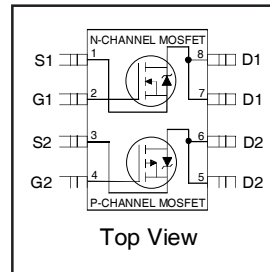
HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

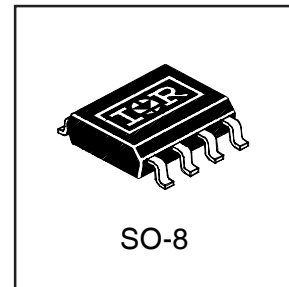
Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



	N-Ch	P-Ch
V_{DS}	20V	-20V
$R_{DS(on)}$	0.050Ω	0.090Ω



Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
$I_D @ T_A = 25^\circ\text{C}$	10 Sec. Pulse Drain Current, $V_{GS} @ 4.5\text{V}$	5.7	-4.7	A
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}$	5.2	-4.3	
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}$	4.1	-3.4	
I_{DM}	Pulsed Drain Current ①	21	-17	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V_{GS}	Gate-to-Source Voltage	± 12		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient③	---	62.5	°C/W

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

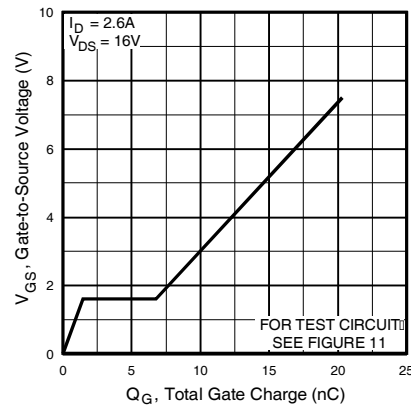
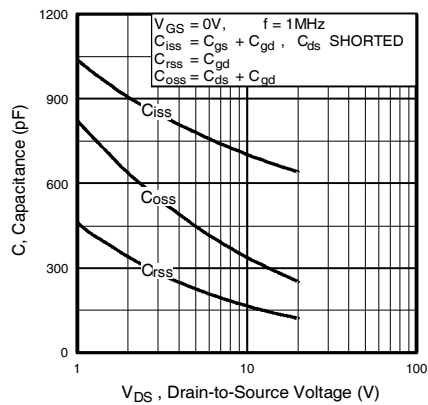
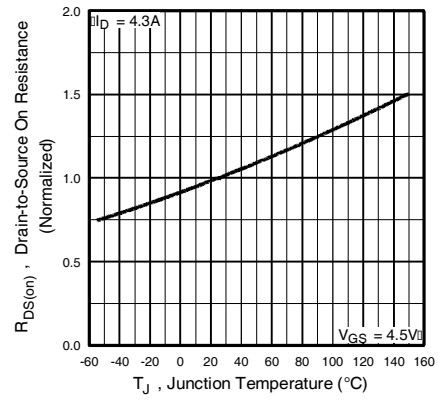
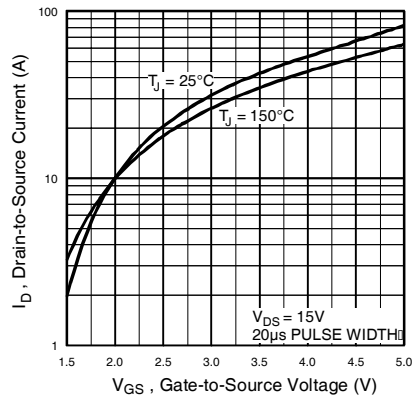
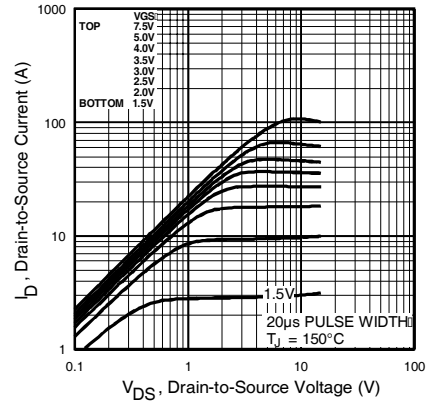
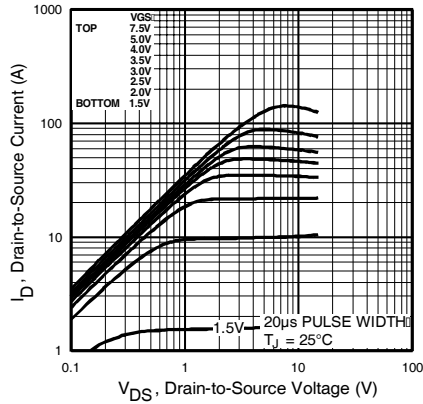
	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-20	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.044	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	-0.012	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.050	Ω	$V_{GS} = 4.5V, I_D = 2.6A$ ③
		N-Ch	—	—	0.070		$V_{GS} = 2.7V, I_D = 2.2A$ ③
		P-Ch	—	—	0.090		$V_{GS} = -4.5V, I_D = -2.2A$ ③
		P-Ch	—	—	0.140		$V_{GS} = -2.7V, I_D = -1.8A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-0.70	—	—		$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	N-Ch	8.30	—	—	S	$V_{DS} = 15V, I_D = 2.6A$ ③
		P-Ch	4.00	—	—		$V_{DS} = -15V, I_D = -2.2A$ ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 16V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -16V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100		$V_{GS} = \pm 12V$
Q_g	Total Gate Charge	N-Ch	—	—	20	nC	N-Channel $I_D = 2.6A, V_{DS} = 16V, V_{GS} = 4.5V$ ③
		P-Ch	—	—	22		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	—	2.2	nC	P-Channel $I_D = -2.2A, V_{DS} = -16V, V_{GS} = -4.5V$
		P-Ch	—	—	3.3		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	8.0	nC	
		P-Ch	—	—	9.0		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	9.0	—	ns	N-Channel $V_{DD} = 10V, I_D = 2.6A, R_G = 6.0\Omega, R_D = 3.8\Omega$ ③
		P-Ch	—	8.4	—		
t_r	Rise Time	N-Ch	—	42	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega, R_D = 4.5\Omega$ ③
		P-Ch	—	26	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	32	—	ns	
		P-Ch	—	51	—		
t_f	Fall Time	N-Ch	—	51	—	ns	
		P-Ch	—	33	—		
L_D	Internal Drain Inductance	N-P	—	4.0	—	nH	Between lead tip and center of die contact
L_S	Internal Source Inductance	N-P	—	6.0	—		
C_{iss}	Input Capacitance	N-Ch	—	660	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	610	—		
C_{oss}	Output Capacitance	N-Ch	—	280	—		
		P-Ch	—	310	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	140	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$
		P-Ch	—	170	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	2.5	A	
		P-Ch	—	—	-2.5		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	21		
		P-Ch	—	—	-17		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.0	V	$T_J = 25^{\circ}\text{C}, I_S = 1.8\text{A}, V_{GS} = 0\text{V}$ ③
		P-Ch	—	—	-1.0		$T_J = 25^{\circ}\text{C}, I_S = -1.8\text{A}, V_{GS} = 0\text{V}$ ③
t_{rr}	Reverse Recovery Time	N-Ch	—	29	44	ns	N-Channel $T_J = 25^{\circ}\text{C}, I_F = 2.6\text{A}, di/dt = 100\text{A}/\mu\text{s}$
		P-Ch	—	56	84		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	22	33	nC	
		P-Ch	—	71	110		
t_{on}	Forward Turn-On Time	N-P	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)
- ② N-Channel $I_{SD} \leq 2.6A, di/dt \leq 100A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
P-Channel $I_{SD} \leq -2.2A, di/dt \leq 50A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.



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N-Channel

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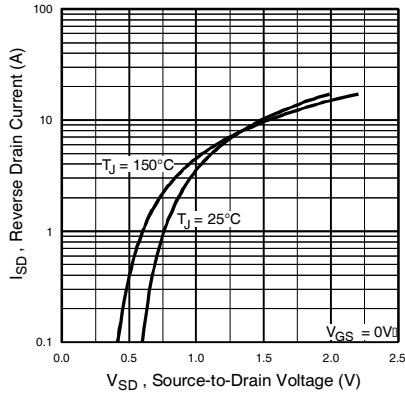


Fig 7. Typical Source-Drain Diode Forward Voltage

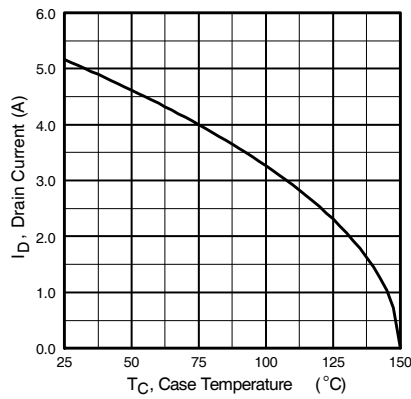


Fig 9. Maximum Drain Current Vs. Ambient Temperature

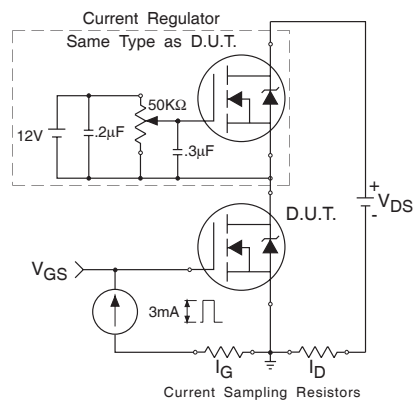


Fig 11a. Gate Charge Test Circuit

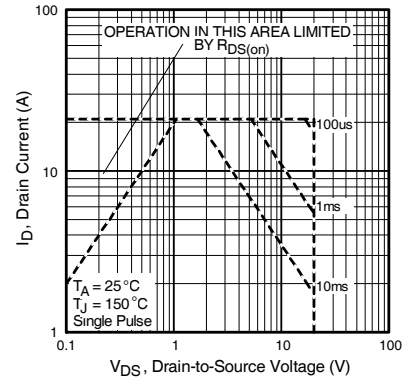


Fig 8. Maximum Safe Operating Area

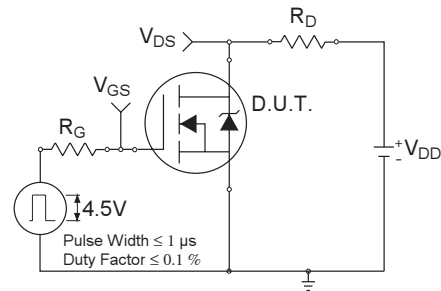


Fig 10a. Switching Time Test Circuit

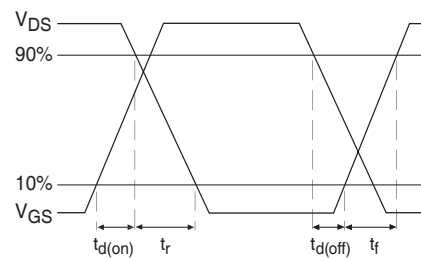


Fig 10b. Switching Time Waveforms

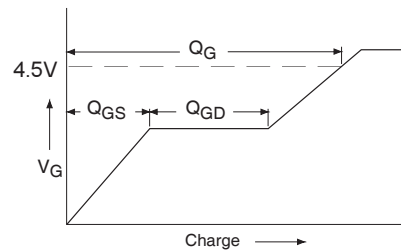
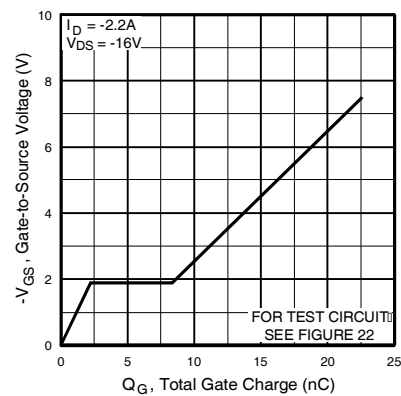
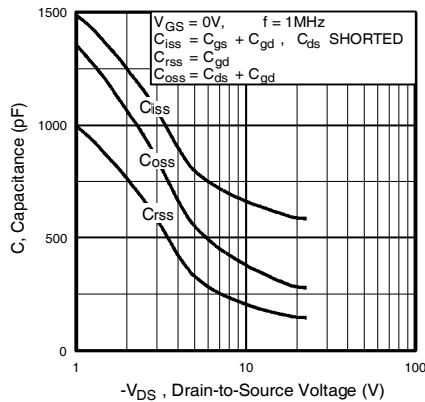
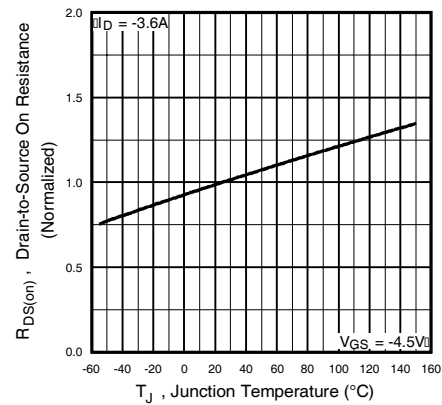
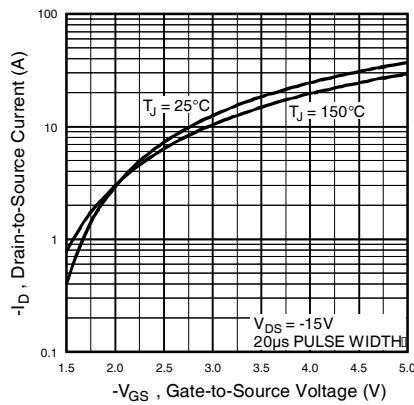
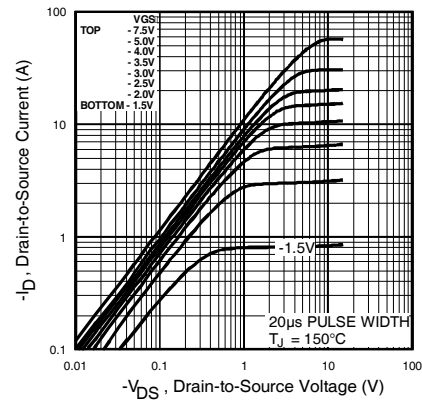
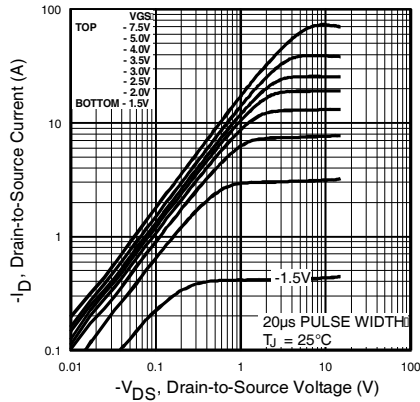


Fig 11b. Basic Gate Charge Waveform



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P-Channel

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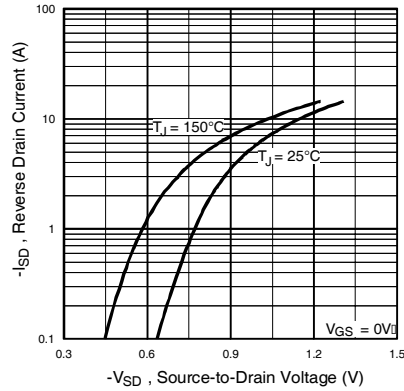


Fig 18. Typical Source-Drain Diode Forward Voltage

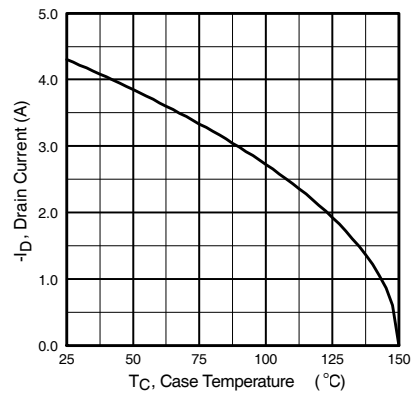


Fig 20. Maximum Drain Current Vs. Ambient Temperature

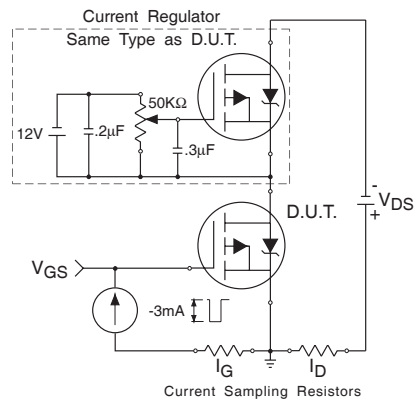


Fig 22a. Gate Charge Test Circuit

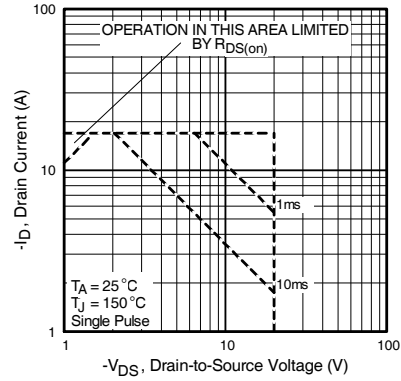


Fig 19. Maximum Safe Operating Area

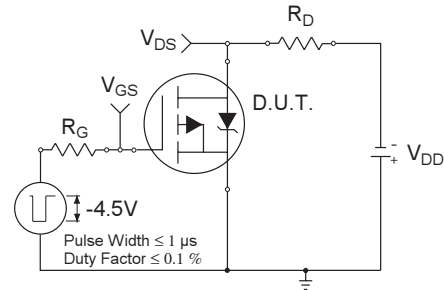


Fig 21a. Switching Time Test Circuit

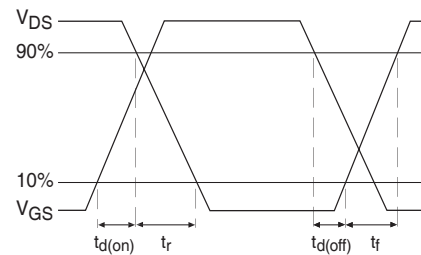


Fig 21b. Switching Time Waveforms

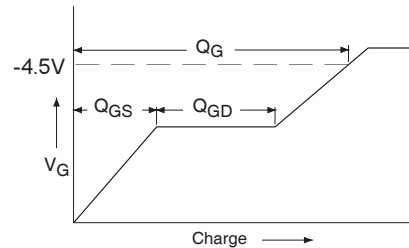


Fig 22b. Basic Gate Charge Waveform

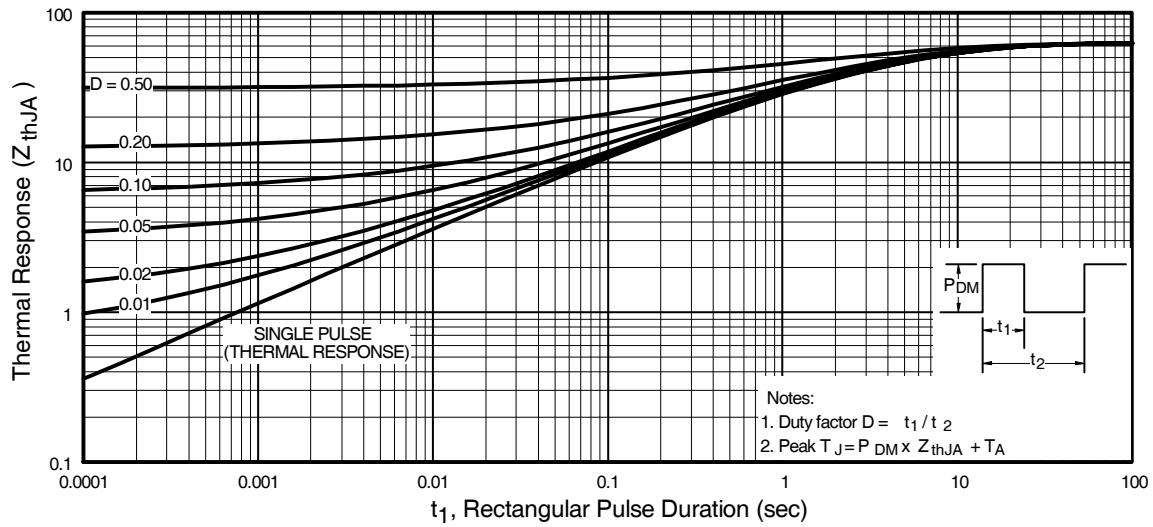
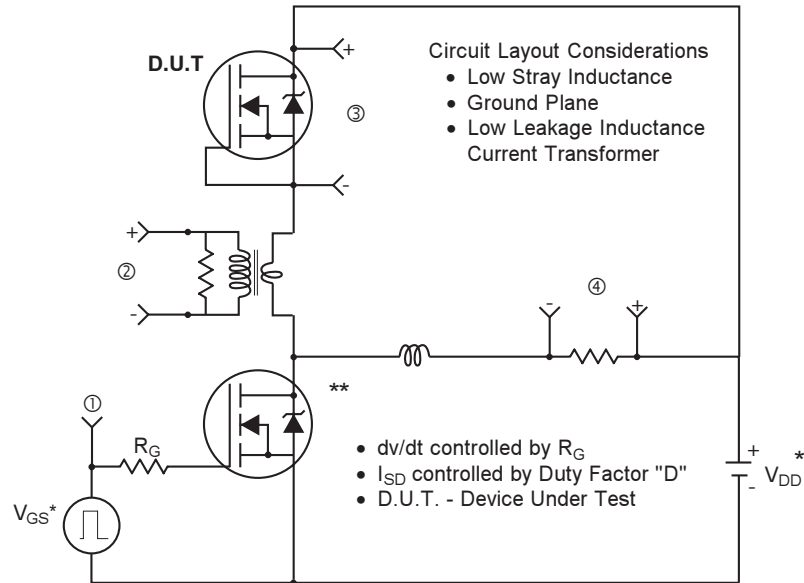


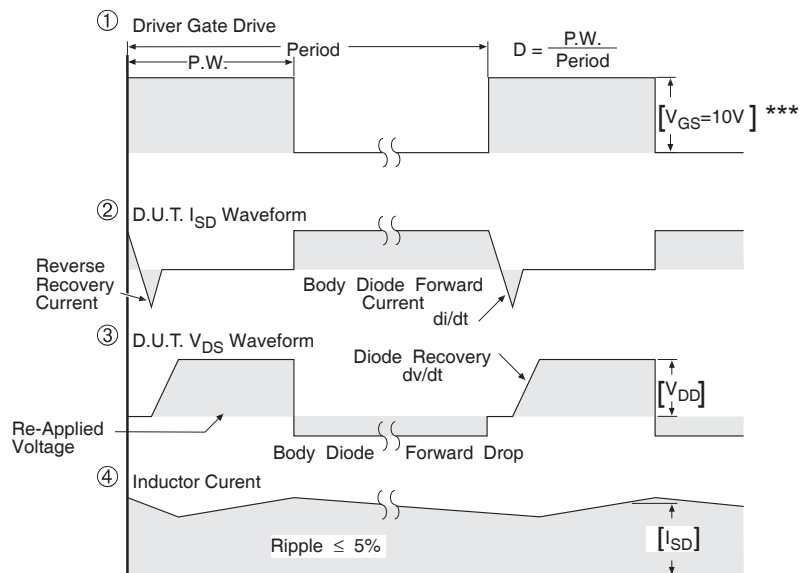
Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements

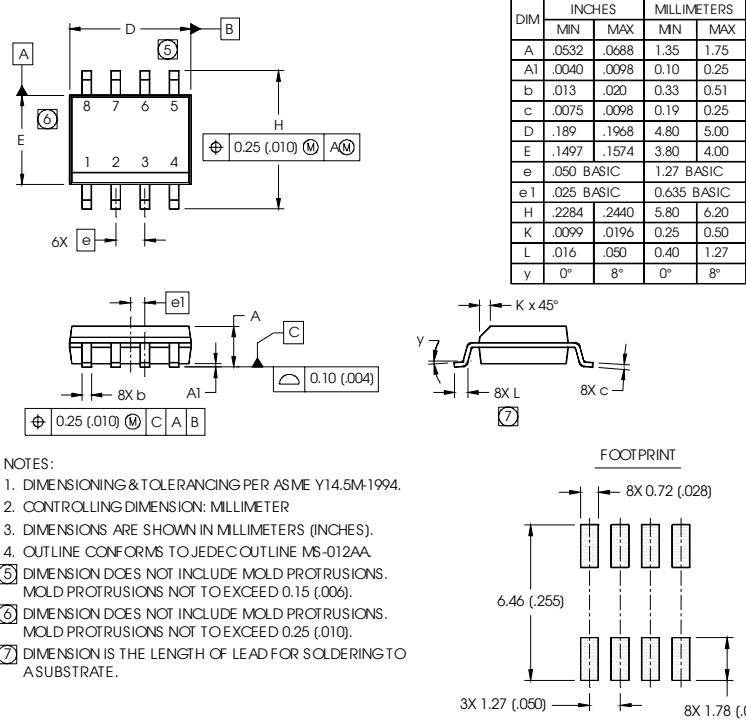


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 24. For N and P Channel HEXFETS

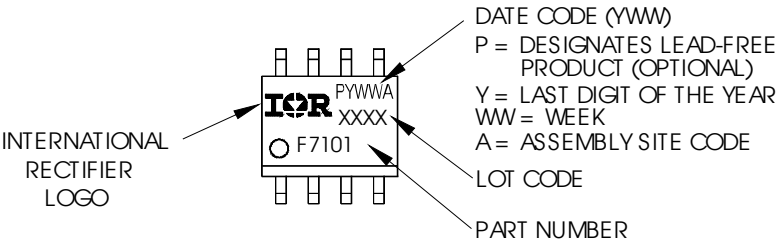
SO-8 Package Outline

Dimensions are shown in millimeters (inches)



SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

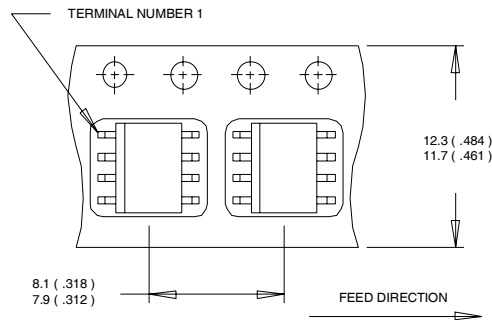


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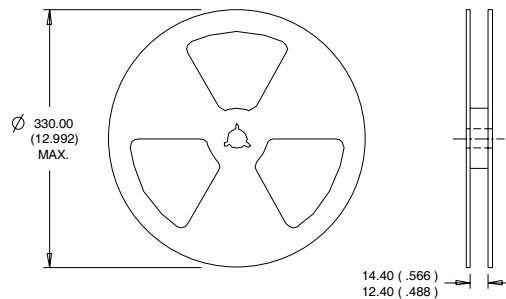
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SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

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