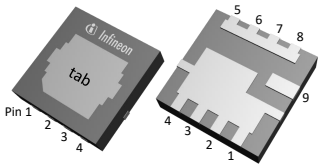
# MOSFET

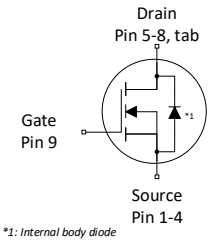
PG-WHTFN-9 (3x3)

## OptiMOS™ 7 Power-Transistor, 25 V




## Features

- N-channel, logic level
- Optimized for hard-switching topologies
- Optimized for best $FOM_{oss}$
- Excellent Miller ratio for dv/dt ruggedness
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance, dual side cooling feature
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

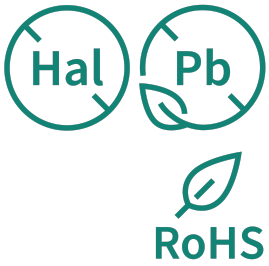



## Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

**Table 1 Key performance parameters**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 25 | V |
| $R_{DS(on),max}$ | 0.5 | mΩ |
| $I_D$ | 422 | A |
| $Q_{oss}$ | 38 | nC |
| $Q_G$ (0V...10V) | 57 | nC |




| Part number | Package | Marking | Related links |
|---|---|---|---|
| IQEH50NE2LM7UCGSC | PG-WHTFN-9 | B | - |

# Table of contents

# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current [1] | $I_D$ | - | - | 422 | A | $V_{GS}$=10 V, $T_C$=25 °C |
| | | | | 298 | | $V_{GS}$=10 V, $T_C$=100 °C |
| | | | | 236 | | $V_{GS}$=4.5 V, $T_C$=100 °C |
| | | | | 54 | | $V_{GS}$=10 V, $T_A$=25 °C, $R_{thJA}$=60 °C/W [2] |
| Pulsed drain current [3] | $I_{D,pulse}$ | - | - | 1688 | A | $T_C$=25 °C |
| Avalanche energy, single pulse [4] | $E_{AS}$ | - | - | 340 | mJ | $I_D$=20 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -16 | - | 16 | V | - |
| Power dissipation | $P_{tot}$ | - | - | 150 | W | $T_C$=25 °C |
| | | | | 2.5 | | $T_A$=25 °C, $R_{thJA}$=60 °C/W [2] |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 175 | °C | - |

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm$^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

# 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case, bottom | $R_{thJC}$ | - | - | 1.0 | °C/W | - |
| Thermal resistance, junction - case, top | $R_{thJC}$ | | 0.7 | - | | |
| Thermal resistance, junction - ambient, 6 cm² cooling area [5] | $R_{thJA}$ | | - | 60 | | |

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm$^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

# 3 Electrical characteristics

at $T_j$=25 °C, unless otherwise specified

**Table 4 Static characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 25 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 1.4 | 1.7 | 2.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=432 µA |
| Zero gate voltage drain current | $I_{DSS}$ | - | 0.1 | 1 | µA | $V_{DS}$=22 V, $V_{GS}$=0 V, $T_j$=25 °C |
| | | | 10 | 100 | | $V_{DS}$=22 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 10 | 100 | nA | $V_{GS}$=16 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.45 | 0.5 | mΩ | $V_{GS}$=10 V, $I_D$=20 A |
| | | | 0.66 | 0.8 | | $V_{GS}$=4.5 V, $I_D$=20 A |
| Gate resistance | $R_G$ | - | 0.75 | - | Ω | - |
| Transconductance | $g_{fs}$ | 55 | 110 | - | S | $\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, $I_D$=20 A |

**Table 5 Dynamic characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 4700 | 6100 | pF | $V_{GS}$=0 V, $V_{DS}$=12 V, $f$=1 MHz |
| Output capacitance | $C_{oss}$ | | 1800 | - | | |
| Reverse transfer capacitance | $C_{rss}$ | | 81 | - | | |
| Turn-on delay time | $t_{d(on)}$ | - | 7.0 | - | ns | $V_{DD}$=12 V, $V_{GS}$=10 V, $I_D$=20 A, $R_{G,ext}$=3 Ω |
| Rise time | $t_r$ | | 2.0 | | | |
| Turn-off delay time | $t_{d(off)}$ | | 29 | | | |
| Fall time | $t_f$ | | 4.4 | | | |

**Table 6 Gate charge characteristics** [6)]

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 13.3 | - | nC | $V_{DD}$=12 V, $I_D$=20 A, $V_{GS}$=0 to 4.5 V |
| Gate charge at threshold | $Q_{g(th)}$ | | 8.1 | | nC | |
| Gate to drain charge | $Q_{gd}$ | | 4.2 | | nC | |
| Switching charge | $Q_{sw}$ | | 9.4 | | nC | |
| Gate charge total | $Q_g$ | | 27 | | nC | |
| Gate plateau voltage | $V_{plateau}$ | | 2.8 | | V | |
| Gate charge total | $Q_g$ | - | 57 | - | nC | $V_{DD}$=12 V, $I_D$=20 A, $V_{GS}$=0 to 10 V |
| Output charge | $Q_{oss}$ | - | 38 | - | nC | $V_{DS}$=12 V, $V_{GS}$=0 V |

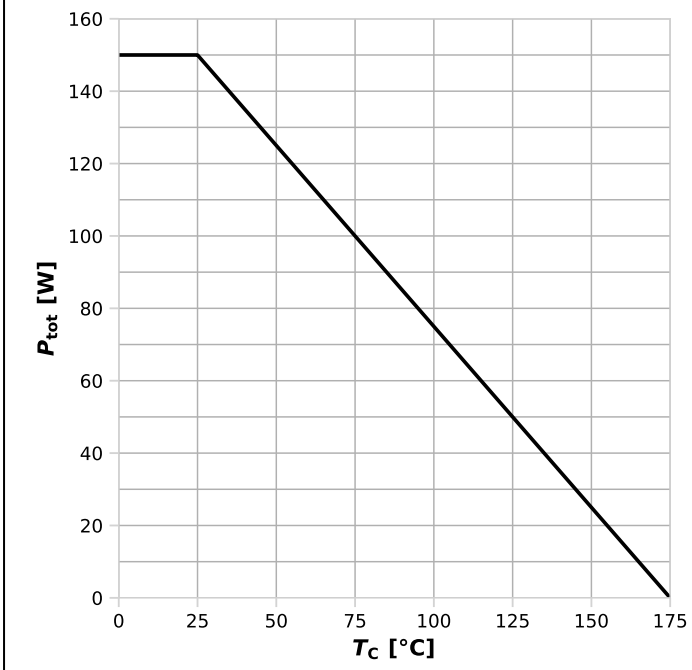
[6)] See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | 138 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | | | 1688 | | |
| Diode forward voltage | $V_{SD}$ | - | 0.76 | 1.0 | V | $V_{GS}$=0 V, $I_F$=20 A, $T_j$=25 °C |
| Reverse recovery time | $t_{rr}$ | - | 25 | - | ns | $V_R$=12 V, $I_F$=20 A, d$i_F$/d$t$=400 A/µs |
| Reverse recovery charge | $Q_{rr}$ | | 88 | | nC | |

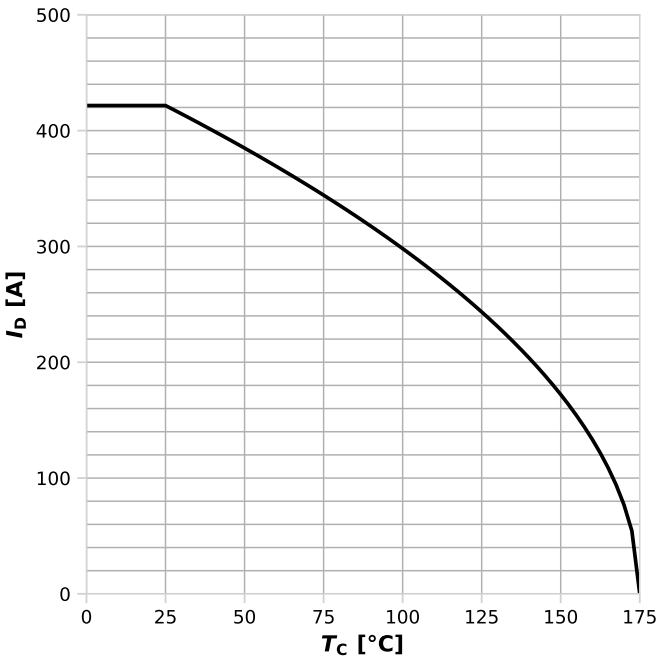
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



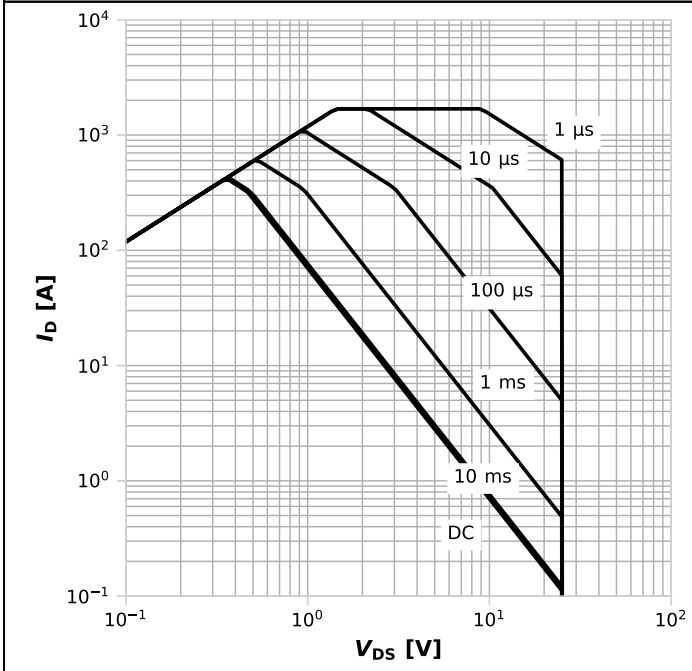

$P_{tot}$=f($T_C$)

**Diagram 2: Drain current**



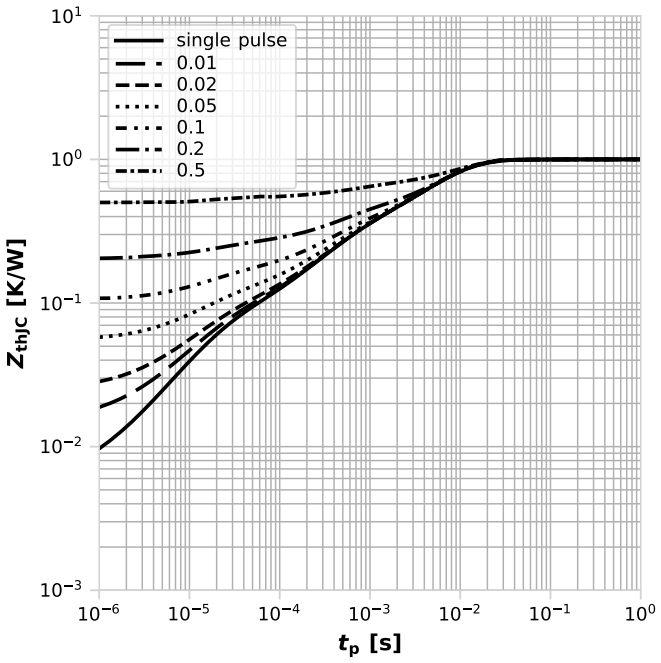

$I_D$=f($T_C$); $V_{GS}$≥10 V

**Diagram 3: Safe operating area**



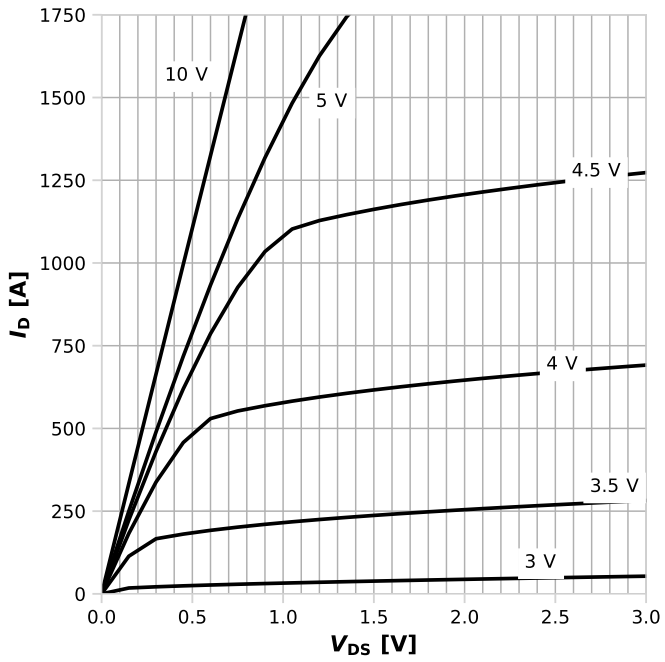

$I_D$=f($V_{DS}$); $T_C$=25 °C; $D$=0; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



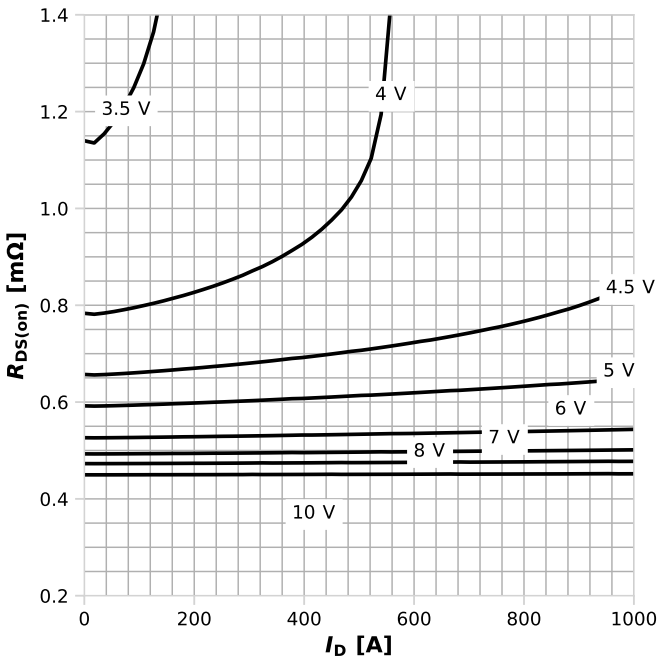

$Z_{thJC}$=f($t_p$); parameter: $D$=$t_p$/$T$

**Diagram 5: Typ. output characteristics**



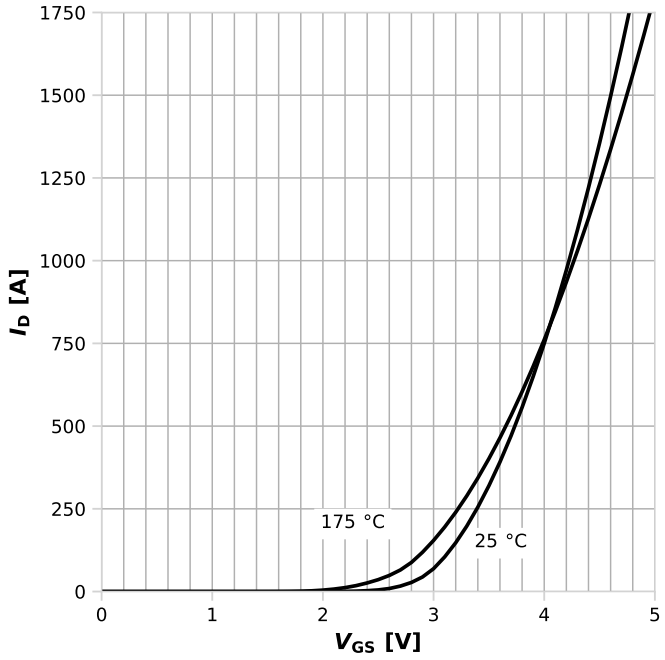

$I_D$=f($V_{DS}$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



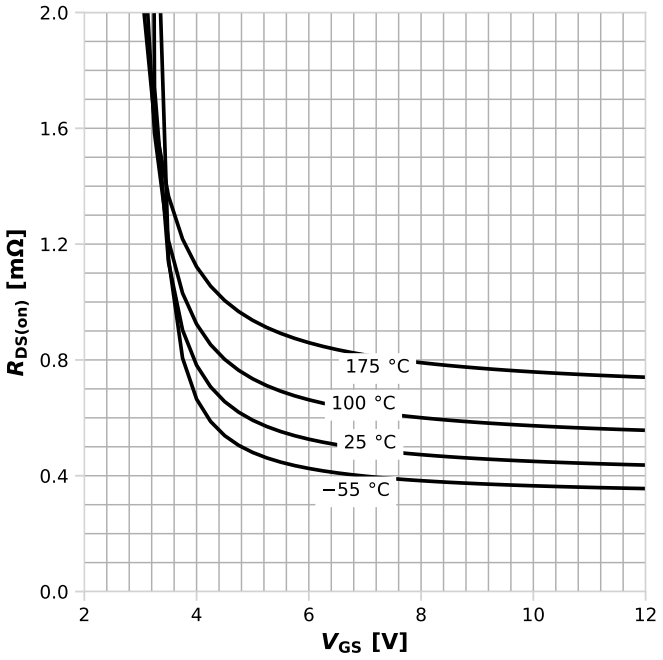

$R_{DS(on)}$=f($I_D$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



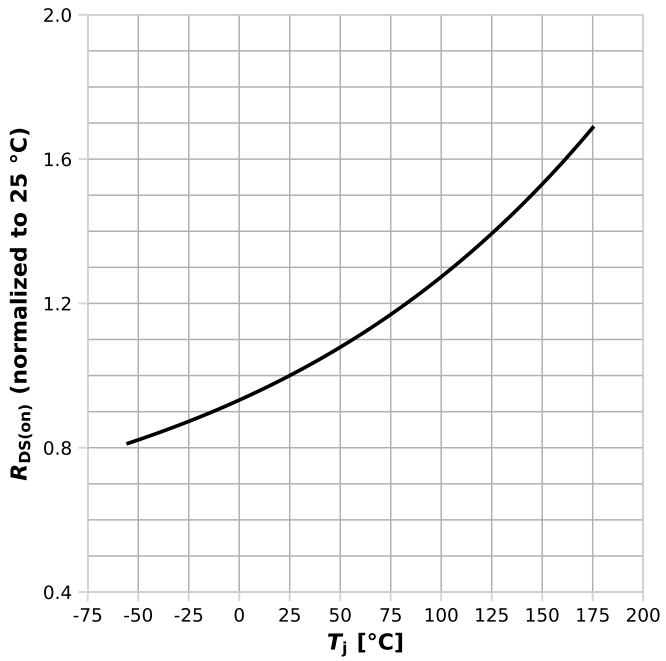

$I_D$=f($V_{GS}$), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. drain-source on resistance**



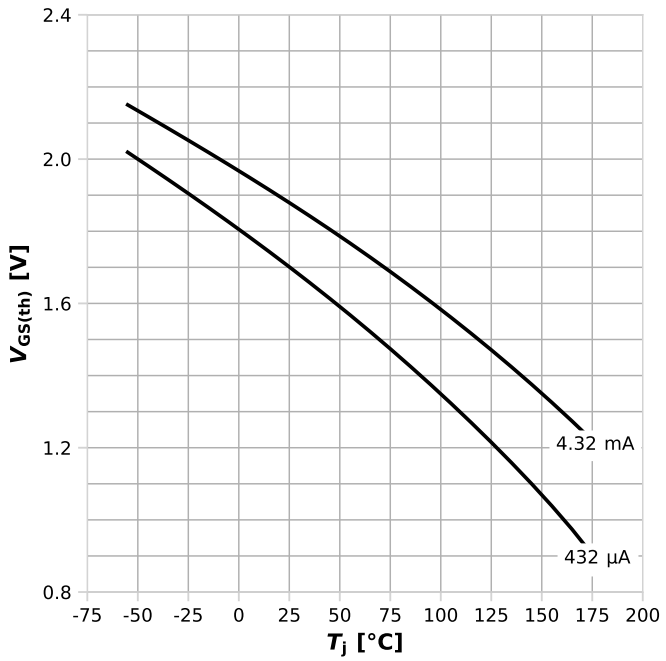

$R_{DS(on)}$=f($V_{GS}$), $I_D$=20 A; parameter: $T_j$

**Diagram 9: Normalized drain-source on resistance**



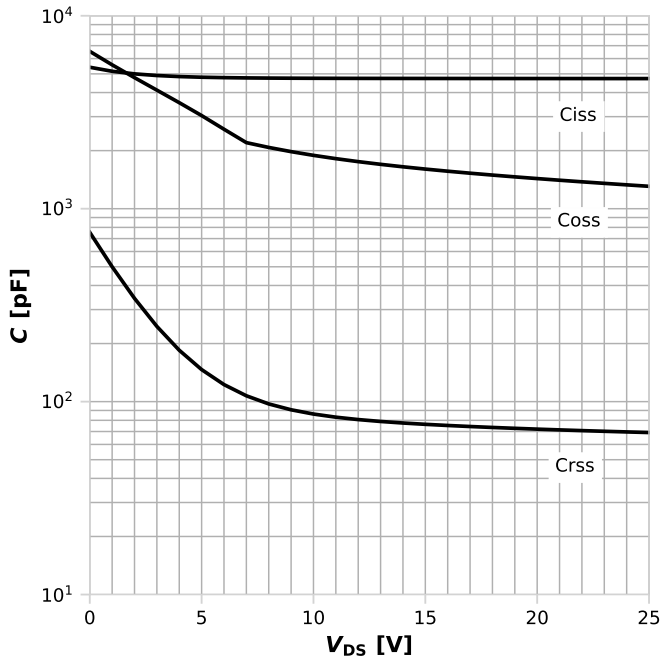

$R_{DS(on)}$=f($T_j$), $I_D$=20 A, $V_{GS}$=10 V

**Diagram 10: Typ. gate threshold voltage**



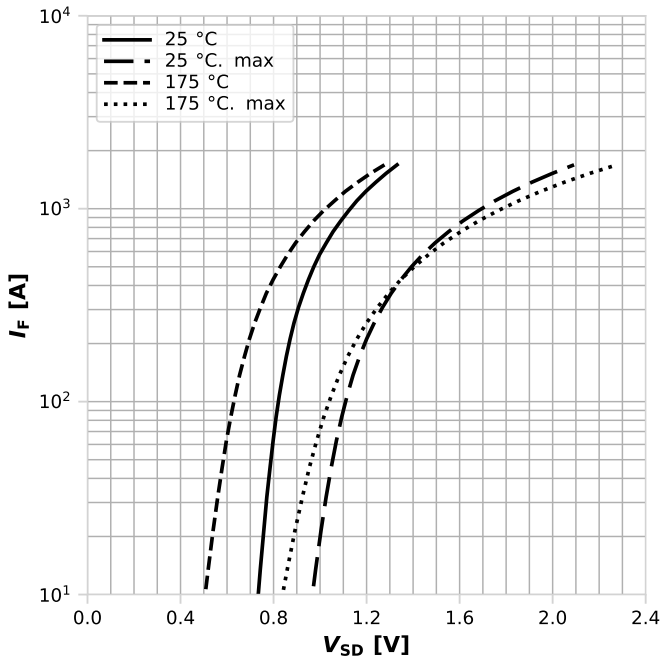

$V_{GS(th}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 11: Typ. capacitances**

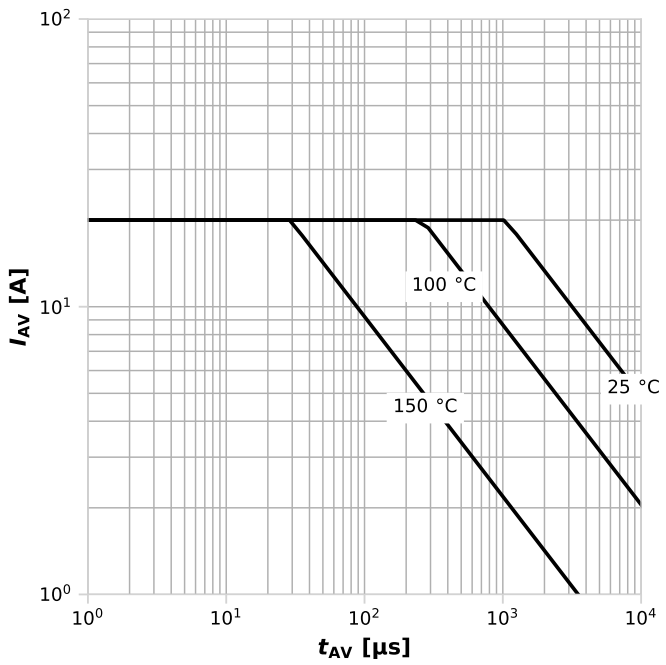
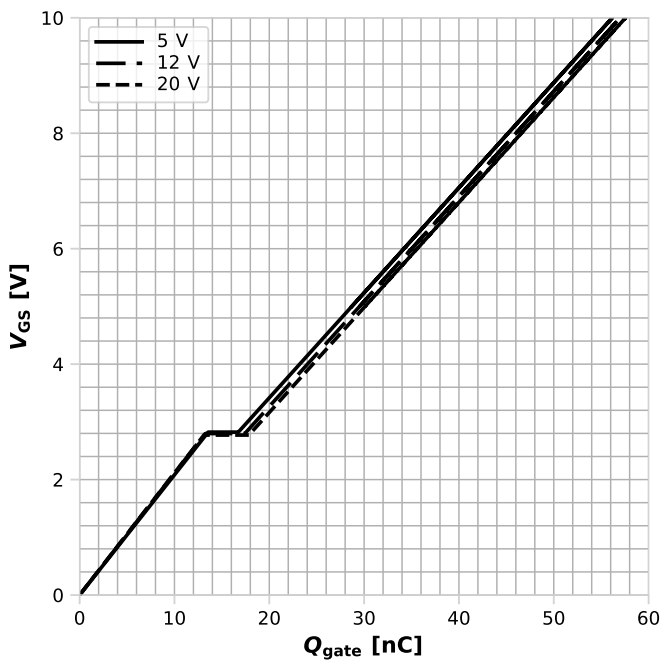


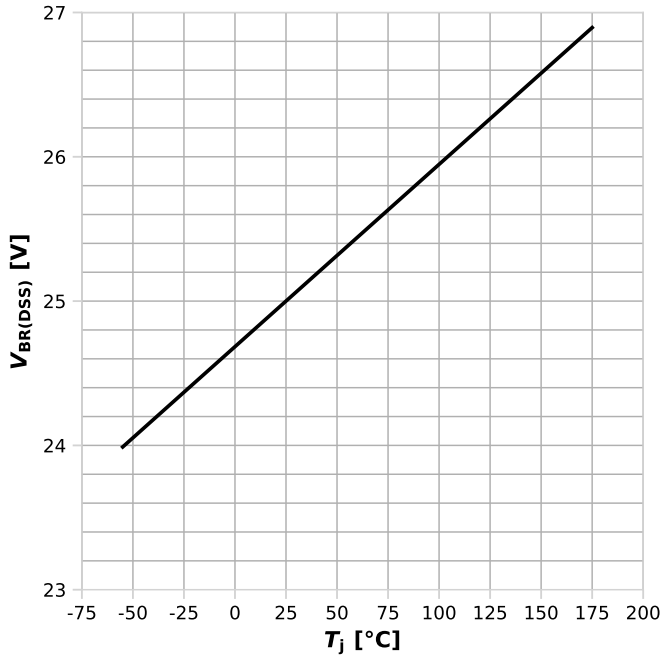
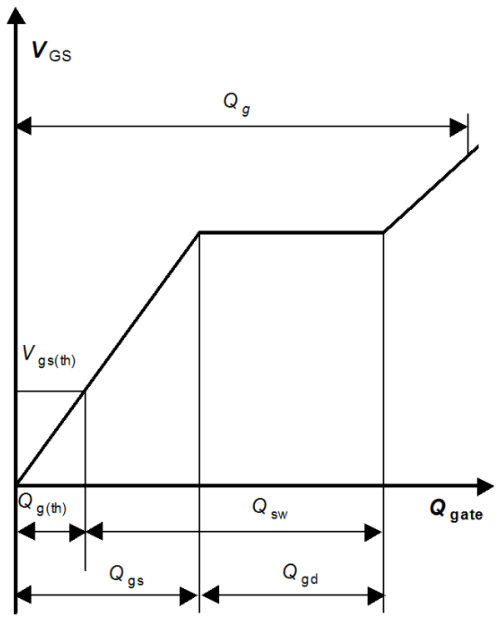

$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Forward characteristics of reverse diode**

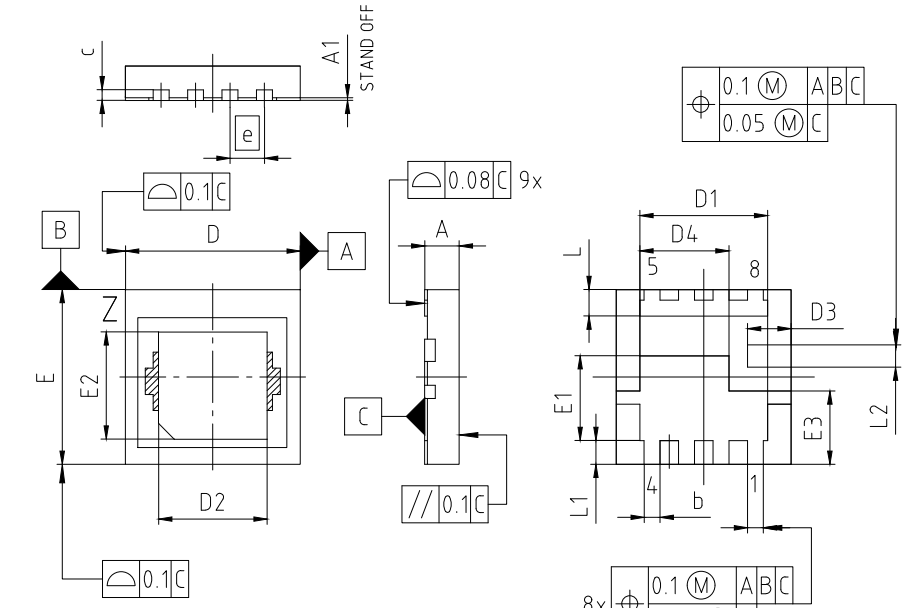



$I_F$=f($V_{SD}$); parameter: $T_j$

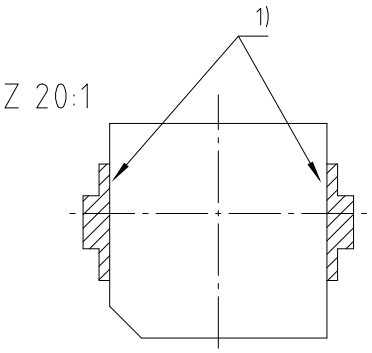
| Diagram 13: Avalanche characteristics | Diagram 14: Typ. gate charge |
|---|---|
|  |  |
| $I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j,start}$ | $V_{GS}$=f($Q_{gate}$), $I_D$=20 A pulsed, $T_j$=25 °C; parameter: $V_{DD}$ |

| Diagram 15: Min. drain-source breakdown voltage | Gate charge waveforms |
|---|---|
|  |  |
| $V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA | - |

# 5 Package outlines




| PACKAGE - GROUP NUMBER: | PG-WHTFN-9-U01 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 0.55 | 0.75 |
| A1 | 0 | 0.05 |
| b | 0.20 | 0.40 |
| c | 0.10 | 0.30 |
| D | 3.20 | 3.40 |
| D1 | 2.31 | 2.51 |
| D2 | 1.95 | 2.25 |
| D3 | 0.73 | 0.93 |
| D4 | 1.58 | 1.78 |
| E | 3.20 | 3.40 |
| E1 | 1.50 | 1.70 |
| E2 | 1.93 | 2.23 |
| E3 | 1.285 | 1.485 |
| e | 0.65 | |
| L | 0.40 | 0.60 |
| L1 | 0.35 | 0.55 |
| L2 | 0.32 | 0.52 |




1) NOT PART OF SPECIFIED HEATSINK AREA -
SHAPE MIGHT VARY DEPENDING ON HEATSINK DESIGN

**Figure 1 Outline PG-WHTFN-9, dimensions in mm**

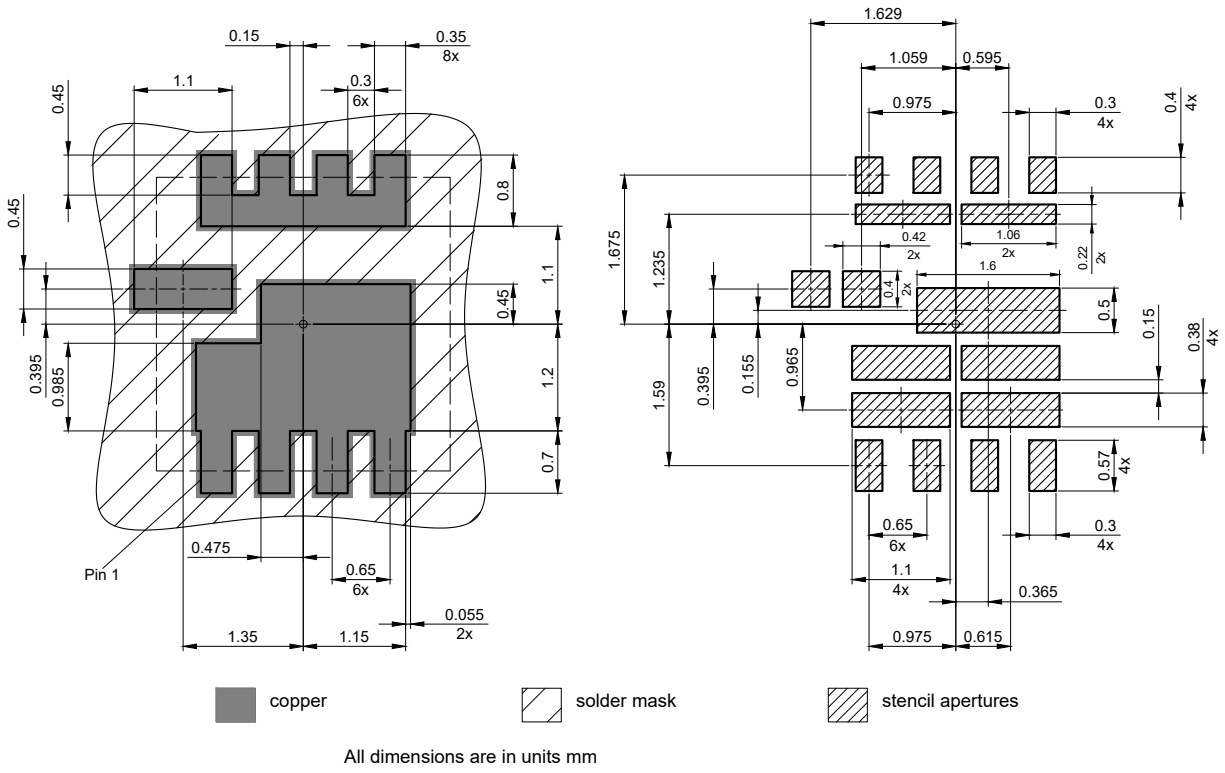



**Figure 2 Footprint drawing PG-WHTFN-9, dimensions in mm**

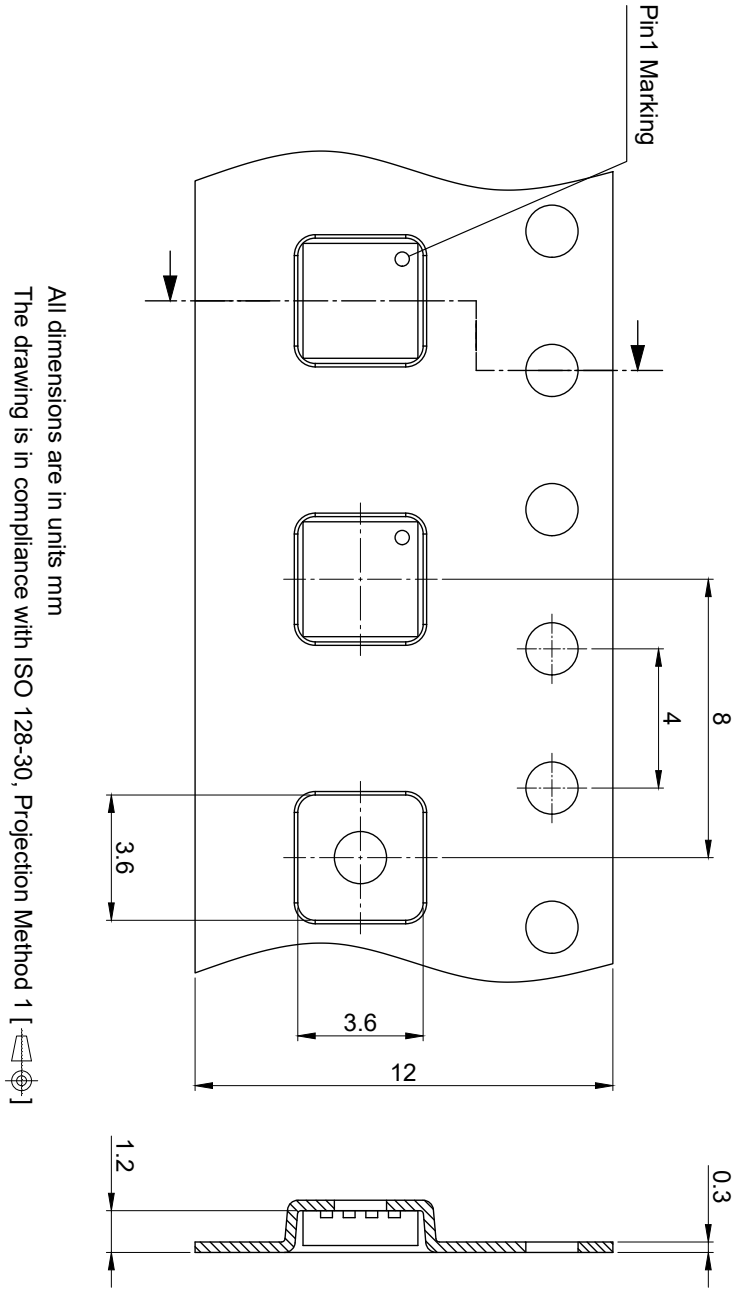



**Figure 3 Packaging variant PG-WHTFN-9, dimensions in mm**

## Revision history

IQEH50NE2LM7UCGSC

### Revision 2025-08-05, Rev. 1.0

Previous revisions

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 1.0 | 2025-08-05 | Release of final datasheet |

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