MOSFET

600V CoolMOS™ CFD7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions. Altogether, CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter and cooler.

Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di_F/dt ruggedness
- Lowest FOM $R_{DS(on)}$*Q_g and $R_{DS(on)}$*E_{oss}
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions

Potential applications

Suiteable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

Product Validation: Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	170	mΩ
$Q_{g,typ}$	28	nC
$I_{D,pulse}$	51	A
E_{oss} @ 400V	3.2	µJ
Body diode di_F/dt	1300	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPP60R170CFD7	PG-TO 220-3	60R170F7	see Appendix A

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1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	14 9	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	51	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	60	mJ	I_D=3.7A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.30	mJ	I_D=3.7A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	3.7	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	75	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	14	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	51	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	70	V/ns	V_{DS}=0...400V, I_{SD}<=14A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt	-	-	1300	A/µs	V_{DS}=0...400V, I_{SD}<=14A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j,max}$.
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.67	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	V_{DS}=V_{GS}, I_D=0.3mA
Zero gate voltage drain current[1]	I_{DSS}	- -	- 7	1 37	µA	V_{DS}=600V, V_{GS}=0V, T_j=25°C V_{DS}=600V, V_{GS}=0V, T_j=125°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.144 0.328	0.17 -	Ω	V_{GS}=10V, I_D=6.0A, T_j=25°C V_{GS}=10V, I_D=6.0A, T_j=150°C
Gate resistance	R_G	-	10.9	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1199	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	22	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[2]	$C_{o(er)}$	-	40	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[3]	$C_{o(tr)}$	-	402	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	31	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=7.0A, R_G=10.2Ω; see table 9
Rise time	t_r	-	15	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=7.0A, R_G=10.2Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	68	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=7.0A, R_G=10.2Ω; see table 9
Fall time	t_f	-	9	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=7.0A, R_G=10.2Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7	-	nC	V_{DD}=400V, I_D=7.0A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	9	-	nC	V_{DD}=400V, I_D=7.0A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	28	-	nC	V_{DD}=400V, I_D=7.0A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=400V, I_D=7.0A, V_{GS}=0 to 10V

[1] Maximum specification is defined by calculated six sigma upper confidence bound
[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	V_{GS}=0V, I_F=6.0A, T_j=25°C
Reverse recovery time	t_{rr}	-	89	134	ns	V_R=400V, I_F=7A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	0.34	0.68	µC	V_R=400V, I_F=7A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	6.8	-	A	V_R=400V, I_F=7A, di_F/dt=100A/µs; see table 8

4 Electrical characteristics diagrams

Diagram 1: Power dissipation

P_{tot}=f(T_C)

Diagram 2: Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area

I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance

Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics

I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance

$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=6.0 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics

I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=7.0 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode

I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy

E_{AS}=f(T_j); I_D=3.7 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances

C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy

E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform

Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

6 Package Outlines

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

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SCALE 0 2.5 0 2.5 5mm

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Figure 1 Outline PG-TO 220-3, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS CFD7 Webpage:** www.infineon.com
- **IFX CoolMOS CFD7 application note:** www.infineon.com
- **IFX CoolMOS CFD7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPP60R170CFD7

Revision: 2018-01-18, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-08-25	Release of final version
2.1	2018-01-18	Raised diode current for dv/dt and dif/dt (table 2) to value of continuous drain current; Changed internal Rg (table 4); Renamed related links (table 11)

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