

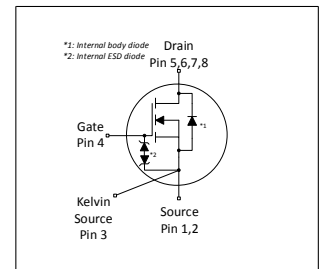
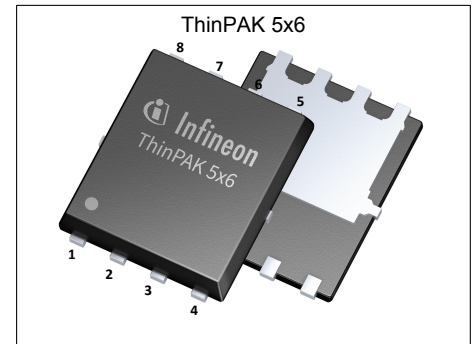
MOSFET

600V CoolMOS™ PFD7 SJ Power Device

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

The latest CoolMOS™ PFD7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, motor drive, lighting, etc.

The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.



Features

- Extremely low losses due to very low FOM $R_{DS(on)} * Q_g$ and $R_{DS(on)} * E_{oss}$
- Low switching losses E_{oss} , excellent thermal behavior
- Fast body diode
- Wide range portfolio of $R_{DS(on)}$ and package variations
- Integrated zener diode

Benefits

- Enables high power density designs and small form factors
- Enables efficiency gains at higher switching frequencies
- Excellent commutation ruggedness
- Easy to select right parts and optimize the design
- High ESD ruggedness

Potential applications

Recommended for ZVS topologies used in high density chargers, adapters, lighting and motor drives applications, etc.

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	600	mΩ
$Q_{g,typ}$	8.5	nC
$I_{D,pulse}$	14	A
$E_{oss} @ 400V$	1.1	μJ
Body diode di_f/dt	1300	A/μs
ESD Class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPLK60R600PFD7	ThinPAK 5x6 SMD	60R600D7	see Appendix A



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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	7 5	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	14	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	17	mJ	$I_D=1.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.08	mJ	$I_D=1.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	1.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	45	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current ¹⁾	I_S	-	-	7	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	14	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 5.6\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di _F /dt	-	-	1300	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 5.6\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_θ

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.80	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	62	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=0.08mA$
Zero gate voltage drain current ¹⁾	I_{DSS}	-	-	1 37	μA	$V_{DS}=600V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=600V, V_{GS}=0V, T_j=125^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	1000	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.517 1.216	0.600 -	Ω	$V_{GS}=10V, I_D=1.7A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=1.7A, T_j=150^\circ\text{C}$
Gate resistance	R_G	-	11.0	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	344	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Output capacitance	C_{oss}	-	8	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Effective output capacitance, energy related ²⁾	$C_{o(er)}$	-	13	-	pF	$V_{GS}=0V, V_{DS}=0\dots400V$
Effective output capacitance, time related ³⁾	$C_{o(tr)}$	-	120	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots400V$
Turn-on delay time	$t_{d(on)}$	-	9.2	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=1.7A,$ $R_G=10.2\Omega$; see table 9
Rise time	t_r	-	10	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=1.7A,$ $R_G=10.2\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	43.5	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=1.7A,$ $R_G=10.2\Omega$; see table 9
Fall time	t_f	-	23	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=1.7A,$ $R_G=10.2\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	2.0	-	nC	$V_{DD}=400V, I_D=1.7A, V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	3.0	-	nC	$V_{DD}=400V, I_D=1.7A, V_{GS}=0$ to 10V
Gate charge total	Q_g	-	8.5	-	nC	$V_{DD}=400V, I_D=1.7A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.6	-	V	$V_{DD}=400V, I_D=1.7A, V_{GS}=0$ to 10V

¹⁾ Maximum specification is defined by calculated six sigma upper confidence bound

²⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

³⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	$V_{GS}=0V, I_F=1.7A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	47	71	ns	$V_R=400V, I_F=1.7A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.10	0.20	μC	$V_R=400V, I_F=1.7A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	3.8	-	A	$V_R=400V, I_F=1.7A, di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

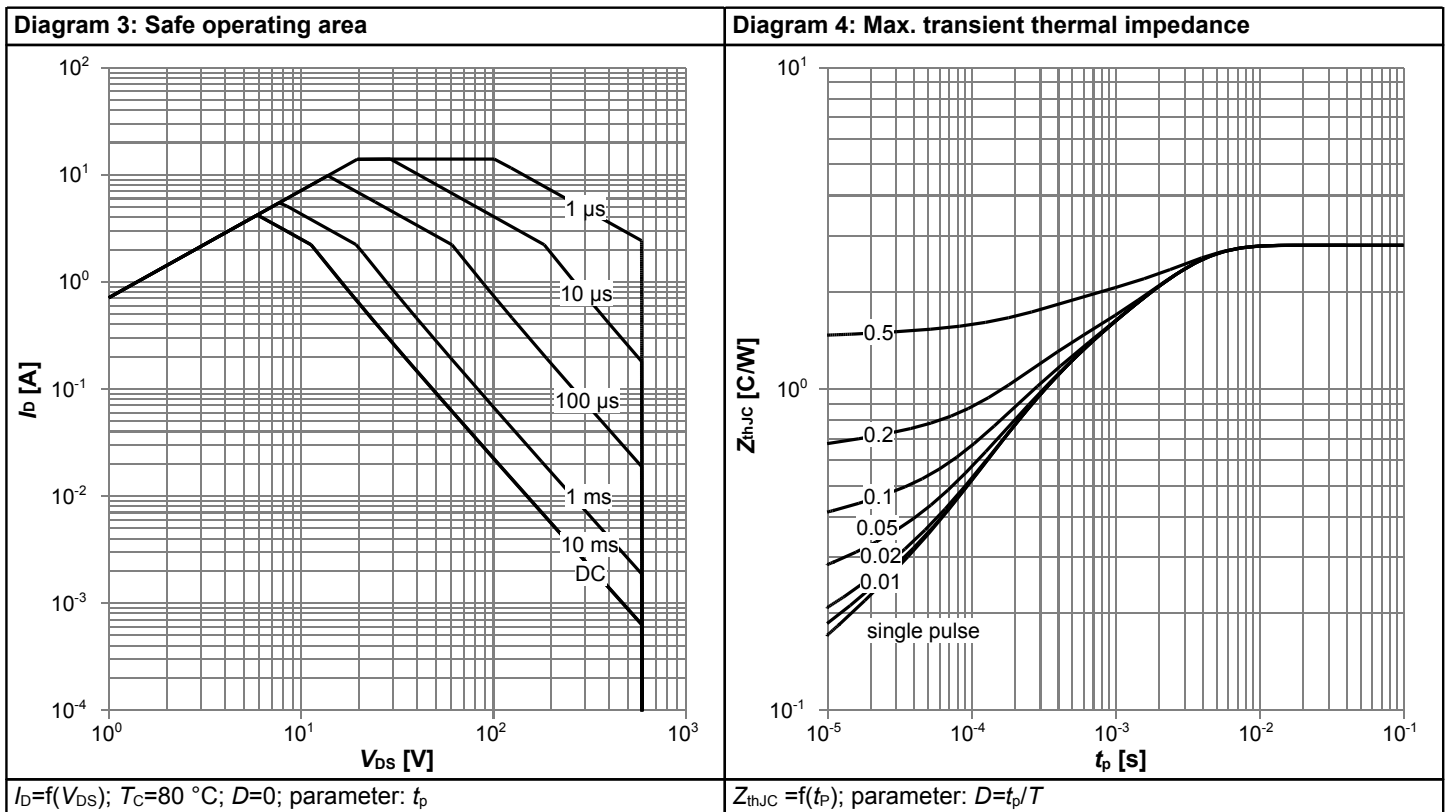
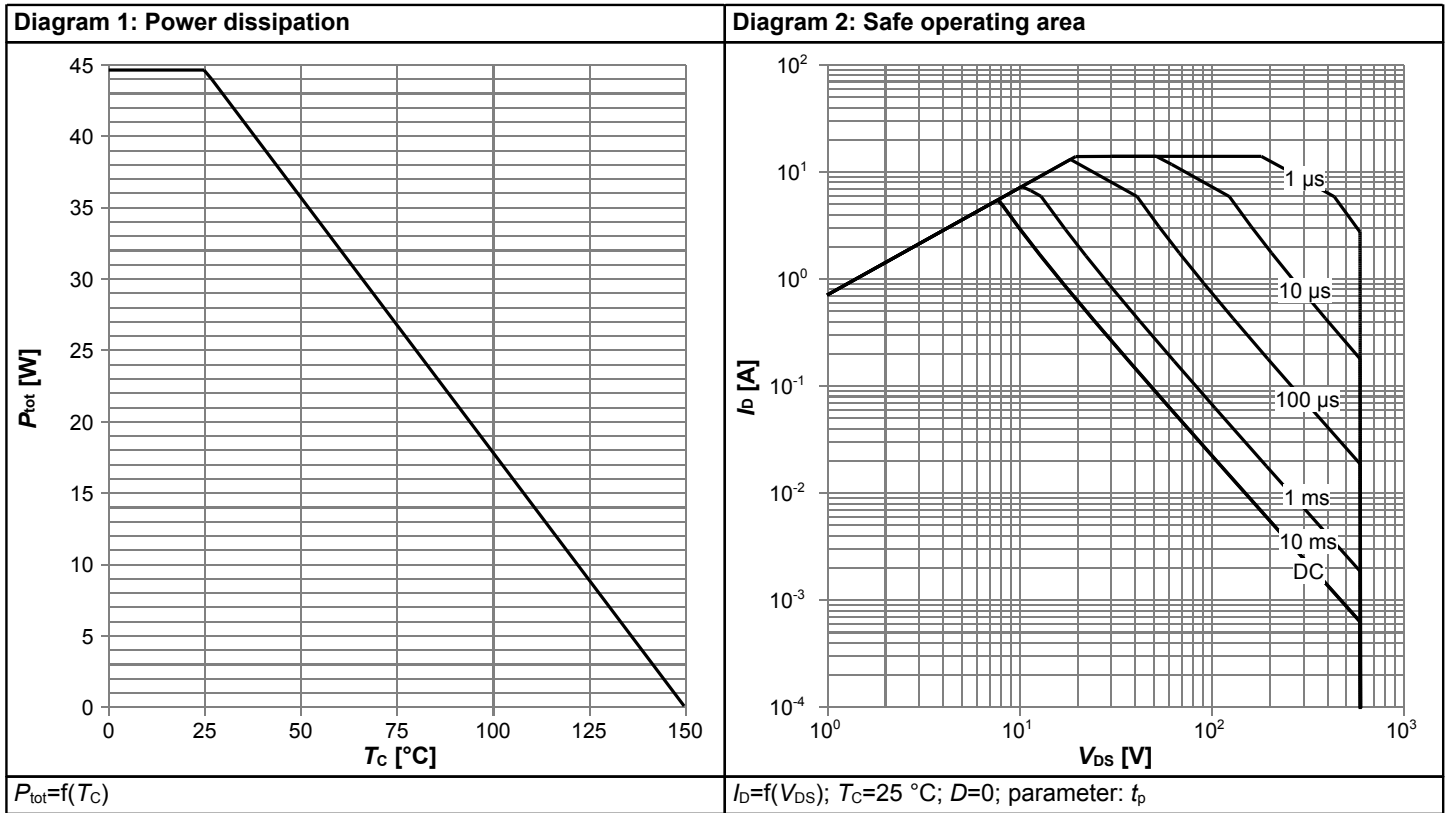
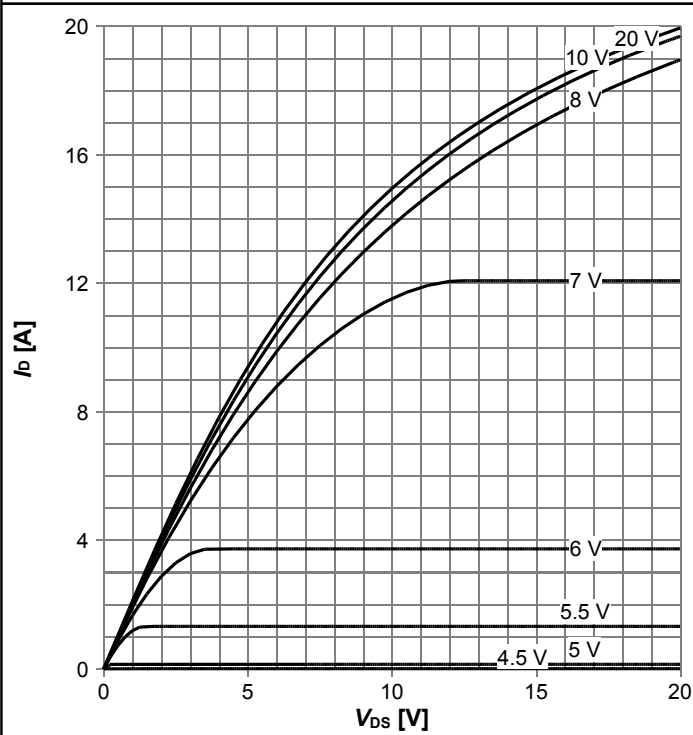
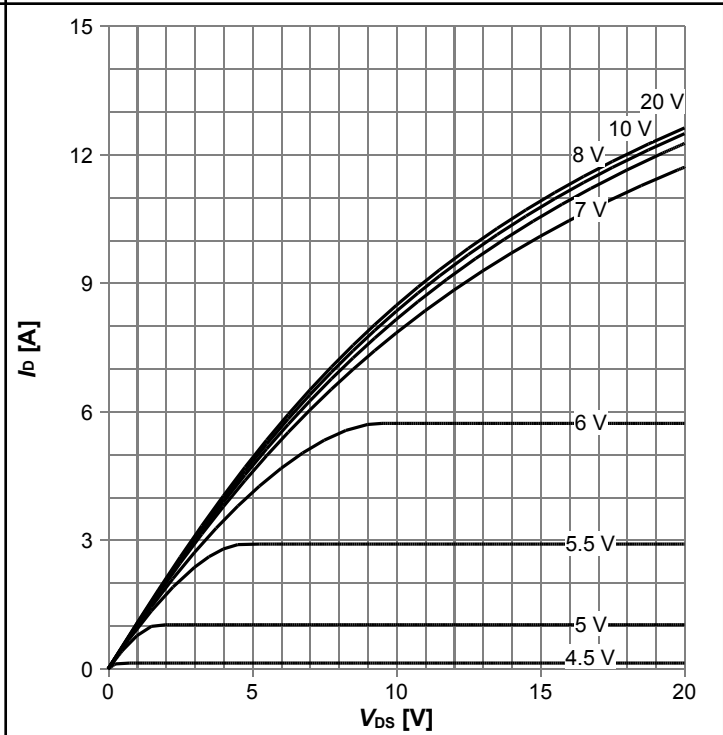


Diagram 5: Typ. output characteristics



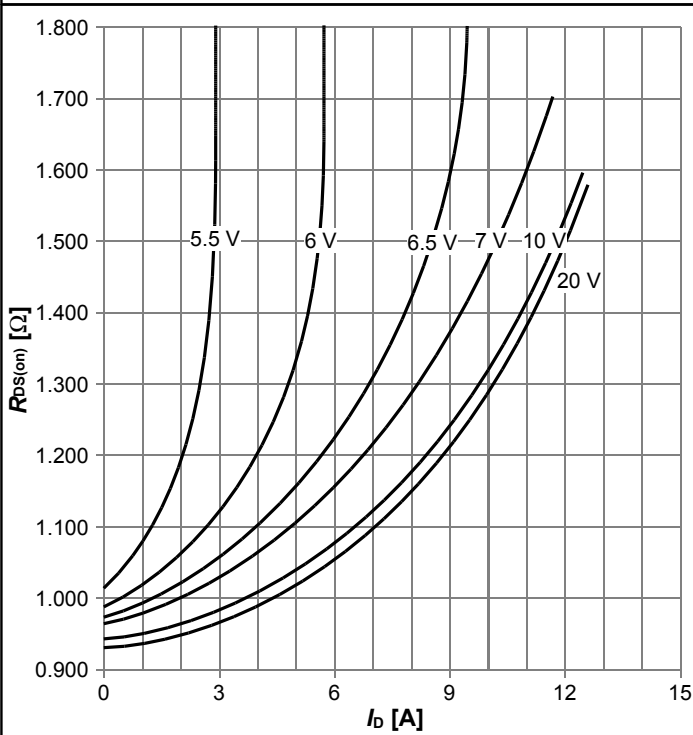
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



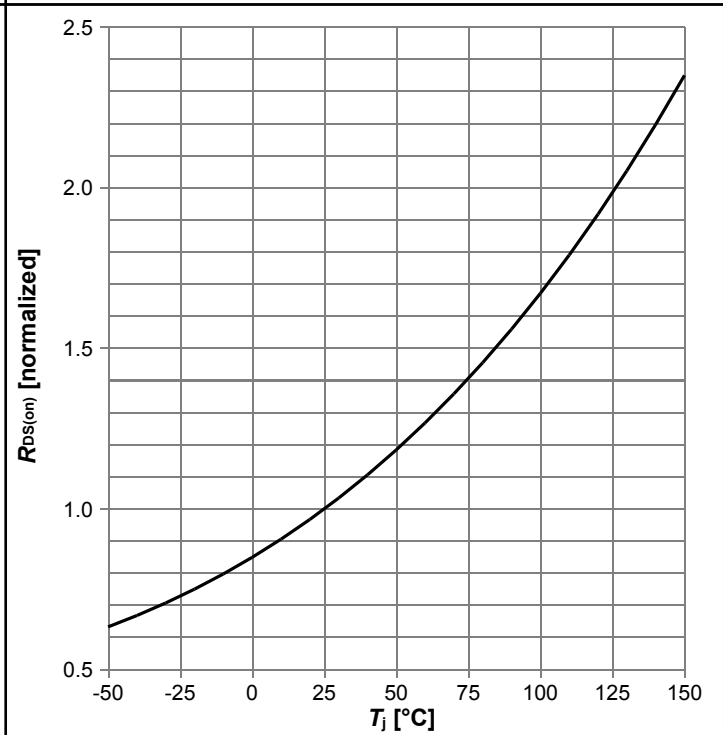
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



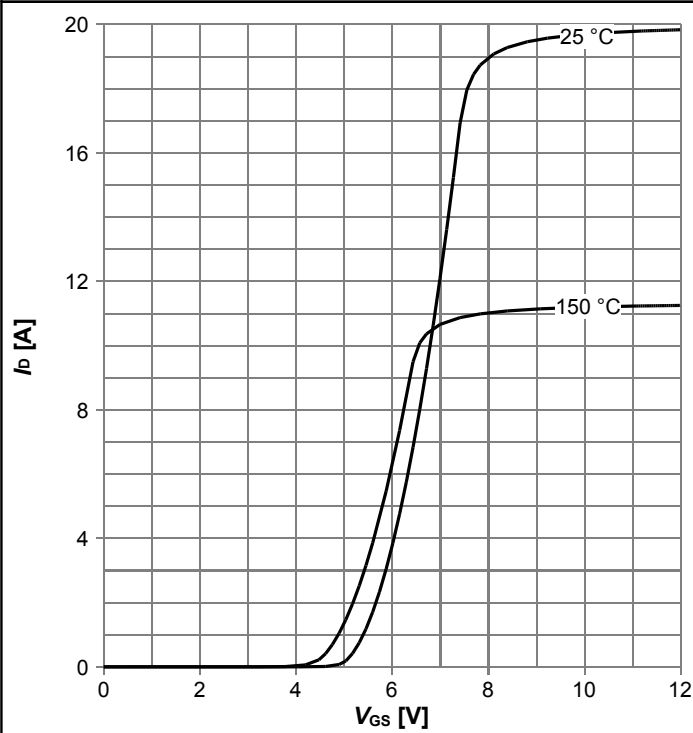
$R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



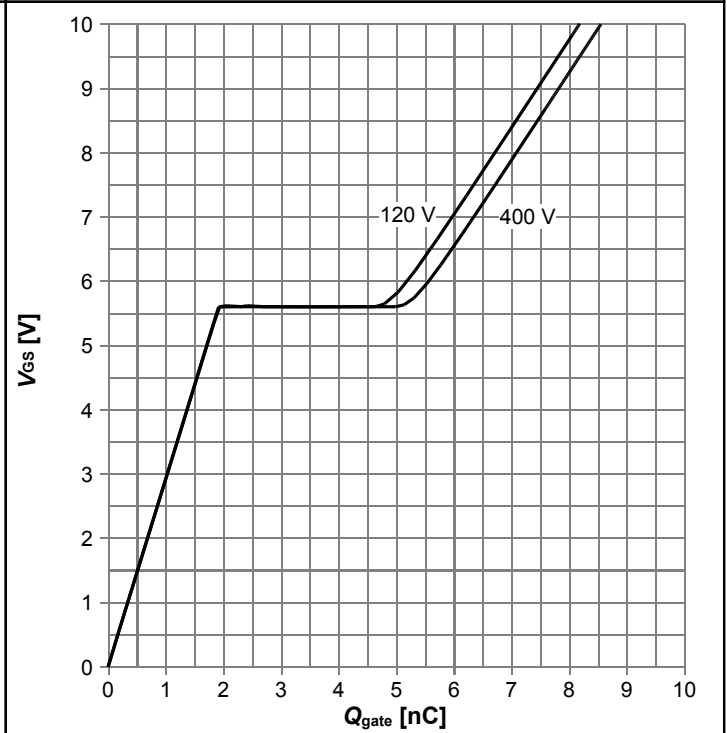
$R_{DS(on)} = f(T_j)$; $I_D = 1.7\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



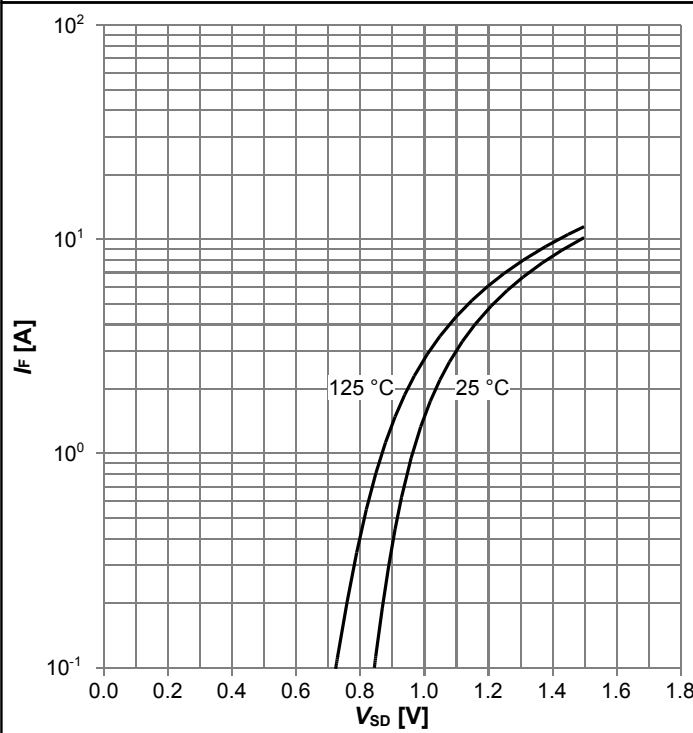
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



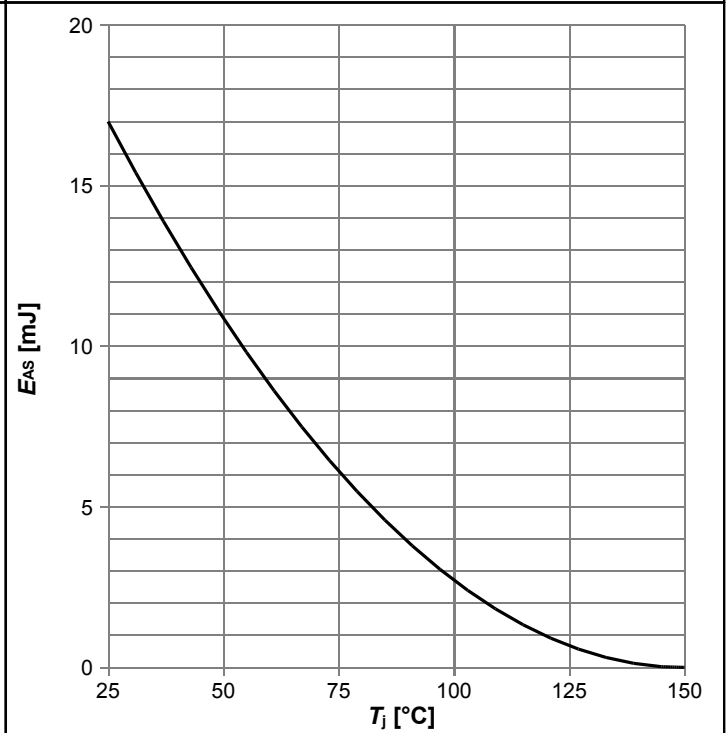
$V_{GS} = f(Q_{gate})$; $I_D = 1.7 A$ pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



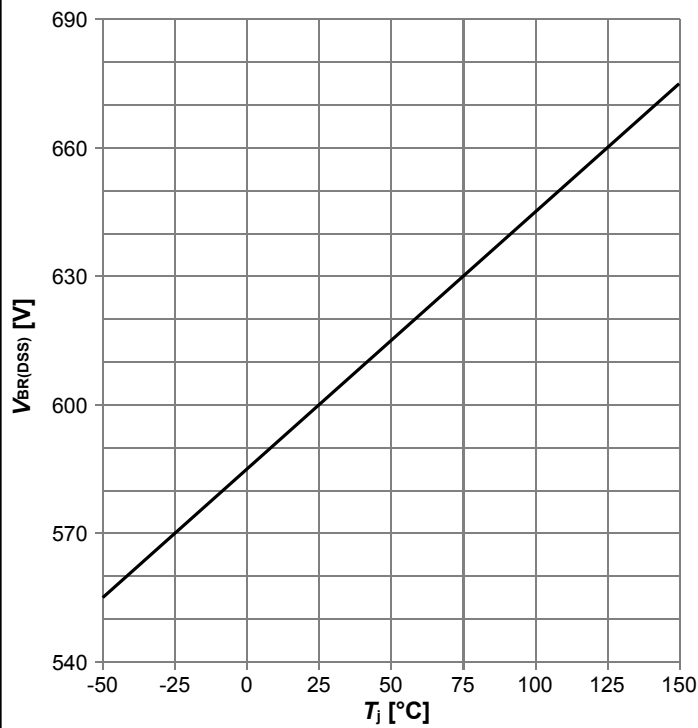
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



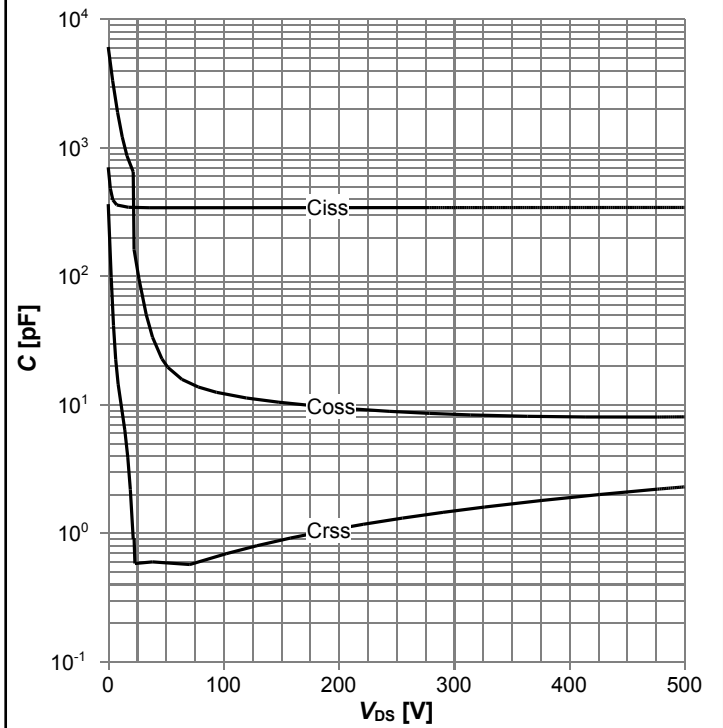
$E_{AS} = f(T_j)$; $I_D = 1.4 A$; $V_{DD} = 50 V$

Diagram 13: Drain-source breakdown voltage



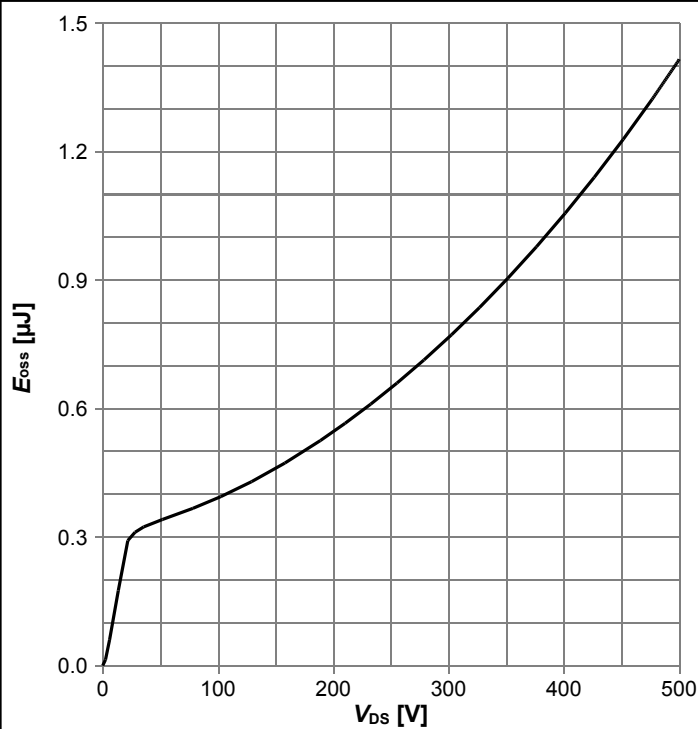
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics



Table 9 Switching times (ss)

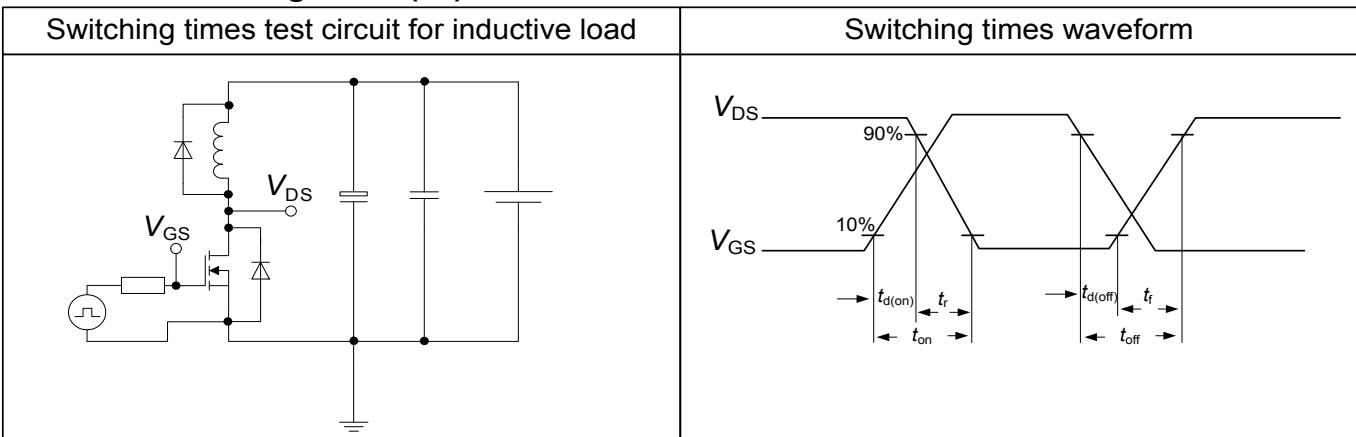
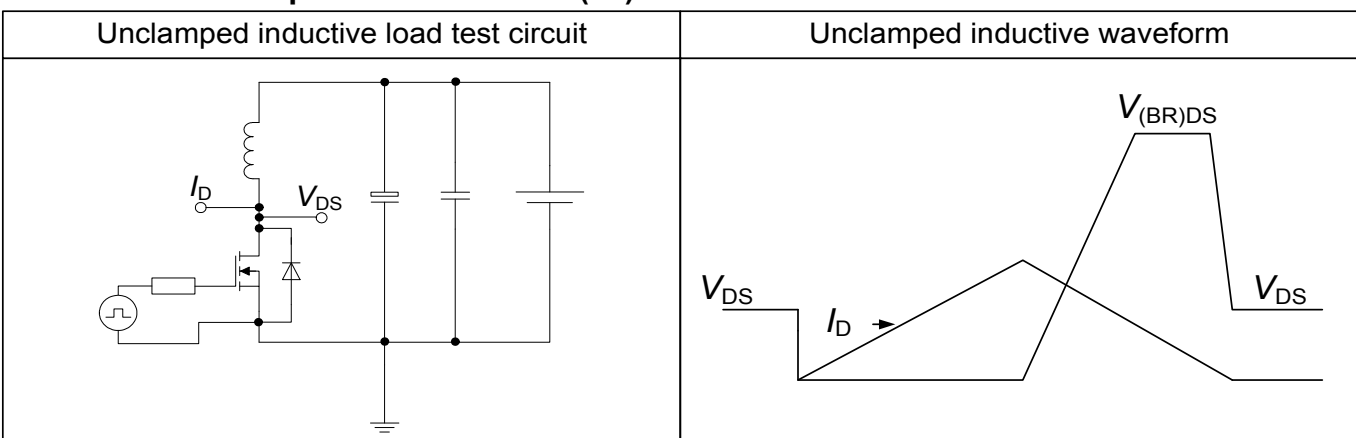
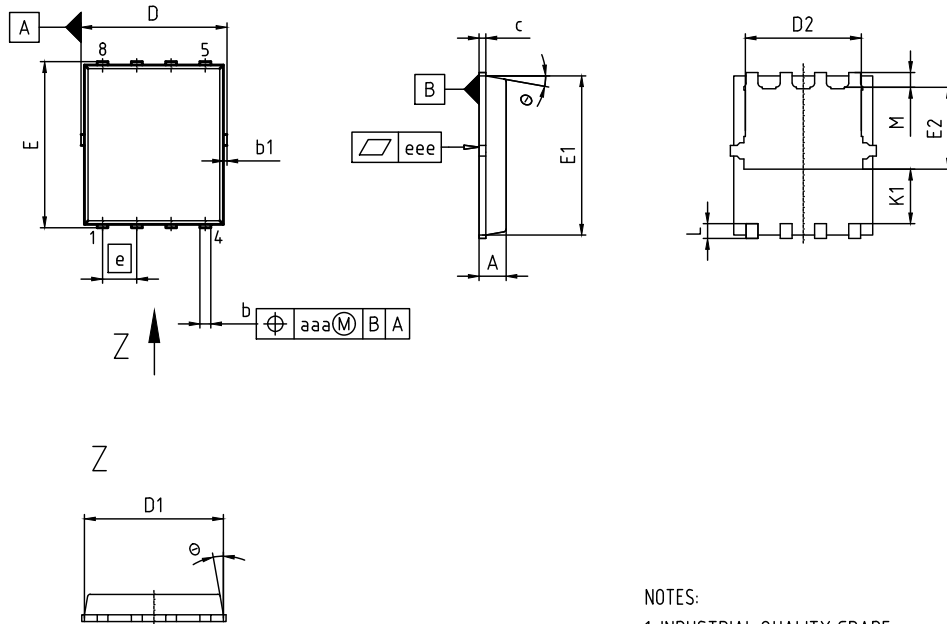


Table 10 Unclamped inductive load (ss)



6 Package Outlines



- NOTES:
1. INDUSTRIAL QUALITY GRADE
 2. ALL DIMENSIONS REFER TO JEDEC STANDARD MO240A NOT INCLUDE MOLD FLASH
 3. REMOVAL ON MOLD GATE, INTRUSION 0.1mm; PROPRUSION 0.1mm
 4. ALL METAL SURFACE ARE PLATED EXCEPT AREA OF CUT

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.03	0.23	0.001	0.009
c	0.15	0.35	0.006	0.014
D	5.15	5.51	0.203	0.217
D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	2.93	3.13	0.115	0.123
e	1.27		0.050	
N	8		8	
K1	1.92	2.12	0.076	0.083
L	0.45	0.65	0.018	0.026
M	0.45	0.65	0.018	0.026
φ	8.5°	12°	8.5°	12°
aaa	0.25		0.010	
eee	0.08		0.003	

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SCALE

EUROPEAN PROJECTION

ISSUE DATE
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REVISION
01

Figure 1 Outline ThinPAK 5x6 SMD, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS PFD7 Webpage: www.infineon.com
- IFX CoolMOS PFD7 application note: www.infineon.com
- IFX CoolMOS PFD7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPLK60R600PFD7

Revision: 2020-01-22, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2020-01-22	Release of final version

Trademarks

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

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Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

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