Datasheet, Version 2.1, 24 May 2011

ICE2HS01G

High Performance Resonant Mode Controller

Power Management & Supply

Never stop thinking.

ICE2HS01G

Revision History:	**11 May 2010**
Previous Version:	2.0
Page	Subjects (major changes since last revision)
19	section 3:10 burst mode enable

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High Performance Resonant Mode Controller for Half-bridge LLC Resonant Converter

Product Highlights

- **30kHz~1MHz switching frequency range**
- **High efficiency over wide load range**
- **Innovative drive method for synchronous rectification**
- **High accuracy frequency setting**
- **High accuracy setting and adjustable dead time**
- **Over load/open loop protection with adjustable blanking time and restart time**
- **Mains undervoltage protection with hysteresis**
- **External latch-off and over temperature protections**

ICE2HS01G

PG-DSO-20-45

Features

- Resonant mode controller for Half-bridge LLC resonant converter with synchronous rectification drives
- 20-pin DSO package
- 30kHz to 1MHz switching frequency
- Adjustable minimum switching frequency with high accuracy
- 50% duty cycle for both primary and secondary gate drives
- Adjustable dead time with high accuracy
- Driving signal for synchronous rectification which support full operation of Half-bridge LLC resonant converter
- Internal and External disable function for synchronous rectification
- Mains input under votlage protection with adjustable hysteresis
- Three levels of overcurrent protection for enhanced dynamic performance
- Open-loop/over load protection with adjustable blanking time and restart time
- Adjustable over-temperature protection with latch-off
- External latch-off enable pin

Applications

- PC power supplies
- Server power supplies
- Telecom power supplies
- Flat panel TV and Flat panel display power supplies
- AC-DC adapter

Type	Package
ICE2HS01G	PG-DSO-20

Typical Application Circuit

The ICE2HS01G is a high performance resonant mode controller designed specially for high efficiency half-bridge LLC converter with synchrnous rectification at the secondary side. With its new driving techqiues, the synchronous rectification can be realized for half-bridge LLC converter operated with secondary switching current in both CCM and DCM conditions. No special synchronous rectification controller IC is needed at the seondary side.For best performance, it is suggested to use half-bridge driver IC in the primary side with ICE2HS01G.

The typical application circuit of ICE2HS01G is shown in Figure 1.

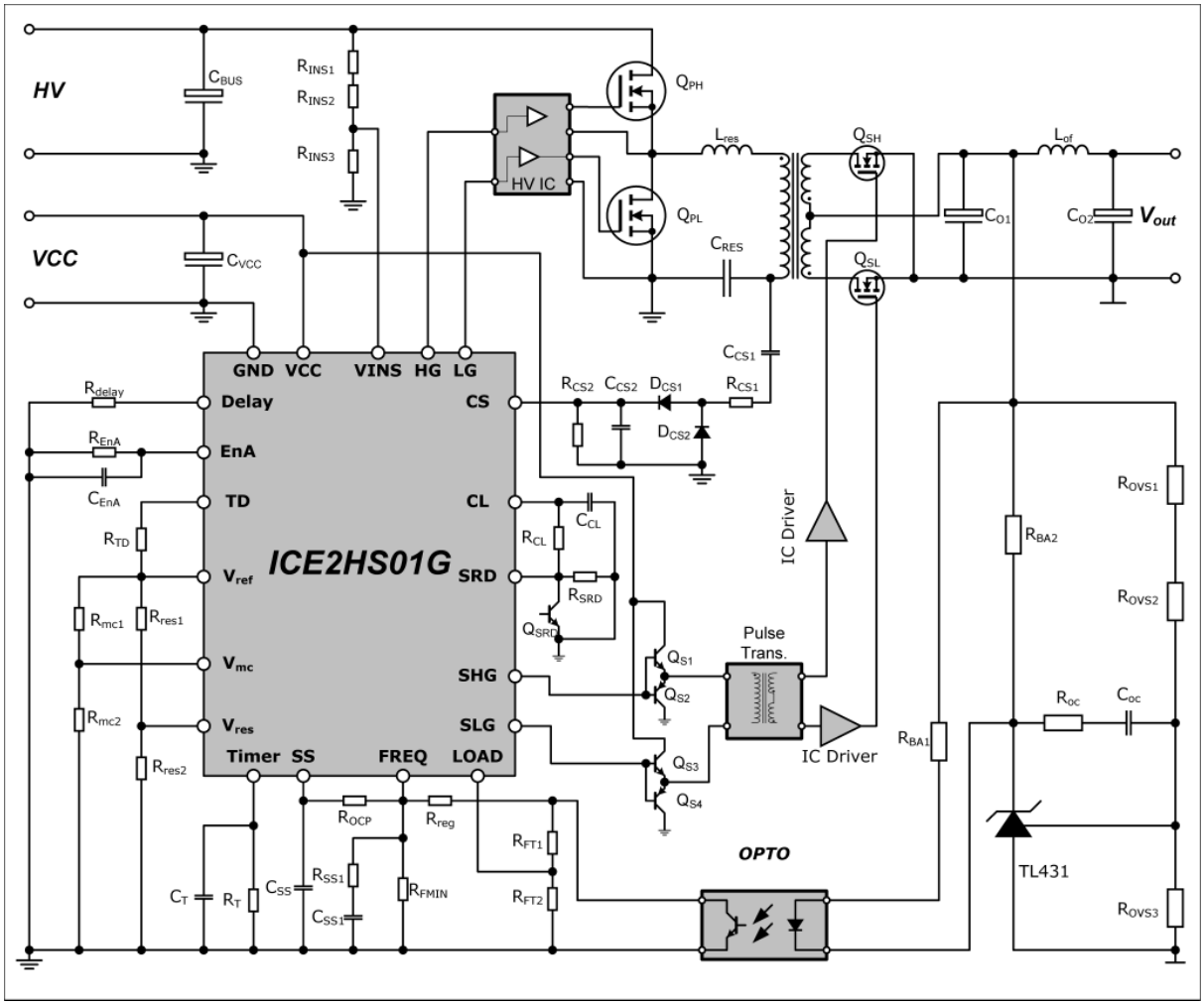

Figure 1 Typical application circuit

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1 Pin Configuration and Functionality

1.1 Pin configuration with PG-DSO-20

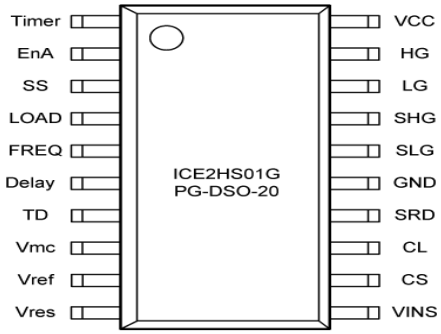

Figure 2 Pin configuration with PG-DSO-20

Table 1 Pin names

Pin	Symbol	Function	Pin	Symbol	Function
1	**Timer**	Over-load blanking time and autorestart time	11	**VINS**	Input bus voltage sense
2	**EnA**	Enable	12	**CS**	Current sense
3	**SS**	Softstart	13	**CL**	Currsnt sense output level
4	**LOAD**	Load detection	14	**SRD**	Sychronous rectification on duration and disable function
5	**FREQ**	Frequency of operation	15	**GND**	IC ground
6	**Delay**	Advance delay time setting	16	**SLG**	Gate logic for secondary low side switch
7	**TD**	Primary dead time setting	17	**SHG**	Gate logic for secondary high side switch
8	**Vmc**	Voltage level for entering and leaving missing cycle mode	18	**LG**	Gate logic for primary low side switch
9	**Vref**	Reference voltage output	19	**HG**	Gate logic for primary highside switch
10	**Vres**	Resonant voltage setting	20	**VCC**	IC power supply

1.2 Pin Functionality

Timer (Over-load blanking time and auto-restart timer)

Timer pin is used to set the blanking time and restart time for over load protection. The RC parallel circuit, C_{TL} and R_{TL}, is connected to this pin. The blanking time is determined by charging time of C_{TL} through IC internal current source, and the restart time is determined by the discharging time of C_{TL} through R_{TL}. This allows the system to face a sudden power surge for a short period of time without triggering the over load protection. In addition, the average power delivered is not influenced by any VCC dip which can not reset internal reference voltage.

EnA (Enable)

Internally, this pin has a pull-up current source of 100µA. By connecting a resistor outside from this pin to ground, certain voltage level is set up on this pin. If the voltage level on this pin is pulled down below certain level, IC is latched. If the external resistor has a negative temperature coefficient, this pin can be used to implement over-

temperature protection. In addition, the burst mode can be enabled/disabled by connnecting different capacitance to this pin. IC will do the set up function the first time VCC rise from a voltage lower than internal reference.

SS (soft start)

SS pin connects an external capacitor C_{SS} to GND and a resistor R_{OCP} to FREQ pin. An internal switch will first fully discharge C_{SS} before soft start or autorestart, which guarantee high operating frequency for soft start or restart. R_{OCP} determines the max operating frequency. During softstart, a internally current source is used to charge up the softstart capacitor. This current is big at first, it will be reduced once the SS voltage increases to some level and it will be further reduced if SS voltage increases to a higher level. In such a way, the smooth rising of output voltage can be achieved. Also, the soft start during time is mainly determined by the C_{SS}. In case of over current condition, SS pin will be discharged through 2 internal resistors toward zero votlage. As a result, the operating frequeny will be increased and the highest frequency in this case is determined by the equivalent resistance of R_{FMIN} and R_{OCP} in parallal.

LOAD (Load condition detection)

A voltage divider, consist of R_{FT1} and R_{FT2}, is connected to the collector of optocoupler, and this divided voltage is delivered to LOAD pin. If LOAD pin voltage is lower than a certain threshold, 0.1V, IC will stop switch. Only if the voltage level is higher than 0.15V, IC will resume swith again.

A second function of this pin is to detect the over-load or open-loop faults. Once the voltage on this pin is higher than 1.8V, IC will start internal and external timer to determine whether entering the protection mode.

The third function on this pin is to disable SR during light load mode. When the voltage on load pin is too low, IC will stop the SR gate drives.

FREQ (Operating frequency)

This pin provides a precise 2V reference and a resistor R_{FMIN} connected from this pin to GND, which defines a current that is used to determin the minimum operating frequency. In order to regulate the converter output voltage by changing the operating frequency, the phototransistor of an optocoupler is connected to this pin through resistor R_{REG}.

Delay (Advance delay time setting)

For SR purpose, the delay time between primary side switch's gate off signal and secondary side SR switch's gate off signal can be adjusted by a resistor R_{delay} connected to Delay pin.

TD (Primary dead time setting)

In order to provide the design flexbility, the dead time between two primary switches can be adjusted by external resistor R_{TD1} connected from Vref pin to TD pin. The TD pin voltage is regulated at 2V. The current flow into this pin determines the dead time, which ranges from 100ns to 1000ns.

Vmc (Voltage levels for entering and leaving missing cycle mdoe)

The voltages on this pin is used to setting the levels, on CL pin, which IC enters missing cycle operation mode or leaves missing cycle mode. Internally, a current source from internal power supply to this pin is provided which will generate the hysteresis voltage between entering and leaving missing cycle voltages.

Vref (Reference voltage ouput)

This pin is the output of refernce voltage, which is tight regulated at 5V. This reference voltage supplies the bias current for dead time setting, and also setting of resonant voltage, missing cylce voltages.

Vres (resonant voltage setting)

The voltage on this pin is used for determination the operation mode of the half-bridge LLC resonant converter, CCM or DCM. There is no turn-on delay between secondary and primary gate signals if the converter is in DCM mode. If the converter is in CCM mode, IC will add the turn-on delay when the Vres voltage is lower than VINS pin voltage.

VINS (mains input voltage sense)

The mains input voltage is fed to this pin via a resistive voltage divider. If the voltage on VINS pin is higher than the threshold V_{INSON}, IC will start to operate with softstart when VCC increases beyond turn on threshold. During operation, if the voltage on this pin falls below the threshold V_{INSON}, IC will stop switching until the voltage on this pin increases again.

CS (current sense)

The current sense signal is fed to this pin. Inside the IC, three comparators are provided for 3 level OCP function. If the voltage on CS pin is higher than the first threshold, IC will increase the switching frequency to limit the maximum output power of the converter. If the voltage on this pin exceeds the second threshold, IC will further increase the switching frequency to a higher value with higher frequency rising slope. If the voltage on this pin exceeds the third threshold, IC will be latched off immediately.

A second function of CS pin is to sense the output power level. If CS voltage is lower than some preset value on Vmc pin, IC will enter the missing cycle mode to improve the converter efficiency.

Protection function is also integrated on this pin for synchoronous rectification. IC will stop the SR gate drives if the CS votlage is too high or it drops too fast.

CL (current sense average level)

A resistor R_{CL} is connected between CL pin and SRD pin. This resistor determines how much the synchrnous rectifcation on duration is changed according to load condition. Internally, CL pin voltage is proportional to the CS pin voltage. A clamp circuit set the maximum voltage of 1.95V on CL pin. A capacitor is recommended to be put between this pin and ground. This can filter out the high ripple component on CS voltage and therefore decrease the variation of SR dirves' on time versus output load.

SRD (SR Disable input)

This pin is used to disable SR function, by pulling down SR pin to zero, in case of softstart, hold up time, OCP or any other conditions specified by customers. A limited current source is built internally which generates a constant 2V voltage on SR pin. The current, depending on the external resistors R_{SRD}, and also R_{CL} and V_{CL} if connected, is used to charge the internal capacitor. Therefore, the on time of secondary gate drives can be set by choosing different R_{SRD} during design or different R_{CL} which sets the dependence of the current on the current sense voltage.

GND (ground)

IC common ground.

SLG (Low side SR gate drive)

This pin delivers gate drive signal for low side synchornous rectification switch.

SHG (High side SR gate drive)

This pin delivers gate drive signal for high side synchronous rectification switch.

LG (low side gate drive)

This pin delivers gate drive signal for primary low side switch.

HG (high-side gate drive)

This pin delivers gate drive signal for primary high side switch.

VCC (IC power supply)

Supply voltage of the IC.

2 Representative Block Diagram

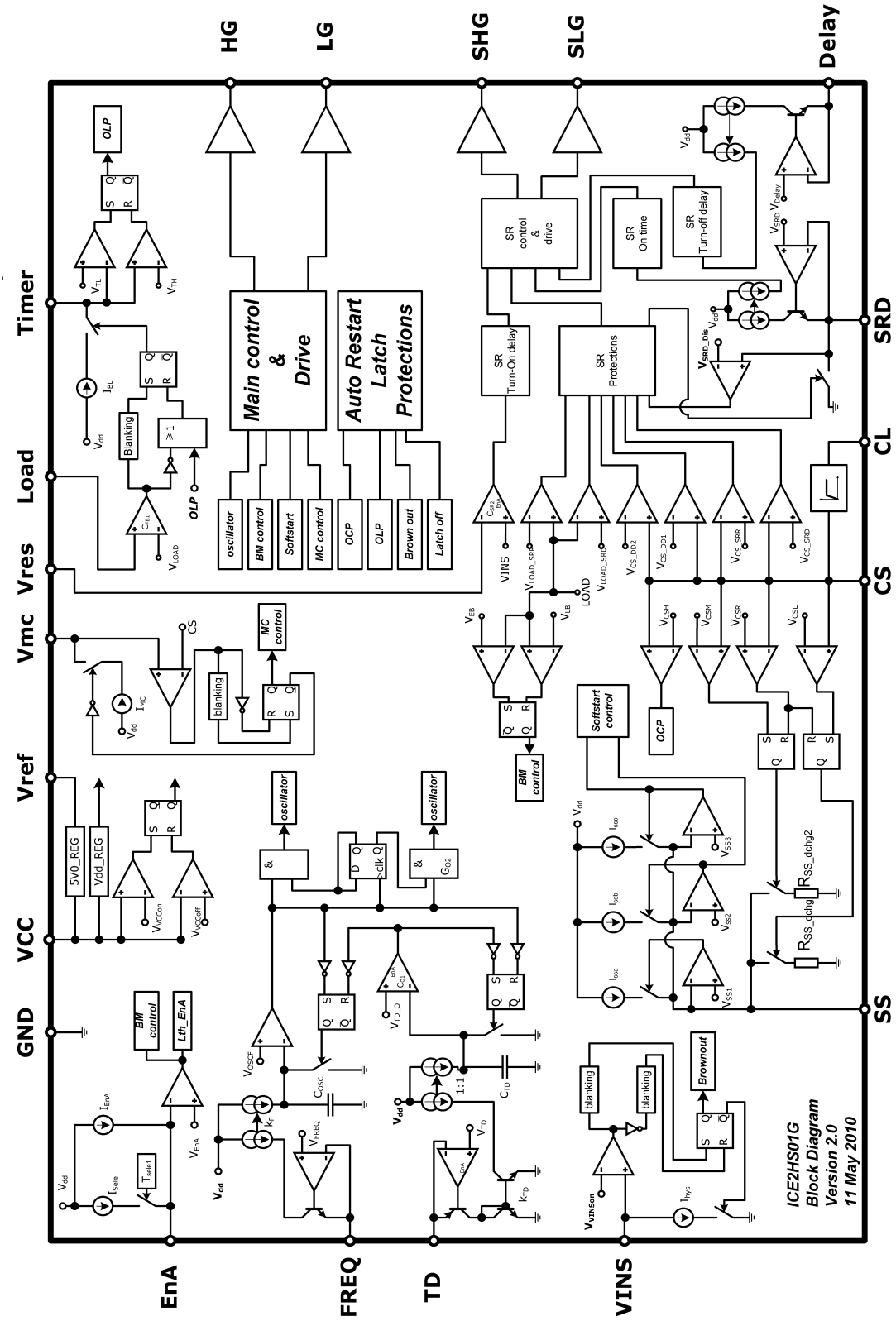

Figure 3 Representative Block Diagram

3 Functional description[1)]

The controller ICE2HS01G, a 20-pin IC, is designed for pulse-frequency-modulated resonant converters, especially half-bridge LLC resonant converter. It operates with 50% duty cylce for two primary gate drives and 180° out of phase. The regulation of output voltage is achieved through adjustment of the switching frequency. To ensure the zero-voltage-switching and safe operation in half-bridge topologies, the dead time between primary high side switch and low side switch is set independently to the switching frequency and also with high accuracy.

In half-bridge LLC resonant converetr, as there is only one voltage control loop, current information in the LLC converter is used for proetctions. The current loop is designed to be much more faster compared to voltage loop and therefore providing a reliable protection for the converter.

As synchronous rectification (SR) is a necessary measure to achieve high efficiency, ICE2HS01G features two driving signal for secondary SR switches. In order to ensure SR safe and proper operation, both the delay time between primary side switch and secondary SR switch and the duration of secondary SR switches can be programmed with external resistors.

ICE2HS01G also offers multiple protections which ease the design of a reliable and high efficiency half-bridge LLC resonant converter.

3.1 IC power supply

The controller ICE2HS01G is targetting at applications with auxiliary power supply. In most cases, a front-end PFC pre-regulator with a PFC controller is used in the same system.

The controller ICE2HS01G starts to operate when the supply voltage V_{VCC} reaches the on-threshold, V_{VCCon} of 12V. The minimum operating voltage after turn-on, V_{VCCoff}, is at 11V. The maximum supply voltage V_{VCCmax} is 18V.

3.2 Oscillator

The pulse-frequency-modulation is built with current controlled oscillators. The period of charging capacitor C_{OSC} determines the on time of primary switches. The period for charging capacitor C_{TD} determines the dead time between two primary swithes. The simplified oscillator circuit is shown in Figure 4. The typical switching waveforms of C_{OSC} and C_{TD} are shown in Figure 5.

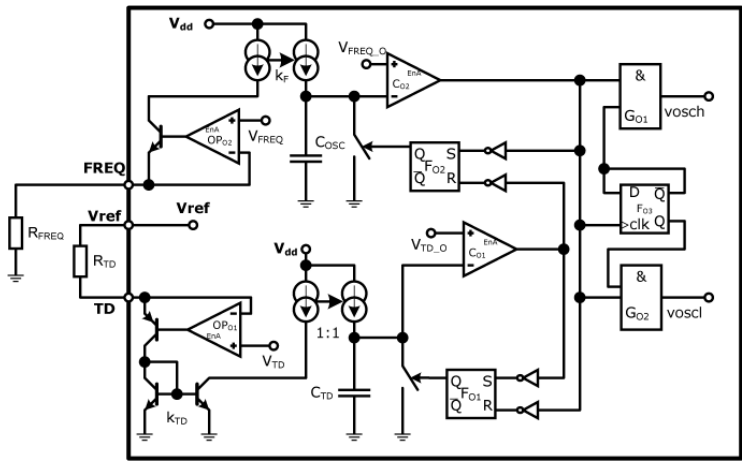

Figure 4 Simplified oscillator circuit

[1)] *All values which are used in the functional description are typical values. For calculating the worst cases the min/max values, which can be found in section 4 Electrical Characteristics, have to be considered.*

Assume the current flows output from FREQ pin and TD pin are I_{FREQ} and I_{TD}, respectively, the switching frequency during normal operation can be obtained according to equation [1].

$$F_S = \frac{0.5}{\frac{V_{OSCF} \cdot C_F}{k_F \cdot I_{FREQ}} + \frac{V_{OSCT} \cdot C_{TD}}{k_{TD} \cdot I_{TD}}} \quad [1]$$

According to the typical application circuit shown in Figure 1, the minimum operating frequency of the converter can be set by choosing R_{FMIN}. Assume the dead time is 300ns, the minimum switching frequency is 50kHz when the R_{FMIN} is 30kΩ. The minimum operating frequency versus various R_{FMIN} is shown in Figure 6.

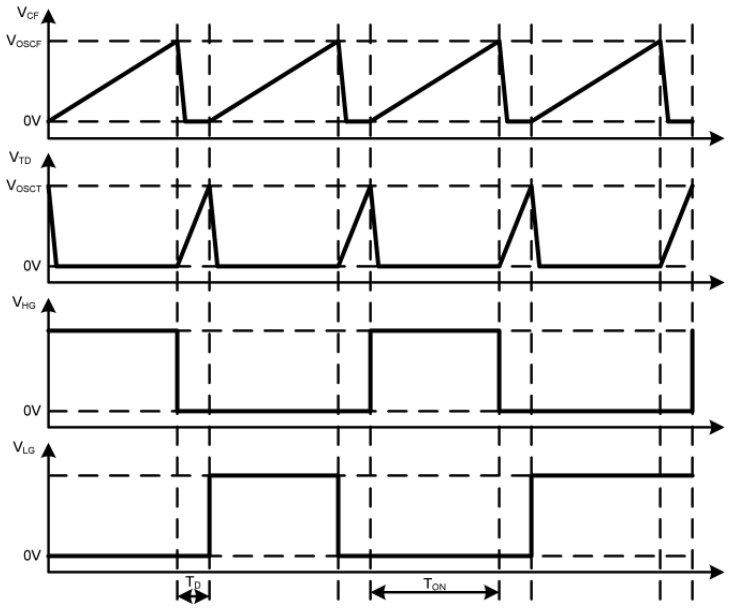

Figure 5 Oscillator waveforms

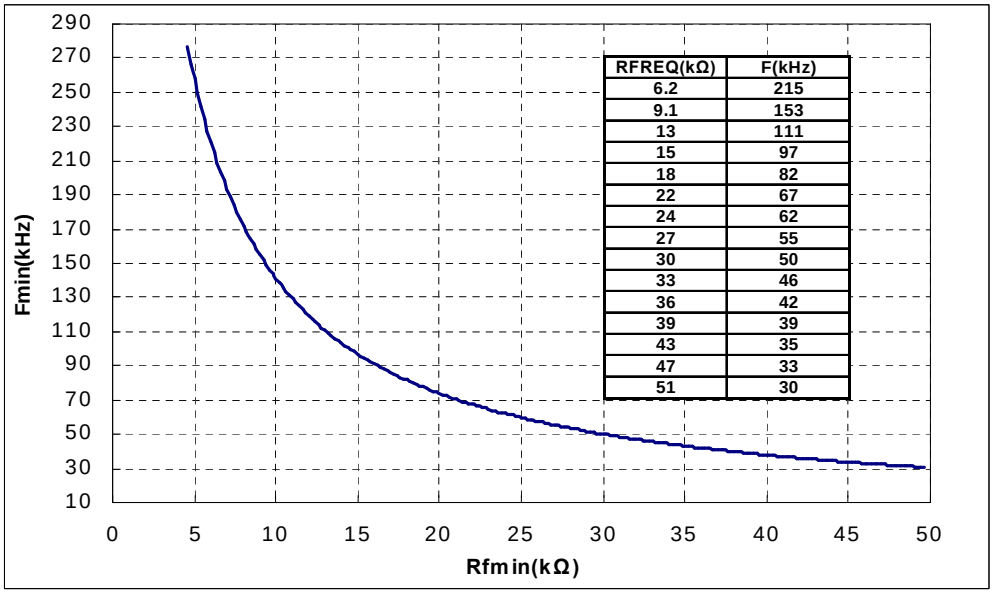

Figure 6 Minimum switching frequency versus R_{FMIN} with T_D=300ns

As shown in Figure 1, the regulation of output voltage is achieved by controlling the current flowing into collector of the opto-coupler. The maximum current flowing through the capacitor is achieved when the collector is pulled to ground. The equivalent resistance at FREQ pin, the resistor R_{reg}, together with R_{FMIN}, determines the maximum

switching frequency during load and line regulation. The actual switching frequency of the converter can also be checked from Figure 6 by using the equivalent resistance at FREQ pin.

3.3 Dead time

As shown in Figure 4, the dead time can be adjusted by changing the current flowing into TD pin. There is a 5V reference voltage provided on Vref pin. By connecting a resistor R_{TD} from Vref pin to TD pin, the current can be set. The dead time is longer if the resistance is larger and vice versa. A typical value of 300ns dead time can be achieved by setting R_{TD}=180kΩ. The relationship between R_{TD} and dead time is shown in Figure 7. Furthermore, a minimum dead time limitation, 135ns, is built inside the IC for protection.

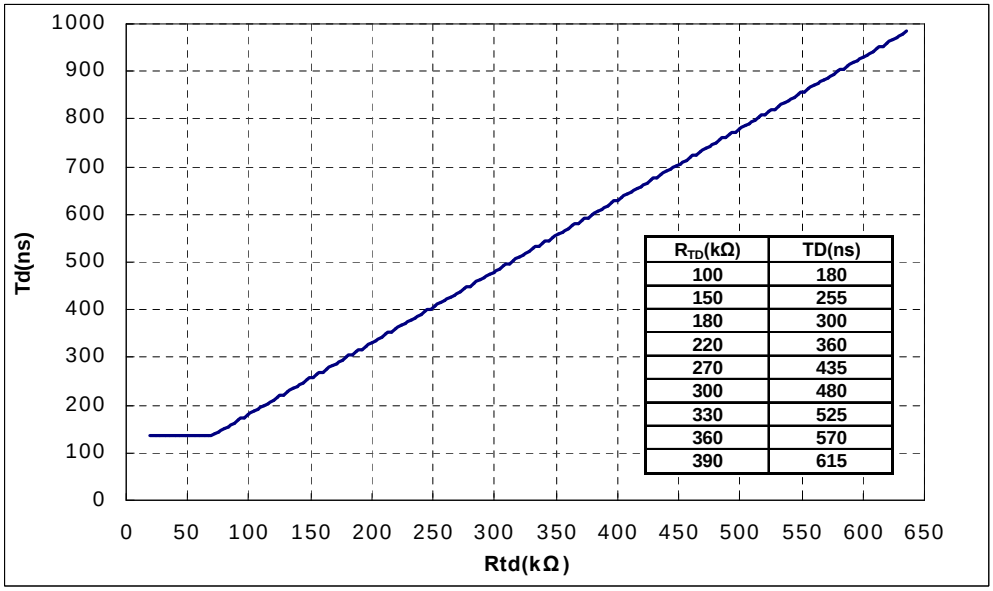

Figure 7 Dead time versus R_{TD}

3.4 Softstart

Soft start is implemented by sweeping the operating frequency from an initial high value until the control loop takes over. This initial switching frequency should be high enough so that the resonant current at first pulse can be limited within the desired value.

The internal block diagram for softstart funciton block is shown in Figure 8. Initially, capacitor C_{OCP} is fully discharged by IC internal switch, so that R_{OCP} is effectively in parallel to R_{FMIN} and the resulting parallel resistance determines the initial frequency.

During start up, C_{SS} is continuously charged until its voltage reaches the internal 2V reference voltage, and accordingly the current through R_{OCP} drops to zero. Before this time, the LLC output voltage will have rise up to a level close to the regulated value and the feedback loop takes over, so that it will be the current through phototransistor to determine the operating frequency.

To ensure a smooth rise of output voltage during start up, different internal current will be used to charge up the softstart capacitor C_{SS}. At the moment softstart block is enabled, all three current sources I_{SS1} through I_{SS3} will turned on. Therefore, the charge current at this moment will be the sum of these three current plus the current flows from FREQ pin, through R_{OCP}, to C_{SS}. When the voltage V_{CSS} is higher than V_{SS1} (1.5V), current source I_{SSa} (150µA) is turned off. When C_{SS} is charged to higher than V_{SS2} (1.8V), the second current source I_{SSb} (50µA) is

turned off. The last threshold V_{SS3} is 1.9V and the third current source I_{SSc} (50µA) is turned off after V_{CSS} is higher than V_{SS3}.

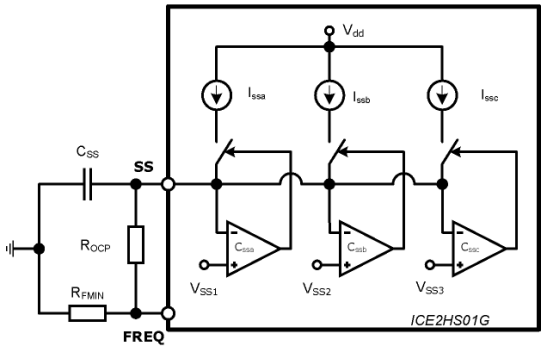

Figure 8 soft start block

In some case the frequency set by R_{OCP} is not high enough for softstart, additional series resistor and capactior can be connected to FREQ pin for further increment the soft start frequency.

During soft start, the overload protection is disabled After V_{SS} is higher than V_{SS3} for 10 ms, softstart block will enable overload protection function and IC will monitor the voltage on LOAD pin to detect any open-loop/over-load conditions. However, the IC will enable the overload protection after 40ms of softstart if SS pin voltage never goes higher than V_{SS3}.

3.5 Current sense and over-current protection

Current sense in LLC half bridge converters is mainly for protection. The circuit is shown in Figure 9.

The controller ICE2HS01G incooperates three-level over current protection. In case of over-load condition, the lower level OCP will be triggerred, the switching frequency will be increased according to the duration and power of the over load. The higher level OCP (1.6V) is used to protect the converter if transformer is saturated. the IC will be latched after a 220ns blanking time.

If the sensed V_{CS} is higher than 0.8V, SS pin capacitor will be discharged by an internal discharge resistor $R_{dischg1}$. This will result in higher switching frequency and less delivered power to secondary side.

If sensed V_{CS} is higher than 0.9V (the 2nd level), another discharge resistor $R_{dischg2}$ is also used to discharge the capacitor C_{SS}.The C_{SS} will be discharged faster which means the switching frequency increases faster. This is to limit the fastly increasing resonant current. This is useful if the system encounter some steep load change at the output side during dynamics.

Both discharge resistors are turned off if the current sense voltage falls belower than 0.75V.

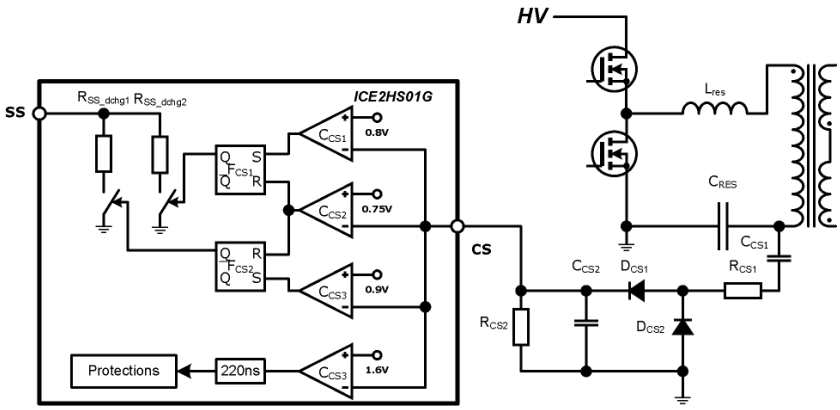

Figure 9 Current sense and over-current protection block

3.6 Light load operation

The switching frequency of a half-bridge LLC resonant converter can be very high at no load or light load operations. High switching frequency results in higher switching loss and magnetized core loss. In most cases, reduction of the switching frequency will result in efficiency increase, which highly depends on the balance between switching losses and conduction losses in the converter.

ICE2HS01G offers various options of light load operation to meet the different requirements in applications. These including Missing Cycle mode in light load and Burst Mode in no load. In addition, both modes can be enabled/ disabled with parameter selctions. For detailed operation of light load, the block diagram is shown in Figure 10.

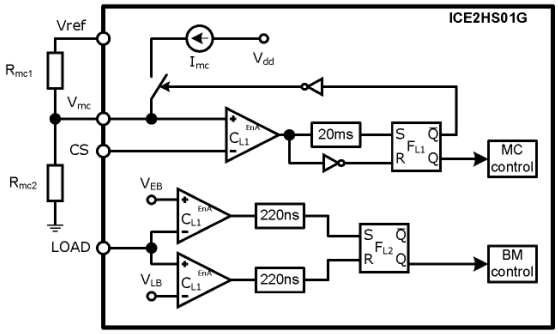

Figure 10 Light load control module

If the current sense voltage is lower than the preset reference level on Vmc pin for 20ms, IC enters into a Missing Cylce (MC) mode, where every two out of five switches are removed to reduce the average switching frequency. Vref pin is the output of internal reference voltage, which is an accurate 5V voltage source, with up to 2 mA. A typical output gate drive waveforms in MC mode is shown in Figure 11.

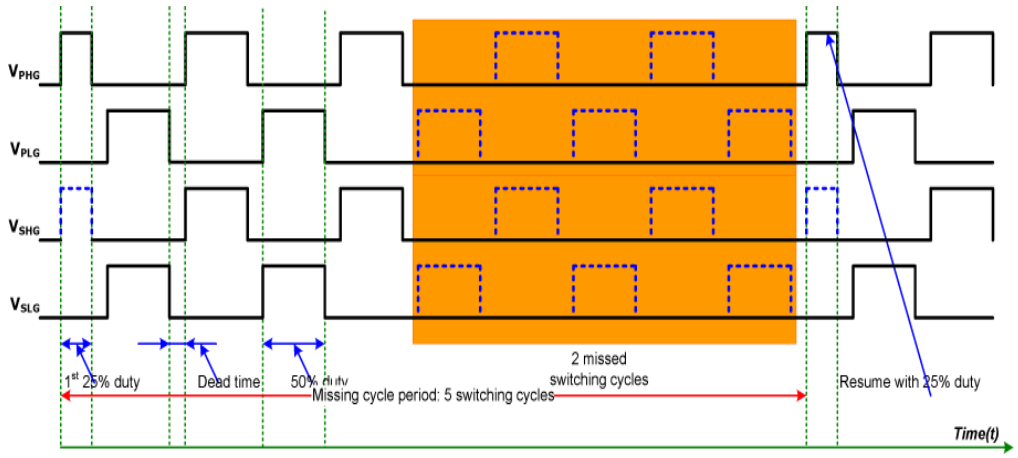

Figure 11 ICE2HS01G gate outpus during Missing Cycle

The entering and leaving missing cycle level can be adjusted through connecting different resistors to V_{mc} pin. The actual values can be calculated from equations [2] and [3]. The current source I_{mc} is 50**µA** built inside with high accuracy. For example, with R_{mc1}=33k**Ω** and R_{mc2}=1.3k**Ω**, the current sense voltage for entering and leaving missing cylce mode can be calculated to be 0.19V and 0.252V.

$$V_{LMC} = V_{ref} \cdot \frac{R_{mc2}}{R_{mc1} + R_{mc2}} \quad [2]$$

$$V_{EMC} = V_{ref} \cdot \frac{R_{mc2}}{R_{mc1} + R_{mc2}} + I_{mc} \cdot \frac{R_{mc1} \cdot R_{mc2}}{R_{mc1} + R_{mc2}} \quad [3]$$

The Missing Cycle mode can be disabled by pulling down Vmc pin to ground. In this case, even very low voltage on CS pin will let the IC works in normal mode. It is recommended to use a 10k resistor for pulling down purpose.

The Burst Mode (BM) operation in ICE2HS01G is implemented with LOAD pin voltage. If the voltage on LOAD pin is lower than 0.1V, all the gate drives will be pulled low after the next high side switch cycle is finished. If the LOAD pin voltage increases higher than 0.15V, IC will resume switch. Every time IC resumes switch from burst mode, the first pulse will be high gate with reduced duty cycle.

In certain conditions, Burst Mode opeation is not wanted and can be disabled. The method will be described in Section 3.10.

3.7 Synchronous Rectification

Synchronous Rectification (SR) in a half-bridge LLC resonant converter is the key to achieve very high efficiency, and this is the major benefits from the patent pending method integrated in ICE2HS01G. The control of Synchronous Rectification in ICE2HS01G have four main parts: On time control, turn-on delay, turn-off delay and protections, with the block diagram shown in Figure 12.

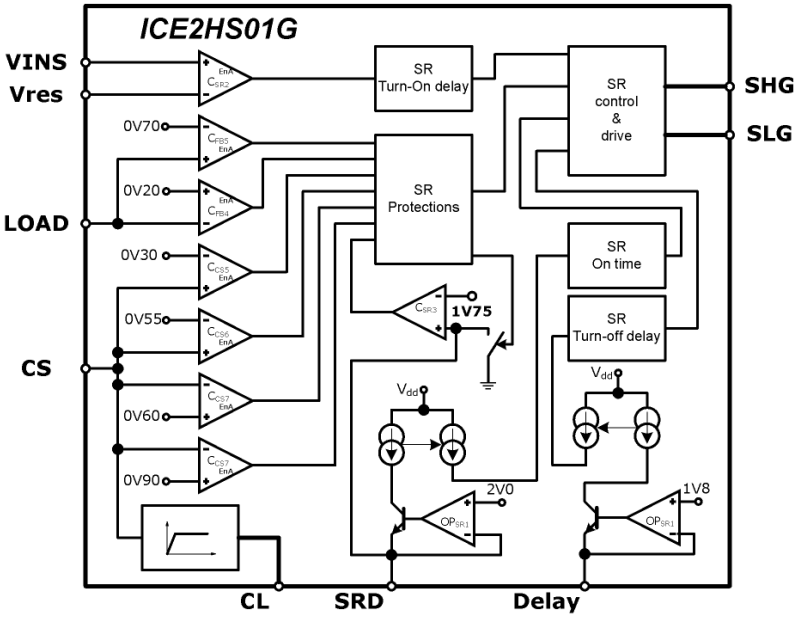

Figure 12 Synchronous rectification control block diagram

3.7.1 SR On time control

The oscillator of SR control, with divide-by-two function, determines the on time of both SR gates. It uses regulated current to charge the capacitor, while the current is proportional to current flowing out of SRD pin and the capacitor is fixed inside the IC. The SRD pin is regulated to 2V. On time of SR gates can then be programmed by regulating the equivalent resistance connected to SRD pin.

In typical conditions, a 5µs SR on time is set when the equivalent resistance from SRD pin to ground is 62k**Ω**. The typical relation between SRD resistance and the corresponding SR on time can be found in Figure 13. The internal circuit of SRD pin is designed with certain limit of maximum current flowing out. The minimum resistor, or equivalent resistance to SRD pin, can not be less than 15k**Ω**.

A simple constant on time control does not provide the best performance of LLC HB converter. In fact, the actual resonant period of secondary current reduces when the output load decreases or input voltage increases. The primary winding current can reflects this change. Certain current sense circuit can be used to get such information and input to ICE2HS01G on CS pin. In ICE2HS01G, a function called current level (CL) pin is implemented. During heavy load and low input voltage, the CL pin voltage is clamped at same voltage of SRD pin. Therefore, the SR on time in such conditions is determined by R_{SRD} only. In case of light load, with low CS voltage, the CL pin voltage is reduced and therefore the actual SR on time is reduced

as well. The resistor R_{CL} can be adjusted to find the suitable reducing speed of SR on time. The relationship between CS voltage and CL voltage is shwon in Figure 14.

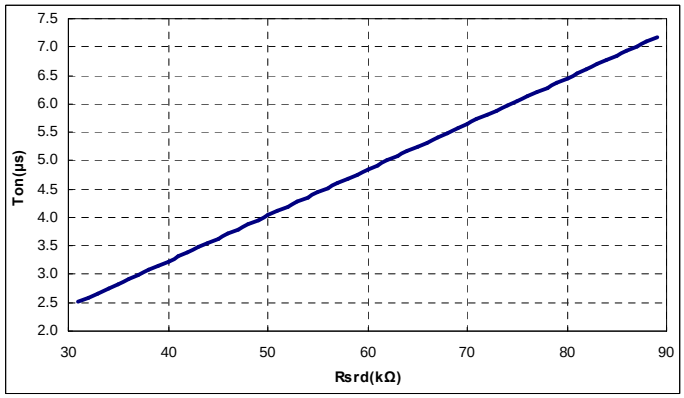

Figure 13 SR on time versus SRD resistance

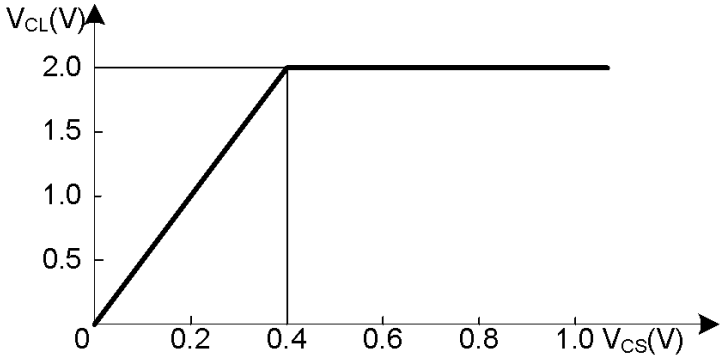

Figure 14 Relationship between V_{CS} and V_{CL}

3.7.2 Turn-on delay

When the input voltage is too high, the LLC converter secondary switches are working in CCM condition. Certain recovery time of the MOSFET body diode is required depending on the turn-off current. For better performance, the other MOSFET should be turned on after the recovery phase. The turn-on delay function is built in ICE2HS01G for such purpose. When the VINS pin voltage is higher than Vres pin, the SR MOSFETs are turned on 250ns after the corresponding primary MOSFETs are turned on.

3.7.3 Turn-off delay

The SR on time control determines the conduction time for secondary switches and the duration is actually link to resonant parameters and output load. However, the SR on time can not be longer than the primary gate signals, which otherwise will cause damage to the system. Therefore, SR gate will be turned off by two conditions: the primary gate signal or the SR on time oscillator, the one comes first will determine the actual SR duation.

However, the delay from IC gate signal to secondary SR switches can be longer than those delay to primary SR swithes. The function turn-off delay is used to adjust this difference. Instead of using the primary gate signal (PHG/PLG) to turn off SR gate, a signal with certain advance time to primary gate signal is used to generate SR gate off signal. And this certain advance time is adjustable through delay pin resistor.

IC delay pin is regulated at a constant voltage, the current, depending on external resistor only, is used to calculate this turn-off delay. The turn-off delay is 330ns when R_{delay} is 51kΩ. In addition, the relationship of turn-off delay time and delay resistance is shown in Figure 15.

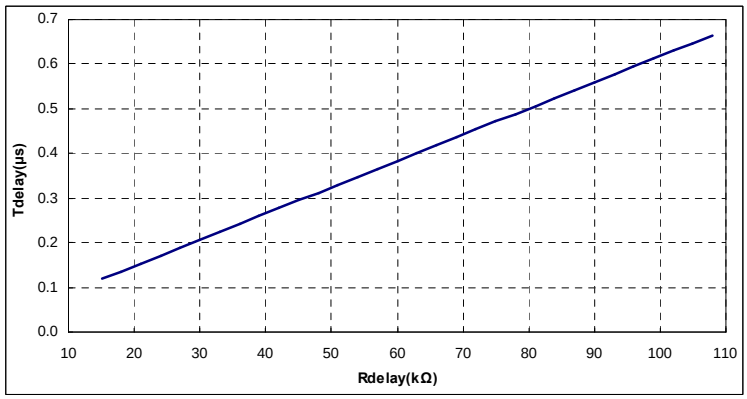

Figure 15 Relationship between Rdelay and Tdelay

3.7.4 SR protections

As the SR control in ICE2HS01G is realized with indirect method, there are some cases that the SR can not work properly. In this cases, the SR gate drive will be disabled. Once the condition is over, IC will restart the SR with SRSoftstart.

During softstart, the SR is disabled. When the softstart pin voltage is higher than 1.9V for 20ms, SR will be enabled with SRSoftstart.

When LOAD pin voltage is lower than 0.2V, IC will disable the SR immediately. If LOAD pin voltage is higher than 0.7V, IC will resume SR with SRSoftstart.

During over-current protection phase, if the softstart pin voltage is lower than 1.8V, SR will be disabled. The SR will resume with softstart 10ms after SS pin voltage is higher than 1.9V again.

In over-current protection, if the CS pin voltage is higher than 0.9V, SR is disabled. SR will be enabled with SRSoftstart after CS pin voltage is lower than 0.6V.

All the above four conditions are built inside the IC. If IC detects such a condition, IC will disable SR and pull down the voltage on SRD pin to zero.

When the CS voltage suddenly drops from 0.55V to below 0.30V within 1ms, the SR gate is turned off for 1ms, after 1ms, SR operation is enabled again with SRsoftstart.

An addition option is also provided. If some fault conditions are not reflected on the four conditions mentioned above but can be detected outside with other measures, the SR can also be disabled and enabled with softstart from outside. This is implemented on SRD pin as well. The internal SRD reference voltage has limited current source capability. If a transistor Q_{SRD} is connected as shown in typical application circuit, the voltage on SRD pin can be pulled to zero if this transistor is turned on, which will stop the SR. If the SRD voltage is released and increases above 1.75V, SR is enabled with softstart.

3.7.5 SR softstart

The SR operaton is enabled after the output voltage has been built up. However, as the SR MOSFET drain-source voltage drop is much lower than the forward voltage drop of the body diodes or the schottky diodes, the output power of the converter will increase a lot if the SR MOSFETs are started with full duty. In ICE2HS01G, SR operation will start with small duty. The SR MOSFET will start with its own softstart, the duty cycle for first pulse is around one-tenth of its normal duty, which will be kept same for 16 consective switching cycles. Then, the duty is increased gradually step by step to the full duty. Total 7 steps are built for the softstart and each step includes 16 switching cycles. Therefore, after 128 switching cycles, the SR duty will reach its normal value.

3.8 Mains Input Voltage Sense

The operation range of mains input voltage needs to be specified for LLC resonant converter. In addition, the input voltage information is used to determines whether the SR turned on delay is added or not. The typical circuit of mains input voltage sense and process is shown Figure 16.

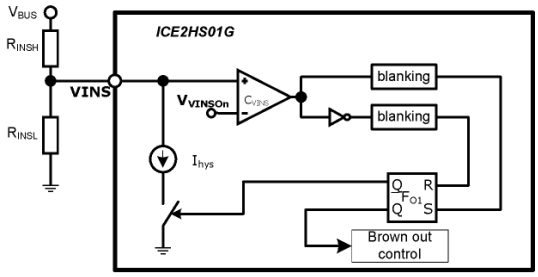

Figure 16 Mains input voltage sense

With the current source I_{hys} connected between VINS and Ground, an adjustable hysteresis between the on and off input voltage can be created as

$$V_{HYS} = R_{INSH} \cdot I_{hys} \quad [4]$$

The mains input voltage is divided by R_{INS1} and R_{INS2}. A current source I_{hys} is connected from VINS pin to ground in the IC. If the on and off threshold for mains voltage is V_{mainon} and $V_{mainoff}$, the resistors can be decided as

$$R_{INSH} = \frac{V_{mainon} - V_{mainoff}}{I_{hys}} \quad [5]$$

$$R_{INSL} = R_{INSH} \cdot \frac{V_{INSON}}{V_{mainoff} - V_{INSON}} \quad [6]$$

The blanking time for leaving brown-out is around 450µs and for entering brown-out is around 47µs. For example, if R_{INS1}=6.2MΩ and R_{INS2}=27kΩ, the turn-on bus voltage is 350V and the turn-off bus voltage is 288V.

3.9 Over load protection

In the typical application circuit, a voltage divider with R_{FT1} and R_{FT2}, is connected to the collector of optocoupler, and this divided voltage is delivered to LOAD pin. This is used to determine the feedback voltage threshold for over load protection. During operation, if V_{LOAD} > 1.8V, and this condition last longer than an adjustable blanking time of T_{OLP}, the IC will immediately stop delivering all the driving signals, and only after an adjustable restart time $T_{restart}$, IC will restart with soft start. This allows the system to face a sudden power surge for a short period of time without triggering the protection.

The Timer pin is used to set the blanking time T_{OLP} and restart time $T_{restart}$ for over load protection. The RC parallel circuit, C_T and R_T, is connected to this pin. When the voltage on load pin is higher than V_{load}, an internal current source of I_{BL} starts charging the external capacitor C_T. This current source turns off only when the capacitor voltage, V_{TL} reaches V_{TLH} or when V_{LOAD} decreases below 1.8V. Once V_{TL} exceeds 4.0V, the overload/openloop protection is triggered by turning off the GATE signal. From this time, C_T slowly discharges through the external resistance R_T. When V_T drops below 0.5V, the IC restarts its operation with soft-start. The charging time and the

discharging time of the capacitor C_T determine respectively the open load/over loop protection blanking time T_{OLP} and the restart time $T_{restart}$ of the IC. The circuit about how this protection works is shown in following Figure 17.

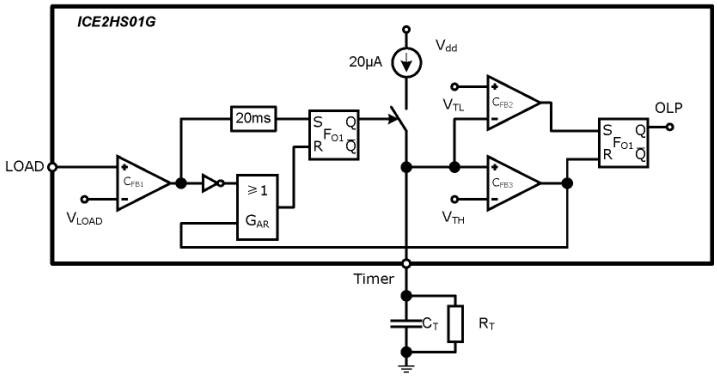

Figure 17 Over-Load protection scheme

The OLP blanking time can be calculated as

$$T_{OLP} = 20ms - R_T \cdot C_T \cdot \ln\left(1 - \frac{V_{TH}}{R_T \cdot I_{BL}}\right) \quad [7]$$

The restart time can be calculated as

$$T_{Restart} = -R_T \cdot C_T \cdot \ln\left(\frac{V_{TL}}{V_{TH}}\right) \quad [8]$$

3.10 EnA pin

In addition, this IC provides an external enable/disable function. Internal current source, I_{EnA}, is used to built up the voltage on EnA pin. During operation, if the voltage on this pin is reduced below 1.0V, IC will stop switch. Recycling the IC VCC supply can reset this protection. This pin can used for external latch enable function. It can also be used for over-temperature protection with latch off protection. The block diagram of Ena function is shown in Figure 18.

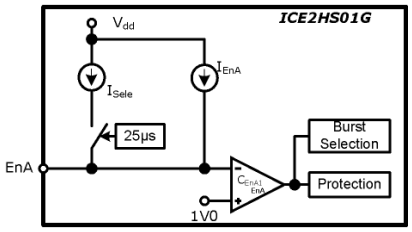

Figure 18 Latch-off enable function block diagram and burst mode selection

In addition to the latch-off enable function, this pin is also built for the selection of burst mode enable or not during softstart. If the burst mode is enabled, the gate drives will be disabled if LOAD pin voltage falls below some threshold. However, if burst mode is not selected, the gate drives will not be stopped by LOAD pin voltage.

The selection block works only after the first time IC VCC increases above UVLO. After CVCC is higher than turn on threshod, a current source I_{sele}, in addition to the I_{EnA}, is turned on to charge the capacitor C_{EnA}. After 26µs, IC will compare the voltage on EnA pin and 1.0V, if voltage on EnA pin is higher than 1.0V, the burst mode function will be enabled. As the voltage on EnA pin depends on R_{EnA} and C_{EnA}, by selection of different capacitance can select whether this IC works with burst mode.

After the selection is done, the current source I_{sele} is turned off. An blanking time of 320µs is given before IC starts to sense the EnA pin voltage latch off enable purpose. This blanking time is used to let the EnA pin votlage be stablized to avoid mistriggering of Latch-off Enable function.

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 13). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 16 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	-0.3	18	V	
V_{HG} Voltage	V_{HG}	-0.3	18	V	
V_{LG} Voltage	V_{LG}	-0.3	18	V	
V_{SHG} Voltage	V_{SHG}	-0.3	18	V	
V_{SLG} Voltage	V_{SLG}	-0.3	18	V	
Timer Voltage	V_{TIMER}	-0.3	V_{dd}+0.3	V	
EnA Voltage	V_{EnA}	-0.3	V_{dd}+0.3	V	
SS Voltage	V_{SS}	-0.3	V_{dd}+0.3	V	
LOAD Voltage	V_{LOAD}	-0.3	V_{dd}+0.3	V	
FREQ Voltage	V_{FREQ}	-0.3	V_{dd}+0.3	V	
FREQ Current	I_{FREQ}	0	3.5	mA	
TD Voltage	V_{TD}	-0.3	V_{dd}+0.3	V	
TD Current	I_{TD}	-200	0	µA	
Delay Voltage	V_{Delay}	-0.3	V_{dd}+0.3	V	
Delay Current	I_{Delay}	-200	0	µA	
Vref Voltage	V_{VR}	-0.3	V_{dd}+0.3	V	
Vref Current	I_{VR}	0	3	mA	
Vmc Voltage	V_{MC}	-0.3	V_{dd}+0.3	V	
Vres Voltage	V_{MC}	-0.3	V_{dd}+0.3	V	
VINS Voltage	V_{VINS}	-0.3	V_{dd}+0.3	V	
CS Voltage	V_{CS}	-0.3	V_{dd}+0.3	V	
CL Voltage	V_{CL}	-0.3	V_{dd}+0.3	V	
CL Current	I_{CL}	-10	2	mA	
SRD Voltage	V_{SRD}	-0.3	V_{dd}+0.3	V	
SRD Current	I_{SRD}	0	2.5	mA	
Junction Temperature	T_j	-40	125	°C	
Storage Temperature	T_S	-55	150	°C	

Thermal Resistance Junction-Ambient for PG-DSO-8	R_{thJA}(DSO)	-	75	K/W	PG-DSO-20
ESD Capability	V_{ESD}	-	2	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCOff}	18	V	
Junction Temperature	T_{jCon}	-25	125	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25 °C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 15 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start up Current	$I_{VCCstart}$		930		µA	V_{VCCon}-0.1V
Supply Current in operation with inactive gate	I_{VCCop}			8	mA	no switching;
Supply Current in normal operation with active gate	$I_{VCCactive}$		7.5		mA	Freq=97kHz R_{FREQ}=15kΩ R_{TD}=180kΩ V_{VCC}=15V V_{CS}>V_{mc}
VCC Turn-On Threshold	V_{VCCon}	11.3	12	12.7	V	
VCC Hysteresis	V_{VCChys}	0.6	1	1.3	V	
VCC Turn-Off Threshold	V_{VCCoff}	-	V_{VCCon} - V_{VCChys}	-	V	
Trimmed Reference Voltage	V_{dd}	4.90	5.0	5.10	V	Guaranteed by design

4.3.2 Oscillator Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Minimum switching frequency	F_{MIN}	48.25	50	51.75	kHz	R_{FMIN}=30kΩ; R_{TD}=180kΩ; V_{SS}=2V
Maximum switching frequency	F_{MAX}	205	215	225	kHz	R_{FMIN_EQ}=6.2kΩ; R_{TD}=180kΩ; V_{SS}=2V
Recommend Maximum switching frequency	F_{MAX_abs}		1000		kHz	R_{FMIN_EQ}=1.1kΩ; R_{TD}=62kΩ; V_{SS}=2V
Reference voltage on FREQ	V_{FREQ}		2		V	
Reference voltage on TD	V_{TD}		2		V	
Dead time	T_d	260	300	330	ns	R_{TD}=180kΩ
Minimum dead time	T_{D_MIN}	115			ns	R_{TD}=62kΩ
Dead time 1	T_{D_MAX1}		870		ns	R_{TD}=560kΩ
Dead time 2	T_{D_MAX2}		1.5		µs	R_{TD}=1200kΩ
Oscillation duty cycle	D	48	50	52	%	based on calculation
First pulse half duty	D_{FISRT}		25		%	First pulse on high side gate at softstart or leaving burst mode or at miss cycle mode

4.3.3 Input voltage sense

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input voltage on threshold	V_{VINSon}	1.2	1.25	1.3	V	
Bias current on VINS pin	I_{hys}	8	10	12	µA	
Blankint time for leaving mains undervoltage protection	T_{VINS_out}		450		µs	
Blanking time for entering mains under voltage protection	T_{VINS_in}		47		µs	
Offset for comparator between VINS pin and Vres pin		-18	0	18	mV	

4.3.4 Current sense and current level

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overcurrent protection 1st	V_{CSL}		0.82		V	
Hysteresis voltage for overcurrent protection low			45		mV	
Overcurrent protection 2nd	V_{CSM}		0.925		V	
Overcurrent protection 3rd	V_{CSH}		1.63		V	
Blanking time for OCP latch	T_{OCP_L}		340		ns	
CL pin clamped voltage	V_{CL_C}	1.89	1.95	2.01	V	V_{CS}=0.6V
Ratio between CL pin and CS pin voltage	R_{CL_CS}		4.8			V_{cs}=0.35V
CL pin maximum source current, output rising	I_{OUTCSL}		1.1		mA	V_{CL}=0V, V_{CS} 0V -> 0.6V step change
CL pin maximum sink current, output falling	I_{INCSL}		6		mA	V_{CL}=1.8V, V_{CS} 0.6V -> 0V step change

4.3.5 Soft start

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Softstart current 1	I_{SS1}		260		µA	V_{SS}=1V
Softstart current 2	I_{SS2}		105		µA	V_{SS}=1.6V
Softstart current 3	I_{SS2}		52.5		µA	V_{SS}=1.9V
Voltage threshold 1	V_{SS1}		1.515		V	
Voltage threshold 2	V_{SS2}		1.815		V	
Voltage threshold 3	V_{SS3}		1.91		V	
Maximum softstart time	T_{SS_MAX}	32	40	48	ms	
Normal softstart time	T_{SS_nom}	8	10	12	ms	After V_{SS} is higher than 1.9V
Discharge resistance 1	R_{SS_dchga}		180		Ω	
Discharge resistance 2	R_{SS_dchgb}		100		Ω	

4.3.6 Light load operation

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Comparator offset for Vmc pin		-25	0	25	mV	
Internal current for hysteresis	I_{MC}	40	50	60	µA	
Entering missing cycle mode blanking time	T_{BL_EM}		20		ms	Test after V_{CS}<V_{MC}

Entering burst mode threshold	V_{EB}	0.07	0.12	0.17	V	
Hysteresis for entering/leaving burst mode	V_{B_Hys}		50		mV	

4.3.7 Reference Voltage

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reference voltage of Vref pin	V_{ref}		5		V	
Current capability of V_{ref} pin	I_{ref_max}			2	mA	guaranteed by design

4.3.8 Over load/Open loop protection

Feedback voltage for open loop/ over load protection	V_{LOAD}	1.73	1.795	1.86	V	V_{LOAD} voltage follows the V_{FREQ} voltage
Fixed over-load blanking time	T_{OLP}		20		ms	
Threshold for adjustable over load blanking time	V_{TH}		4.015		V	
Threshold for adjustable restart time	V_{TL}		0.525		V	
Current for adjustable over load blanking teim	I_{BL}	16	20	24	µA	

4.3.9 Enable function

Current on EnA pin in normal operation	I_{EnA}	94	100	106	µA	-
Current on EnA pin for burst mode selection	I_{sele}	80	100	120	µA	
Charing time for burst mode selection	T_{sele1}	19	26	33	µs	
Threshold for Latch-off Enable	V_{EnA}	0.95	1.0	1.05	V	
Delay for Latch-off Enable	T_{DEnA}		5		µs	guaranteed by design

4.3.10 Synchronous rectification

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reference voltage on SRD	V_{SRD}		2		V	
SR on time setting	T_{SRD}	4.875	5	5.125	µs	R_{SRD}=62kΩ, with typical gate load of 300pf
Rising edge delay between primary and secondary drive	T_{D_ON}	225	250	275	ns	V_{VINS}>V_{RES}
Reference voltage on Delay pin	V_{Delay}		1.785		V	
Minimum Falling edge delay between primary and secondary drive	T_{D_OFF}	270	330	390	ns	R_{Delay}=51kΩ, R_{FREQEQ}=15kΩ
SRD voltage to stop SR externally	V_{SRD_Dis}	1.7	1.75	1.8	V	
SR disable blanking time	T_{SRD_Dis}		775		ns	
SRD voltage when SR is disabled internally	V_{SRD_Stop}			0.2	V	
LOAD voltage to stop SR	V_{LOAD_SRD}	0.18	0.22	0.26	V	
LOAD voltage to restart SR	V_{LOAD_SRR}	0.67	0.715	0.76	V	
CS voltage to stop SR	V_{CS_SRD}	0.875	0.925	0.975	V	V_{CS_SRD} and V_{CS_SRR} follows each other
Blanking time of CS pin 0.9V comparator			220		ns	
CS voltage to restart SR	V_{CS_SRR}	0.575	0.625	0.675		V_{CS_SRD} and V_{CS_SRR} follows each other
CS voltage to start dynamic load detector	V_{CS_DD1}		0.55		V	
CS voltage to set dynamic load protection	V_{CS_DD2}		0.3		V	
SS voltage to stop SR	V_{SS_SRD}	1.765	1.815	1.865	V	
Hysteresis on SS voltage to restart SR	$V_{SS\_SR\_Hys}$	0.06	0.1	0.14	V	
Blanking time for restart SR if V_{SS}>1.9V		8	10	12	ms	
SR softstart steps			8			
SR softstart first time on time		1.2	1.49	1.8	µs	R_{SRD}=62kΩ
Difference between CL clamped voltage and SRD pin reference voltage	V_{SRD}-V_{CL_C}	0	45	90	mv	V_{CS}=0.6V

4.3.11 Primary gate drive (HG, LG)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage at logic low	$V_{GATElow}$		-	1.5	V	V_{VCC}=5V I_{OUT} = 5mA
Output voltage at logic high	$V_{GATEhigh}$		10.5		V	I_{OUT} = -5mA
			9.8		V	V_{VCC}=V_{VCCoff}+0.2V C_L=0.3nF
Rise Time	t_{rise}	-	25	-	ns	C_L = 0.3nF
Fall Time	t_{fall}	-	25	-	ns	C_L = 0.3nF

4.3.12 Secondary gate drive (SHG, SLG)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage at logic low	$V_{GATElow}$		-	1.5	V	V_{VCC}=5V I_{OUT} = 5mA
Output voltage at logic high	$V_{GATEhigh}$		10.5		V	I_{OUT} = -5mA
			9.8		V	V_{VCC}=V_{VCCoff}+0.2V C_L=0.3nF
Rise Time	t_{rise}	-	25	-	ns	C_L = 0.3nF
Fall Time	t_{fall}	-	25	-	ns	C_L = 0.3nF

5 Outline Dimension

PG-DSO-20
(Plastic Dual Small Outline)

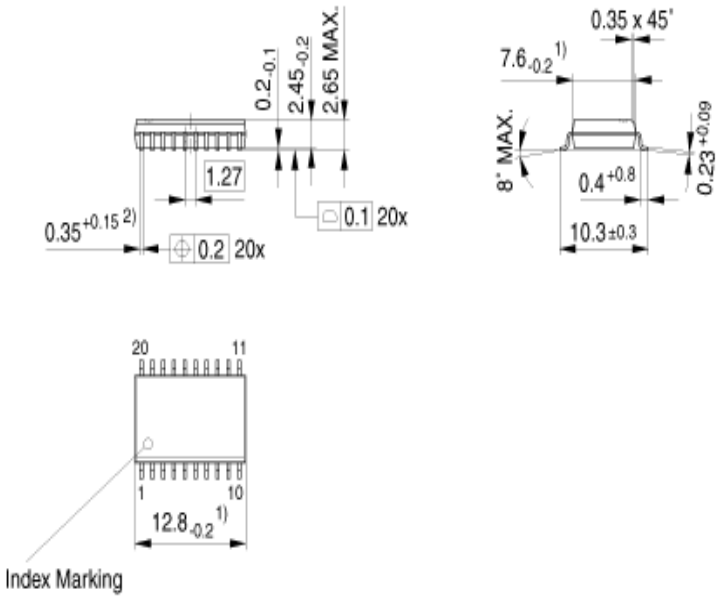

Figure 19 PG-DSO-20

*Dimensions in mm

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