OptiMOS™-5 Power Transistor

AEC Qualified RoHS

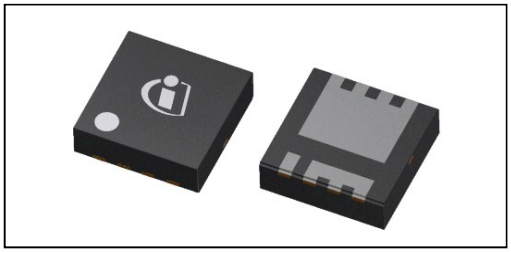
Features

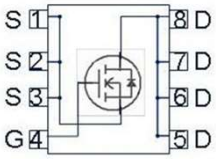
- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	12	mΩ
I_D	40	A

PG-TSDSON-8-33





Type	Package	Marking
IAUZ40N10S5L120	PG-TSDSON-8-33	5N1L120

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	V_{GS}=10 V, Chip limitation[1,2)]	46	A
		V_{GS}=10V, DC current[3)]	40	
		T_a=85 °C, V_{GS}=10 V, R_{thJA} on 2s2p [2,4)]	9	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	160	
Avalanche energy, single pulse[2)]	E_{AS}	I_D=20 A	33	mJ
Avalanche current, single pulse	I_{AS}	-	22	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25 °C	62	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.4	K/W
Thermal resistance, junction - ambient[4]	R_{thJA}	-	-	35.5	-	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=1mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=27 µA	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=100V, V_{GS}=0V, T_j=25°C	-	0.1	1	µA
		V_{DS}=100V, V_{GS}=0V, T_j=125°C[2]	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=20A	-	13.6	18.5	mΩ
		V_{GS}=10V, I_D=20A	-	10.3	12	
Gate resistance[2]	R_G	-	-	1.3	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=50V, f=1MHz	-	1222	1589	pF
Output capacitance	C_{oss}		-	213	277	
Reverse transfer capacitance	C_{rss}		-	12	18	
Turn-on delay time	$t_{d(on)}$	V_{DD}=50V, V_{GS}=10V, I_D=20A, $R_{G,ext}$=3.5Ω	-	3	-	ns
Turn-off delay time	$t_{d(off)}$		-	11	-	
Rise time	t_r		-	1	-	
Fall time	t_f		-	6	-	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V	-	3.8	4.9	nC
Gate to drain charge	Q_{gd}		-	3.3	5.0	
Gate charge total	Q_g		-	17.4	22.6	
Gate plateau voltage	$V_{plateau}$		-	3.1	-	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25°C	-	-	40	A
Diode pulse current[2]	$I_{S,pulse}$	T_C=25 °C	-	-	160	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=20 A, T_j=25°C	-	0.9	1.1	V
Reverse recovery time[2]	t_{rr}	V_R=50V, I_F=40A, di_F/dt=100A/µs	-	38	-	ns
Reverse recovery charge[2]	Q_{rr}		-	34	-	nC

[1] Practically the current is limited by the overall system design including the customer-specific PCB.

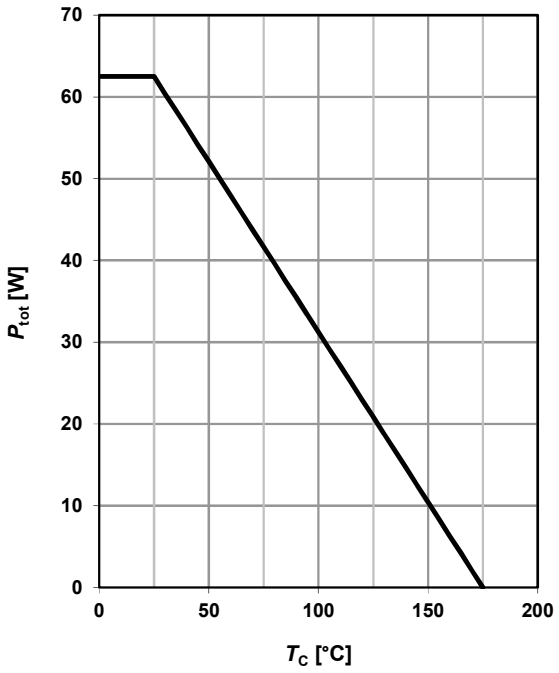
[2] The parameter is not subject to production test - verified by design/characterization.

[3] The product can operate at a specified current based on best practice to minimize electro-migration at the solder joint. For rare events and inrush currents, the value may be exceeded.

[4] Device on a four-layer 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.

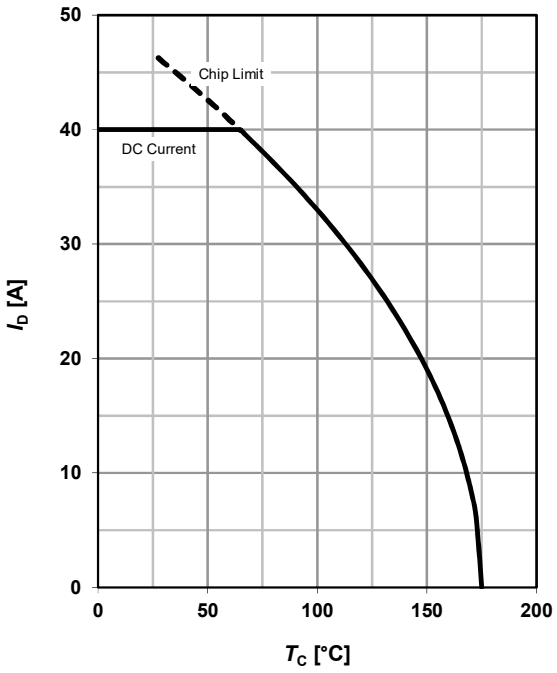
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} = 10$ V



2 Drain current

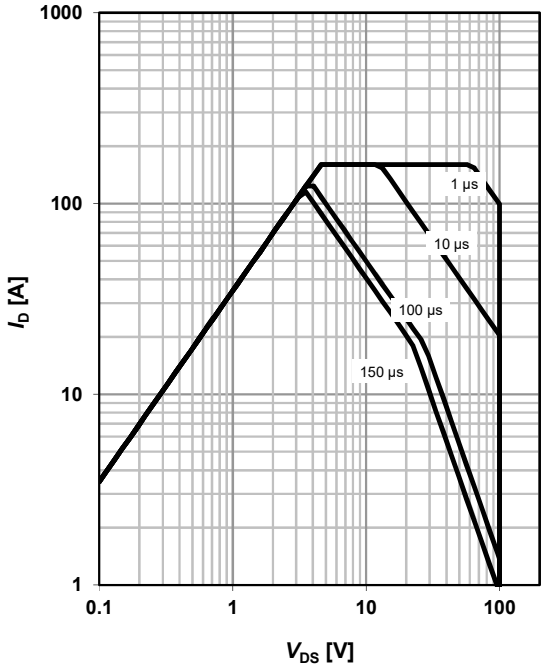
$I_D = f(T_C)$; $V_{GS} = 10$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

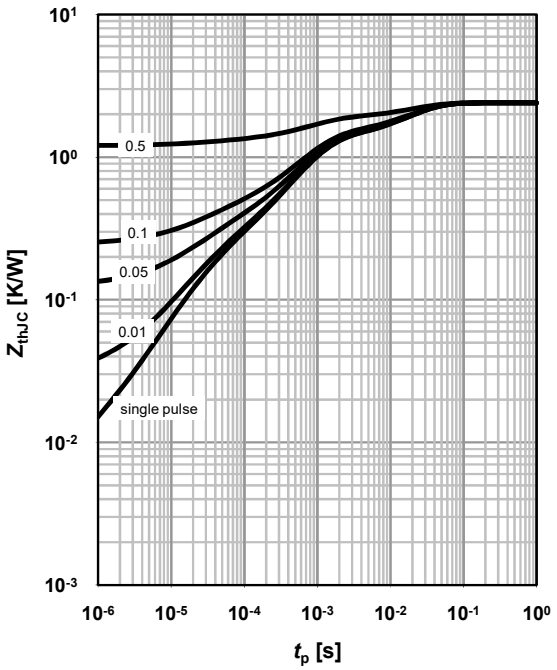
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

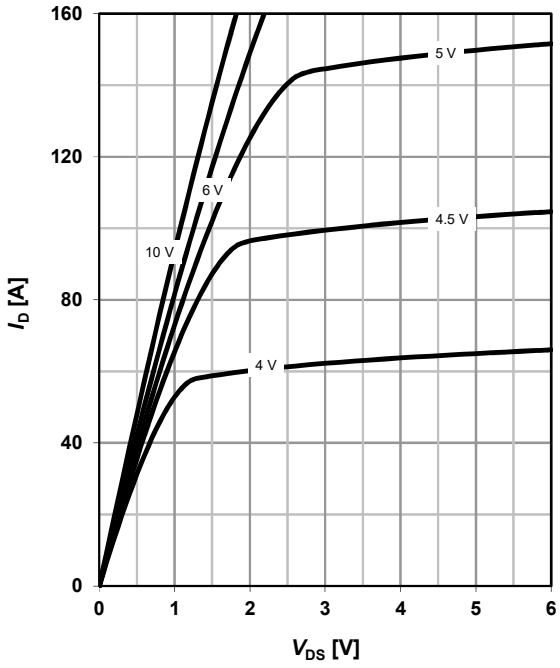
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

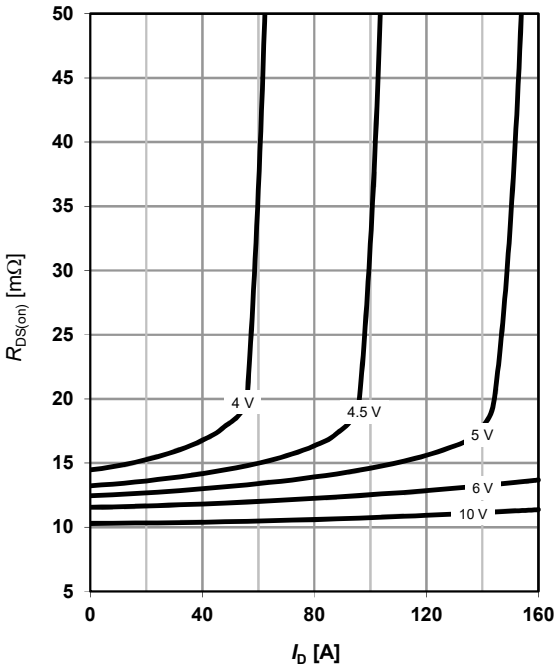
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

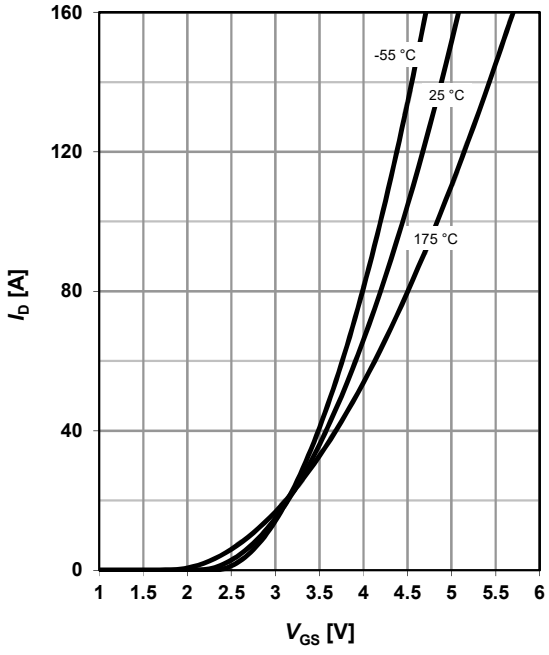
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V

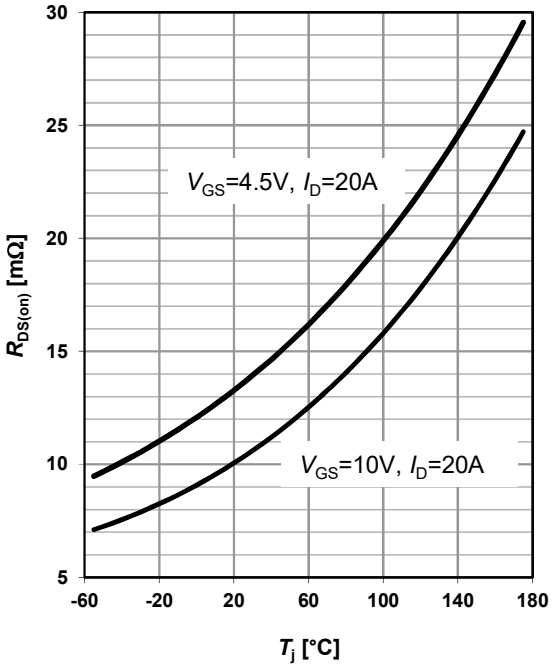
parameter: T_j



8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$;

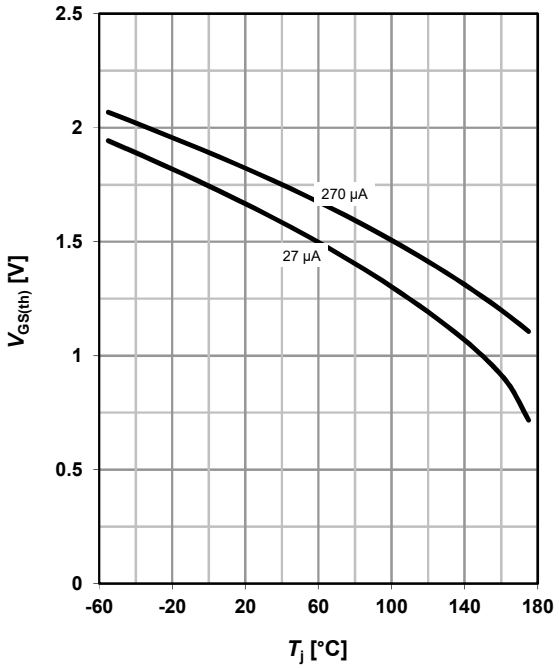
parameter: I_D, V_{GS}



9 Typ. gate threshold voltage

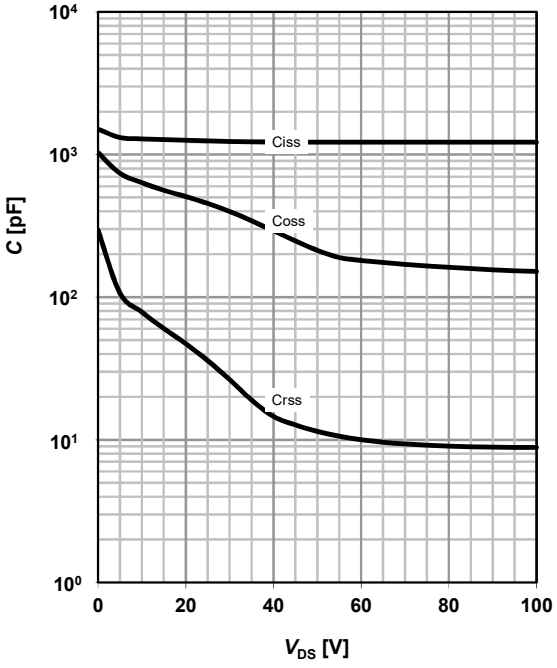
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

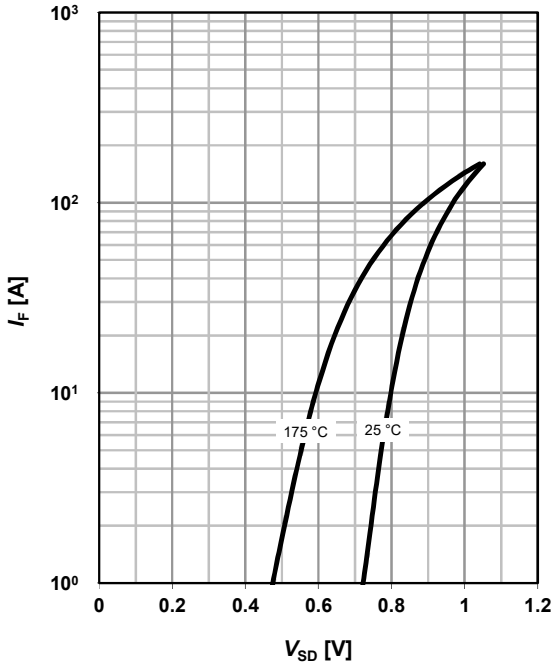
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

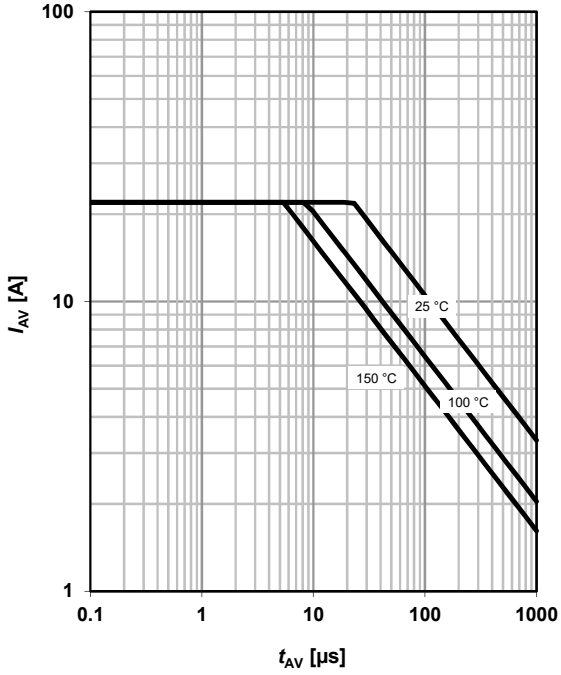
parameter: T_j



12 Avalanche characteristics

$I_{AS} = f(t_{AV})$

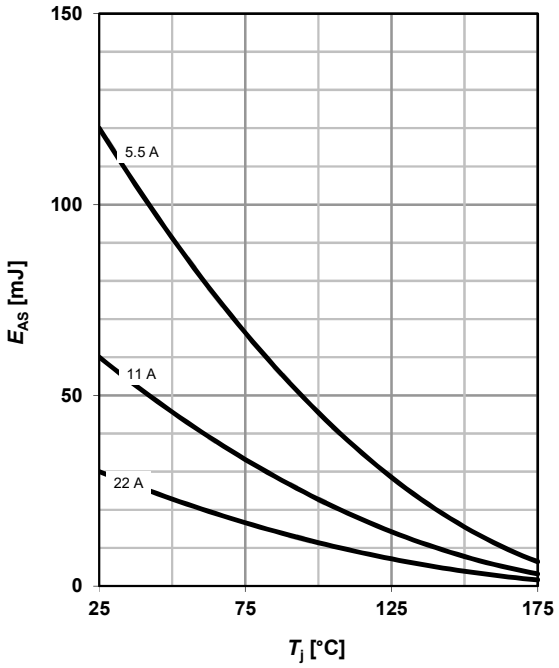
parameter: $T_{j(start)}$



13 Avalanche energy

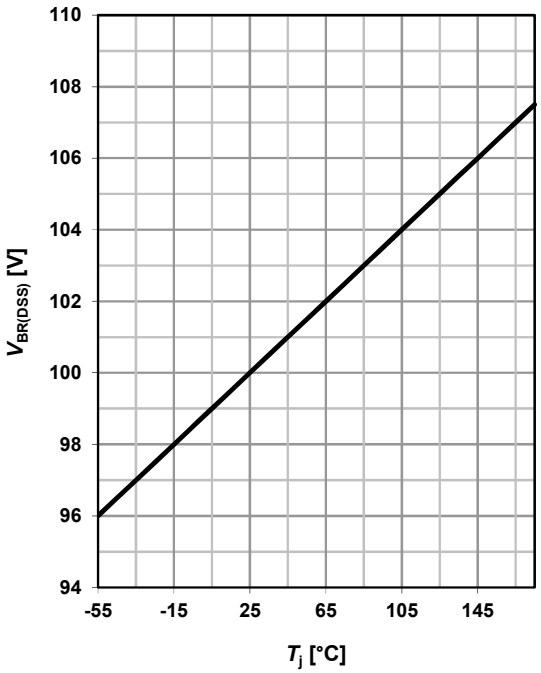
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

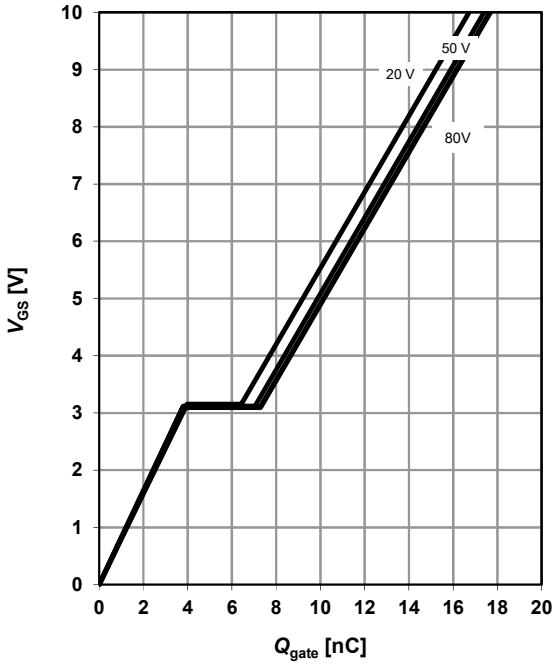
$V_{BR(DSS)} = f(T_j)$; I_D = 1 mA



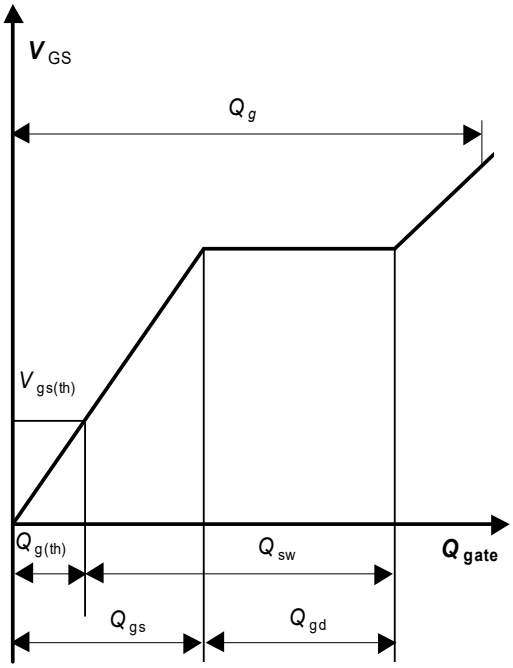
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; I_D = 20 A pulsed

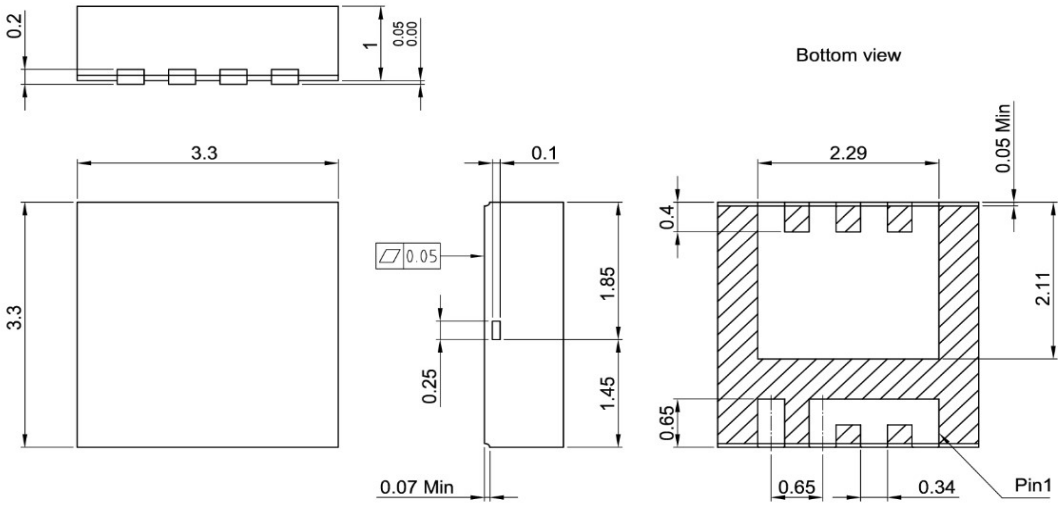
parameter: V_{DD}



16 Gate charge waveforms

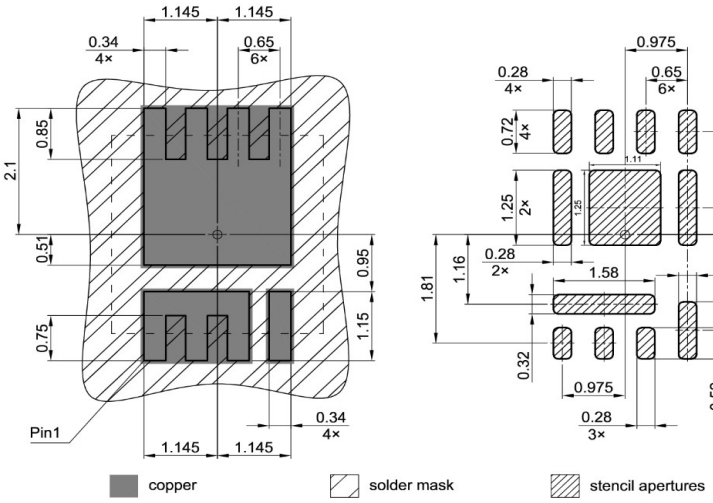


Package Outline



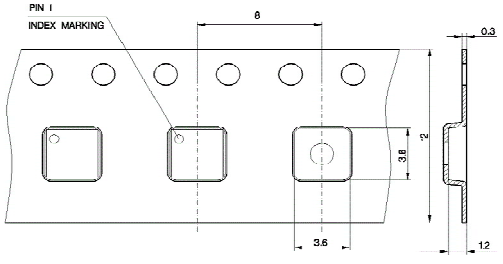
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊣⊕]

Footprint



All undimensioned radii is 0.075
Based on stencil thickness 0.13 mm
All dimensions are in units mm

Packaging



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	2021-05-14	Final Data Sheet
Revision 1.1	2021-06-18	Datasheet file name updated