IAUA180N10S5N029

Automotive MOSFET

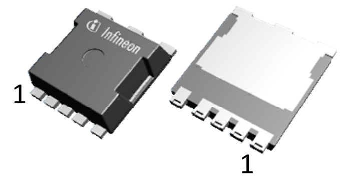
OptiMOS™-5 Power-Transistor

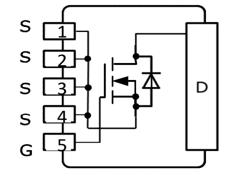
RoHS

Infineon Automotive Quality

AEC Qualified

PG-HSOF-5-4





Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL3 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Potential applications

General automotive applications.

Product Summary

V_{DS}	100	V
$R_{DS(on)}$	2.9	mΩ
I_D (chip limited)	180	A

Type	Package	Marking
IAUA180N10S5N029	PG-HSOF-5-4	5N10029

Table of Contents

Maximum ratings

at Tj=25 °C, unless otherwise specified

Parameter	**Symbol**	**Conditions**	**Value**	**Unit**
Continuous drain current	I_D	V_{GS}=10 V, Chip limitation[1]	180	A
		V_{GS}=10V, DC current[2]	180	
		T_a=85 °C, V_{GS}=10 V, R_{thJA} on 2s2p[2,3]	24	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C, t_p= 100 µs	561	
Avalanche energy, single pulse[2]	E_{AS}	I_D=90 A	220	mJ
Avalanche current, single pulse	I_{AS}	-	150	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25 °C	221	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Thermal characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	-	-	0.68	K/W
Thermal resistance, junction - ambient[3)]	R_{thJA}	–	-	22.8	-	

Electrical characteristics

at Tj=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=130 µA	2.2	3	3.8	
Zero gate voltage drain current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=100 V, V_{GS}=0 V, T_j=100 °C[2)]	-	1	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=6 V, I_D=45 A	-	2.8	3.4	mΩ
		V_{GS}=10 V, I_D=90 A	-	2.3	2.9	
Gate resistance[2)]	R_G	-	-	1.4	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz	-	5902	7673	pF
Output capacitance	C_{oss}		-	947	1231	
Reverse transfer capacitance	C_{rss}		-	37	55	
Turn-on delay time	$t_{d(on)}$	V_{DD}=50 V, V_{GS}=10 V, I_D=90 A, R_G=3.5 Ω	-	14	-	ns
Rise time	t_r		-	7	-	
Turn-off delay time	$t_{d(off)}$		-	28	-	
Fall time	t_f		-	17	-	
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=50 V, I_D=90 A, V_{GS}=0 to 10 V	-	28	36	nC
Gate to drain charge	Q_{gd}		-	16	24	
Gate charge total	Q_g		-	81	105	
Gate plateau voltage	$V_{plateau}$		-	4.7	-	V
Reverse Diode						
Diode continous forward current[2)]	I_S	T_C=25 °C	-	-	180	A
Diode pulse current[2)]	$I_{S,pulse}$	T_C=25 °C, t_p= 100 µs	-	-	561	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=90 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time[2)]	t_{rr}	V_R=50 V, I_F=50A, di_F/dt =100 A/µs	-	62	-	ns
Reverse recovery charge[2)]	Q_{rr}		-	99	-	nC

[1)] Practically the current is limited by the overall system design including the customer-specific PCB.

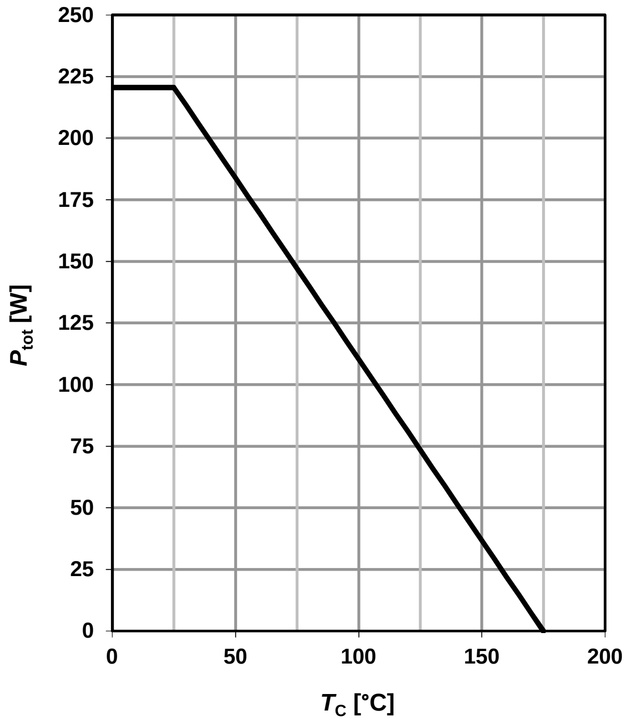
[2)] The parameter is not subject to production testing – specified by design.

[3)] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

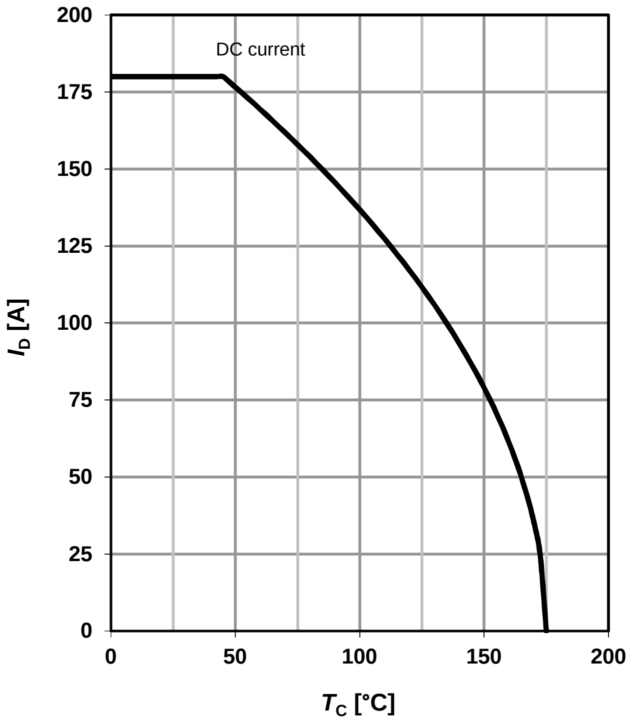
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



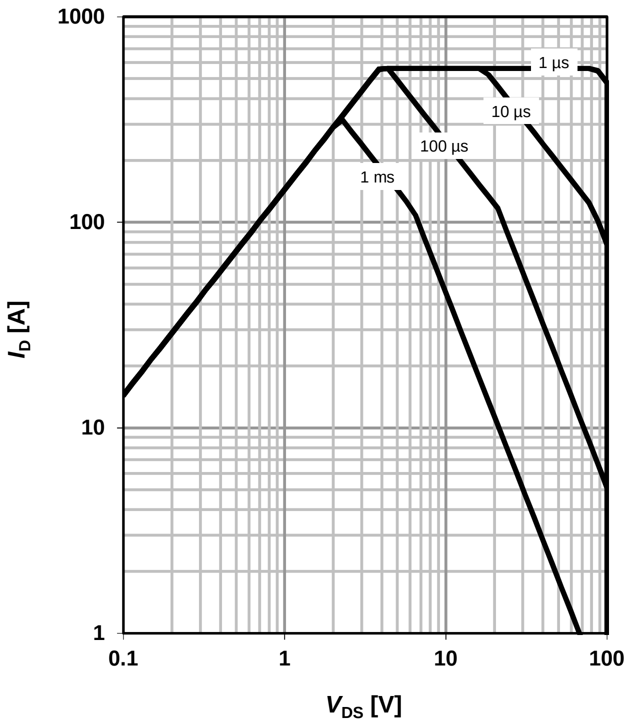
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6$ V



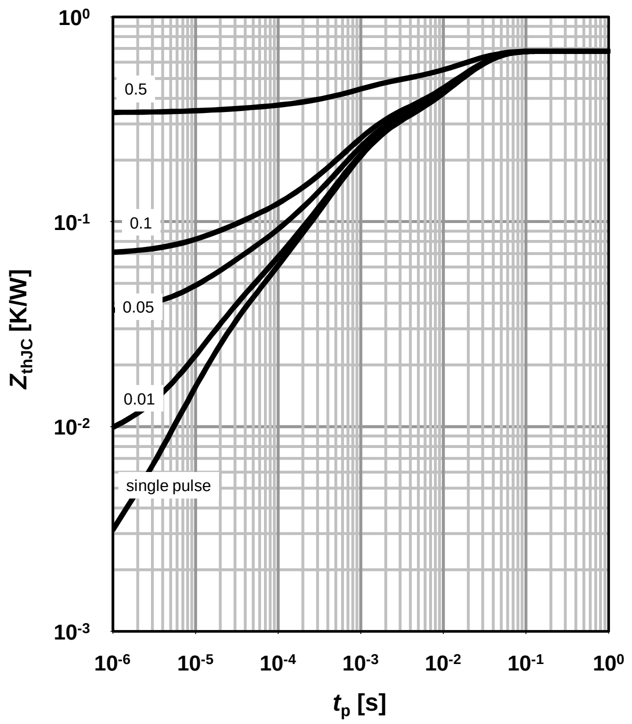
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



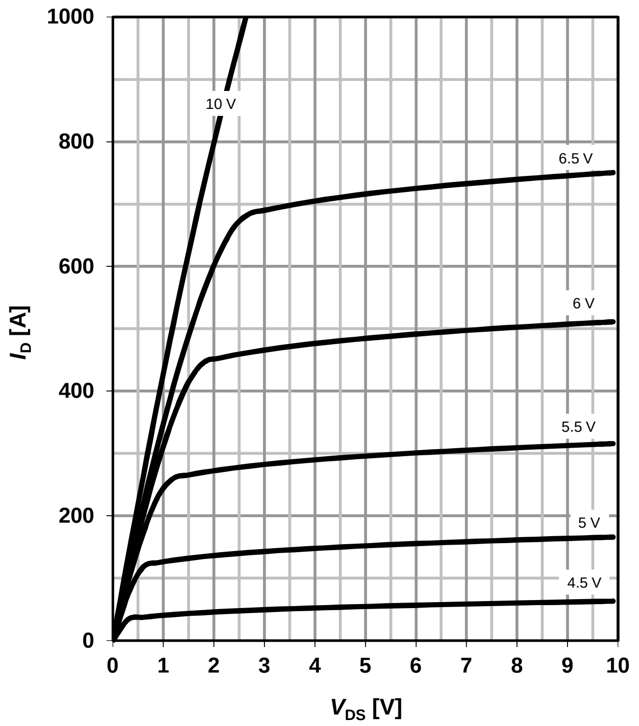
4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$



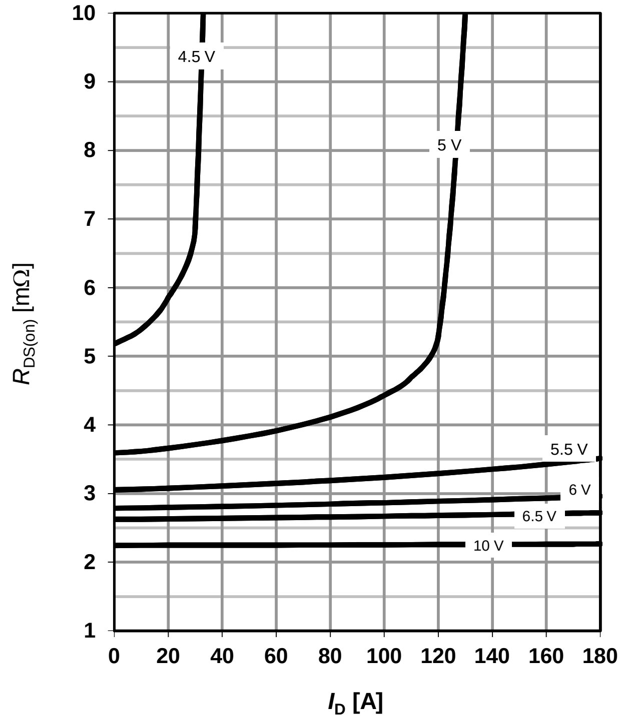
5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



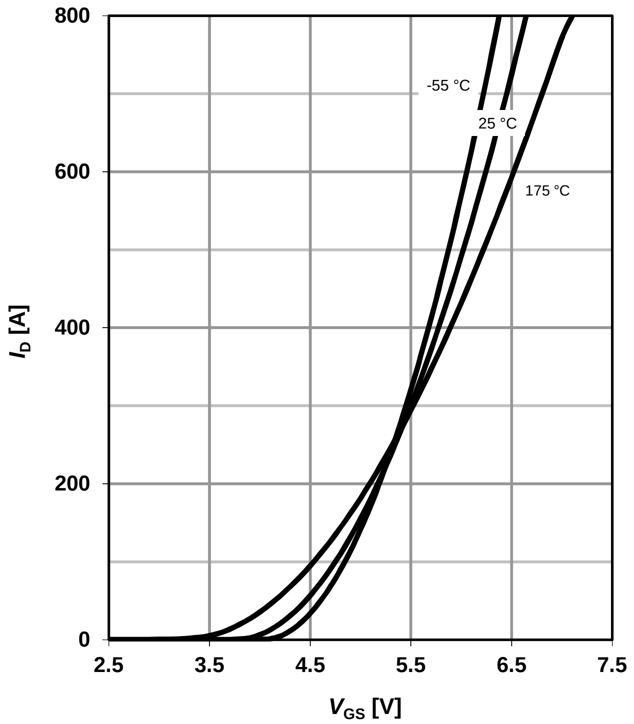
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



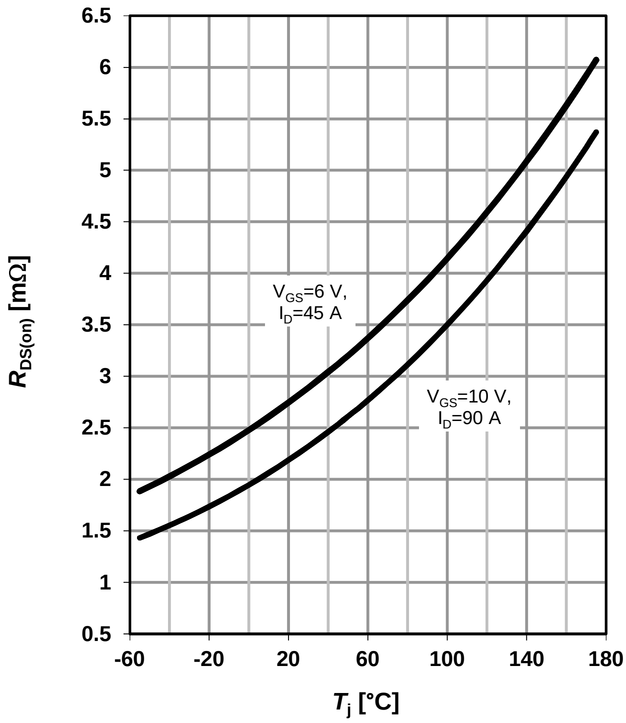
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V: parameter: T_j



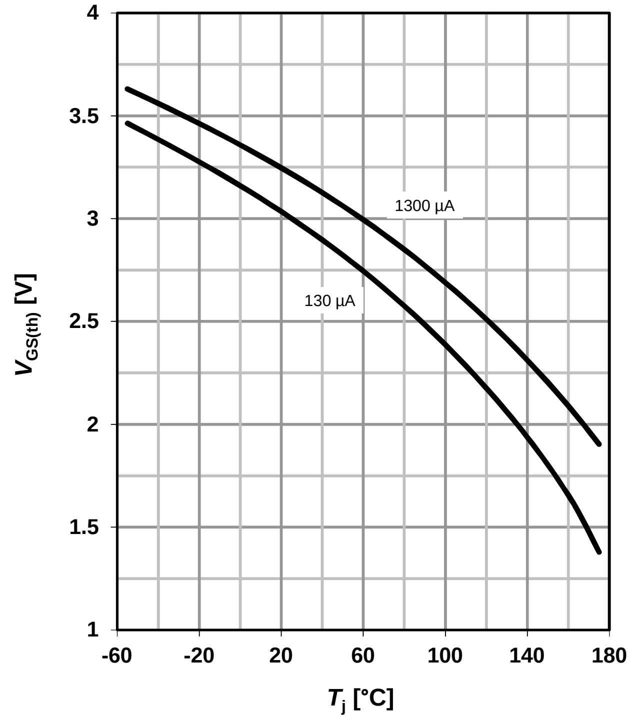
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



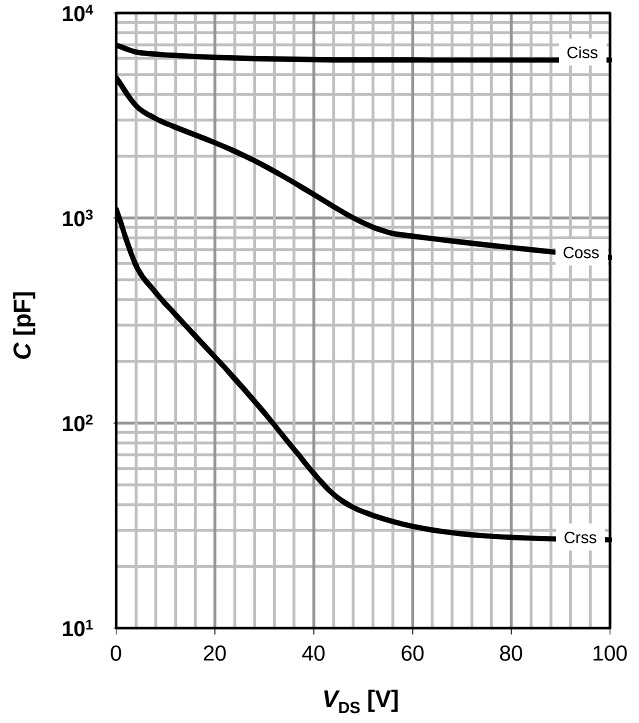
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



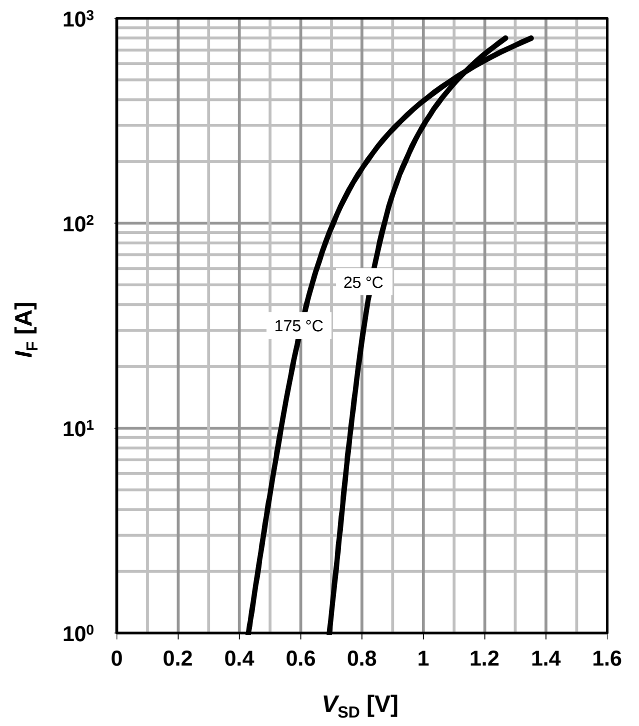
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



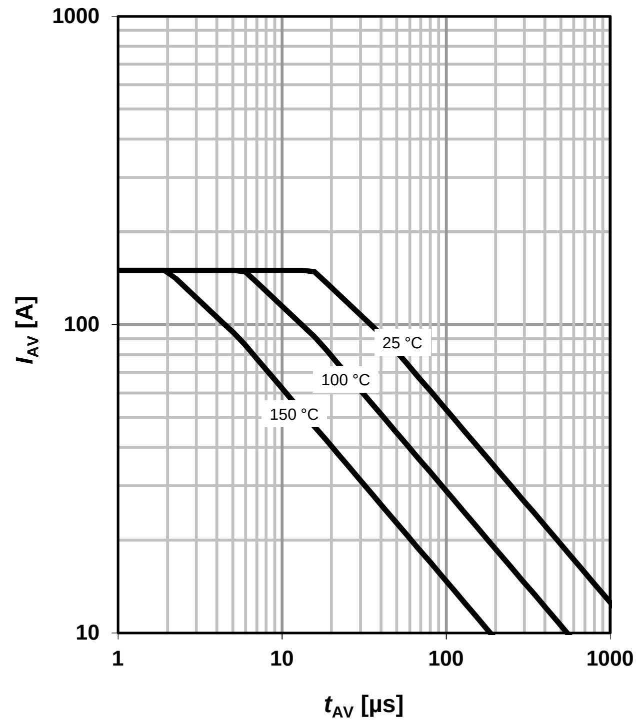
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



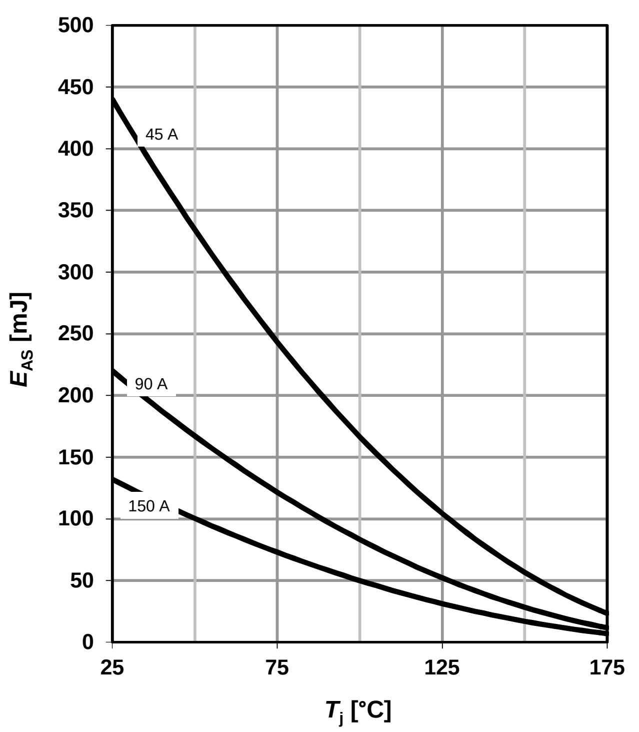
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



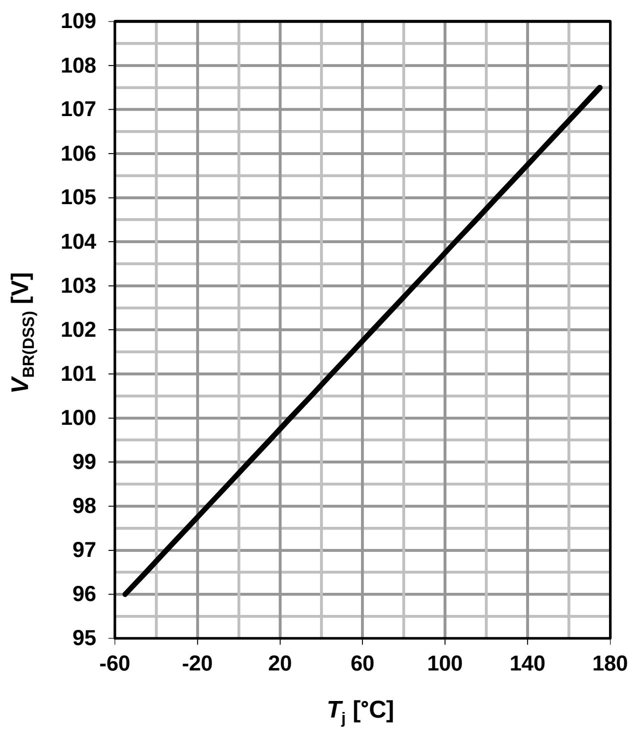
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: ID



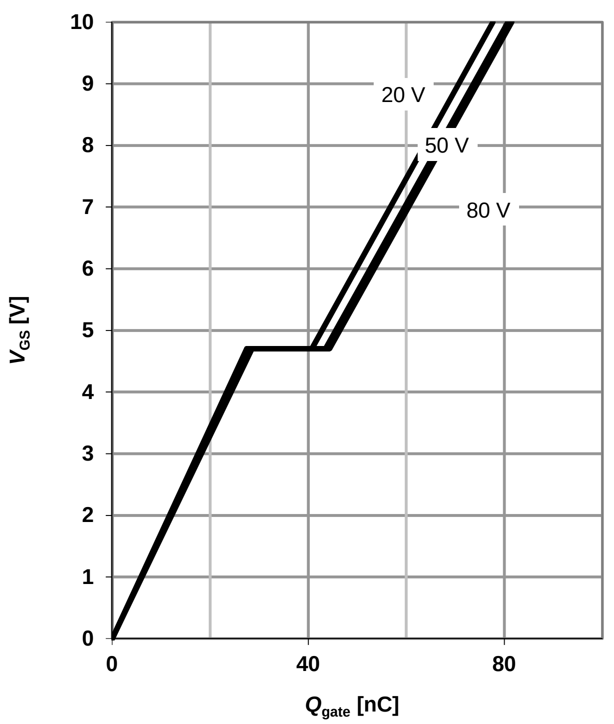
14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; $I_{D\_typ} = 1$ mA

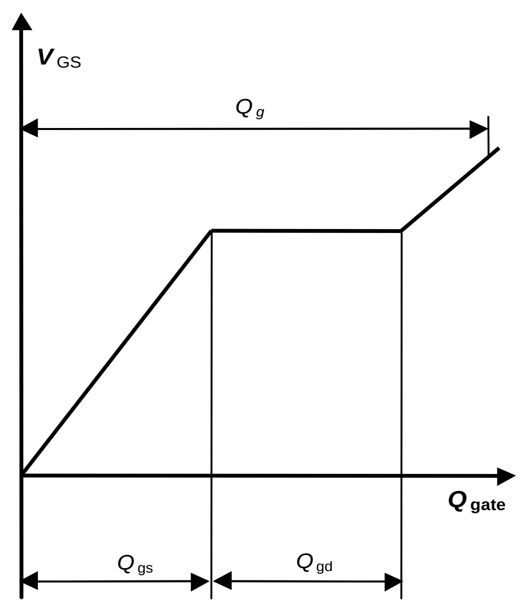


15 Typ. gate charge

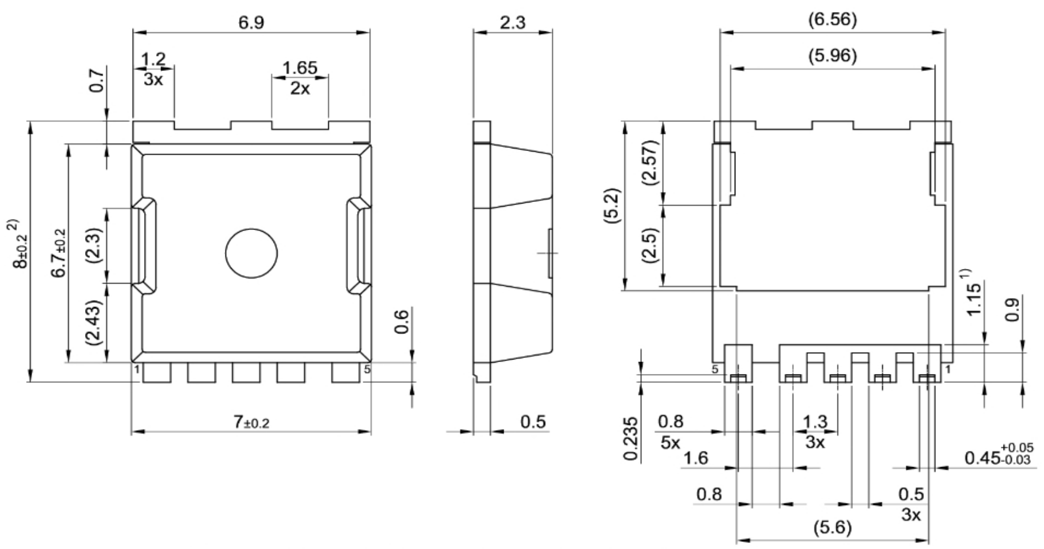
$V_{GS} = f(Q_{gate})$; $I_D = 90$ A pulsed; parameter: V_{DD}



16 Gate charge waveforms

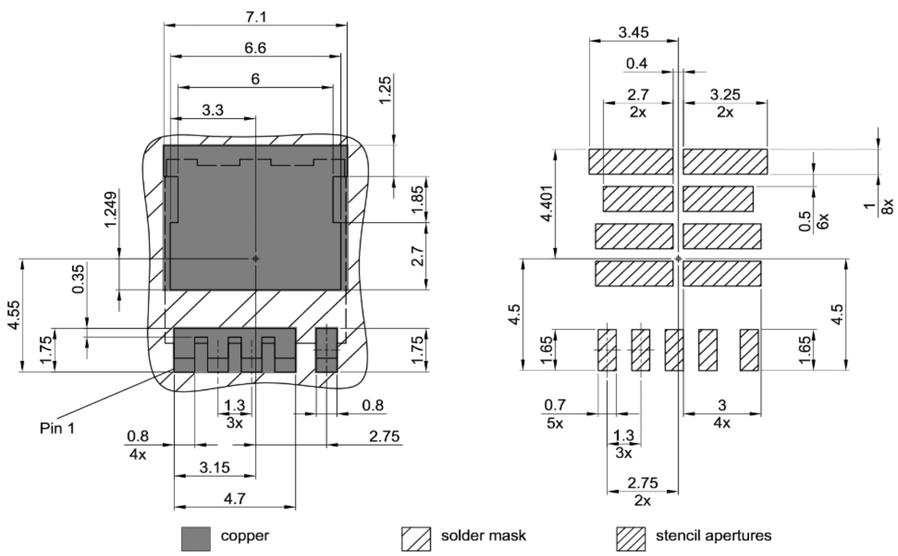


Package Outline



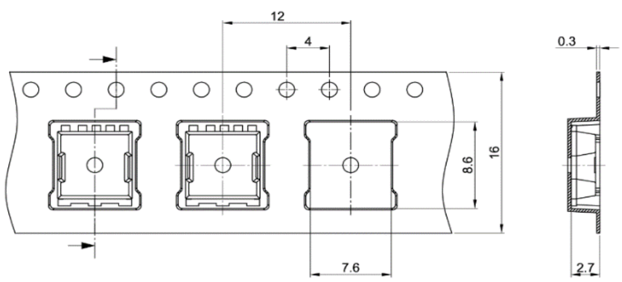
1) Lead length up to anti flash profile; mold flashes excluded
2) Excluding burr
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Footprint



All dimensions are in units mm

Packaging



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Revision History

Revision	Date	Changes
Revision 1.0	17.03.2021	Final Datasheet
Revision 1.1	12.11.2021	Corrected figure 14

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Email: erratum@infineon.com