

# AN2019-21 EVAL-1ED3121Mx12H

## Evaluation board description

### About this document

#### Scope and purpose

The gate driver evaluation board EVAL-1ED3121Mx12H with the 1ED3121MU12H or 1ED3121MC12H gate driver IC demonstrates the functionality and key features of the Infineon EiceDRIVER™ Compact gate driver ICs.

The boards contain a short circuit protection which is described in more detail in the key feature section of this document.

Details about the EiceDRIVER™ Compact 1ED3121MU12H or 1ED3121MC12H can be found at our product pages at <https://www.infineon.com/gd> or the product search.

The design of the EVAL-1ED3121Mx12H was performed with respect to the environmental conditions described in this document. The design was tested as described in this document, but not qualified regarding manufacturing, lifetime or over the full range of ambient operating conditions. The boards provided by Infineon are not subject to full production test.

Evaluation boards are not subject to the same procedures as regular products regarding Returned Material Analysis (RMA), Process Change Notification (PCN) and Product Discontinuation (PD). Evaluation boards are intended to be used under laboratory conditions and by trained specialists only.

#### Intended audience

- Engineers who want to learn how to use the Infineon EiceDRIVER™
- Experienced design engineers designing circuits with Infineon EiceDRIVER™, IGBT and CoolSiC™ MOSFET
- Design engineers designing power electronic devices, like inverters

### Table of contents

|          |                                                                          |    |
|----------|--------------------------------------------------------------------------|----|
|          | <b>Table of contents</b> .....                                           | 1  |
| <b>1</b> | <b>Electrical description</b> .....                                      | 2  |
| 1.1      | Key features .....                                                       | 2  |
| 1.2      | Absolute maximum ratings, operating conditions and supply voltages ..... | 2  |
| 1.3      | Start-up .....                                                           | 4  |
| 1.4      | Overcurrent protection .....                                             | 4  |
| 1.5      | Connectors and pin assignment .....                                      | 5  |
| <b>2</b> | <b>Schematics</b> .....                                                  | 6  |
| <b>3</b> | <b>PCB layout</b> .....                                                  | 10 |
| <b>4</b> | <b>Bill of material</b> .....                                            | 11 |
|          | <b>Disclaimer</b> .....                                                  | 13 |

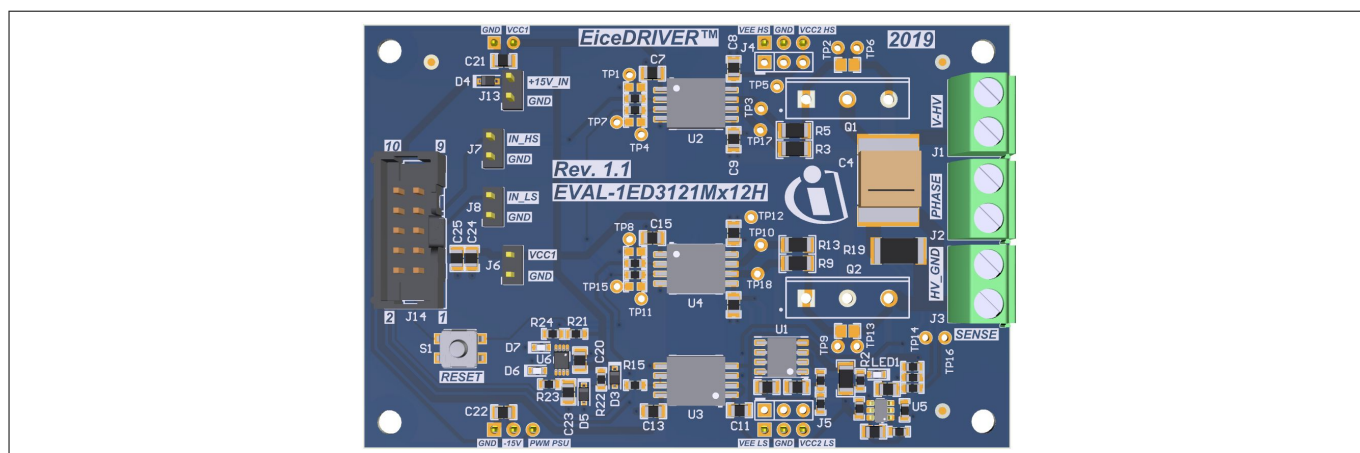
## 1 Electrical description

# 1 Electrical description

## 1.1 Key features

The evaluation board EVAL-1ED3121Mx12H is intended for the product feature evaluation of the Infineon EiceDRIVER™ Compact 1ED3121MU12H or 1ED3121MC12H in an application circuit. The key elements of the board and the product are listed here.

- Evaluation board in half-bridge configuration with two gate driver ICs to drive power switches such as IGBTs and SiC MOSFETs. The switch type can be freely chosen as seen in [Figure 1](#)
- Additional gate driver IC for isolated over-current feedback signal from high voltage side to logic control side
- Fast operational amplifier used as comparator for over-current detection



**Figure 1** EVAL-1ED3121Mx12H top view

The board has a size of 85 x 55 x 15 mm<sup>3</sup>. Power switches are not included in this evaluation board and need to be ordered separately.

This board is best suited for so-called double-pulse testing. However, it requires additional considerations on thermal and power load for continuous operation. An additional high-voltage DC blocking capacitor at the high-voltage supply is recommended.

The low-voltage interface can be controlled by a pulse generator, a microcontroller or other digital circuits.

For safe operation, a fast over-current detection and protection circuit is implemented with a galvanically isolated feedback path to the low-voltage input side. The input side flip-flop latches the over-current event information. This circuit will report the fault and turn off both gate driver ICs. The S1 button, also labeled with *RESET*, clears the flip-flop to enable the gate driver ICs again.

## 1.2 Absolute maximum ratings, operating conditions and supply voltages

The selected components on this evaluation board as well as the gate driver ICs have maximum ratings and operating conditions to avoid damaging the individual parts and the evaluation board overall.

**Table 1** Absolute maximum ratings

| Pin/parameter name | Abs. Max.   | Unit | Note                          |
|--------------------|-------------|------|-------------------------------|
| +15V_IN            | -0.2 ... 20 | V    | input, support supply voltage |

(table continues...)

## 1 Electrical description

**Table 1** (continued) **Absolute maximum ratings**

| Pin/parameter name | Abs. Max.           | Unit | Note                                                                                                              |
|--------------------|---------------------|------|-------------------------------------------------------------------------------------------------------------------|
| VCC1               | -0.2 ... 5.3        | V    | input, gate driver IC supply voltage                                                                              |
| FAULT              | -0.2 ... VCC1 + 0.2 | V    | output, digital signal                                                                                            |
| RST                | -0.2 ... VCC1 + 0.2 | V    | input, digital signal                                                                                             |
| IN_HS              | -0.2 ... VCC1 + 0.2 | V    | input, digital signal                                                                                             |
| IN_LS              | -0.2 ... VCC1 + 0.2 | V    | input, digital signal                                                                                             |
| VCC2_HS,VCC2_LS    | -0.2 ... 40         | V    | overall isolated secondary supply with reference to VEE2_HS/VEE2_LS                                               |
| VCC2_HS,VCC2_LS    | -0.2 ... 25         | V    | positive secondary supply voltage with reference to GND2_HS/GND2_LS                                               |
| GND2_HS,GND2_LS    | -0.2 ... 25         | V    | gate reference supply pin with reference to VEE2_HS/VEE2_LS                                                       |
| V-HV               | -0.2 ... 1200       | V    | input, high-voltage supply, for voltages above 42 V, special high voltage lab environment is strongly recommended |
| Phase peak current | 25                  | A    | phase peak current for double pulse tests                                                                         |
| $t_{\text{pulse}}$ | 100                 | μs   | maximum ON pulse length for double-pulse tests                                                                    |
| $f_{\text{sw}}$    | 100                 | kHz  | maximum switching frequency for continuous operation, careful consideration of power dissipation required         |

The PCB assembly is optimized for a VCC1 supply voltage of 3.3 V. For higher supply voltages, adjustment to the current limiting resistors of the status LEDs is required.

**Table 2** **Operating conditions and supply voltages**

| Pin name        | Min. | Typ. | Max.      | Unit | Note                                                                |
|-----------------|------|------|-----------|------|---------------------------------------------------------------------|
| +15V_IN         | 15.5 | 16   | 16.5      | V    | input, support supply voltage                                       |
| VCC1            | 3.2  | 3.3  | 3.4       | V    | input, gate driver IC supply voltage                                |
| FAULT           | -0.1 | 3.3  | VCC1+ 0.1 | V    | output, digital signal                                              |
| RST             | -0.1 | 3.3  | VCC1+ 0.1 | V    | input, digital signal                                               |
| IN_HS           | -0.1 | 3.3  | VCC1+ 0.1 | V    | input, digital signal                                               |
| IN_LS           | -0.1 | 3.3  | VCC1+ 0.1 | V    | input, digital signal                                               |
| VCC2_HS,VCC2_LS | 12   | 15   | 30        | V    | overall isolated secondary supply with reference to VEE2_HS/VEE2_LS |

**(table continues...)**

## 1 Electrical description

**Table 2** (continued) Operating conditions and supply voltages

| Pin name                | Min. | Typ. | Max. | Unit | Note                                                                                                              |
|-------------------------|------|------|------|------|-------------------------------------------------------------------------------------------------------------------|
| <i>GND2_HS, GND2_LS</i> | 0    |      | 15   | V    | gate reference supply pin with reference to <i>VEE2_HS/VEE2_LS</i>                                                |
| <i>V-HV</i>             | 25   |      | 600  | V    | input, high voltage supply, for voltages above 42 V, special high voltage lab environment is strongly recommended |

### 1.3 Start-up

Follow the steps below to set up, power up and perform first evaluations with the board.

#### Prerequisites

- Assemble fitting power switches at the location Q1 and Q2, e.g. IKQ75N120CH3 IGBTs
- Assemble an external high-voltage DC capacitor (> 100 µF) between *J1-1/2 (V-HV)* and *J3-2 (HV\_GND)*
- Have low-voltage power supplies ready for input support and logic supply (+15V\_IN, VCC1)
- Have isolated low-voltage power sources ready for gate driver output supply (VCC2\_LS, VCC2\_HS, GND2\_LS, GND2\_HS, VEE2\_LS and VEE2\_HS)
- Have a high-voltage power supply ready for HV-DC between *J1-1/2 (V-HV)* and *J3-2 (HV\_GND)*
- Have an inductive load for double-pulse tests ready
- Have a dual channel PWM generator ready for half-bridge PWM input

To adapt the circuit to the application requirements, resistor or capacitor values can be changed to optimize the performance.

#### Power-up sequence

1. Supply +15V\_IN at connector *J13.2* with +16 V and connect supply *GND* to connector *J13.1*
2. Supply VCC1 at connector *J6.2* with +3.3 V and connect supply *GND* to connector *J6.1*
3. The red LED D7 will turn on
4. Supply both secondary gate driver supplies with individual power sources at VCC2\_HS, GND2\_HS, and VEE2\_HS at connector *J4*, and VCC2\_LS, GND2\_LS and VEE2\_LS at connector *J5* according to the assembled power switch needs
5. The green LED1 will turn on
6. Push S1 to reset the error flip-flop
7. The red LED D7 will turn off and green LED D6 will turn on
8. Connect the digital PWM generator to the digital interface connectors *J7* and *J8* labeled with *IN\_HS* and *GND* as well as *IN\_LS* and *GND*
9. Connect the high-voltage supply to connector *J1.1* or *J1.2* and *HV\_GND* to *J3.2*.
10. Connect one end of the inductive load to *J2.1* and the other end according to the double-pulse requirements to either *J1.1* or *J3.2* (low side or high side testing)
11. The board is now ready for double-pulse evaluation

### 1.4 Overcurrent protection

An overcurrent protection is implemented to protect the board and components against high current. The current is determined by measuring the voltage across the shunt resistor R19. This is available at the two test points TP14 and TP16.

The detection circuit measures the voltage across R19, sends the signal through a low pass filter R18 and C18 and compares it to a reference voltage with the comparator U5. The reference voltage is defined by the voltage

## 1 Electrical description

divider R12 and R20. The trip point is at approx. 32 A and can be adapted to application requirements by changing R19 and/or adapting the reference voltage divider R12 and R20.

The output signal is transferred with U3 to the low voltage domain to trigger the flip-flop and store the overcurrent event. Once the flip-flop is triggered, it turns off both gate driver ICs by the *ENABLE* signal. In addition, it reports the overcurrent event to the digital interface connector as *FAULT* signal and turns the LED7 on.

To return to normal operation, S1 needs to be pushed to reset the flip-flop. As a feedback, LED7 turns off and LED6 turns back on again.

### 1.5 Connectors and pin assignment

The following table describes connectors and their pin assignments on the PCB.

**Table 3** Connectors and pin assignment

| Connector                 | Pin  | Marking/<br>function | Note                                                    |
|---------------------------|------|----------------------|---------------------------------------------------------|
| J1                        | 1, 2 | V-HV                 | High voltage power supply                               |
| J2                        | 1, 2 | PHASE                |                                                         |
| J3                        | 1    | SENSE                |                                                         |
| J3                        | 2    | HV_GND               |                                                         |
| J4, J9                    | 1    | VEE2_HS              | High side negative gate driver supply                   |
| J4, J9                    | 2    | GND2_HS              | High side gate driver supply reference                  |
| J4, J9                    | 3    | VCC2_HS              | High side positive gate driver supply                   |
| J5, J10                   | 1    | VEE2_LS              | Low side negative gate driver supply                    |
| J5, J10                   | 2    | GND2_LS              | Low side gate driver supply reference                   |
| J5, J10                   | 3    | VCC2_LS              | Low side positive gate driver supply                    |
| J6, J7, J8, J11, J12, J13 | 1    | GND                  | Logic side ground reference                             |
| J6, J12                   | 2    | VCC1                 | Logic side supply voltage, 3.3 V or 5 V                 |
| J7                        | 2    | IN_HS                | Logic PWM input high side gate driver                   |
| J8                        | 2    | IN_LS                | Logic PWM input low side gate driver                    |
| J11                       | 2    | +15V                 | 15 V for external power supply without protection diode |
| J11                       | 3    | PWM_PSU              | PWM output for external power supply from J14.9         |
| J13                       | 2    | +15V_IN              | 15 V input supply voltage for external power supply     |
| J14                       | 1, 2 | n.c.                 | not connected                                           |
| J14                       | 3    | VCC1                 | Logic side supply voltage, 3.3 V or 5 V                 |
| J14                       | 4    | GND                  | Logic side ground reference                             |
| J14                       | 5    | RST                  | Reset input for overcurrent flip-flop, connected to S1  |
| J14                       | 6    | FAULT                | Fault feedback signal                                   |
| J14                       | 7    | IN_HS                | Logic PWM input high side gate driver                   |

(table continues...)

## 2 Schematics

**Table 3** (continued) **Connectors and pin assignment**

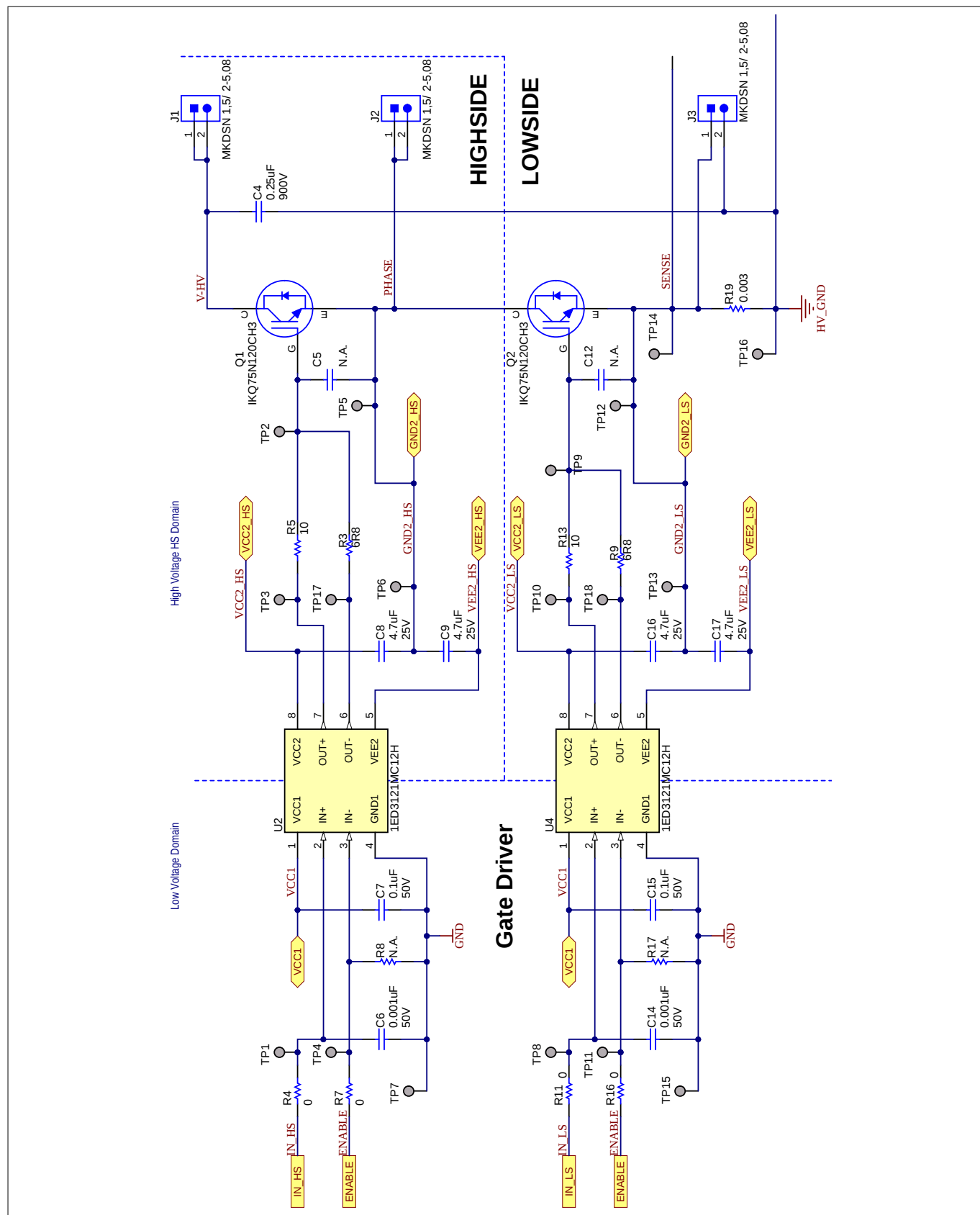
| Connector | Pin | Marking/<br>function | Note                                                    |
|-----------|-----|----------------------|---------------------------------------------------------|
| J14       | 8   | <i>IN_LS</i>         | Logic PWM input low side gate driver                    |
| J14       | 9   | <i>PWM_PSU</i>       | PWM input for external power supply to J11.3            |
| J14       | 10  | <i>+15V</i>          | 15 V for external power supply without protection diode |

## 2 Schematics

The schematics of the evaluation board are separated into the following parts:

- Gate driver ICs with surrounding circuit
- Overcurrent detection
- Overcurrent status display
- Interfaces with connectors and reset switch

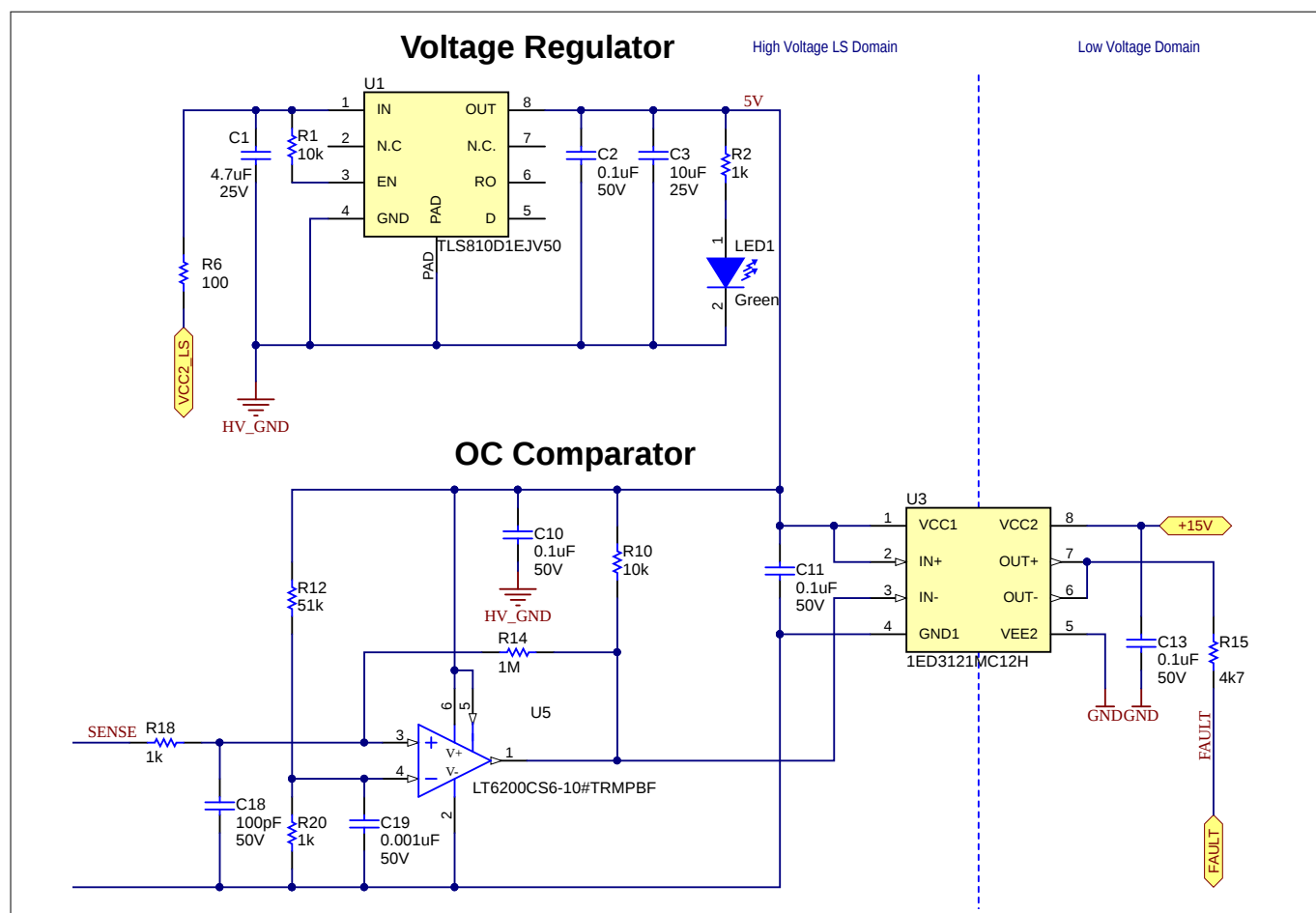
## 2 Schematics



**Figure 2 Schematic of gate driver ICs and surrounding circuits**

Gate driver circuit with optional external input filter, output gate resistors for source and sink connection.

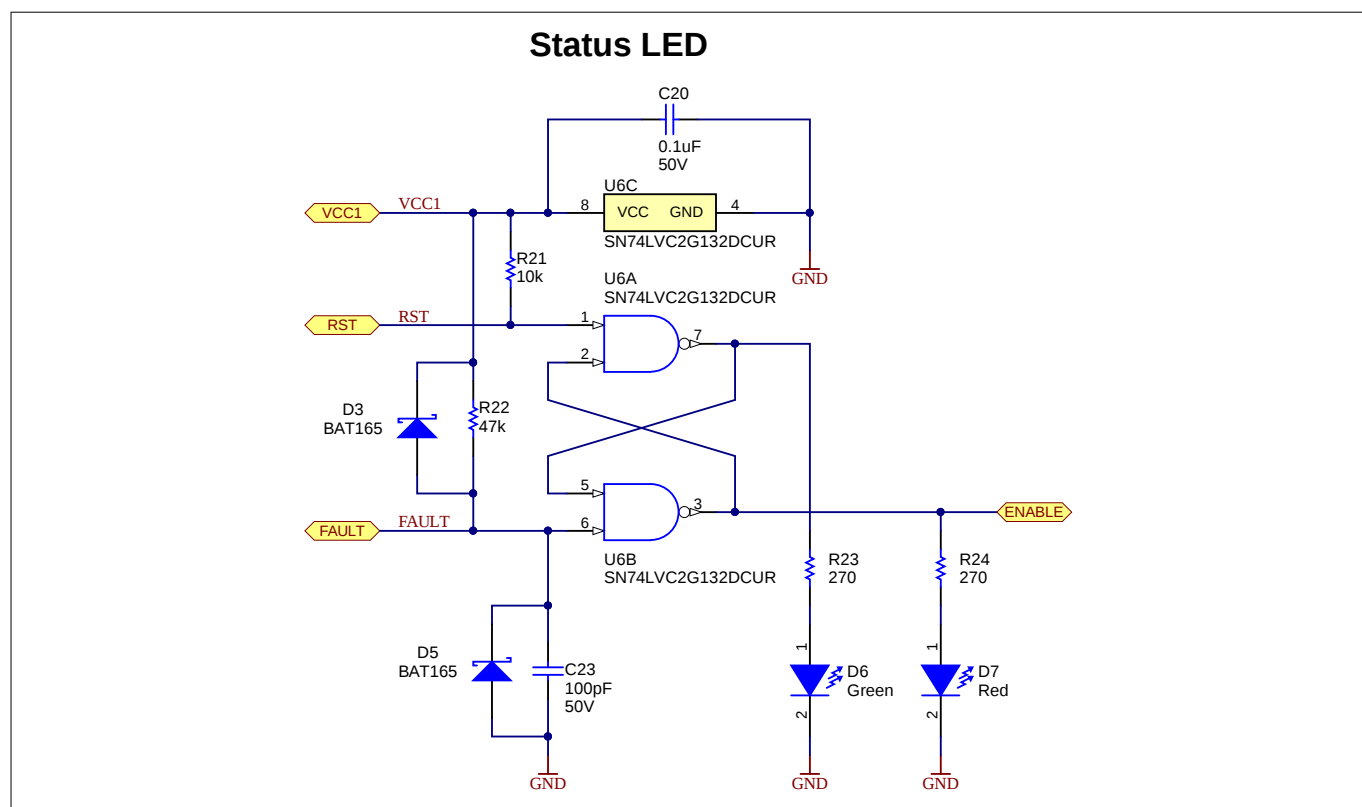
## 2 Schematics



**Figure 3 Schematic of overcurrent detection circuit**

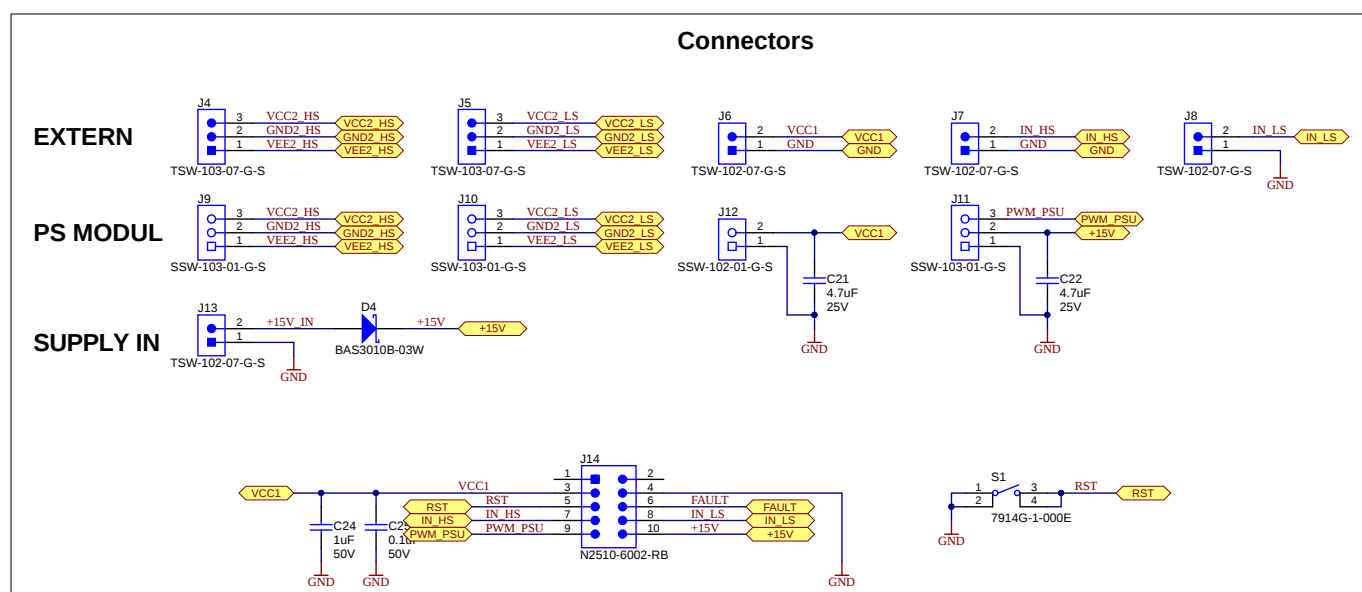
Overcurrent comparator with additional gate driver IC for isolated signal transmission and supporting voltage regulator.

## 2 Schematics



**Figure 4 Schematic of overcurrent status indication**

Fault signal and reset input of flip-flop including status LEDs.



**Figure 5 Schematic of connectors and reset switch**

Interface connectors and reset button.



#### 4 Bill of material

## 4 Bill of material

The BOM lists all components used for the PCB.

**Table 4 Bill of material**

| Designator                           | Quantity | Description                                                | Manufacturer          | Part number       |
|--------------------------------------|----------|------------------------------------------------------------|-----------------------|-------------------|
| C1, C8, C9, C16, C17, C21, C22       | 7        | CAP, CERM, 4.7µF, 25V, +/- 10%, X7R, 0805                  | Samsung               | CL21B475KAFNNNE   |
| C2, C7, C10, C11, C13, C15, C20, C25 | 8        | CAP, CERM, 0.1µF, 50V, +/- 10%, X7R, 0805                  | Würth Electronics     | 885012207098      |
| C3                                   | 1        | CAP, CERM, 10µF, 25V, +/- 10%, X7R, 1206                   | Würth Electronics     | 885012208069      |
| C4                                   | 1        | CAP, CERM, 0.25µF, 900V, 20%, CeraLink                     | TDK                   | B58031I9254M062   |
| C18, C23                             | 2        | CAP, CERM, 100pF, 50V, +/- 5%, NP0, 0805                   | Würth Electronics     | 885012007057      |
| C19                                  | 1        | CAP, CERM, 0.001µF, 50V, +/- 10%, X7R, 0603                | Würth Electronics     | 885012206083      |
| C24                                  | 1        | CAP, CERM, 1µF, 50V, +/- 10%, X7R, 0805                    | Würth Electronics     | 885012207103      |
| D3, D5                               | 2        | Diode, Schottky, 40 V, 0.75 A, AEC-Q101, SOD-323           | Infineon Technologies | BAT165            |
| D4                                   | 1        | Diode, Schottky, 30V, 1A, AEC-Q101, SOD-323                | Infineon Technologies | BAS3010B-03W      |
| D6, LED1                             | 2        | LED, Green, SMD                                            | Lite-On               | LTST-C190GKT      |
| D7                                   | 1        | LED, Red, SMD                                              | Lite-On               | LTST-C190CKT      |
| J1, J2, J3                           | 3        | TERM BLOCK 2POS 5mm, TH                                    | Phoenix Contact       | MKDSN 1,5/ 2-5,08 |
| J6, J7, J8, J13                      | 4        | Header, 100mil, 2x1, Gold, TH                              | Samtec                | TSW-102-07-G-S    |
| J9, J10, J11                         | 3        | Receptacle, 2.54mm, 3x1, Gold, TH                          | Samtec                | SSW-103-01-G-S    |
| J12                                  | 1        | Receptacle, 2x1, 2.54mm, Gold, TH                          | Samtec                | SSW-102-01-G-S    |
| J14                                  | 1        | Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH | 3M                    | N2510-6002-RB     |
| Q1, Q2                               | n.a.     | 1200 V power switch (not included)                         | Infineon Technologies | e.g. IKQ75N120CH3 |
| R1, R10, R21                         | 3        | RES, 10k, 1%, 0.1W, 0603                                   | Vishay-Dale           | CRCW060310K0FKEA  |
| R2, R18, R20                         | 3        | RES, 1k, 1%, 0.1W, 0603                                    | Vishay-Dale           | CRCW06031K00FKEA  |
| R3, R9                               | 2        | RES, 4R7, 1%, 0.25W, 1206                                  | Vishay-Dale           | CRCW12066R80FK    |
| R4, R7, R11, R16                     | 4        | RES, 0R, 1%, 0.1W, 0603                                    | Vishay-Dale           | CRCW0603000Z0EA   |
| R5, R13                              | 2        | RES, 10R, 1%, 0.25W, 1206                                  | Vishay-Dale           | CRCW120610R0FKEA  |

**(table continues...)**

#### 4 Bill of material

**Table 4** (continued) **Bill of material**

| Designator | Quantity | Description                                                         | Manufacturer          | Part number         |
|------------|----------|---------------------------------------------------------------------|-----------------------|---------------------|
| R6         | 1        | RES, 100R, 1%, 0.1W, 0603                                           | Vishay-Dale           | CRCW0603100RFKEA    |
| R12        | 1        | RES, 51k, 1%, 0.1W, 0603                                            | Vishay-Dale           | CRCW060351K0FKEA    |
| R14        | 1        | RES, 1M, 1%, 0.1W, 0603                                             | Vishay-Dale           | CRCW06031M00FKEA    |
| R15        | 1        | RES, 4k7, 1%, 0.1W, 0603                                            | Vishay-Dale           | CRCW06034K70FKEA    |
| R19        | 1        | RES, 0R003, 1%, 3W, 2512                                            | Bourns Inc.           | CRE2512-FZ-R003E-3  |
| R22        | 1        | RES, 47k, 1%, 0.1W, 0603                                            | Vishay-Dale           | CRCW060347K0FKEA    |
| R23, R24   | 2        | RES, 270R, 1%, 0.1W, 0603                                           | Vishay-Dale           | CRCW0603270RFKEA    |
| S1         | 1        | Switch, Tactile, SPST-NO, 0.1A, 16V, SMT                            | Bourns                | 7914G-1-000E        |
| U1         | 1        | Linear Voltage Regulator 5V                                         | Infineon Technologies | TLS810D1EJV50       |
| U2, U3, U4 | 3        | Single channel IGBT gate driver IC in wide body package dual output | Infineon Technologies | 1ED3121MC12H        |
| U5         | 1        | Rail-to-Rail Input and Output, 0.95nV/√Hz Low Noise, Op Amp         | Linear Technology     | LT6200CS6-10#TRMPBF |
| U6         | 1        | Dual 2-Input NAND Gate with Schmitt-Trigger Inputs                  | Texas Instruments     | SN74LVC2G132DCUR    |

## Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2024-09-04**

**Published by**

**Infineon Technologies AG**  
**81726 Munich, Germany**

**© 2024 Infineon Technologies AG**  
**All Rights Reserved.**

**Do you have a question about any aspect of this document?**

**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

**Document reference**  
**IFX-vjr1570183103864**

## Important notice

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

## Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.