EiceDRIVER™ 1EDN71x6G

200 V high-side TDI gate driver IC for GaN SG HEMTs and MOSFETs

Features

- Optimized for driving GaN SG HEMTs and Si MOSFETs
- Fully differential logic input circuitry to avoid false triggering in low-side or high-side operation
- High common-mode input voltage range (CMR) up to ± 200 V for high side operation
- High immunity to common-mode voltage transitions (100 V/ns) for robust operation during fast switching
- Compatible with 3.3 V or 5 V input logic
- Four driving strength variants to optimize switching speed without external gate resistors - up to 2 A source/sink current capability
- Active bootstrap clamp to avoid bootstrap capacitor overcharging during dead-time
- Active Miller clamp with 5 A sink capability to avoid induced turn-on
- Adjustable charge pump for negative turn-off supply voltage
- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

RoHS Halogen-Free

Description

The 1EDN71x6G is a single-channel gate-driver IC optimized for driving Infineon CoolGaN™ Schottky Gate HEMTs, as well as other GaN SG HEMTs and Si MOSFETs. This gate driver includes several key features that enable a high-performance system design with fast-switching transistors, including Truly Differential Input (TDI), four driving strength options, active Miller clamp, bootstrap voltage clamp, and adjustable charge pump.

Potential applications

- Single channel:
  - Synchronous rectifier
  - Class-E resonant wireless power
- Half-bridge (2 x 1EDN71x6G):
  - DC-DC converter
  - BLDC/PMSM motor drive
  - Class-D audio amplifier
  - Class-D resonant wireless power

Product portfolio

Part number	Peak source/ sink current	Input pulse blanking time	Package
1EDN7116G	2.0 A	20 ns	PG-VSON-10
1EDN7126G	1.5 A	40 ns	PG-VSON-10
1EDN7136G	1.0 A	60 ns	PG-VSON-10
1EDN7146G	0.5 A	80 ns	PG-VSON-10

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1 Pin configuration and description

Figure 1 **Pin configuration 1EDN71X6G in PG-VSON-10 package, top view**

Table 1 **Pin definitions and functions**

Pin	Name	Function
1	CF-	Flying capacitor charge pump negative connection.
2	CF+	Flying capacitor charge pump positive connection.
3	VOFF_ADJ	Connect a resistance between this pin and VSS to select the negative rail voltage.
4	IN+	Connected to PWM output of controller via 47 kΩ or 75 kΩ resistor.
5	IN-	Connected to controller ground via 47 kΩ or 75 kΩ resistor.
6	VDD	Gate drive supply.
7	BST	Bootstrap diode anode connection point, when used as a low-side driver in a half-bridge configuration.
8	OUT_SNK	Low-impedance gate pull-down to V_{OFF} (including active Miller clamp).
9	OUT_SRC	Low-impedance gate pull-up to V_{DD}.
10	VOFF	Negative rail voltage for the turn-off.
11	VSS	Return path for VDD and thermal dissipation pad.

2 Product information

2.1 Functional description

The 1EDN71x6G is a single-channel gate-driver IC optimized for driving Infineon CoolGaN™ SG HEMTs, as well as other GaN SG HEMTs and Si MOSFETs. Thanks to the truly differential input feature, the gate driver output state is exclusively controlled by the voltage difference between the two inputs, independent of the driver's reference (ground) potential as long as the common-mode voltage is below 150 V (static) and 200 V (dynamic). This eliminates the risk of false triggering due to ground bounce in low-side applications, while also allowing 1EDN71x6G to address even high-side applications.

The product is equipped with several key features especially designed to enhance the performance of GaN SG HEMTs:

- four driving strength variants to optimize switching speed without external gate resistors
- active bootstrap clamping to avoid overcharging the bootstrap capacitor during dead-time
- an active Miller clamp with exceptionally strong pull-down to avoid induced turn-on
- and an optional charge pump to provide an adjustable negative turn-off supply, for additional induced turn-on immunity when needed.

Figure 2 **Typical circuit for low-side single-channel application using 1EDN71X6G to drive a GaN SG HEMT**

2.2 Truly differential input (TDI)

The TDI feature offers common-mode voltage rejection up to 150 V for static voltage and 200 V for dynamic voltage transients, enabling both low-side and high-side gate driving without the need for a digital isolator at the input. The dynamic voltage rating is relevant for any voltage spikes shorter than the specified blanking time (that is, minimum pulse width). When used as a low-side gate driver, the TDI greatly enhances ground bounce immunity during fast GaN switching transitions.

At the positive and negative signal inputs two symmetrical resistor dividers are used to scale down and compensate common mode bouncing voltages. A fully differential amplifier stage provides high common mode rejection and high sensitivity to differential input signals. The amplified differential output voltage is finally evaluated by the subsequent differential Schmitt-Trigger circuit.

At the IN+ and IN- pins, two external resistors R_{in1} and R_{in2} are used to scale down common mode voltages of up to ± 150 V to a level which can be processed by low voltage CMOS circuitry. These input resistors serve the function of "blocking" the high common-mode voltage, so that the IN+ and IN- pins of the driver are not exposed to this high voltage. As such, the selection of these resistors is critical to the proper operation of the TDI circuit.

Figure 3 Functional block diagram

The resistance values for R_{in1} and R_{in2} must be selected based on the logic level of the input signals. For a 3.3 V logic, both external input resistors must be 47 kΩ. For a 5 V logic, they must be 75 kΩ. Furthermore, R_{in1} and R_{in2} must be very closely matched. A tolerance of ± 0.1 % is required to maintain control over the full common mode swing. Resistors with wider tolerance limit the common-mode range of the TDI driving circuit. Any asymmetries in these resistors may cause a a common-mode voltage to be interpreted as an input signal, including stray impedances in the PCB layout. Recommendations for a PCB layout are given later in this datasheet.

To compensate for small asymmetries in the TDI circuit, low pass filters are used to further enhance the high frequency common mode rejection. Two different input filter options are available to accommodate different designs, with a total blanking time of 20 ns for 1EDN7116G, 40 ns for 1EDN7126G, 60 ns for 1EDN7136G, and 80 ns for 1EDN7146G.

2.3 Undervoltage lockout

The undervoltage lockout (UVLO) functions ensure that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltages. In the 1EDN71x6G, two UVLOs are implemented: one for the VDD pin, and one for the adjustable charge pump voltage.

The UVLO for VDD ensures that the transistors are not switched on if the driving voltage is too low, thereby avoiding excessive power dissipation due to linear-mode operation. The charge pump UVLO ensures the desired negative voltage is available for VOFF before any switching activity starts. Both UVLOs must be inactive to allow the propagation of the input control signals (IN+, IN-) to the output.

The VDD UVLO level is set to a typical value of 3.85 V, with a maximum of 4.0 V. The maximum value of the rising edge is the value that ensures all the device among the production is turned on during start up. The designer

must provide a voltage higher than 4.0 V to turn on all the devices in the production of their equipment within the specified temperature range. On the opposite side, the minimum voltage necessary to switch off all the devices is the minimum of the falling edge, which is 3.6 V. Therefore, a voltage lower than 3.6 V ensures that the driver does not start switching. Once the driver has exceeded the UVLO, the supply voltage must remain above the maximum falling edge level of 3.9 V to avoid a UVLO shutdown. The hysteresis is the voltage gap between rising edge and falling edge, which ensures some margin on noise effects such as false turn off.

The charge pump also have a UVLO function that is only active at the power-up of the 1EDN71x6G. If the charge pump is disabled, then this UVLO can be ignored. If it is enabled, then the driver does not transfer signals to the output until the charge pump UVLO threshold has been exceeded. After that time, the UVLO latches and does not trigger a shutdown of the driver, even if the charge pump voltage drops below its UVLO threshold later. The UVLO threshold level is a function of the voltage selected for the adjustable charge pump.

The output states depend on the inputs configuration and the status of the two UVLOs. The truth table of the driver is represented below.

Table 2 Input logic truth table

CP	Differential input	UVLO VDD	UVLO VOFF	OUT_SNK	OUT_SRC	BST
ENABLED	X	ACTIVE	ACTIVE	HiZ	HiZ	HiZ
ENABLED	X	ACTIVE	INACTIVE	HiZ	HiZ	HiZ
ENABLED	X	INACTIVE	ACTIVE	L	HiZ	L
ENABLED	L	INACTIVE	INACTIVE	L	HiZ	L
ENABLED	H	INACTIVE	INACTIVE	HiZ	H	H
DISABLED	X	ACTIVE	X	HiZ	HiZ	HiZ
DISABLED	L	INACTIVE	X	L	HiZ	L
DISABLED	H	INACTIVE	X	HiZ	H	H

Where:

- UVLO active means V_{DD} < UVLOVDDL
- UVLO inactive means V_{DD} > UVLOVDDH
- Differential input = L means (V_{IN+} - V_{IN-}) < input logic threshold
- Differential input = H means (V_{IN+} - V_{IN-}) > input logic threshold

2.4 Minimum input pulse

The minimum input pulse is the shortest duration pulse at the differential input that will generate an output pulse. Pulses with durations shorter than the minimum pulse are neglected and therefore will not generate any output pulse. Once the input pulse has sufficient duration to be propagated, the duration of the output pulse is equal to the duration of the input pulse, having therefore a linear transfer function between input and output.

The minimum input pulse is specified here as "shortest input pulse transferred to the output." The maximum value for this parameter is the pulse width at which all the drivers in production will provide an output signal. In other words, the designer must provide a pulse width longer than the maximum specified value to ensure an output pulse for every driver of their equipment. Likewise, any pulses shorter than the minimum specified value will be ignored by all drivers in production. This minimum specification can be treated as the guaranteed blanking time for de-glitching, which helps to prevent spurious switching during common-mode transient events.

2.5 Driver outputs

The output stage of the driver has a peak source and sink current as defined for the given product variant, which corresponds to an equivalent resistance of the pull-up and pull-down transistor. The designer can

optimize the switching speed of the driven transistor by selecting one of the four product variants, without the need for external gate resistors. If external gate resistors are used, it is highly recommended to avoid placing a resistor in the output sinking path, as this limits the effectiveness of the active Miller clamp described in the next section.

Source and sink outputs are actively held low with a clamp in case of floating inputs or during startup or power down. Under any situation, outputs are held under defined conditions to avoid unstable or unknown behavior of the driven transistor.

2.6 Active Miller clamp

The sink output of the gate driver has an active Miller clamp feature to provide high immunity to spurious turn-on events. During a turn-off transition, the peak sinking current and equivalent pull-down resistance is defined according to the product variant. However, once the driver detects that the gate voltage (at the sink output) has fallen below 0.4 V, the active Miller clamp is engaged within 3 ns, increasing the strength of the Sink output significantly. With the clamp engaged, all four product variants can sink up to 5 A, with an equivalent pull-down resistance of 0.3 Ω. This feature allows the designer to optimize the turn-off speed without sacrificing the driver's "keep-off" strength. If an external gate resistor is placed at the sink output, the effectiveness of the active Miller clamp is reduced.

2.7 Adjustable negative charge pump

GaN HEMTs are more susceptible to spurious turn-on events, owing to their low threshold voltage, lower gate capacitance, and faster switching transitions. A good PCB layout with low parasitic inductances can help to minimize the risk, but this is not feasible in all designs. In situations where spurious turn-on is likely to occur, the 1EDN71x6G gate driver provides an adjustable negative power supply to reinforce the off-state of the driven transistor during a fast switching event. This is achieved by the integrated negative charge pump. The negative voltage is adjustable to allow designers to optimize the tradeoff between spurious turn-on risk and higher reverse conduction losses during dead-time. GaN HEMTs have a reverse conduction mechanism that mimics a MOSFET body diode, with the exception that the "body diode" voltage drop is directly proportional to the negative voltage applied. Therefore, applying a more negative off-state voltage than necessary produces higher losses during the dead-time.

The negative voltage can be adjusted according to the resistance value connected to VOFF_ADJ in according to the following table:

Table 3 Resistance value connected to VOFF_ADJ

R_{VOFF_ADJ}	Unit	Negative voltage @VOFF	Unit
< 0.75	kΩ	Disabled	
1.5	kΩ	-0.5	V
3.3	kΩ	-1.0	V
6.8	kΩ	-1.5	V
15	kΩ	-2.0	V
33	kΩ	-2.5	V
68	kΩ	-3.0	V

With a resistance of lower than 0.75 kΩ, the negative charge pump is disabled, and the VOFF output is floating with respect to VSS. In this case, the VOFF pin must be directly connected to VSS on the PCB. Resistances with ± 10% accuracy are recommended to avoid overlapping of different levels. The resistance value is sampled during the startup transition of the gate driver, so the charge pump voltage cannot be adjusted on-the-fly during operation. As described in the absolute maximums and recommended operating condition tables, the driver's supply voltage rating is specified as the voltage swing between VDD and VOFF. If the charge pump is active with VOFF = - 3 V, the maximum voltage supplied to VDD is 3 V lower than it would be with the charge

pump disabled. In this way, designers can supply the driver with up to 11 V (for example for normal-level MOSFETs) when the charge pump is disabled, or they can instead choose to enable the charge pump and slightly reduce the positive supply voltage accordingly.

The charge pump is designed to absorb current coming from the Miller capacitance C_{GD}, with a typical rms value of 50 mA and a peak value up to 5 A, while maintaining ± 5% regulation.

2.8 Active bootstrap clamp

When using the bootstrapping technique to supply the high-side gate driver in a half-bridge topology, it is sometimes necessary to regulate the bootstrap capacitor voltage to avoid damaging the gate of the high-side transistor. This is especially important for GaN HEMTs for two reasons:

1. GaN SG HEMTs are often sensitive to gate over-voltage, with driving voltages typically in the range of 5 V +/- 1 V.
2. The "body diode" mechanism of GaN HEMTs causes a higher voltage drop than MOSFETs, which leads to excessive over-charging of the bootstrap capacitor during dead-time conduction.

In a half-bridge configuration, the bootstrap capacitor is normally charged during the low-side switch conduction time. Figure 4 shows this charging path, which includes the power supply (VDD), the bootstrap diode, current-limiting resistor, the bootstrap capacitor, and the low-side switch. When the low-side switching is turned fully on, the voltage applied to the bootstrap capacitor is slightly lower than VDD, due to the drop across the bootstrap diode, which can be partially compensated by the drop across the low-side transistor. However, during dead-time intervals, the low-side transistor operates in "body diode" mode, with a voltage drop in the range of 1.5 ~ 2.5 V, or even higher when a negative off-state V_{GS} is applied. This causes over-charging of the bootstrap capacitor during the dead-time, resulting in a bootstrap voltage that varies significantly with dead-time duration and operating current, with a high risk of exceeding the maximum rated V_{GS} of the driven transistor.

This is not a problem for a typical MOSFET, since the operating range of the gate is fairly wide. However, this variable bootstrap capacitor voltage may pose a serious risk of damage to the Schottky gate of a GaN SG HEMT. Therefore, it is necessary to apply some form of regulation to this circuit. For example, a Zener diode can be used as shown in Figure 4, as long as the dead-time interval is well-controlled and paired with a current-limiting resistor that avoids overheating the Zener diode.

The 1EDN71X6G driver offers an alternative bootstrap clamping scheme. Figure 5 shows the implementation of this bootstrap clamping scheme in a half-bridge circuit. The clamp circuit avoids over-charging the bootstrap capacitor instead of directly regulating the capacitor voltage, which would likely contribute additional losses. Rather than connecting the bootstrap diode to the VDD supply rail, it is connected to the BST output of the low-side driver. The BST output operates as a clone of the source and sink output pins, synchronized to the timing of the low-side transistor turning on and off. Therefore, the bootstrap diode can only conduct current when the low-side transistor is turned fully on, but not when it is operating in "body diode" mode during dead-time.

The active bootstrap clamping scheme is very useful in regulating the high-side driving voltage without the need for additional components. However, in applications where over-charging of the bootstrap capacitor is desired, the bootstrap diode can be connected to the VDD pin instead of the BST pin. A Zener-based regulation scheme is recommended in this case, as shown in Figure 4 .

Figure 4 **Half-bridge with Zener bootstrap regulation (CP enabled)**

Figure 5 **Half-bridge with active bootstrap clamping (CP enabled)**

2.9 Unpowered gate clamp

The unpowered gate clamp circuit ensures that the driver output is pullowed low when no supply voltage is applied to the driver. It is common practice to place a resistor between the gate and source of transistors to ensure that there is no spurious voltage when the system is powered off. However, this is not necessary with the 1EDN71x6G. The driver has an internal pull-down MOSFET between the OUT_SNK pin and VSS pin, which pulls down the gate voltage to VSS with a peak current capability of 3 mA, whenever VDD is not sufficiently supplied to turn on the driver. Once the 1EDN71x6G is fully powered on, this pull-down MOSFET is disabled.

Figure 6 **Functional diagram of unpowered gate clamp circuit**

3 General product characteristics

3.1 Absolute maximum ratings

All voltages are referred to VSS unless otherwise specified.

Table 4 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Positive supply voltage	V_{DD}	-0.3	–	12	V	
Driver supply to negative rail LS, DC	V_{DD} - V_{OFF}	–	–	12	V	
Driver supply to negative rail LS, AC	V_{DD} - V_{OFF}	–	–	13.2	V	< 3 ns
Negative charge pump output voltage	V_{OFF} - V_{SS}	-4	–	0.3	V	
Negative charge pump offset adjust voltage	V_{OFF_ADJ}	-0.3	–	V_{DD} + 0.3	V	
Voltage at CF+ pin	V_{CF+}	-0.3	–	4	V	
Voltage at CF- pin	V_{CF-}	V_{OFF} - 0.3	–	0.3	V	
Voltage at IN+ pin	V_{IN+}	-8.5	–	8.5	V	
Voltage at IN- pin	V_{IN-}	-8.5	–	8.5	V	
Voltage at OUT_SRC, OUT_SNK, BST pins	V_{OUT_SRC}, V_{OUT_SNK}, V_{BST}	V_{OFF} - 0.3	pins	VDD + 0.3	V	
Junction temperature	T_J	-40	–	150	°C	
Storage temperature	T_S	-55	–	150	°C	
Soldering temperature		–	–	260	°C	

3.2 Recommended operating conditions

The following operating conditions must not be exceeded to ensure correct operation and reliability of the device. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 5 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	4.2	–	11	V	
Driver output voltage swing	V_{DD} - V_{OFF}	–	–	11	V	
Operating frequency w/o charge pump	F_{SW}	–	–	15	MHz	[1]
Operating frequency with charge pump	F_{SW}	–	–	4	MHz	With C_L = 1 nF. [1]
Common mode voltage range (static)	*CMR*	-150	–	150	V	R_{ext} = 47k ± 0.1%, V_{logic} = 3.3 V.
Common mode voltage range (dynamic)	CMR_{dyn}	-200	–	200	V	R_{ext} = 47k ± 0.1%, V_{logic} = 3.3 V. Duration of voltage transient event must be shorter than specified blanking time. [1]
Common mode voltage slew rate	*CMSR*	–	–	100	V/ns	[1]
Junction temperature	T_J	-40	–	125	°C	

3.3 ESD ratings

Table 6 ESD ratings

Symbol	Description	Value	Unit
ESD_{HBM}	Human Body Model sensitivity as per ANSI/ESDA/JEDEC JS-001	2000	V
ESD_{CDM}	Charged Device Model sensitivity as per ANSI/ESDA/JEDEC JS-002	1000	V

1 Verified by design/characterization. Not subject to production test.

3.4 Thermal resistance

Table 7 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-ambient thermal resistance	R_{thJA}	–	102	–	°C/W	JEDEC 2s2p with thermal vias. [2)]
Junction-to-case thermal resistance - bottom	$R_{thJC(BOT)}$	–	46	–	°C/W	
Junction-to-case thermal resistance - top	$R_{thJC(TOP)}$	–	117	–	°C/W	

3.5 Static electrical characteristics

V_{DD} = 5 V, V_{OFF} = V_{SS} = 0 V, T_c = - 40°C to 125°C unless otherwise specified.

Table 8 Static electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Undervoltage lockout thresholds						
VDD supply UVLO rising threshold	$UVLO_{VDDH}$	3.7	3.85	4	V	
VDD supply UVLO falling threshold	$UVLO_{VDDL}$	3.6	3.75	3.9	V	
Current consumption						
VDD quiescent current w/o charge pump	I_{QDD}	–	–	2.6	mA	Charge pump disabled, VOFF and VOFF_ADJ shorted to VSS. IN+ = IN- = 0 V.
VDD quiescent current w/ charge pump	I_{QDD_CP}	–	–	19	mA	Charge pump set to - 0.5 V (worst case). No load at VOFF. C_{VOFF} = 680 nF, *Cfly* = 100 nF. See plots.

(table continues...)

2 Obtained in a simulation on a JEDEC-standard 2s2p four-layer PCB with thermal vias, as specified in JESD51-7, in an environment described in JESD51-2a.

Table 8 (continued) Static electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD current consumption when switching w/o charge pump	I_{ODD}	–	–	3.5	mA	Charge pump disabled. f_{SW} = 500 kHz, no load on OUT_SRC/ OUT_SNK and no load on BST. Apply PWM to IN+, set IN- = 0 V. Common mode = 0 V.
VDD current consumption when switching w/ charge pump	I_{ODD_CP}	–	–	20.5	mA	Charge pump set to -0.5 V (worst case). f_{SW} = 500 kHz, no load on OUT_SRC/ OUT_SNK and no load on BST. Apply PWM to IN+, set IN- = 0 V. Common mode = 0 V. See plots.
Input characteristics						
Differential input voltage threshold for low-high transition	ΔV_{RinH}	1.7	1.95	2.2	V	Thresholds valid for R_{EXT} = 47 kΩ. VCM = 0 V and T = 25 °C.
Differential input voltage threshold for low-high transition	ΔV_{RinH}	1.2	1.95	2.65	V	Thresholds valid for R_{EXT} = 47 kΩ. VCM = -150 V to 150 V.
Differential input voltage threshold for high-low transition	ΔV_{RinL}	1.1	1.35	1.6	V	Thresholds valid for R_{EXT} = 47 kΩ. VCM = 0 V and T = 25 °C.
Differential input voltage threshold for high-low transition	ΔV_{RinL}	0.7	1.35	2.15	V	Thresholds valid for R_{EXT} = 47 kΩ. VCM = -150 V to 150 V.
Negative charge pump						
Negative rail adjusting range	V_{OFF_RANGE}	-3	–	0	V	
Negative rail voltage accuracy	$V_{OFF_ACCURACY}$	-5	–	5	%	

(table continues...)

Table 8 (continued) Static electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Charge pump steady-state average sink capability		–	–	50	mA	
VOFF_ADJ Pin output current	I_{ADJ_OFF}	–	–	800	uA	Only for 17 us pulse at initial startup of IC. [3]

3.6 Driver output characteristics

VDD = 5 V, VOFF = VSS = 0 V, *Tc* = 25°C unless otherwise specified.

Table 9 Driver output characteristics

Parameter	Symbol	Typical values				Unit	Note or condition
		1EDN7116G	1EDN7126G	1EDN7136G	1EDN7146G		
Peak source current	I_{OUT_SRC}	2	1.5	1	0.5	A	OUT_SRC = 0 V [3]
Peak sink current	I_{OUT_SNK}	2	1.5	1	0.5	A	OUT_SNK = 5 V [3]
Peak sink current w/ Miller clamp	$I_{OUT_SNK_MC}$	5	5	5	5	A	OUT_SNK = 5 V [3]
Pull-up resistance	R_{PU}	0.8	1.0	1.5	3.0	Ω	I_SRC = 100 mA
Pull-down resistance	R_{PD}	0.8	1.0	1.5	3.0	Ω	I_SNK = 100 mA
Pull-down resistance w/ Miller clamp	R_{PD_MC}	0.3	0.3	0.3	0.3	Ω	I_SNK = 100 mA
Active Miller clamp voltage threshold	V_{MC_TH}	0.4	0.4	0.4	0.4	V	[3]
Active Miller clamp propagation delay	T_{MCD}	3	3	3	3	ns	No load. [3]
Unpowered gate clamp sinking current	$I_{OUT_SNK_UGC}$	3	3	3	3	mA	VDD floating. 1.2 V applied externally to OUT_SNK.

(table continues...)

[3] Verified by design/characterization. Not subject to production test.

Table 9 (continued) Driver output characteristics

Parameter	Symbol	Typical values				Unit	Note or condition
		1EDN7116G	1EDN7126G	1EDN7136G	1EDN7146G		
Rise time	T_R	3	4	5.5	11	ns	OUT_SRC and OUT_SNK shorted. C_L = 1 nF[3)]
Fall time	T_F	3	4	5.5	11	ns	
BST peak source current	I_{BST_SRC}	2	2	2	2	A	BST = 0 V [3)]
BST peak sink current	I_{BST_SNK}	2	2	2	2	A	BST = 5 V [3)]
BST pull-up resistance	R_{BST_PU}	0.8	0.8	0.8	0.8	Ω	I_BST_SRC = 100 mA
BST pull-down resistance	R_{BST_PD}	0.8	0.8	0.8	0.8	Ω	I_BST_SNK = 100 mA

3.7 Timing characteristics

Timings are obtained considering OUT_SRC and OUT_SNK shorted together, C_{LOAD} = 0 nF and over common mode range -150 V to 150 V, VDD = 5 V, VOFF = 0 V, R_{EXT} = 47 kΩ unless specified otherwise.

Table 10 Timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Startup time, after UVLO threshold is reached (charge pump disabled)	t_{ST}	–	17	25	µs	VSS = 0 V, T_j = 25°C. Including VOFF_ADJ readout.
Startup time, after UVLO threshold is reached (charge pump enabled)	t_{STCP}	–	55	135	µs	VSS = 0 V, T_j = 25°C, V_{OFF} = -2 V. C_{FLY} = 100 nF, C_{VOFF} = 680 nF, including VOFF_ADJ readout.
Turn-on propagation delay matching OUT to BST	ΔT_{LH_BST}	-2	–	2	ns	Calculated as TLH - TLH_{BST}. VCM = 0 V, T_j = 25°C.
Turn-off propagation delay matching OUT to BST	ΔT_{HL_BST}	-2	–	2	ns	Calculated as THL - THL_{BST}. VCM = 0 V, T_j = 25°C.

(table continues...)

Table 10 (continued) Timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
1EDN7116G						
Turn-on propagation delay	*TLH*	53	55	57	ns	VCM = 0 V, T_j = 25°C.
Turn-off propagation delay	*THL*	53	55	57	ns	VCM = 0 V, T_j = 25°C.
Propagation delay matching	*ΔTLH_HL*	-2.2	0	2.2	ns	Calculated as TLH - THL. VCM = 0 V, T_j = 25°C.
Shortest input pulse transferred to the output	*TPW_MIN*	20	–	25	ns	VCM = 0 V, T_j = 25°C.
1EDN7126G						
Turn-on propagation delay	*TLH*	73	75	77	ns	VCM = 0 V, T_j = 25°C.
Turn-off propagation delay	*THL*	73	75	77	ns	VCM = 0 V, T_j = 25°C.
Propagation delay matching	*ΔTLH_HL*	-2.8	–	2.8	ns	Calculated as TLH - THL. VCM = 0 V, T_j = 25°C.
Shortest input pulse transferred to the output	*TPW_MIN*	40	–	47	ns	VCM = 0 V, T_j = 25°C.
1EDN7136G						
Turn-on propagation delay	*TLH*	101	105	109	ns	VCM = 0 V, T_j = 25°C.
Turn-off propagation delay	*THL*	101	105	109	ns	VCM = 0 V, T_j = 25°C.
Propagation delay matching	*ΔTLH_HL*	-3.4	–	3.4	ns	Calculated as TLH - THL. VCM = 0 V, T_j = 25°C.
Shortest input pulse transferred to the output	*TPW_MIN*	60	–	71	ns	VCM = 0 V, T_j = 25°C.

(table continues...)

Table 10 (continued) Timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
1EDN7146G						
Turn-on propagation delay	*TLH*	121	125	129	ns	VCM = 0 V, T_j = 25°C.
Turn-off propagation delay	*THL*	121	125	129	ns	VCM = 0 V, T_j = 25°C.
Propagation delay matching	*ΔTLH_HL*	-3.8	–	3.8	ns	Calculated as TLH - THL. VCM = 0 V, T_j = 25°C.
Shortest input pulse transferred to the output	*TPW_MIN*	80	–	93	ns	VCM = 0 V, T_j = 25°C.

4 Typical characteristics

Figure 7 Differential input voltage threshold versus temperature

Figure 8 Differential input voltage threshold versus common mode voltage

Figure 9 **Quiescent current versus temperature (with charge pump disabled)**

Figure 10 **Quiescent current versus supply voltage (with charge pump disabled)**

Figure 11 Operating current with load versus frequency (with charge pump disabled)

Figure 12 Operating current with load versus charge pump voltage

Figure 13 **Turn-on propagation delay versus temperature**

Figure 14 **Turn-off propagation delay versus temperature**

Figure 15 **Turn-on propagation delay versus common mode voltage**

Figure 16 **Turn-off propagation delay versus common mode voltage**

Figure 17 **OUT_SRC pull-up resistance versus temperature**

Figure 18 **OUT_SNK pull-down resistance versus temperature (before active Miller clamp is engaged)**

Figure 19 OUT_SNK pull-down resistance versus temperature (after Miller clamp is engaged)

Figure 20 BST pull-up and pull-down resistance versus temperature

Figure 21 **Undervoltage lockout threshold versus temperature**

Figure 22 **Minimum input pulse versus temperature**

5 Application information

5.1 Typical application circuits

The 1EDN71x6G can be used as a single low-side driver or a single high-side driver, and two can be used together to drive a half-bridge. Figure 23 and Figure 24 depict example circuit schematics for single-device drivers with the optional charge pump enables and disabled respectively, giving the designer the option to generate a negative off-state voltage within the IC if this is required to avoid false triggering. Figure 4 and Figure 5 show two examples of half-bridge circuit schematics with two 1EDN71x6G, with conventional bootstrapping and Zener regulation in the first, and active bootstrap clamping enabled in the second. Figure 25 shows an additional example of half-bridge implementation, in this case with cross-connected PWM inputs for the high-side and low-side drivers. This option adds robustness against accidental cross-conduction in case the controller ever generates overlapping PWM signal. However, it may also limit the minimum dead-time as measured at the gate signals of the driven devices, due to asymmetrical turn-on and turn-off delay times of the driven transistors. It is important to note that the charge pump is enabled in all three of these example half-bridge circuits, however it can be easily disabled by modifying each individual driving circuit according to Figure 24.

Figure 23 **Single channel with charge pump enabled**

Figure 24 **Single channel with charge pump disabled**

Figure 25 **Half-bridge with cross-connected signal inputs (CP enabled, active bootstrap clamping)**

Figure 26 **TDI application circuit, including input external resistors and stray capacitance**

5.2 Selection of TDI input resistors

The 1EDN71X6G requires precise input resistors at the IN+ and IN- pins, with resistance values of 47 kΩ or 75 kΩ, depending on the voltage level of the input logic signals. The driver is compatible with either a 3.3 V or a 5 V logic. These resistors are not optional, even if the application does not require the TDI function (for example low-side applications with no ground bounce concerns). The input logic thresholds at the IN+ and IN- pins are designed to be paired with the specified input resistor values. These input resistors should be selected with a 0.1% tolerance, especially in high-side applications, where the common-mode voltage rating is contingent upon tight matching of R_{IN1} and R_{IN1}. Extra care should be taken to ensure that these resistors are symmetrical, so that stray capacitance across them is also tightly matched. Figure 26 shows an example of how stray capacitances C_{p1} and C_{p2} could interfere with the symmetry and matching of R_{IN1} and R_{IN2}. To optimize this symmetry, the two resistors should have identical part numbers with the same package and footprint. Further PCB layout recommendations for ensuring symmetry are given later.

In high-side applications, the input resistors must also be rated for the power dissipation expected in the worst-case operating conditions. The common-mode voltage observed by the high-side transistor is "blocked" by each input resistor, so that the 1EDN71X6G is not exposed to the high voltage. The resistors dissipate power during the intervals where CM voltage is high, typically during the high-side transistor's duty ratio of each switching period. The power rating of the resistors should therefore be selected based on

$$P_{Rin1} = P_{Rin2} = \frac{V_{dc,max}^{2}}{R_{in1}} \times D$$

Equation 1

where:

P_{Rin1} = Required power rating for R_{in1}

P_{Rin2} = Required power rating for R_{in2}

D = High-side duty ratio

$V_{dc,max}$ = Maximum expected dc bus voltage, experienced as CM voltage during the high-side duty ratio

It is important to consider that the duty ratio may not be constant, so D should be selected as the duty ratio when operating at the maximum dc bus voltage.

The table below lists some examples for selecting the input resistors, based on logic voltage level, expected dc bus voltage, and duty ratio. For most applications, the power requirement is quite low, thereby allowing the designer to select very small resistor packages such as 0402 or 0603. In some extreme scenarios with a high dc voltage and high duty ratio simultaneously, larger packages with higher power ratings may be needed.

Table 11 Examples for selected input resistors

Maximum dc bus **voltage**	**Logic** voltage	**Duty ratio**	**TDI** input resistance	**Resistor tolerance**	**Minimum** Rin **power rating**
60 V	3.3 V	0.25	47 kΩ	0.1%	0.02 W
60 V	5 V	0.25	75 kΩ	0.1%	0.01 W
80 V	3.3 V	0.75	47 kΩ	0.1%	0.10 W
80 V	5 V	0.75	75 kΩ	0.1%	0.06 W

5.3 Selection of VDD bypass capacitor

The V_{DD} bypass capacitor provides the gate charge to drive the transistor, as well as additional power consumption by the driver itself and the charge pump (if enabled). It should be placed as close as possible to the VDD and VSS pins of the gate driver, which may require a particular footprint size for most applications.

The minimum value for this bypass capacitor can be calculated based on the maximum allowable voltage ripple in the design. This ripple should be minimized such that the lowest possible V_{DD} is above the UVLO limit of the gate driver as well as above the safe driving voltage of the transistor. The charge dissipated per switching event is the total of the driven transistor's gate charge and the additional consumption by the charge pump (if enabled). The minimum value can therefore be calculated as

$$C_{Vdd} \gg \frac{Q_G + Q_{CP}}{\Delta V_{DD,\,max}}$$

Equation 2

where the charge pump consumption can be determined through linear approximation. The typical operating consumption for the gate driver with a particular charge pump voltage is given in Figure 12 for 500 kHz with 1 nF of gate capacitance. The equivalent charge for the same charge pump voltage when operating at a different frequency with a different gate capacitance (C_{ISS}) can be approximated as

$$Q_{CP} \approx \left(\frac{I_{CP}}{500\ \ kHz}\right) \times \left(\frac{C_{ISS}}{1\ \ nF}\right)$$

Equation 3

If the charge pump is disabled, Q_{CP} can be ignored.

In a half-bridge configuration, the V_{DD} bypass capacitor also provides the charge for the bootstrap capacitor during the charging period. Therefore, the V_{DD} bypass capacitor should be sized to be much larger than the bootstrap capacitor. The minimum value should be calculated as

$$C_{Vdd} \gg \frac{Q_G + Q_{CP} + Q_{BOOT}}{\Delta V_{DD,\,max}}$$

Equation 4

where Q_{BOOT} is the charge consumed by the bootstrapping circuit each cycle. This value is calculated in a later section.

In practice, this capacitance value should be increased somewhat to account for dc bias effects in the capacitor and other non-idealities in the circuit.

5.4 Selection of external bootstrap diode

When used in a half-bridge configuration, a bootstrapping circuit is often used to supply the high-side driver's V_{DD}. A fast recovery or schottky diode with low forward voltage drop is recommended in order to minimize the losses and leakage current. It should be chosen such that it can handle the peak transient current during start-up conditions and the blocking voltage rating should be higher than the maximum input voltage (V_{IN}) with added margin. It is important to consider that the output capacitance and reverse recovery of this bootstrap diode contributes to the total switch-node capacitance of the half-bridge, thereby increasing the total switching losses of the application circuit. A schottky diode with low output capacitance is therefore the best choice for most applications.

The 1EDN71x6G gate driver provides two options for bootstrap diode connection. The conventional approach is to connect the anode of the diode to the low-side V_{DD} rail, often with a current-limiting resistor between them to limit surge current during startup. However, the recommended approach with 1EDN71x6G is to connect the anode of the bootstrap diode to the BST pin of the low-side driver as shown in Figure 4 . This enables the integrated bootstrap clamping function of the driver, and it also provides current-limiting at startup without the need for an added resistor.

5.5 Selection of bootstrap capacitor

The bootstrap capacitor provides the necessary charge to drive the high-side transistor. It must be sized in such a way that its lowest voltage will be much higher than the UVLO threshold as well as above the minimum safe driving voltage of the transistor, during transient and normal operations.

To determine the minimum required bootstrap capacitance, the maximum allowable ripple in V_{BOOT} must be calculated as follows.

$$\Delta V_{BOOT,\,max} = V_{DD} - V_F - V_{BOOT,\,min}$$

Equation 5

where:

V_{DD} = Low-side gate driver supply voltage

V_F = Bootstrap diode forward voltage drop

$V_{BOOT,min}$ is the minimum allowable voltage for the bootstrap capacitor, including transient events. This voltage must be at least high enough to avoid UVLO shutdown, as given by:

$$V_{BOOT,\,min} \geq V_{HBR} + V_{HBH}$$

Equation 6

where:

V_{HBR} = High-side driver UVLO rising threshold

V_{HBH} = High-side driver UVLO threshold hysteresis

However, the driven transistor may require a higher voltage than this UVLO minimum, in order to remain fully on and avoid linear-mode operation. If the calculated minimum V_{BOOT} is lower than the safe driving voltage of the transistor, then $V_{BOOT,min}$ should be increased accordingly.

Next, determine the total charge (Q_{BOOT}) that must be delivered by the bootstrap capacitor at maximum duty cycle. There are several factors that contribute to the discharge of the bootstrap capacitor such as the high-side transistor's total gate charge and gate-source leakage current, charge pump consumption, bootstrap diode reverse bias leakage current, and bootstrap capacitor leakage current. For the sake of simplicity, the bootstrap capacitor leakage current can typically be neglected. The total bootstrap charge can be estimated as follows:

$$Q_{BOOT} \approx Q_G + Q_{CP} + \frac{I_{Vdd} + (I_{diode} \times D_{max})}{f_{sw}}$$

Equation 7

where:
Q_G = High-side transistor total gate charge
Q_{CP} = Additional consumption by charge pump, if enabled (equation given in earlier section)
I_{Vdd} = High-side driver maximum quiescent current
I_{diode} = Bootstrap diode reverse bias leakage current
D_{max} = Maximum high-side duty cycle
f_{sw} = Switching frequency
The minimum bootstrap capacitor value can then be calculated using the formula:

$$C_{BOOT} \gg \frac{Q_{BOOT}}{\Delta V_{BOOT,max}}$$

Equation 8

In practice, this capacitance value should be increased somewhat to account for dc bias effects in the capacitor and other non-idealities in the circuit.

5.6 Selection of external gate resistors

The turn-on and turn-off external gate resistors control the turn-on and turn-off current of the gate driver providing an external way to control the switching speed of the MOSFET for purposes such as voltage overshoot control, ringing reduction, EMI mitigation, spurious turn-on protection, shoot –through protection, etc. In most designs, no external gate resistor is needed. Each of the four product variants offers a different pull-up and pull-down resistance, along with a corresponding peak source and sink current. However, in cases where the designers prefers a different source and sink driving strength, an external gate resistor may be used.

The following formulas show the effect of the external gate resistor to the output current capability of the gate driver.

$$I_{SRC,PK} \leq \frac{V_{DD}}{R_{PU} + R_{G,int} + R_{Gon,ext}}$$

Equation 9

$$I_{SNK,PK} \leq \frac{V_{DD}}{R_{PD} + R_{G,int} + R_{Goff,ext}}$$

Equation 10

where:
$I_{SRC,PK}$ = Peak source current
$I_{SNK,PK}$ = Peak sink current
R_{PU} = Gate driver pull-up resistance
R_{PD} = Gate driver pull-down resistance
V_{DD} = Gate driver supply voltage (equivalent to V_{BOOT} for high-side transistor)
$R_{G,int}$ = Internal gate resistance of driven transistor
$R_{Gon,ext}$ = External gate resistance connected between Source output and gate
$R_{Goff,ext}$ = External gate resistance connected between Sink output and gate
It is important to consider that the peak current may not reach this level during a fast switching transition, as is typical with GaN HEMTs. It is also worth nothing that this peak current cannot exceed the specified peak source/sink current of the gate driver, as the pull-up and pull-down transistors within the driver saturate at that current. However, the selection of product variant according to pull-up and pull-down resistance provides a close approximation to selection of external gate resistance in most cases.

Use of a non-zero R_{Goff_ext} is not recommended for most designs, as this limits the effectiveness of the active Miller clamp feature. It is therefore preferable to choose the product variant based on the desired sinking or pull-down strength, and then add R_{Gon_ext} only if needed to optimize the design.

5.7 Selection of adjustable charge pump circuit components

The charge pump is an optional feature of the 1EDN71X6G gate driver. At power-up of the driver (for example system startup), the driver senses the resistance at the VOFF_ADJ pin, then it enables the charge pump circuit if it senses a resistance greater than 750 Ω.

If the charge pump is not enabled at system startup, then the output of V_{OFF} is floating with respect to VSS. There is no configuration that causes the V_{OFF} output to be 0 V with respect to VSS, so this short-circuit connection must be provided externally on the PCB. Otherwise, the off-state gate voltage of the transistor may not be 0 V.

If the driver senses a resistor greater than 750 Ω, the charge pump is enabled with a negative V_{OFF} voltage determined by the resistor value. This resistance must be selected based on the table given earlier in the datasheet. In this scenario, the designer must add a 100 nF flying capacitor between CF+ and CF- pins to support the internal charge pump circuit. Furthermore, a bypass capacitor must be placed between V_{OFF} and VSS to provide a stable VOFF voltage and to supply the dynamic gate current during turn-off transitions. This capacitance value should selected based on the gate charge of the driven transistor, similar to the VDD bypass capacitor. The minimum required V_{OFF} bypass capacitance can be determined by

$$C_{Voff} \gg \frac{C_{ISS} \times V_{OFF}}{\Delta V_{OFF,max}}$$

Equation 11

where:

C_{ISS} = Input capacitance of the driven transistor

V_{OFF} = Selected charge-pump output voltage

$\Delta V_{OFF,max}$ = Maximum deviation in V_{OFF} allowable in the design

As with the other bypass capacitors, it is recommended to add some margin to this capacitance value to account for capacitor dc bias effects and other circuit non-idealities.

5.8 PCB layout recommendations

The combination of the gate driver, bypass capacitors, and driven transistor forms a high-frequency current loop that defines the parasitic inductance in series with that loop. Likewise, in a half-bridge, the combination of the high-side and low-side transistors forms a high-frequency current loop with the bypass capacitors for the dc bus (for example Vin for a buck converter). The relative location on the PCB of those components is essential to reach high level of performance. The parasitic inductances within these loops can cause serious efficiency degradation due to dynamic effects. In addition, any coupling between the gate driving loops and half-bridge power loop can cause spurious switching events or other performance degradation. Coupling between either of these loops and the signal paths feeding to the TDI input resistors can also cause spurious switching. Finally, as mentioned previously, the TDI input circuit may be affected by stray capacitance and other asymmetries in the PCB design. Careful layout can help minimize or eliminate such unwanted effects.

The following recommendations help the designer to optimize the PCB layout, as demonstrated in the half-bridge example pictures below.

1. Keep all high-frequency loops as short as possible, and use differential returns for current paths to cancel the magnetic fields and reduce parasitic inductance.
2. Minimize stray inductance, especially on low impedance lines. All high-current traces (VDD, VSS, OUT_SRC, OUT_SNK, VOFF) should be short and wide, and copper pours are recommended over traces when the design allows.
3. To optimize heat spreading, electrical shielding, and magnetic field cancellation, a VSS-connected copper pour should be placed directly underneath the IC as well as all components encompassed by the gate driving loop (for example bypass capacitors, gate and source pads of transistor). For the low-side

driver, this shielding pour should be connected to PGND. For the high-side driver, it should be connected to the switch-node, which is the mid-point of the half-bridge.

4. To avoid interference between the power loop and gate loops, separate shielding layers should be used for each loop, even if they are both connected to the same net.
5. To optimize the symmetry of the TDI input resistors, they should be placed directly beside each other and symmetrically shielded on the first inner layer. The controller-side of the two resistors should be shielded by the controller ground net (SGND), and the driver-side of the two resistors should be shielded by the same VSS-connected copper used to shield the rest of the driving circuit.
6. The dielectric spacing between the top copper layer and first inner layer should be minimized to enhance the magnetic field cancellation effects. A spacing of 80 ~ 100 microns is used in the example below.

Figure 27 **3D top-side view of example half-bridge implementation**

Figure 28 **Top copper layer of example half-bridge implementation**

Figure 29 **First inner copper layer of example half-bridge implementation**

6 Package information

Base part number	Package type	From	Quantity	Orderable part number	Marking code
1EDN7116G	PG-VSON-10	Tape and reel	4000	1EDN7116GXTMA1	1EDN7116G
1EDN7126G	PG-VSON-10	Tape and reel	4000	1EDN7126GXTMA1	1EDN7126G
1EDN7136G	PG-VSON-10	Tape and reel	4000	1EDN7136GXTMA1	1EDN7136G
1EDN7146G	PG-VSON-10	Tape and reel	4000	1EDN7146GXTMA1	1EDN7146G

Figure 30 **PG-VSON-10 packaging**

Figure 31 **PG-VSON-10 package dimensions**

Figure 32 **PG-VSON-10 recommended landing pattern**

Revision History

1EDN71x6G

Revision: 2021-10-18, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-07-26	Release of final version
2.1	2021-10-18	Title changed, added package dimension image, other editorial revisions

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