

PROFET™ +24 V

BTT6030-2ERA

Smart High-Side Power Switch Single Channel, 32 $m\Omega$

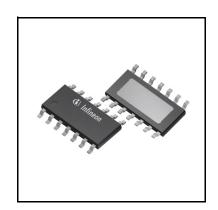


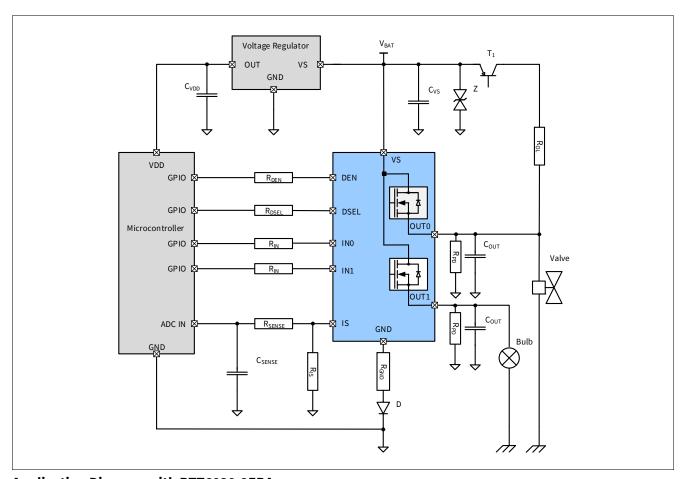
Package	PG-TDSO-14
Marking	6030-2ERA

1 Overview

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 12 V and 24 V Trucks and Transportation System





Application Diagram with BTT6030-2ERA

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BTT6030-2ERA



Overview

Basic Features

- Two channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state
- Green product (RoHS compliant) and AEC qualified

Description

The BTT6030-2ERA is a 32 mΩ dual channel Smart High-Side Power Switch, embedded in a PG-TDSO-14, Exposed Pad package, providing protective functions and diagnosis. The power transistor is built by an N-channel vertical power MOSFET with charge pump. The device is integrated in Smart6 technology. It is specially designed to drive lamps up to 3 x P21 W 24 V or 1 x 70 W 24 V, as well as LEDs in the harsh automotive environment.

Table 1 **Product Summary**

Parameter	Symbol	Value
Operating voltage range	$V_{S(OP)}$	5 V 36 V
Maximum supply voltage	$V_{S(LD)}$	65 V
Maximum ON state resistance at $T_J = 150$ °C per channel	R _{DS(ON)}	62 mΩ
Nominal load current (one channel active)	I _{L(NOM)1}	6 A
Nominal load current (both channels active)	I _{L(NOM)2}	4 A
Typical current sense ratio	k _{ILIS}	2240
Minimum current limitation	I _{L5(SC)}	56 A
Maximum standby current with load at $T_J = 25$ °C	I _{S(OFF)}	500 nA

Diagnostic Functions

- Proportional load current sense for both channels multiplexed
- Open load in ON and OFF
- Short circuit to battery and ground
- Overtemperature
- Stable diagnostic signal during short circuit
- Enhanced k_{HIS} dependency with temperature and load current

Protection Functions

- Stable behavior during undervoltage
- Reverse polarity protection with external components
- Secure load turn-off during logic ground disconnect with external components
- Overtemperature protection with latch
- Overvoltage protection with external components
- Voltage dependent current limitation
- Enhanced short circuit operation

Block Diagram



2 Block Diagram

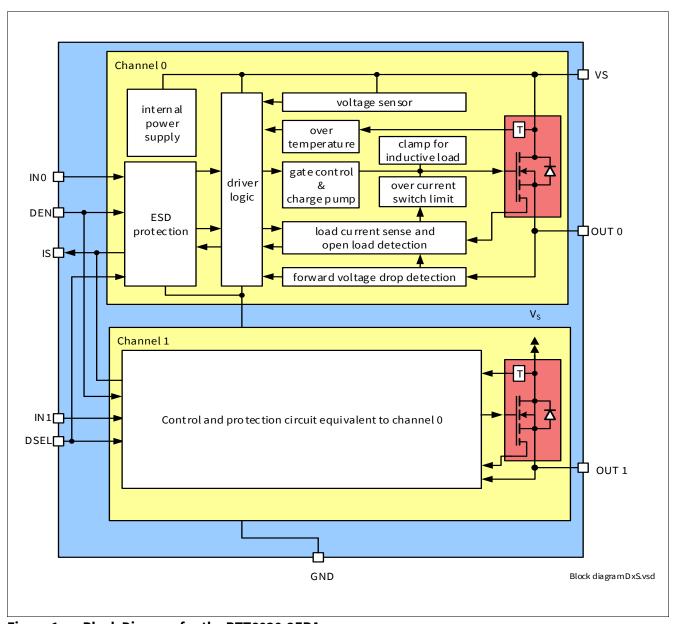


Figure 1 Block Diagram for the BTT6030-2ERA

Pin Configuration



Pin Configuration 3

Pin Assignment 3.1

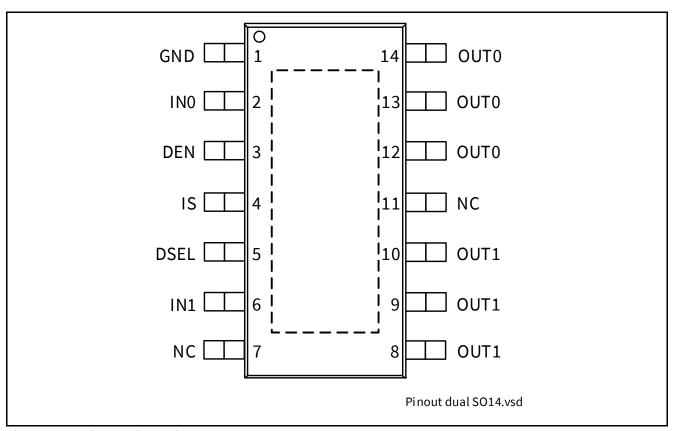


Figure 2 **Pin Configuration**

Pin Definitions and Functions 3.2

Table 2 **Pin Definitions and Functions**

Pin	Symbol	Function
1	GND	GrouND; Ground connection
2	IN0	INput channel 0; Input signal for channel 0 activation
3	DEN	Diagnostic ENable; Digital signal to enable/disable the diagnosis of the device
4	IS	Sense; Sense current of the selected channel
5	DSEL	Diagnostic SELection; Digital signal to select the channel to be diagnosed
6	IN1	INput channel 1; Input signal for channel 1 activation
7, 11	NC	Not Connected; No internal connection to the chip
8, 9, 10	OUT1	OUTput 1; Protected high side power output channel 1 ¹⁾
12, 13, 14	OUT0	OUTput 0; Protected high side power output channel 0 ¹⁾
Cooling Tab	VS	Voltage Supply; Battery voltage

¹⁾ All output pins of a given channel must be connected together on the PCB. All pins of an output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

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Pin Configuration

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

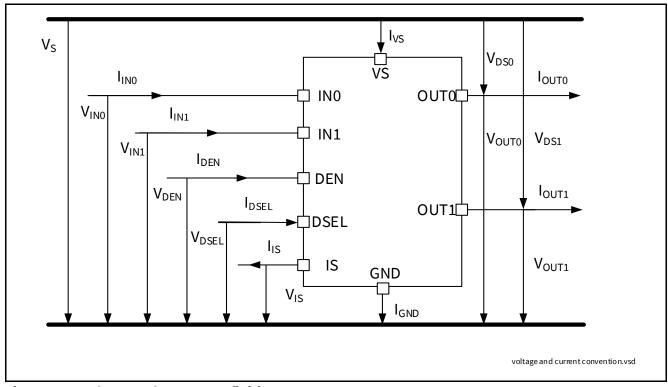


Figure 3 Voltage and Current Definition

General Product Characteristics

General Product Characteristics 4

Absolute Maximum Ratings 4.1

Absolute Maximum Ratings1)

 $T_{\rm J}$ = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol		Value	s	Unit	Note or Test Condition	Number
		Min.	Тур.	Max.			
Supply Voltages	1				1		1
Supply voltage	V_{S}	-0.3	_	48	V	_	P_4.1.1
Reverse polarity voltage	-V _{S(REV)}	0	_	28	V	t < 2 min $T_A = 25^{\circ}\text{C}$ $R_L \ge 12 \Omega$ $R_{GND} = 150 \Omega$	P_4.1.2
Supply voltage for short circuit protection	V _{BAT(SC)}	0	_	36	V	$R_{\text{ECU}} = 20 \text{ m}\Omega$ $R_{\text{Cable}} = 16 \text{ m}\Omega/\text{m}$ $L_{\text{Cable}} = 1 \mu\text{H/m},$ l = 0 or 5 m See Chapter 6 and Figure 53	P_4.1.3
Supply voltage for Load dump protection	$V_{S(LD)}$	_	-	65	V	$R_{L} = 2 \Omega$ $R_{L} = 12 \Omega$	P_4.1.12
Short Circuit Capability			·	·			
Permanent short circuit IN pin toggles	n_{RSC1}	-	-	100	k cycles	$^{3)}$ $V_{\text{Supply}} = 28 \text{ V}$	P_4.1.4
Input Pins				<u> </u>			1
Voltage at INPUT pins	V _{IN}	-0.3 -	-	6 7	V	- t < 2 min	P_4.1.13
Current through INPUT pins	I _{IN}	-2	_	2	mA	_	P_4.1.14
Voltage at DEN pin	V_{DEN}	-0.3 -	-	6 7	V	- t<2 min	P_4.1.15
Current through DEN pin	I _{DEN}	-2	-	2	mA	_	P_4.1.16
Voltage at DSEL pin	V _{DSEL}	-0.3 -	-	6 7	V	- t < 2 min	P_4.1.17
Current through DSEL pin	I _{DSEL}	-2	_	2	mA	_	P_4.1.18
Sense Pin	1						
Voltage at IS pin	V_{IS}	-0.3	_	V_{S}	V	_	P_4.1.19
Current through IS pin	I _{IS}	-25	_	50	mA	_	P_4.1.20
Power Stage	1	ı	l	l .	,	-	1
Load current	<i>I</i> _	-	-	$I_{L(LIM)}$	Α	-	P_4.1.21

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BTT6030-2ERA



General Product Characteristics

Table 3 Absolute Maximum Ratings¹⁾

 $T_{\rm J}$ = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or	Number
		Min.	Тур.	Max.		Test Condition	
Power dissipation (DC)	P _{TOT}	-	-	2.0	W	$T_A = 85^{\circ}\text{C}$ $T_J < 150^{\circ}\text{C}$	P_4.1.22
Maximum energy dissipation Single pulse (one channel)	E _{AS}	-	-	85	mJ	$I_{L(0)} = 4 \text{ A}$ $T_{J(0)} = 150^{\circ}\text{C}$ $V_{S} = 28 \text{ V}$	P_4.1.23
Voltage at power transistor	V_{DS}	_	_	65	V	_	P_4.1.26
Currents	1	-	"	-	<u>'</u>	,	
Current through ground pin	I _{GND}	-20 -200	-	20 20	mA	- t < 2 min	P_4.1.27
Temperatures	1		1				
Junction temperature	T_{J}	-40	-	150	°C	_	P_4.1.28
Storage temperature	T_{STG}	-55	_	150	°C	-	P_4.1.30
ESD Susceptibility					- 1		- 1
ESD susceptibility (all pins)	V_{ESD}	-2	_	2	kV	⁴⁾ HBM	P_4.1.31
	V _{ESD}	-4	-	4	kV	⁴⁾ HBM	P_4.1.32
ESD susceptibility	V_{ESD}	-500	_	500	V	⁵⁾ CDM	P_4.1.33
ESD susceptibility pin (corner pins)	V _{ESD}	-750	-	750	V	⁵⁾ CDM	P_4.1.34

- 1) Not subject to production test. Specified by design
- 2) $V_{\rm S(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1
- 3) Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short circuit capability on the Back Cover of this document
- 4) ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002
- 5) ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011

Notes

- 1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- 2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

BTT6030-2ERA



General Product Characteristics

Functional Range 4.2

Functional Range T_J = -40°C to +150°C; (unless otherwise specified) Table 4

Parameter	Symbol		Value	S	Unit	Note or Test Condition	Number
		Min.	Тур.	Max.			
Nominal operating voltage	V_{NOM}	8	28	36	٧	-	P_4.2.1
Extended operating voltage	$V_{S(OP)}$	5	_	48	V	$V_{IN} = 4.5 \text{ V}$ $R_{L} = 12 \Omega$ $V_{DS} < 0.5 \text{ V}$ See Figure 15	P_4.2.2
Minimum functional supply voltage	V _{S(OP)_MIN}	3.8	4.3	5	V	$I^{1)}$ $V_{IN} = 4.5 \text{ V}$ $R_L = 12 \Omega$ From $I_{OUT} = 0 \text{ A}$ to $V_{DS} < 0.5 \text{ V}$; See Figure 15 See Figure 29	P_4.2.3
Undervoltage shutdown	V _{S(UV)}	3	3.5	4.1	V	1) $V_{IN} = 4.5 \text{ V}$ $V_{DEN} = 0 \text{ V}$ $R_L = 12 \Omega$ From $V_{DS} < 1 \text{ V}$; to $I_{OUT} = 0 \text{ A}$ See Figure 15 See Figure 30	P_4.2.4
Undervoltage shutdown hysteresis	V _{S(UV)_HYS}	-	850	_	mV	2) _	P_4.2.13
Operating current One channel active	I _{GND_1}	-	5.5	9	mA	$V_{IN} = 5.5 \text{ V}$ $V_{DEN} = 5.5 \text{ V}$ Device in $R_{DS(ON)}$ $V_S = 36 \text{ V}$ See Figure 31	P_4.2.5
Operating current All channels active	I _{GND_2}	-	9	12	mA	$V_{IN} = 5.5 \text{ V}$ $V_{DEN} = 5.5 \text{ V}$ Device in $R_{DS(ON)}$ $V_S = 36 \text{ V}$ See Figure 32	P_4.2.6
Standby current for whole device with load (ambient)	I _{S(OFF)}	_	0.1	0.5	μΑ	1) $V_S = 36 \text{ V}$ $V_{OUT} = 0 \text{ V}$ V_{IN} floating V_{DEN} floating $T_J \le 85^{\circ}\text{C}$ See Figure 33	P_4.2.7

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General Product Characteristics

Table 4 Functional Range $T_J = -40^{\circ}\text{C}$ to +150°C; (unless otherwise specified)

Parameter	Symbol		Value	S	Unit	Note or Test Condition	Number
		Min.	Тур.	Max.			
Maximum standby current for whole device with load	I _{S(OFF)_150}	-	6	15	μА	$V_{\rm S} = 36 \text{ V}$ $V_{\rm OUT} = 0 \text{ V}$ $V_{\rm IN}$ floating $V_{\rm DEN}$ floating $T_{\rm J} = 150 ^{\circ} \text{C}$ See Figure 33	P_4.2.10
Standby current for whole device with load, diagnostic active	I _{S(OFF_DEN)}	-	0.6	-	mA	$^{2)}V_{S} = 36 \text{ V}$ $V_{OUT} = 0 \text{ V}$ $V_{IN} \text{ floating}$ $V_{DEN} = 5.5 \text{ V}$	P_4.2.8

¹⁾ Test at $T_1 = -40$ °C only

Note:

Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Thermal Resistance 4.3

Table 5 **Thermal Resistance**

Parameter	Symbol	Symbol Values			Unit	Note or	Number
		Min.	Тур.	Max.		Test Condition	
Junction to case	R_{thJC}	_	2	_	K/W	1)	P_4.3.1
Junction to ambient Both channels active	R _{thJA}	-	25	-	K/W	1) 2)	P_4.3.2

¹⁾ Not subject to production test. Specified by design.

²⁾ Not subject to production test. Specified by design.

²⁾ Specified $R_{\rm thJA}$ value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board with 1 W power dissipation equally dissipated for both channel at T_A =105°C; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 μm Cu, 2 x 35 μm Cu). Where applicable, a thermal via array under the exposed pad contacts the first inner copper layer. Please refer to Figure 4.



General Product Characteristics

4.3.1 PCB Set-Up

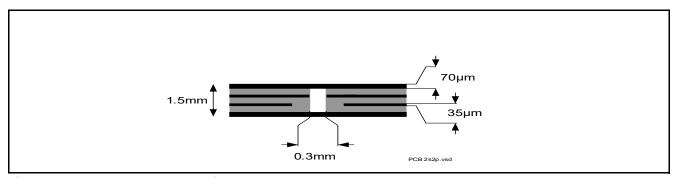


Figure 4 2s2p PCB Cross Section

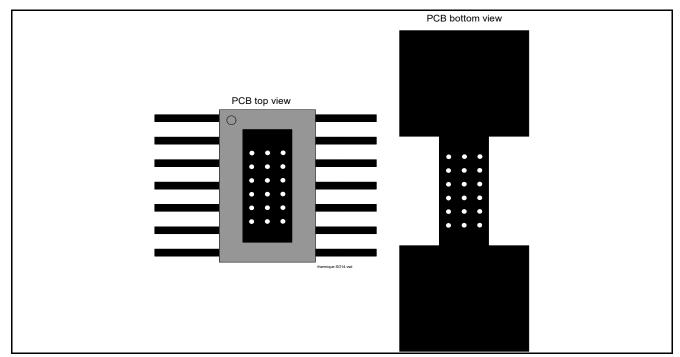
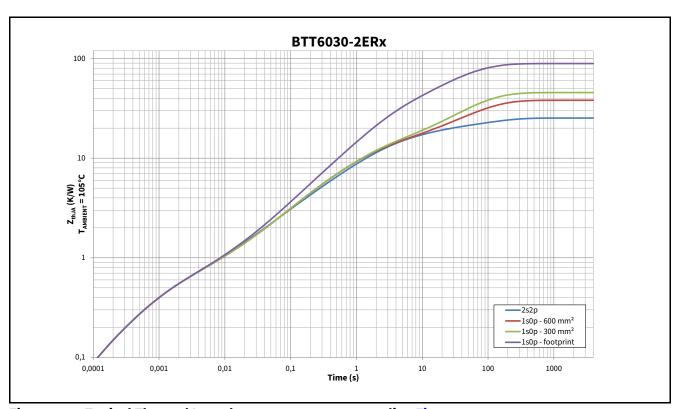


Figure 5 PC Board Top and Bottom View for Thermal Simulation with 600 mm² Cooling Area

General Product Characteristics

Thermal Impedance 4.3.2



Typical Thermal Impedance. 2s2p set-up according Figure 4 Figure 6

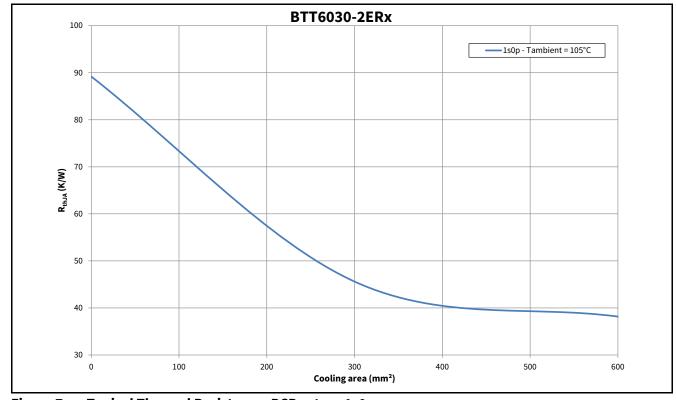


Figure 7 Typical Thermal Resistance. PCB set-up 1s0p

Power Stage



5 Power Stage

The power stages are built using an N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Output ON-State Resistance

The ON-state resistance $R_{\rm DS(ON)}$ depends on the supply voltage as well as the junction temperature $T_{\rm J}$. Figure 8 shows the dependencies in terms of temperature and supply voltage for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

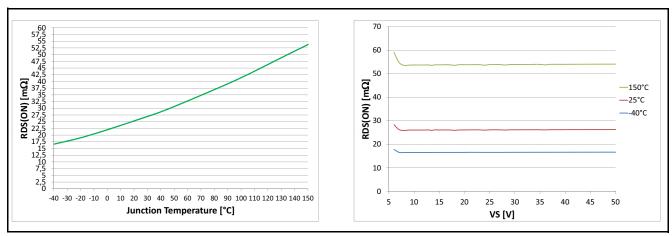


Figure 8 Typical ON-State Resistance

A high signal (see **Chapter 8**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.2 Turn ON/OFF Characteristics with Resistive Load

Figure 9 shows the typical timing when switching a resistive load.

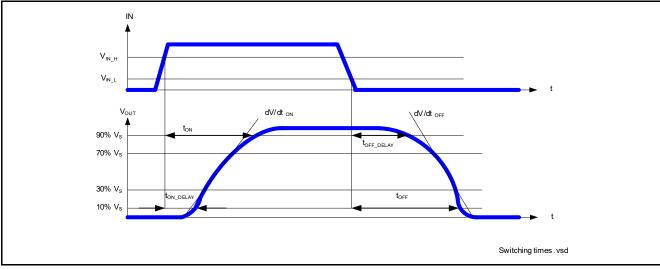


Figure 9 Switching a Resistive Load Timing

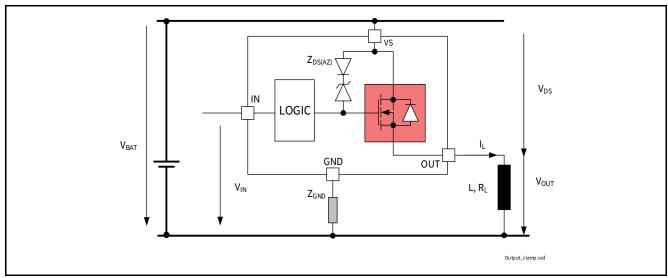
Power Stage



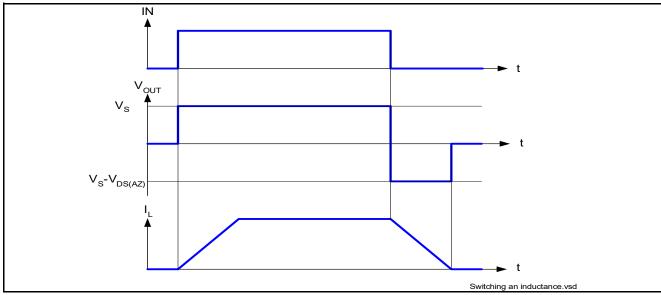
Inductive Load 5.3

5.3.1 **Output Clamping**

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism $Z_{\mathrm{DS(AZ)}}$ implemented that limits negative output voltage to a certain level ($V_S - V_{DS(AZ)}$). Please refer to **Figure 10** and **Figure 11** for details. Nevertheless, the maximum allowed load inductance is limited.



Output Clamp (OUT0 and OUT1) Figure 10



Switching an Inductive Load Timing Figure 11

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Power Stage

5.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTT6030-2ERA. This energy can be calculated with following equation:

$$E = V_{\text{DS(AZ)}} \cdot \frac{L}{R_{\text{L}}} \cdot \left[\frac{V_{\text{S}} - V_{\text{DS(AZ)}}}{R_{\text{L}}} \cdot \ln\left(1 - \frac{R_{\text{L}} \cdot I_{\text{L}}}{V_{\text{S}} - V_{\text{DS(AZ)}}}\right) + I_{\text{L}} \right]$$
(5.1)

Following equation simplifies under the assumption of $R_1 = 0 \Omega$.

$$E = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right) \tag{5.2}$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 12** for the maximum allowed energy dissipation as a function of the load current.

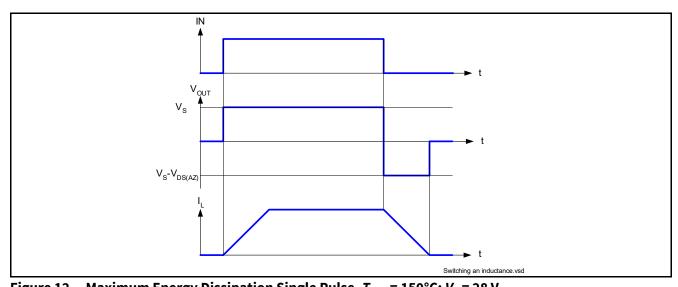


Figure 12 Maximum Energy Dissipation Single Pulse, $T_{J(0)} = 150$ °C; $V_S = 28 \text{ V}$

Power Stage

5.4 **Inverse Current Capability**

In case of inverse current, meaning a voltage V_{INV} at the OUTput higher than the supply voltage V_{S} , a current I_{INV} will flow from output to V_{S} pin via the body diode of the power transistor (please refer to **Figure 13**). The output stage follows the state of the IN pin, except if the IN pin goes from OFF to ON during inverse. In that particular case, the output stage is kept OFF until the inverse current disappears. Nevertheless, the current I_{INV} should not be higher than $I_{L(INV)}$. Otherwise, the second channel can be corrupted and erratic behavior can be observed. If the affected channel is OFF, the diagnostic will detect an open load at OFF. If the affected channel is ON, the diagnostic will detect open load at ON (the overtemperature signal is inhibited). At the appearance of V_{INV} , a parasitic diagnostic can be observed at the unaffected channel. After, the diagnosis is valid and reflects the output state. At V_{INV} vanishing, the diagnosis is valid and reflects the output state. During inverse current, no protection function are available.

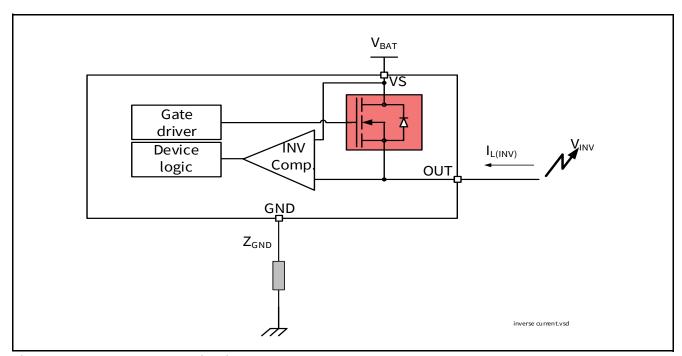


Figure 13 Inverse Current Circuitry

Power Stage



Electrical Characteristics Power Stage 5.5

Table 6 **Electrical Characteristics: Power Stage**

 $V_S = 8 \text{ V to } 36 \text{ V}$, $T_1 = -40 ^{\circ}\text{C}$ to $+150 ^{\circ}\text{C}$ (unless otherwise specified). Typical values are given at $V_S = 28 \text{ V}$, $T_J = 25 ^{\circ}\text{C}$

Parameter	Symbol		Value	s	Unit	Note or	Number
		Min.	Тур.	Max.		Test Condition	
ON-state resistance per channel	R _{DS(ON)_150}	40	55	62	mΩ	$I_{L} = I_{L4} = 7 \text{ A}$ $V_{IN} = 4.5 \text{ V}$ $T_{J} = 150 ^{\circ}\text{C}$ See Figure 8	P_5.5.1
ON-state resistance per channel	R _{DS(ON)_25}	-	32	_	mΩ	¹⁾ T _J = 25°C	P_5.5.21
Nominal load current One channel active	I _{L(NOM)1}	-	6	-	А	$T_{A} = 85^{\circ}C$ $T_{J} < 150^{\circ}C$	P_5.5.2
Nominal load current All channels active	I _{L(NOM)2}	-	4	-	А		P_5.5.3
Output voltage drop limitation at small load currents	$V_{DS(NL)}$	-	10	22	mV	$I_{L} = I_{L0} = 50 \text{ mA}$ See Figure 34	P_5.5.4
Drain to source clamping voltage $V_{\text{DS(AZ)}} = [V_{\text{S}} - V_{\text{OUT}}]$	$V_{DS(AZ)}$	66	70	75	V	I _{DS} = 20 mA See Figure 11 See Figure 35	P_5.5.5
Output leakage current per channel; T _J ≤ 85°C	I _{L(OFF)}	-	0.05	0.5	μΑ	V_{IN} floating $V_{\text{OUT}} = 0 \text{ V}$ $T_{\text{J}} \le 85^{\circ}\text{C}$	P_5.5.6
Output leakage current per channel; $T_J = 150$ °C	I _{L(OFF)_150}	-	2	10	μΑ	V_{IN} floating $V_{OUT} = 0 \text{ V}$ $T_{J} = 150^{\circ}\text{C}$	P_5.5.8
Slew rate 30% to 70% V _S	$\Delta V/dt_{ON}$	0.3	0.8	1.4	V/µs	$R_L = 12 \Omega$ $V_S = 28 V$	P_5.5.11
Slew rate 70% to 30% $V_{\rm S}$	$-\Delta V/dt_{OFF}$	0.3	0.8	1.4	V/µs	See Figure 9 See Figure 36	P_5.5.12
Slew rate matching dV/dt_{ON} - dV/dt_{OFF}	$\Delta dV/dt$	-0.15	0	0.15	V/µs	See Figure 37 See Figure 38 See Figure 39	P_5.5.13
Turn-ON time to $V_{\text{OUT}} = 90\% V_{\text{S}}$	t _{ON}	20	50	150	μs	See Figure 40	P_5.5.14
Turn-OFF time to $V_{\text{OUT}} = 10\% V_{\text{S}}$	t _{OFF}	20	55	150	μs		P_5.5.15
$\overline{\text{Turn-ON / OFF matching } t_{\text{OFF}} - t_{\text{ON}}}$	Δt_{SW}	-50	0	50	μs		P_5.5.16
Turn-ON time to $V_{\text{OUT}} = 10\% V_{\text{S}}$	t _{ON_delay}	-	30	70	μs		P_5.5.17
Turn-OFF time to $V_{\text{OUT}} = 90\% V_{\text{S}}$	t_{OFF_delay}	-	30	70	μs		P_5.5.18

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BTT6030-2ERA



Power Stage

Electrical Characteristics: Power Stage (cont'd) Table 6

 $V_{\rm S}$ = 8 V to 36 V, $T_{\rm J}$ = -40°C to +150°C (unless otherwise specified).

Typical values are given at $V_S = 28 \text{ V}$, $T_J = 25 ^{\circ}\text{C}$

Parameter	Symbol		Values			Note or	Number
		Min.	Тур.	Max.		Test Condition	
Switch ON energy	E _{ON}	-	0.6	-	mJ	$^{1)}$ R_{L} = 12 Ω V_{OUT} = 90% V_{S} V_{S} = 36 V See Figure 41	P_5.5.19
Switch OFF energy	E _{OFF}	-	0.8	-	mJ	$^{1)}$ R_{L} = 12 Ω V_{OUT} = 10% V_{S} V_{S} = 36 V See Figure 42	P_5.5.20

¹⁾ Not subject to production test, specified by design.

²⁾ Test at $T_J = -40^{\circ}$ C only



6 Protection Functions

The device provides integrated protection functions. These functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

6.1 Loss of Ground Protection

In case of loss of the module ground and the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pins.

In case of loss of device ground, it's recommended to use input resistors between the microcontroller and the BTT6030-2ERA to ensure switching OFF of the channels.

In case of loss of module or device ground, a current $(I_{OUT(GND)})$ can flow out of the DMOS. **Figure 14** sketches the situation.

 Z_{GND} is recommended to be a resistor in series to a diode.

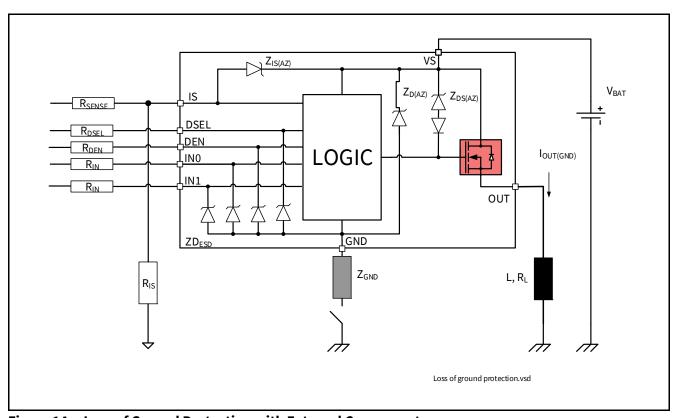


Figure 14 Loss of Ground Protection with External Components

6.2 Undervoltage Protection

Between $V_{S(UV)}$ and $V_{S(OP)}$, the undervoltage mechanism is triggered. $V_{S(OP)}$ represents the minimum voltage where the switching ON and OFF can takes place. $V_{S(UV)}$ represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism $V_{S(UV)}$, the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism $V_{S(OP)}$, then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until V_S is in the V_{NOM} range. **Figure 15** sketches the undervoltage mechanism.

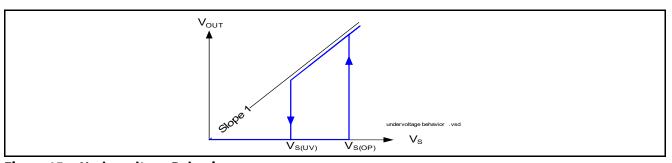
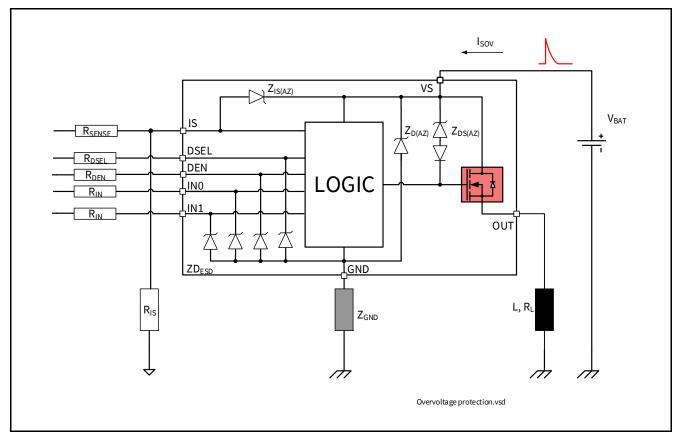


Figure 15 **Undervoltage Behavior**

6.3 **Overvoltage Protection**

There is an integrated clamp mechanism for overvoltage protection $(Z_{D(AZ)})$. To guarantee this mechanism operates properly in the application, the current in the Zener diode has to be limited by a ground resistor. Figure 16 shows a typical application to withstand overvoltage issues. In case of supply voltage higher than $V_{S(AZ)}$, the power transistor switches ON and the voltage across the logic section is clamped. As a result, the internal ground potential rises to $V_S - V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at pin IN and DEN rises almost to that potential, depending on the impedance of the connected circuitry. In the case the device was ON, prior to overvoltage, the BTT6030-2ERA remains ON. In the case the BTT6030-2ERA was OFF, prior to overvoltage, the power transistor can be activated. In the case the supply voltage is in above $V_{\text{BAT(SC)}}$ and below $V_{\rm DS(AZ)}$, the output transistor is still operational and follows the input. If at least one channel is in the ON state, parameters are no longer guaranteed and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy E_{AS} capability.

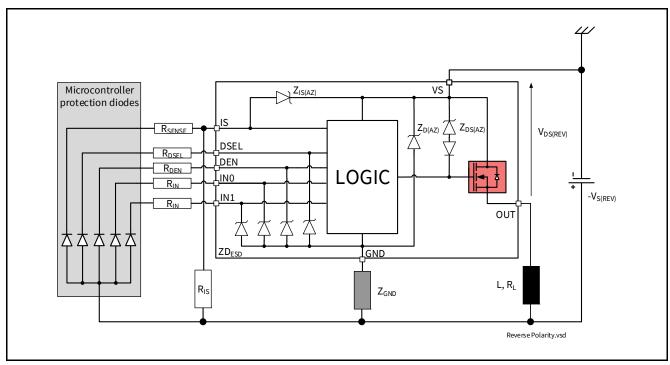


Overvoltage Protection with External Components

6.4 **Reverse Polarity Protection**

In case of reverse polarity, the intrinsic body diodes of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logic pins has to be limited to the maximum current described in **Chapter 4.1** with an external resistor. Figure 17 shows a typical application. R_{GND} resistor is used to limit the current in the Zener protection of the device. Resistors $R_{\rm DSEL}$, $R_{\rm DEN}$, and $R_{\rm IN}$ are used to limit the current in the logic of the device and in the ESD protection stage. R_{SENSE} is used to limit the current in the sense transistor which behaves as a diode. The recommended value for $R_{\text{DEN}} = R_{\text{DSEL}} = R_{\text{IN}} = R_{\text{SENSE}} = 10 \text{ k}\Omega$. Z_{GND} is recommended to be a resistor in series to a diode.

During reverse polarity, no protection functions are available.



Reverse Polarity Protection with External Components



6.5 Overload Protection

In case of overload, such as high inrush of cold lamp filament, or short circuit to ground, the BTT6030-2ERA offers several protection mechanisms.

6.5.1 Current Limitation

At first step, the instantaneous power in the switch is maintained at a safe value by limiting the current to the maximum current allowed in the switch $I_{L(SC)}$. During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS. The current limitation value is V_{DS} dependent. **Figure 18** shows the behavior of the current limitation as a function of the drain to source voltage.

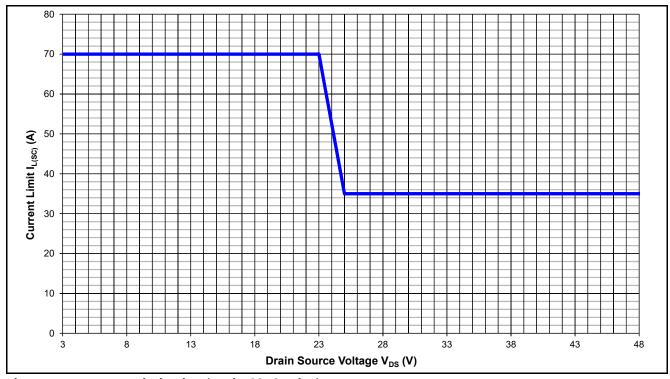


Figure 18 Current Limitation (typical behavior)



6.5.2 Temperature Limitation in the Power DMOS

Each channel incorporates both an absolute $(T_{J(SC)})$ and a dynamic $(T_{J(SW)})$ temperature sensor. Activation of either sensor will cause an overheated channel to switch OFF to prevent destruction. Any protective switch OFF latches the output until the temperature has reached an acceptable value. **Figure 19** gives a sketch of the situation.

No retry strategy is implemented such that when the DMOS temperature has cooled down enough, the switch is switched ON again. Only the IN pin signal toggling can re-activate the power strage. (latch behavior).

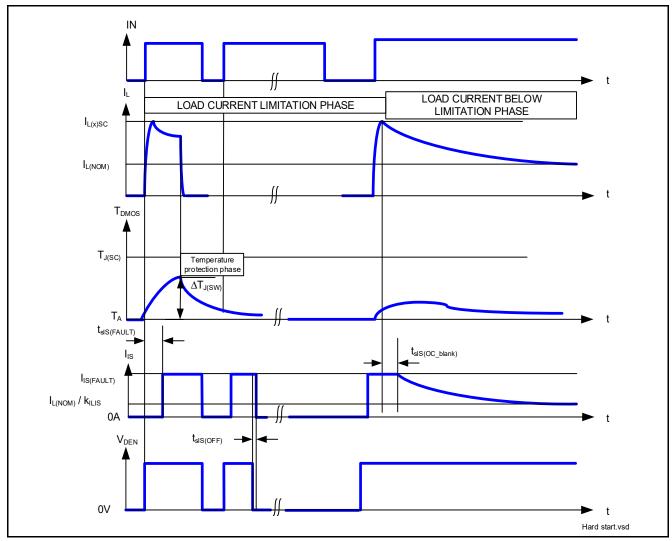


Figure 19 Overload Protection

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.



Electrical Characteristics for the Protection Functions 6.6

Electrical Characteristics: Protection Table 7

 V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).

Typical values are given at $V_S = 28 \text{ V}$, $T_J = 25 ^{\circ}\text{C}$

Parameter	Symbol		Values	;	Unit	Note or Test Condition	Number
		Min.	Тур.	Max.			
Loss of Ground							
Output leakage current while GND disconnected	I _{OUT(GND)}	-	0.1	_	mA	^{1) 2)} V _S = 48 V See Figure 14	P_6.6.1
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{\rm DS(REV)}$	200	610	700	mV	$I_L = -4 \text{ A}$ $T_J = 150^{\circ}\text{C}$ See Figure 17	P_6.6.2
Overvoltage							
Overvoltage protection	V _{S(AZ)}	65	70	75	V	I _{SOV} = 5 mA See Figure 16	P_6.6.3
Overload Condition							
Load current limitation	I _{L5(SC)}	56	70	84	А	³⁾ V _{DS} = 5 V See Figure 43	P_6.6.4
Load current limitation	I _{L28(SC)}	-	35	-	А	²⁾ V _{DS} = 42 V See Figure 43	P_6.6.7
Dynamic temperature increase while switching	$\Delta T_{J(SW)}$	-	80	-	K	4) See Figure 19	P_6.6.8
Thermal shutdown temperature	$T_{J(SC)}$	150	170 ⁴⁾	200 4)	°C	5) See Figure 19	P_6.6.10
Thermal shutdown hysteresis	$\Delta T_{J(SC)}$	_	30	-	K	^{5) 4)} See Figure 19	P_6.6.11

¹⁾ All pins are disconnected except VS and OUT.

²⁾ Not Subject to production test, specified by design

³⁾ Test at $T_1 = -40$ °C only

⁴⁾ Functional test only

⁵⁾ Test at $T_J = +150$ °C only



Diagnostic Functions 7

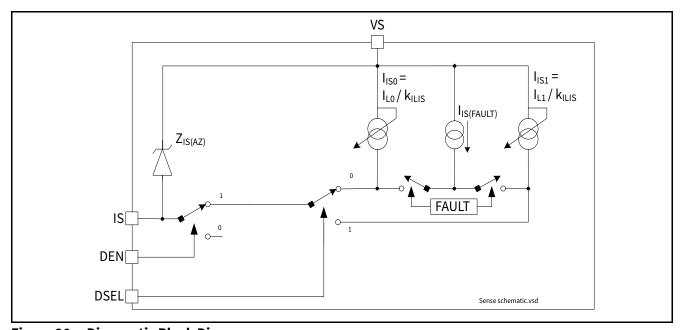
For diagnosis purpose, the BTT6030-2ERA provides a combination of digital and analog signals at pin IS. These signals are called SENSE. In case the diagnostic is disabled via DEN, pin IS becomes high impedance. In case DEN is activated, the sense current of the channel X is enabled/disabled via associated pin DSEL. Table 8 gives the truth table.

Table 8 **Diagnostic Truth Table**

DEN	DSEL	IS
0	don't care	Z
1	0	Sense output 0 I _{IS(0)}
1	1	Sense output 1 I _{IS(1)}

7.1 **IS Pin**

The BTT6030-2ERA provides a SENSE current written $I_{\rm IS}$ at pin IS. As long as no "hard" failure mode occurs (short circuit to GND / current limitation / overtemperature / excessive dynamic temperature increase or open load at OFF) a proportional signal to the load current (ratio $k_{\rm ILIS} = I_{\rm L}/I_{\rm IS}$) is provided. The complete IS pin and diagnostic mechanism is described on Figure 20. The accuracy of the SENSE depends on temperature and load current. The IS pin multiplexes the current $I_{IS(0)}$ and $I_{IS(1)}$, via the pin DSEL. Thanks to this multiplexing, the matching between $k_{\text{ILISCHANNEL0}}$ and $k_{\text{ILISCHANNEL1}}$ is optimized. Due to the ESD protection, in connection to V_{S} , it is not recommended to share the IS pin with other devices if these devices are using another battery feed. The consequence is that the unsupplied device would be fed via the IS pin of the supplied device.



Diagnostic Block Diagram Figure 20



SENSE Signal in Different Operating Modes 7.2

Table 9 gives a quick reference for the state of the IS pin during device operation.

Table 9 **Sense Signal, Function of Operation Mode**

Operation Mode	Input level Channel X	DEN ¹⁾	Output Level	Diagnostic Output	
Normal operation	OFF	Н	Z	Z	
Short circuit to GND			~ GND	Z	
Overtemperature			Z	Z	
Short circuit to V _S			V_{S}	I _{IS(FAULT)}	
Open Load			< V _{OL(OFF)} > V _{OL(OFF)} 2)	Z I _{IS(FAULT)}	
Inverse current			~ V _{INV}	I _{IS(FAULT)}	
Normal operation	ON		~ V _S	$I_{\rm IS} = I_{\rm L} / k_{\rm ILIS}$	
Current limitation			< V _S	I _{IS(FAULT)}	
Short circuit to GND			~ GND	I _{IS(FAULT)}	
Overtemperature $T_{J(SW)}$ event			Z	I _{IS(FAULT)}	
Short circuit to V _S			V_{S}	$I_{\rm IS} < I_{\rm L} / k_{\rm ILIS}$	
Open Load			~ V _S ³⁾	$I_{\rm IS} < I_{\rm IS(OL)}$	
Inverse current			~ V _{INV}	$I_{\rm IS} < I_{\rm IS(OL)}^{4)}$	
Underload			~ V _S ⁵⁾	$I_{\rm IS(OL)} < I_{\rm IS} < I_{\rm L/kILIS}$	
Don't care	Don't care	L	Don't care	Z	

¹⁾ The table doesn't indicate but it is assumed that the appropriate channel is selected via the DSEL pin.

²⁾ With additional pull-up resistor.

³⁾ The output current has to be smaller than $I_{L(OL)}$.

⁴⁾ After maximum t_{INV} .

⁵⁾ The output current has to be higher than $I_{L(OL)}$.



7.3 SENSE Signal in the Nominal Current Range

Figure 21 show the current sense as a function of the load current in the power DMOS. Usually, a pull-down resistor $R_{\rm IS}$ is connected to the IS pin. This resistor has to be higher than 560 Ω to limit the power losses in the sense circuitry. A typical value is 1.2 kΩ. The blue curve represents the ideal SENSE, assuming an ideal $k_{\rm ILIS}$ factor value. The red curves show the accuracy the device provides across full temperature range, at a defined current.

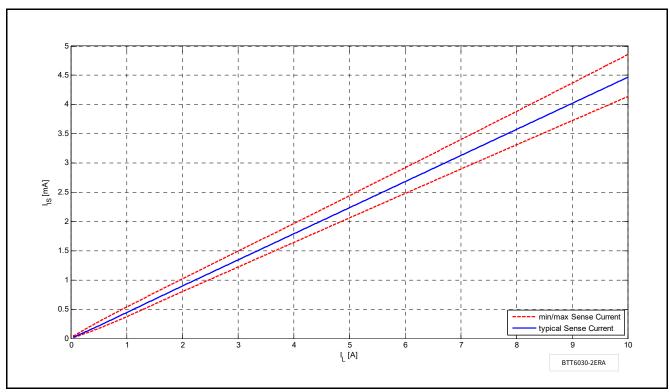


Figure 21 Current Sense for Nominal Load

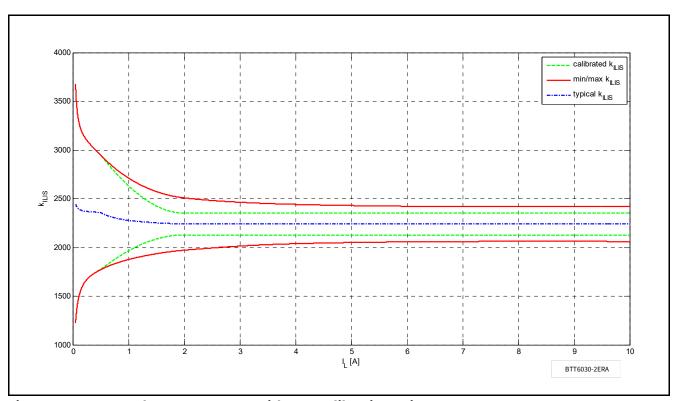
7.3.1 SENSE Signal Variation as a Function of Temperature and Load Current

In some applications a better accuracy is required around half the nominal current $I_{L(NOM)}$. To achieve this accuracy requirement, a calibration on the application is possible. To avoid multiple calibration points at different load and temperature conditions, the BTT6030-2ERA allows limited derating of the k_{ILIS} value, at nominal load current (I_{L3} ; T_J = +25°C). This derating is described by the parameter Δk_{ILIS} . **Figure 22** shows the behavior of the SENSE current, assuming one calibration point at nominal load at +25°C.

The blue line indicates the ideal k_{ILIS} ratio.

The green lines indicate the derating on the parameter across temperature and voltage, assuming one calibration point at nominal temperature and nominal battery voltage.

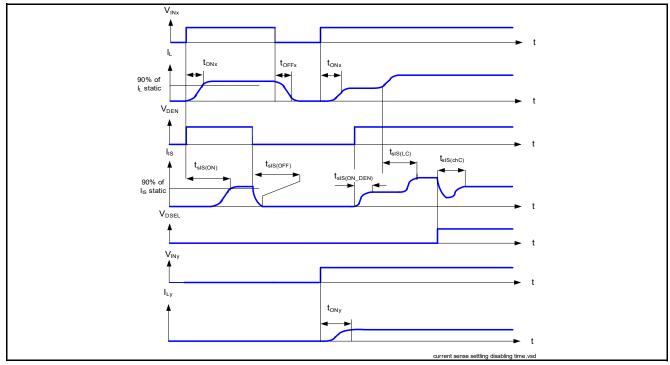
The red lines indicate the $k_{\rm ILIS}$ accuracy without calibration.



Improved SENSE Accuracy with One Calibration Point Figure 22

SENSE Signal Timing 7.3.2

Figure 23 shows the timing during settling and disabling of the SENSE.



SENSE Settling / Disabling Timing



7.3.3 SENSE Signal in Open Load

7.3.3.1 Open Load in ON Diagnostic

If the channel is ON, a leakage current can still flow through an open load, for example due to humidity. The parameter $I_{L(OL)}$ gives the threshold of recognition for this leakage current. If the current I_L flowing out the power DMOS is below this value, the device recognizes a failure, if the DEN (and DSEL) is selected. In that case, the SENSE current is below $I_{IS(OL)}$. Otherwise, the minimum SENSE current is given above parameter $I_{IS(OL)}$. Figure 24 shows the SENSE current behavior in this area. The red curve shows a typical product curve. The blue curve shows the ideal k_{ILIS} ratio.

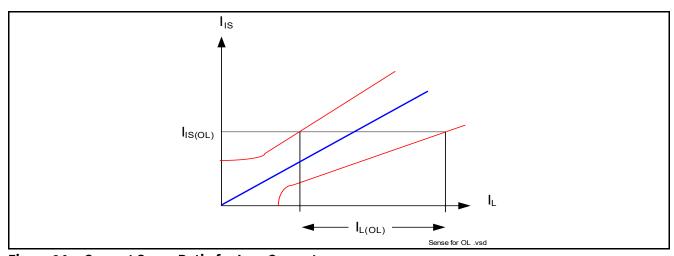


Figure 24 Current Sense Ratio for Low Currents

7.3.3.2 Open Load in OFF Diagnostic

For open load diagnosis in OFF-state, an external output pull-up resistor ($R_{\rm OL}$) is recommended. For the calculation of pull-up resistor value, the leakage currents and the open load threshold voltage $V_{\rm OL(OFF)}$ have to be taken into account. **Figure 25** gives a sketch of the situation. $I_{\rm leakage}$ defines the leakage current in the complete system, including $I_{\rm L(OFF)}$ (see **Chapter 5.5**) and external leakages, e.g, due to humidity, corrosion, etc... in the application.

To reduce the stand-by current of the system, an open load resistor switch S_{OL} is recommended. If the channel x is OFF, the output is no longer pulled down by the load and V_{OUT} voltage rises to nearly V_S . This is recognized by the device as an open load. The voltage threshold is given by $V_{OL(OFF)}$. In that case, the SENSE signal is switched to the $I_{IS(FAULT)}$.

An additional R_{PD} resistor can be used to pull V_{OUT} to 0 V. Otherwise, the OUT pin is floating. This resistor can be used as well for short circuit to battery detection, see **Chapter 7.3.4**.

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Diagnostic Functions

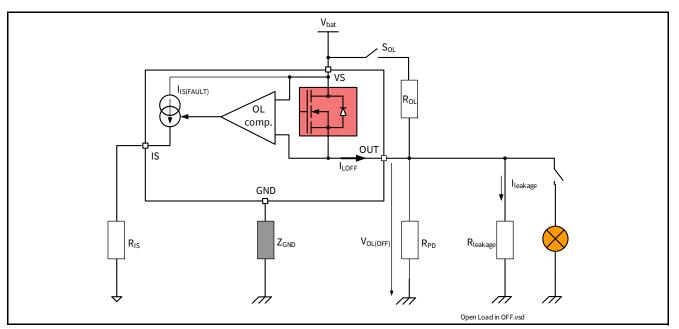


Figure 25 Open Load Detection in OFF Electrical Equivalent Circuit

7.3.3.3 Open Load Diagnostic Timing

Figure 26 shows the timing during either Open Load in ON or OFF condition when the DEN pin is HIGH. Please note that a delay $t_{\rm sIS(FAULT_OL_OFF)}$ has to be respected after the falling edge of the input, when applying an open load in OFF diagnosis request, otherwise the diagnosis can be wrong.

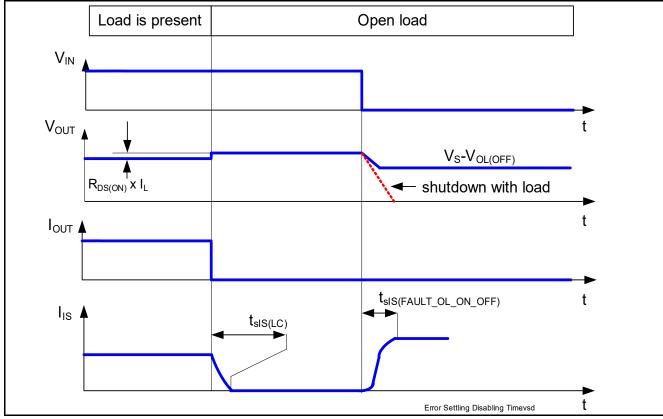


Figure 26 SENSE Signal in Open Load Timing



7.3.4 SENSE Signal with OUT in Short Circuit to V_s

In case of a short circuit between the OUTput-pin and the V_S pin, all or portion (depending on the short circuit impedance) of the load current will flow through the short circuit. As a result, a lower current compared to the normal operation will flow through the DMOS of the BTT6030-2ERA, which can be recognized at the SENSE signal. The open load at OFF detection circuitry can also be used to distinguish a short circuit to V_S . In that case, an external resistor to ground R_{SC} vs is required. Figure 27 gives a sketch of the situation.

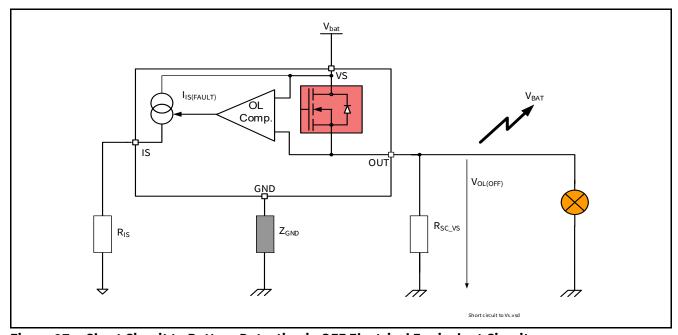


Figure 27 Short Circuit to Battery Detection in OFF Electrical Equivalent Circuit

7.3.5 SENSE Signal in Case of Overload

An overload condition is defined by a current flowing out of the DMOS reaching the current limitation and / or the absolute dynamic temperature swing $T_{J(SW)}$ is reached, and / or the junction temperature reaches the thermal shutdown temperature $T_{J(SC)}$. Please refer to **Chapter 6.5** for details.

In that case, the SENSE signal given is by $I_{\text{IS(FAULT)}}$ when the diagnostic is selected.

The device has a thermal latch behavior, such that when the overtemperature or the exceed dynamic temperature condition has disappeared, the DMOS is reactivated only when the IN is toggled LOW to HIGH. If the DEN pin is activated, and DSEL pin is selected to the correct channel, the SENSE follows the output stage. If no reset of the latch occurs, the device remains in the latching phase and $I_{\rm IS(FAULT)}$ at the IS pin, even though the DMOS is OFF.

7.3.6 SENSE Signal in Case of Inverse Current

In the case of inverse current, the sense signal of the affected channel will indicate open load in OFF state during OFF state and indicate open load in ON during ON state. The unaffected channel indicates normal behavior as long as the I_{INV} current is not exceeding the maximum value specified in **Chapter 5.4**.



7.4 Electrical Characteristics Diagnostic Function

Table 10 Electrical Characteristics: Diagnostics

 $V_{\rm S}$ = 8 V to 36 V, $T_{\rm J}$ = -40°C to +150°C (unless otherwise specified). Typical values are given at $V_{\rm S}$ = 28 V, $T_{\rm J}$ = 25°C

Parameter	Symbol	Values			Unit	Note or	Number
		Min.	Тур.	Max.		Test Condition	
Load Condition Threshold fo	or Diagnostic	1					1
Open load detection threshold in OFF state	V _S - V _{OL(OFF)}	4	_	6	V	$V_{IN} = 0 \text{ V}$ $V_{DEN} = 4.5 \text{ V}$ See Figure 26	P_7.5.1
Open load detection threshold in ON state	I _{L(OL)}	4	-	25	mA	$V_{IN} = V_{DEN} = 4.5 \text{ V}$ $I_{IS(OL)} = 5 \mu A$ See Figure 24 See Figure 46	P_7.5.2
Sense Pin	-1	1		<u> </u>		·	1
IS pin leakage current when sense is disabled	I _{IS_(DIS)}	_	0.02	1	μΑ	$V_{IN} = 4.5 \text{ V}$ $V_{DEN} = 0 \text{ V}$ $V_{L} = V_{L4} = 7 \text{ A}$	P_7.5.4
Sense signal saturation voltage	V _S - V _{IS (RANGE)}	1	-	3.5	V	$V_{IN} = 0 \text{ V}$ $V_{OUT} = V_{S} > 10 \text{ V}$ $V_{DEN} = 4.5 \text{ V}$ $V_{IS} = 6 \text{ mA}$ See Figure 47	P_7.5.6
Sense signal maximum current in fault condition	I _{IS(FAULT)}	6	15	40	mA	$V_{\rm IS} = V_{\rm IN} = V_{\rm DSEL} = 0 \text{ V}$ $V_{\rm OUT} = V_{\rm S} > 10 \text{ V}$ $V_{\rm DEN} = 4.5 \text{ V}$ See Figure 20 See Figure 48	P_7.5.7
Sense pin maximum voltage	$V_{IS(AZ)}$	65	70	75	V	I _{IS} = 5 mA See Figure 20	P_7.5.3
Current Sense Ratio Signal	in the Nomina	al Area,	Stable L	oad Curr	ent Co	ndition	1
Current sense ratio $I_{L0} = 50 \text{ mA}$ Current sense ratio	$k_{\rm ILIS0}$ $k_{\rm ILIS1}$	-50% -25%	2450	+50% +25%		$V_{IN} = 4.5 \text{ V}$ $V_{DEN} = 4.5 \text{ V}$ See Figure 21	P_7.5.8 P_7.5.9
$I_{L1} = 0.5 \text{ A}$	ILISI					$T_{\rm J}$ = -40°C; 150°C	
Current sense ratio $I_{L2} = 2 \text{ A}$	k _{ILIS2}	-12%	2240	+12%			P_7.5.10
Current sense ratio I _{L3} = 4 A	k _{ILIS3}	-9%	2240	+9%			P_7.5.11
Current sense ratio I _{L4} = 7 A	k _{ILIS4}	-8%	2240	+8%			P_7.5.12
$k_{\rm ILIS}$ derating with current and temperature	Δk_{ILIS}	-5	0	+5	%	$^{2)} k_{\rm ILIS3}$ versus $k_{\rm ILIS2}$ See Figure 22	P_7.5.17

PROFET™ +24 V **BTT6030-2ERA**

Diagnostic Functions

Electrical Characteristics: Diagnostics (cont'd) Table 10

 $V_{\rm S}$ = 8 V to 36 V, $T_{\rm J}$ = -40°C to +150°C (unless otherwise specified).

Typical values are given at $V_S = 28 \text{ V}$, $T_J = 25 ^{\circ}\text{C}$

Parameter	Symbol	Values			Unit	Note or	Number
		Min.	Тур.	Max.		Test Condition	
Diagnostic Timing in Norma	Condition		·	·			
Current sense settling time to $k_{\rm ILIS}$ function stable after positive input slope on both INput and DEN	t _{sIS(ON)}	-	-	150	μς	$^{2)}$ V _{DEN} = V _{IN} = 0 to 4.5 V V _S = 28 V R _{IS} = 1.2 kΩ C _{SENSE} < 100 pF I _L = I _{L3} = 4 A See Figure 23	P_7.5.18
Current sense settling time with load current stable and transition of the DEN	t _{sis(on_den)}	-	_	10	μs	$^{1)}$ V_{IN} = 4.5 V V_{DEN} = 0 to 4.5 V R_{IS} = 1.2 k Ω C_{SENSE} < 100 pF I_{L} = I_{L3} = 4 A See Figure 23	P_7.5.19
Current sense settling time to I_{1S} stable after positive input slope on current load	t _{sIS(LC)}	-	-	20	μs	$^{1)}$ $V_{IN} = 4.5 \text{ V}$ $V_{DEN} = 4.5 \text{ V}$ $R_{IS} = 1.2 \text{ k}\Omega$ $C_{SENSE} < 100 \text{ pF}$ $I_L = I_{L2} = 2 \text{ A to}$ $I_L = I_{L3} = 4 \text{ A}$ See Figure 23	P_7.5.20
Diagnostic Timing in Open L	oad Conditio	n			I		
Current sense settling time to $I_{\rm IS}$ stable for open load detection in OFF state	$t_{ m sis(fault_ol_}$	_	-	100	μs	$V_{IN} = 0$ V $V_{DEN} = 0$ to 4.5 V $R_{IS} = 1.2$ kΩ $C_{SENSE} < 100$ pF $V_{OUT} = V_{S} = 28$ V See Figure 26	P_7.5.22
Current sense settling time for open load detection in ON-OFF transition	t _{sIS(FAULT_OL_} ON_OFF)	-	200	-	μs	$^{1)}$ V_{IN} = 4.5 to 0 V V_{DEN} = 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF V_{OUT} = V_{S} = 28 V See Figure 26	P_7.5.23
Diagnostic Timing in Overloa	ad Condition						
Current sense settling time to I_{IS} stable for overload detection	t _{sis(fault)}	-	-	150	μs	$^{2)} V_{IN} = V_{DEN} = 0 \text{ to}$ 4.5 V $R_{IS} = 1.2 \text{ k}\Omega$ $C_{SENSE} < 100 \text{ pF}$ $V_{DS} = 24 \text{ V}$ See Figure 19	P_7.5.24

PROFET™ +24 V **BTT6030-2ERA**



Diagnostic Functions

Electrical Characteristics: Diagnostics (cont'd) Table 10

 $V_{\rm S}$ = 8 V to 36 V, $T_{\rm J}$ = -40°C to +150°C (unless otherwise specified).

Typical values are given at $V_S = 28 \text{ V}$, $T_J = 25 ^{\circ}\text{C}$

Parameter	Symbol	Values			Unit	Note or	Number
		Min.	Тур.	Max.		Test Condition	
Current sense over current blanking time	t _{sIS(OC_blank)}	-	350	_	μs	$^{2)} V_{IN} = V_{DEN} = 4.5 \text{ V}$ $R_{IS} = 1.2 \text{ k}\Omega$ $C_{SENSE} < 100 \text{ pF}$ $V_{DS} = 5 \text{ V to 0 V}$ See Figure 19	P_7.5.32
Diagnostic disable time DEN transition to $I_{\rm IS} < 50\% I_{\rm L}/k_{\rm ILIS}$	t _{sIS(OFF)}	-	-	20	μs	¹⁾ V_{IN} = 4.5 V V_{DEN} = 4.5 V to 0 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF I_{L} = I_{L3} = 4 A See Figure 23	P_7.5.25
Current sense settling time from one channel to another	t _{sIS(ChC)}	-	-	20	μs	$V_{\text{IN0}} = V_{\text{IN1}} = 4.5 \text{ V}$ $V_{\text{DEN}} = 4.5 \text{ V}$ $V_{\text{DSEL}} = 0 \text{ to } 4.5 \text{ V}$ $R_{\text{IS}} = 1.2 \text{ k}\Omega$ $C_{\text{SENSE}} < 100 \text{ pF}$ $I_{\text{L(OUT0)}} = I_{\text{L3}} = 4 \text{ A}$ $I_{\text{L(OUT1)}} = I_{\text{L2}} = 2 \text{ A}$ See Figure 23	P_7.5.26

¹⁾ DSEL pin select channel 0 only.

²⁾ Not subject to production test, specified by design

Input Pins



8 Input Pins

8.1 Input Circuitry

The input circuitry is compatible with 3.3 and 5 V microcontrollers. The concept of the input pin is to react to voltage thresholds. An implemented Schmitt trigger avoids any undefined state if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state. The input circuitry is compatible with PWM applications. **Figure 28** shows the electrical equivalent input circuitry. In case the pin is not needed, it must be left opened, or must be connected to device ground (and not module ground) via a $4.7 \text{ k}\Omega$ input resistor.

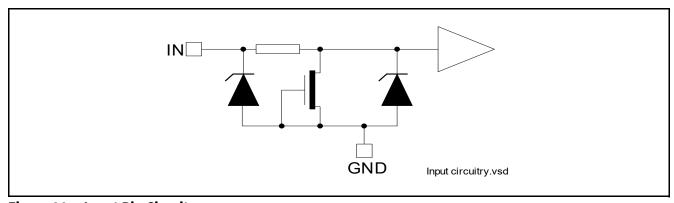


Figure 28 Input Pin Circuitry

8.2 DEN / DSEL Pin

The DEN / DSEL pins enable and disable the diagnostic functionality of the device. The pins have the same structure to INput pins, please refer to Figure 28.

8.3 Input Pin Voltage

The IN, DSEL and DEN use a comparator with hysteresis. The switching ON / OFF takes place in a defined region, set by the thresholds $V_{\rm IN(L)}$ Max. and $V_{\rm IN(H)}$ Min. The exact value where the ON and OFF take place are unknown and depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, a hysteresis is implemented. This ensures a certain immunity to noise.

Input Pins



Electrical Characteristics 8.4

Electrical Characteristics: Input Pins Table 11

 V_S = 8 V to 36 V, T_J = -40°C to +150°C (unless otherwise specified).

Typical values are given at $V_S = 28 \text{ V}$, $T_J = 25 ^{\circ}\text{C}$

Parameter	Symbol	Values			Unit	Note or	Number
		Min.	Тур.	Max.		Test Condition	
INput Pins Characteristics			-		1		
Low level input voltage range	$V_{IN(L)}$	-0.3	-	0.8	٧	See Figure 49	P_8.4.1
High level input voltage range	$V_{\text{IN(H)}}$	2	-	6	٧	See Figure 50	P_8.4.2
Input voltage hysteresis	V _{IN(HYS)}	_	250	_	mV	1) See Figure 51	P_8.4.3
Low level input current	I _{IN(L)}	1	10	25	μΑ	V _{IN} = 0.8 V	P_8.4.4
High level input current	I _{IN(H)}	2	10	25	μΑ	V _{IN} = 5.5 V See Figure 52	P_8.4.5
DEN Pin							
Low level input voltage range	$V_{DEN(L)}$	-0.3	-	0.8	٧	_	P_8.4.6
High level input voltage range	$V_{DEN(H)}$	2	-	6	٧	_	P_8.4.7
Input voltage hysteresis	V _{DEN(HYS)}	_	250	_	mV	1)	P_8.4.8
Low level input current	I _{DEN(L)}	1	10	25	μΑ	V _{DEN} = 0.8 V	P_8.4.9
High level input current	I _{DEN(H)}	2	10	25	μΑ	V _{DEN} = 5.5 V	P_8.4.10
DSEL Pin	•	•		•			•
Low level input voltage range	V _{DSEL(L)}	-0.3	-	0.8	٧	-	P_8.4.11
High level input voltage range	V _{DSEL(H)}	2	-	6	٧	_	P_8.4.12
Input voltage hysteresis	V _{DSEL(HYS)}	_	250	_	mV	1)	P_8.4.13
Low level input current	I _{DSEL(L)}	1	10	25	μΑ	V _{DSEL} = 0.8 V	P_8.4.14
High level input current	I _{DSEL(H)}	2	10	25	μΑ	V _{DSEL} = 5.5 V	P_8.4.15

¹⁾ Not subject to production test, specified by design

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Characterization Results

9 Characterization Results

The characterization has been performed on 3 lots, with 3 devices each. Characterization has been performed at 8 V, 28 V and 36 V, from -40°C to 160°C. When no dependency to voltage is seen, only one curve (28 V) is sketched.

9.1 General Product Characteristics

9.1.1 Minimum Functional Supply Voltage

P_4.2.3

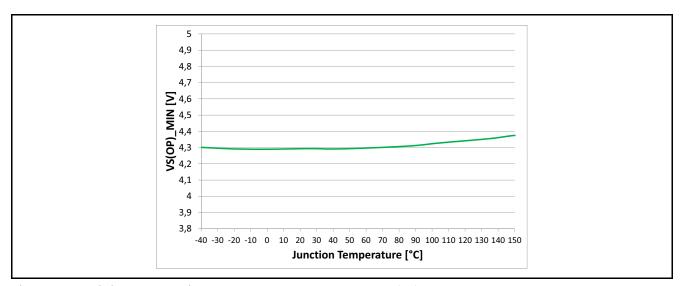


Figure 29 Minimum Functional Supply Voltage $V_{S(OP) MIN} = f(T_J)$

9.1.2 Undervoltage Shutdown

P_4.2.4

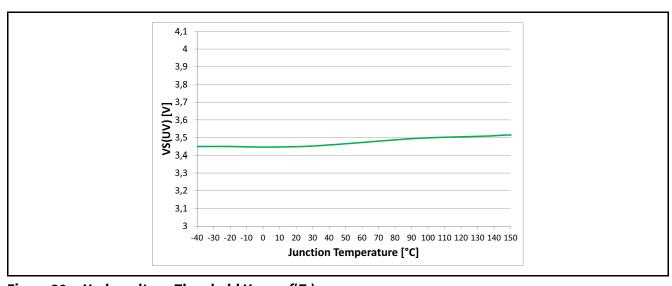
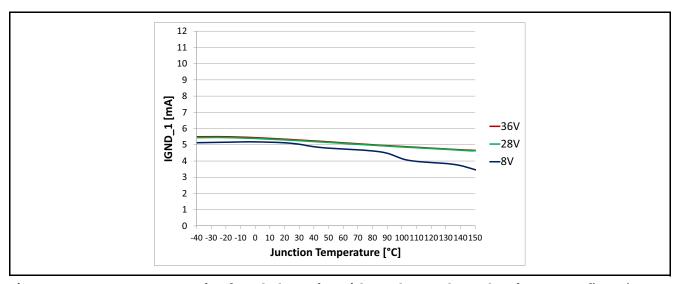


Figure 30 Undervoltage Threshold $V_{S(UV)} = f(T_J)$



Current Consumption One Channel Active 9.1.3

P_4.2.5



Current Consumption for Whole Device with Load. One Channel Active $I_{GND_1} = f(T_1; V_S)$ Figure 31

Current Consumption Two Channels Active 9.1.4

P_4.2.6

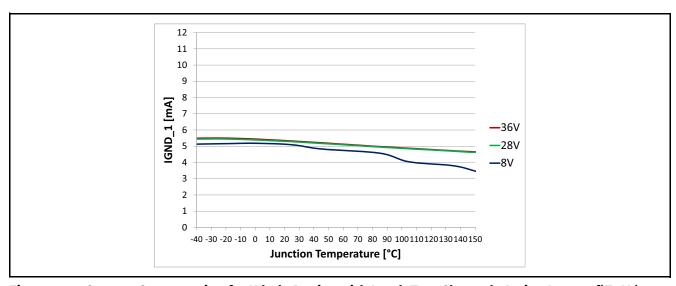


Figure 32 Current Consumption for Whole Device with Load. Two Channels Active $I_{GND} = f(T_J; V_S)$

Standby Current for Whole Device with Load 9.1.5

P_4.2.7, P_4.2.10

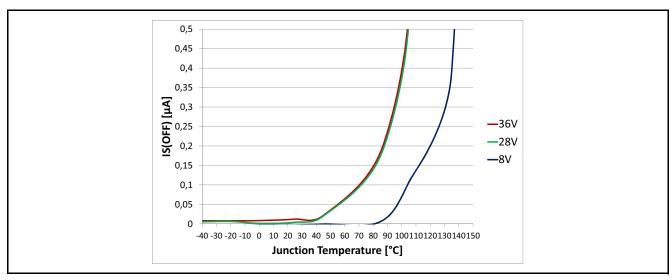


Figure 33 Standby Current for Whole Device with Load. $I_{S(OFF)} = f(T_J; V_S)$

Characterization Results

9.2 Power Stage

9.2.1 Output Voltage Drop Limitation at Low Load Current

P_5.5.4

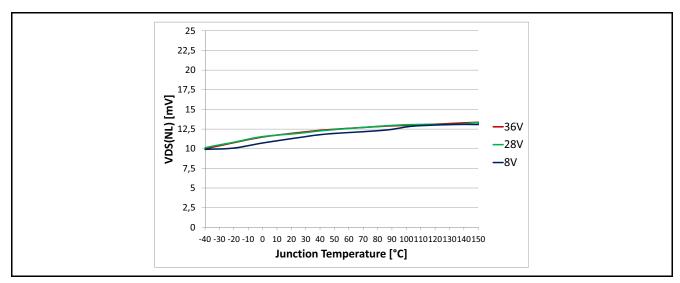


Figure 34 Output Voltage Drop Limitation at Low Load Current $V_{DS(NL)} = f(T_J; V_S) I_L = I_{L(0)} = 50 \text{ mA}$

9.2.2 Drain to Source Clamp Voltage

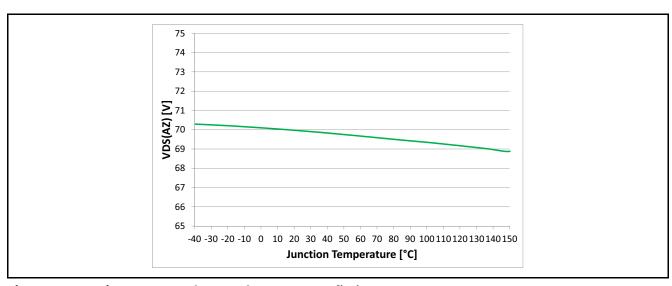


Figure 35 Drain to Source Clamp Voltage $V_{DS(AZ)} = f(T_J)$

Characterization Results

9.2.3 Slew Rate at Turn ON

P_5.5.11

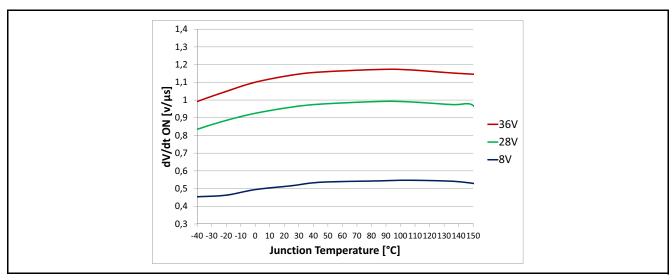


Figure 36 Slew Rate at Turn ON $dV/dt_{ON} = f(T_J; V_S)$, $R_L = 12 \Omega$

9.2.4 Slew Rate at Turn OFF

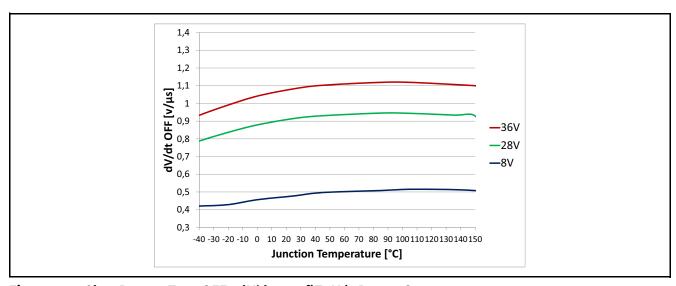


Figure 37 Slew Rate at Turn OFF - $dV/dt_{OFF} = f(T_J; V_S)$, $R_L = 12 \Omega$



9.2.5 Turn ON

P_5.5.14

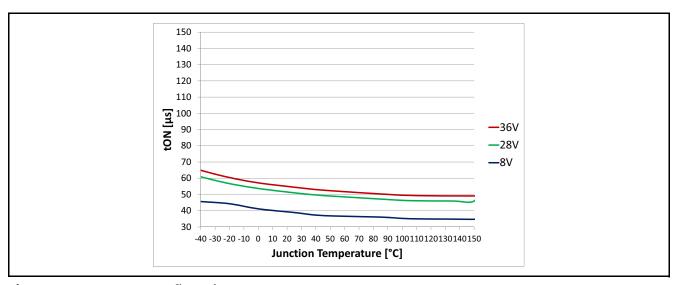


Figure 38 Turn ON $t_{ON} = f(T_J; V_S), R_L = 12 \Omega$

9.2.6 Turn OFF

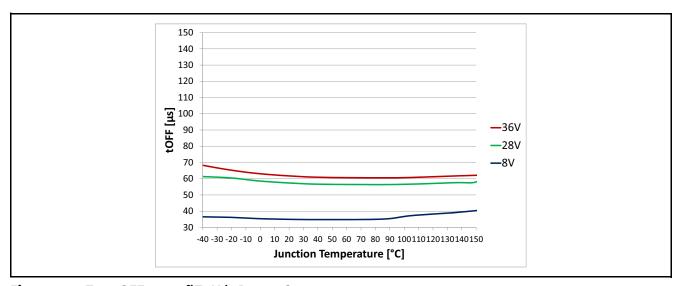


Figure 39 Turn OFF $t_{OFF} = f(T_J; V_S), R_L = 12 \Omega$

9.2.7 Turn ON / OFF Matching

P_5.5.16

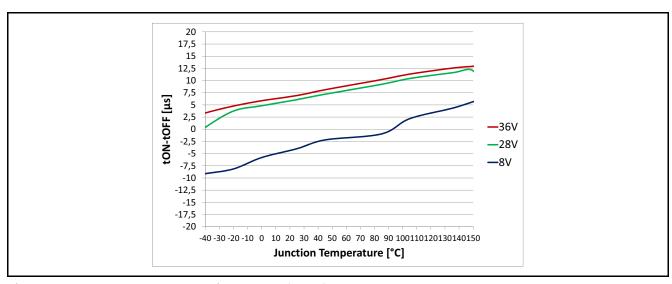


Figure 40 Turn ON / OFF matching $\Delta t_{SW} = f(T_J; V_S)$, $R_L = 12 \Omega$

9.2.8 Switch ON Energy

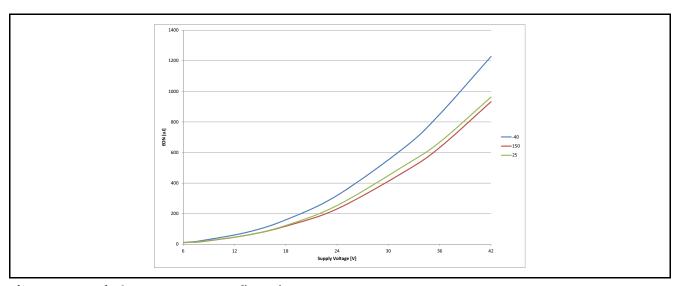


Figure 41 Switch ON Energy $E_{ON} = f(T_J; V_S)$, $R_L = 12 \Omega$

Characterization Results

9.2.9 Switch OFF Energy

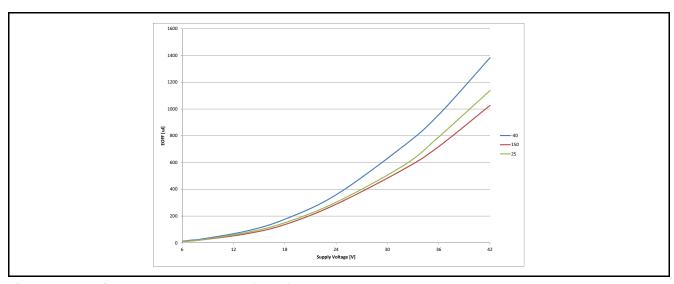


Figure 42 Switch OFF Energy $E_{OFF} = f(T_J; V_S), R_L = 12 \Omega$

Characterization Results

9.3 Protection Functions

9.3.1 Overload Condition in the Low Voltage Area

P_6.6.4

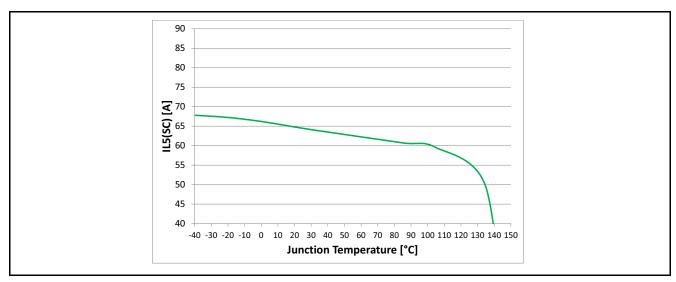
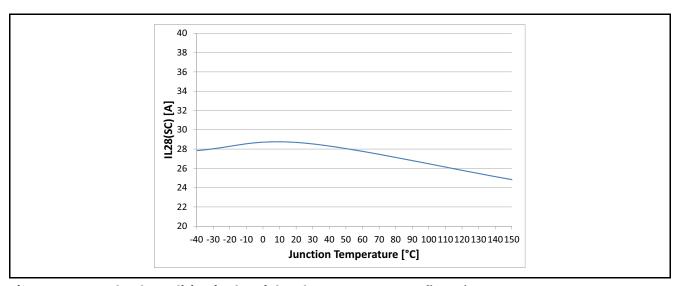


Figure 43 Overload Condition in the Low Voltage Area $I_{L5(SC)} = f(T_J; V_S)$

9.3.2 Overload Condition in the High Voltage Area

P_6.6.7



44

Figure 44 Overload Condition in the High Voltage Area $I_{L28(SC)} = f(T_J; V_S)$

Characterization Results

9.4 Diagnostic Mechanism

9.4.1 Current Sense at no Load

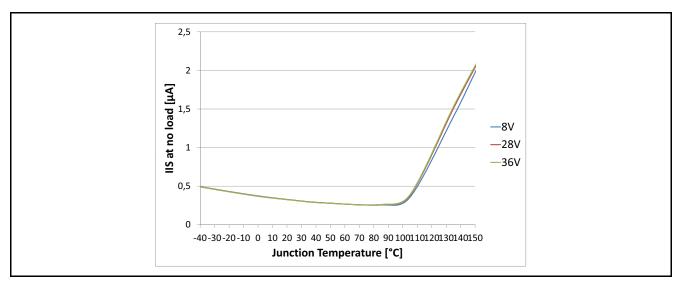
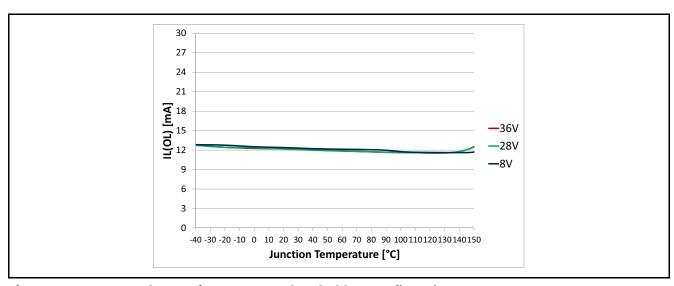


Figure 45 Current Sense at no Load $I_{L(OL)} = f(T_J; V_S)$, $I_L = 0$ A

9.4.2 Open Load Detection Threshold in ON State

P_7.5.2



45

Figure 46 Open Load Detection ON State Threshold $I_{L(OL)} = f(T_J; V_S)$



9.4.3 Sense Signal Maximum Voltage

P_7.5.3

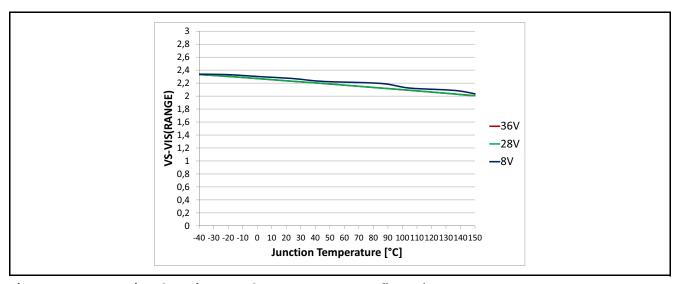


Figure 47 Sense Signal Maximum Voltage $V_S - V_{IS (RANGE)} = f(T_J; V_S)$

9.4.4 Sense Signal Maximum Current

P_7.5.7

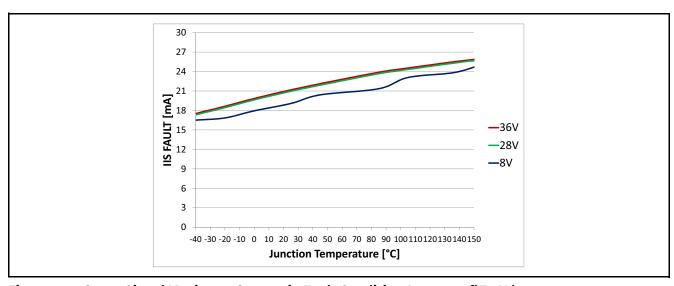


Figure 48 Sense Signal Maximum Current in Fault Condition $I_{IS(FAULT)} = f(T_J; V_S)$

9.5 Input Pins

9.5.1 Input Voltage Threshold ON to OFF

P_8.4.1

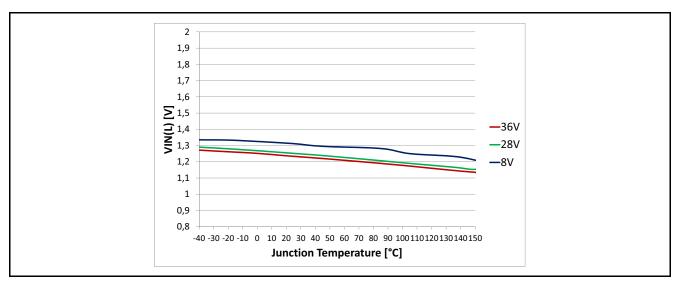
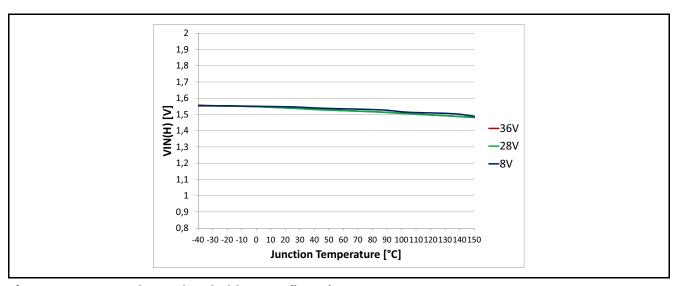


Figure 49 Input Voltage Threshold $V_{IN(L)} = f(T_J; V_S)$

9.5.2 Input Voltage Threshold OFF to ON

P_8.4.2



47

Figure 50 Input Voltage Threshold $V_{IN(H)} = f(T_J; V_S)$

Characterization Results

9.5.3 Input Voltage Hysteresis

P_8.4.3

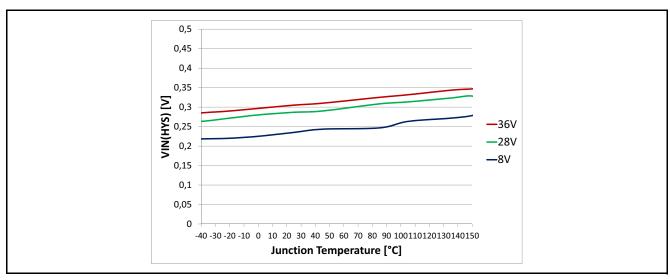


Figure 51 Input Voltage Hysteresis $V_{IN(HYS)} = f(T_J; V_S)$

9.5.4 Input Current High Level

P_8.4.5

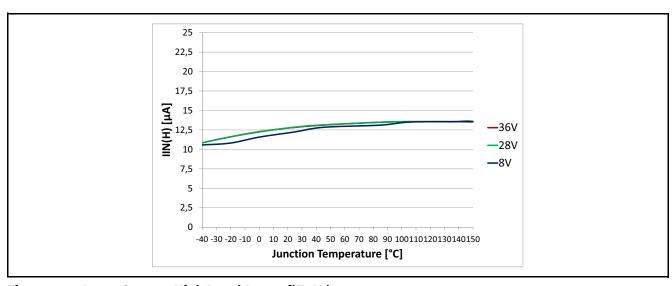


Figure 52 Input Current High Level $I_{IN(H)} = f(T_J; V_S)$

Application Information



10 Application Information

Note:

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

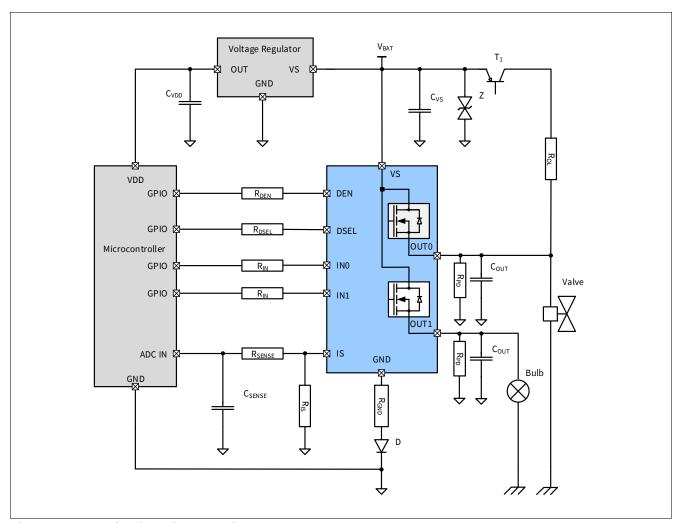


Figure 53 Application Diagram with BTT6030-2ERA

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 12 Bill of Material

Reference	Value	Purpose
R _{IN}	10 kΩ	Protection of the microcontroller during overvoltage, reverse polarity Guarantee BTT6030-2ERA channels OFF during loss of ground
R_{DEN}	10 kΩ	Protection of the microcontroller during overvoltage, reverse polarity
$R_{\rm DSEL}$	10 kΩ	Protection of the microcontroller during overvoltage, reverse polarity
R _{PD}	47 kΩ	Polarization of the output for short circuit to $V_{\rm S}$ detection Improve BTT6030-2ERA immunity to electromagnetic noise

PROFET™ +24 V BTT6030-2ERA



Application Information

Table 12 **Bill of Material** (cont'd)

Reference	Value	Purpose
R _{OL}	1.5 kΩ	Ensures polarization of the BTT6030-2ERA output during open load in OFF diagnostic
R_{IS}	1.2 kΩ	Sense resistor
R _{SENSE}	4.7 kΩ	Overvoltage, reverse polarity, loss of ground. Value to be tuned with microcontroller specification.
C_{SENSE}	100 pF	Sense signal filtering.
C_{OUT}	10 nF	Protection of the device during ESD and BCI
T1	Dual NPN/PNP	Switch the battery voltage for open load in OFF diagnostic
R_{GND}	27 Ω	Protection of the BTT6030-2ERA during overvoltage
D	BAS21	Protection of the BTT6030-2ERA during reverse polarity
Z	58 V Zener diode	Protection of the device during overvoltage
C_{VS}	100 nF	Filtering of voltage spikes at the battery line

Further Application Information 10.1

- Please contact us to get the pin FMEA
- Existing App. Notes
- For further information you may visit www.infineon.com

Package Outlines



11 Package Outlines

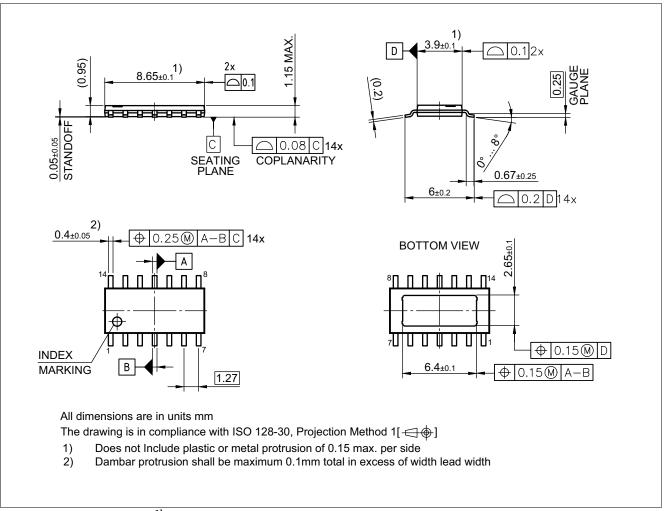


Figure 54 PG-TDSO-14¹⁾ (Plastic Dual Small Outline Package) (RoHS-Compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Legal Disclaimer for Short-Circuit Capability

Infineon disclaims any warranties and liablilities, whether expressed or implied, for any short-circuit failures below the threshold limit.

Further information on packages

https://www.infineon.com/packages

¹⁾ Dimensions in mm

PROFET™ +24 V

BTT6030-2ERA



Revision History

Revision History 12

Version	Date	Changes
1.00	2019-03-09	Creation of the datasheet

PROFET™ +24 V BTT6030-2ERA



Table of Contents

1	Overview	. 1
2	Block Diagram	. 3
3	Pin Configuration	. 4
3.1	Pin Assignment	
3.2	Pin Definitions and Functions	
3.3	Voltage and Current Definition	. 5
4	General Product Characteristics	. 6
4.1	Absolute Maximum Ratings	
4.2	Functional Range	
4.3	Thermal Resistance	
4.3.1 4.3.2	PCB Set-Up Thermal Impedance Thermal Impedance	
	•	
5	Power Stage	
5.1 5.2	Output ON-State Resistance	
5.3	Inductive Load	
5.3.1	Output Clamping	
5.3.2	Maximum Load Inductance	
5.4	Inverse Current Capability	
5.5	Electrical Characteristics Power Stage	16
6	Protection Functions	
3.1	Loss of Ground Protection	
3.2	Undervoltage Protection	
6.3 6.4	Overvoltage Protection	
5. 4 6.5	Overload Protection	
5.5 6.5.1	Current Limitation	
6.5.2	Temperature Limitation in the Power DMOS	
6.6	Electrical Characteristics for the Protection Functions	
7	Diagnostic Functions	24
7.1	IS Pin	
7.2	SENSE Signal in Different Operating Modes	25
7.3	SENSE Signal in the Nominal Current Range	26
7.3.1	SENSE Signal Variation as a Function of Temperature and Load Current	
7.3.2	SENSE Signal Timing	
7.3.3	SENSE Signal in Open Load	
7.3.3.1 7.3.3.2	Open Load in OFF Diagnostic	
7.3.3.2 7.3.3.3	Open Load in OFF Diagnostic	
7.3.4	SENSE Signal with OUT in Short Circuit to V_S	
7.3.5	SENSE Signal in Case of Overload	
7.3.6	SENSE Signal in Case of Inverse Current	
7.4	Electrical Characteristics Diagnostic Function	
8	Input Pins	34
3.1	Input Circuitry	
3.2	DEN / DSEL Pin	
3.3	Input Pin Voltage	
3.4	Electrical Characteristics	35

PROFET™ +24 V BTT6030-2ERA



9	Characterization Results	. 36
9.1	General Product Characteristics	. 36
9.1.1	Minimum Functional Supply Voltage	. 36
9.1.2	Undervoltage Shutdown	. 36
9.1.3	Current Consumption One Channel Active	. 37
9.1.4	Current Consumption Two Channels Active	. 37
9.1.5	Standby Current for Whole Device with Load	. 38
9.2	Power Stage	. 39
9.2.1	Output Voltage Drop Limitation at Low Load Current	. 39
9.2.2	Drain to Source Clamp Voltage	
9.2.3	Slew Rate at Turn ON	. 40
9.2.4	Slew Rate at Turn OFF	. 40
9.2.5	Turn ON	
9.2.6	Turn OFF	. 41
9.2.7	Turn ON / OFF Matching	. 42
9.2.8	Switch ON Energy	
9.2.9	Switch OFF Energy	
9.3	Protection Functions	
9.3.1	Overload Condition in the Low Voltage Area	
9.3.2	Overload Condition in the High Voltage Area	
9.4	Diagnostic Mechanism	
9.4.1	Current Sense at no Load	
9.4.2	Open Load Detection Threshold in ON State	
9.4.3	Sense Signal Maximum Voltage	
9.4.4	Sense Signal Maximum Current	
9.5	Input Pins	
9.5.1	Input Voltage Threshold ON to OFF	
9.5.2	Input Voltage Threshold OFF to ON	
9.5.3	Input Voltage Hysteresis	
9.5.4	Input Current High Level	. 48
10	Application Information	. 49
10.1	Further Application Information	. 50
11	Package Outlines	. 51
12	Revision History	. 52
	Table of Contents	53

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Document reference BTT6030-2ERA

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