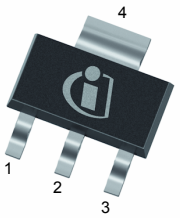
MOSFET

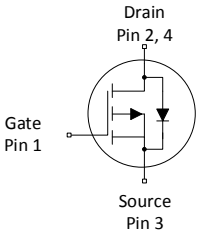
Small Signal MOSFET, -60 V

PG-SOT223



Features

- P-channel
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

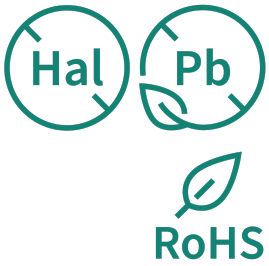


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	-60	V
$R_{DS(on),max}$	250	mΩ
I_D	-3.2	A
Q_{oss}	-4.4	nC
Q_G	-6.7	nC



Part number	Package	Marking	Related links
BSP171I	PG-SOT223	BSP171I	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	-3.2	A	V_{GS}=-10 V, T_C=25 °C
				-2		V_{GS}=-10 V, T_C=100 °C
				-1.81		V_{GS}=-4.5 V, T_C=100 °C
				-1.9		V_{GS}=-10 V, T_A=25 °C, R_{thJA}=70 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	-12.8	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	257	mJ	I_D=-1.9 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	5	W	T_C=25 °C
				1.8		T_A=25 °C, R_{thJA}=70 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	25	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5]	R_{thJA}			70		

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-60	-	-	V	V_{GS}=0 V, I_D=-250 µA
Gate threshold voltage	$V_{GS(th)}$	-1.0	-1.5	-2.0	V	V_{DS}=V_{GS}, I_D=-270 µA
Zero gate voltage drain current	I_{DSS}	-	-0.1	-1	µA	V_{DS}=-60 V, V_{GS}=0 V, T_j=25 °C
			-10	-100		V_{DS}=-60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	V_{GS}=-20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	177.1	250	mΩ	V_{GS}=-10 V, I_D=-1.9 A
			210.7	310		V_{GS}=-4.5 V, I_D=-1.7 A
Gate resistance	R_G	-	5.6	-	Ω	-
Transconductance	g_{fs}	-	4.4	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=-1.9 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [6]	C_{iss}	-	420	550	pF	V_{GS}=0 V, V_{DS}=-30 V, f=1 MHz
Output capacitance [6]	C_{oss}		60	78		
Reverse transfer capacitance [6]	C_{rss}		15	26		
Turn-on delay time	$t_{d(on)}$	-	4.0	-	ns	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-1.9 A, $R_{G,ext}$=6 Ω
Rise time	t_r		2.0			
Turn-off delay time	$t_{d(off)}$		24.0			
Fall time	t_f		11.9			

[6] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-1.21	-	nC	V_{DD}=-30 V, I_D=-1.9 A, V_{GS}=0 to -4.5 V
Gate charge at threshold	$Q_{g(th)}$		-0.63	-	nC	
Gate to drain charge [8)]	Q_{gd}		-3.3	-4.9	nC	
Switching charge	Q_{sw}		-3.9	-	nC	
Gate charge total [8)]	Q_g		-6.7	-8.4	nC	
Gate plateau voltage	$V_{plateau}$		-2.9	-	V	
Gate charge total [8)]	Q_g	-	-13.9	-18.5	nC	V_{DD}=-30 V, I_D=-1.9 A, V_{GS}=0 to -10 V
Output charge [8)]	Q_{oss}	-	-4.4	-5.9	nC	V_{DS}=-30 V, V_{GS}=0 V

7) See "Gate charge waveforms" for parameter definition

8) Defined by design. Not subject to production test.

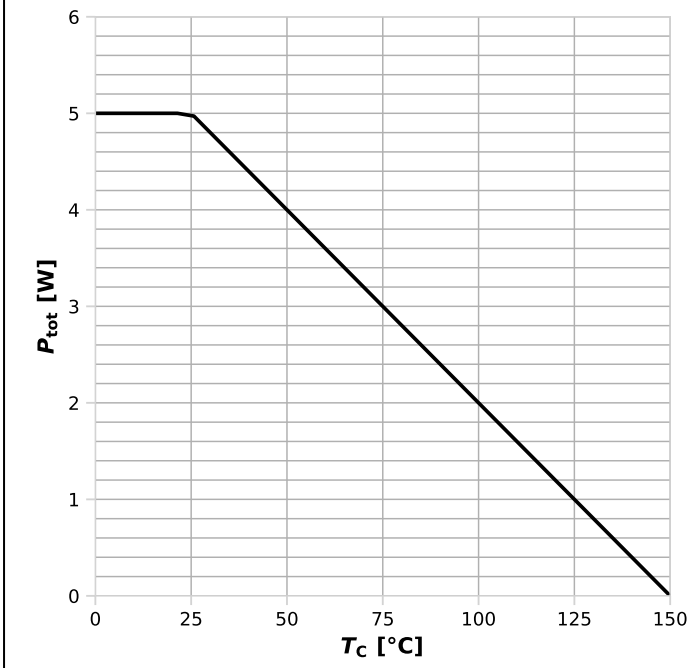
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-3.2	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			-12.8		
Diode forward voltage	V_{SD}	-	-0.81	-1.2	V	V_{GS}=0 V, I_F=-1.5 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	31.8	63.6	ns	V_R=-30 V, I_F=-1.9 A, di_F/dt=-100 A /µs
Reverse recovery charge [9)]	Q_{rr}		42.6	85.2	nC	

9) Defined by design. Not subject to production test.

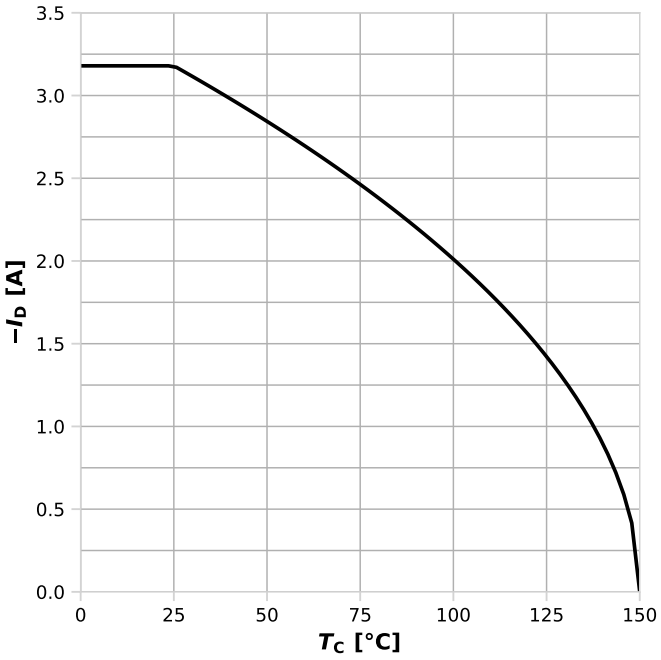
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



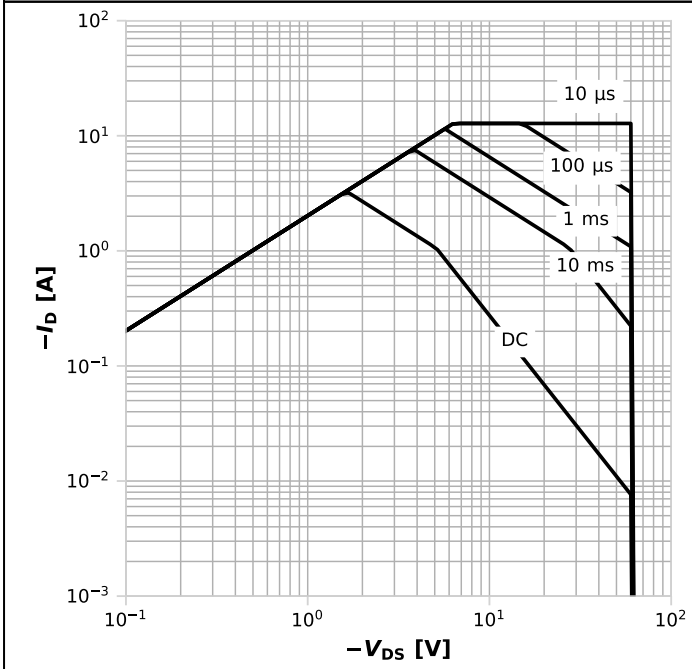
P_{tot}=f(T_C)

Diagram 2: Drain current



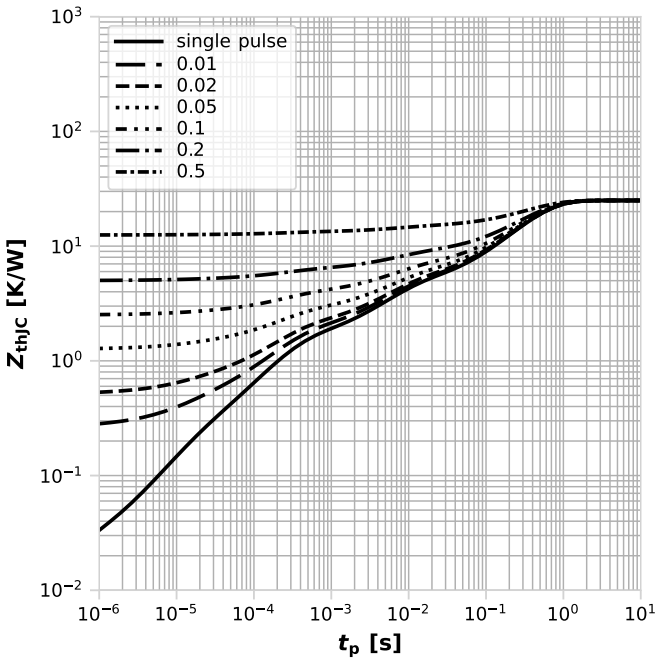
I_D=f(T_C); $|V_{GS}|$≥10 V

Diagram 3: Safe operating area



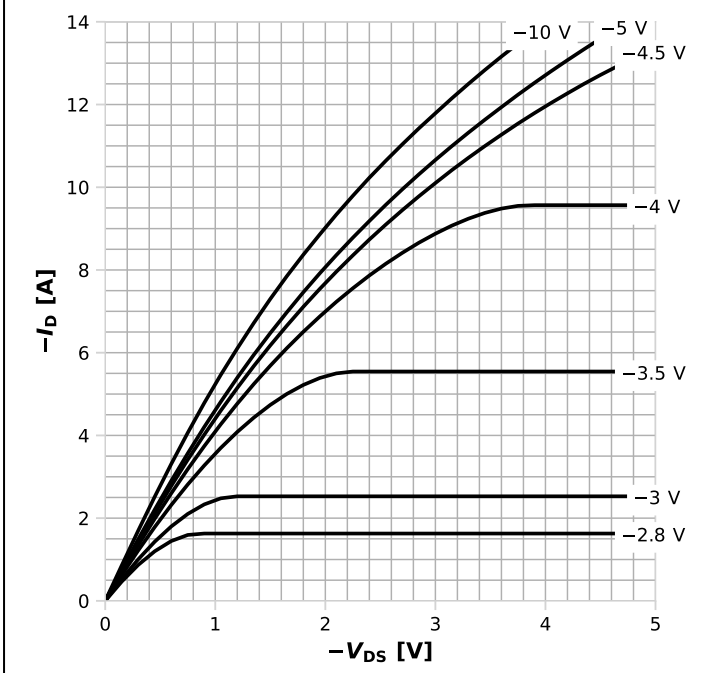
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



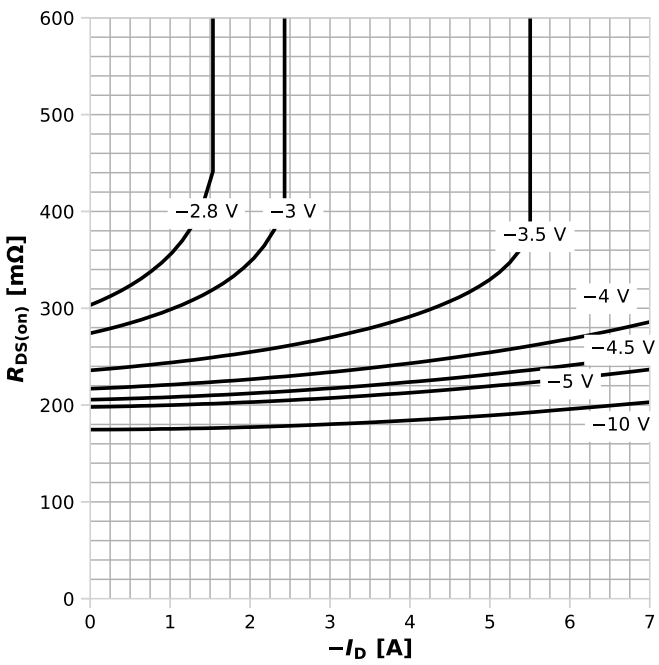
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



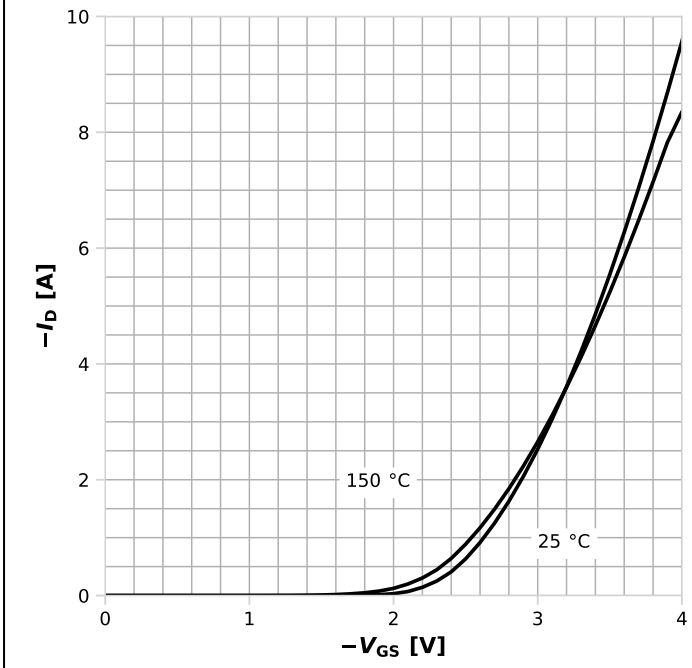
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



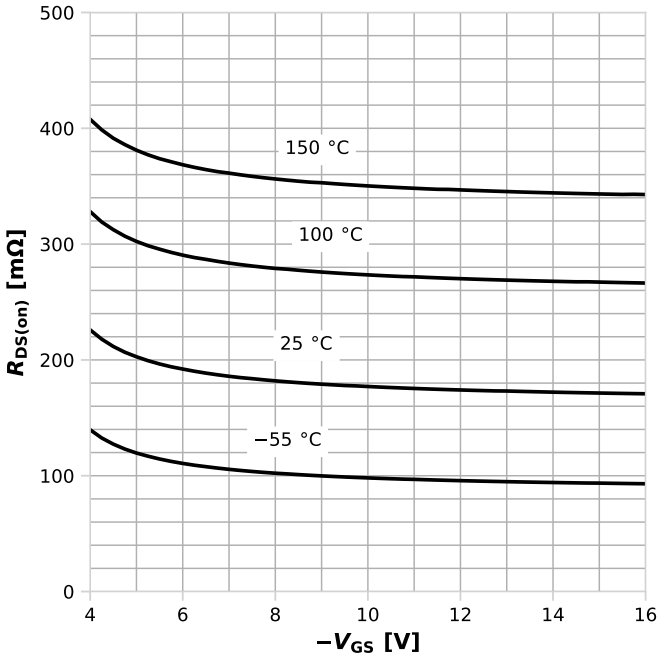
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



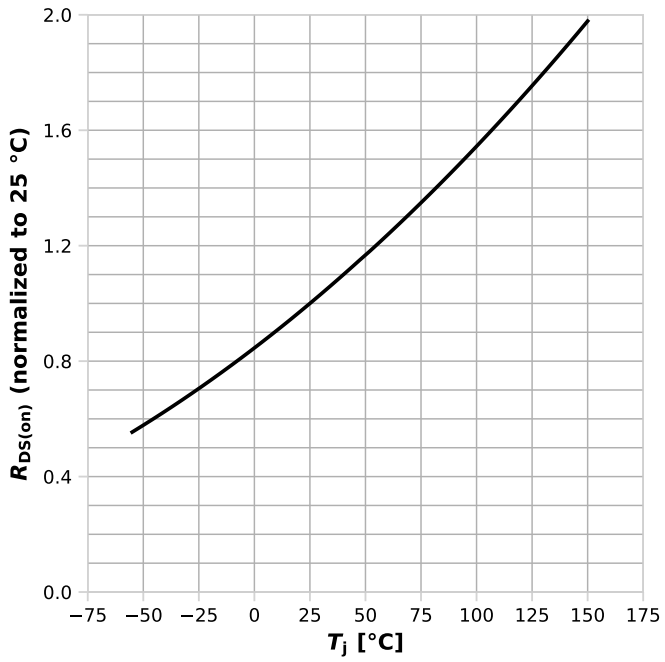
I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



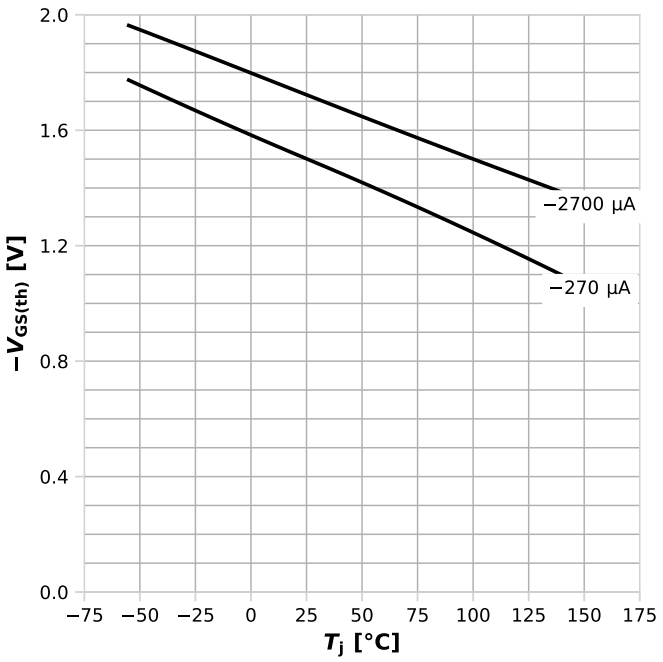
$R_{DS(on)}$=f(V_{GS}), I_D=-1.9 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



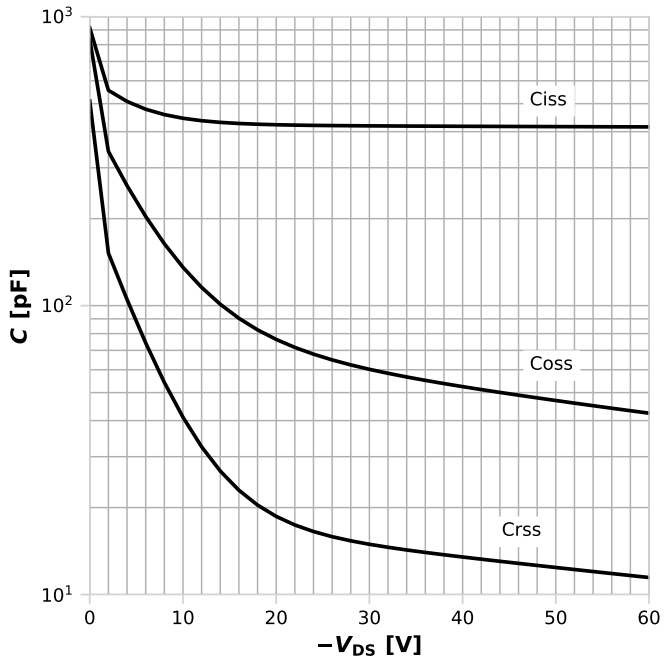
$R_{DS(on)}$=f(T_j), I_D=-1.9 A, V_{GS}=-10 V

Diagram 10: Typ. gate threshold voltage



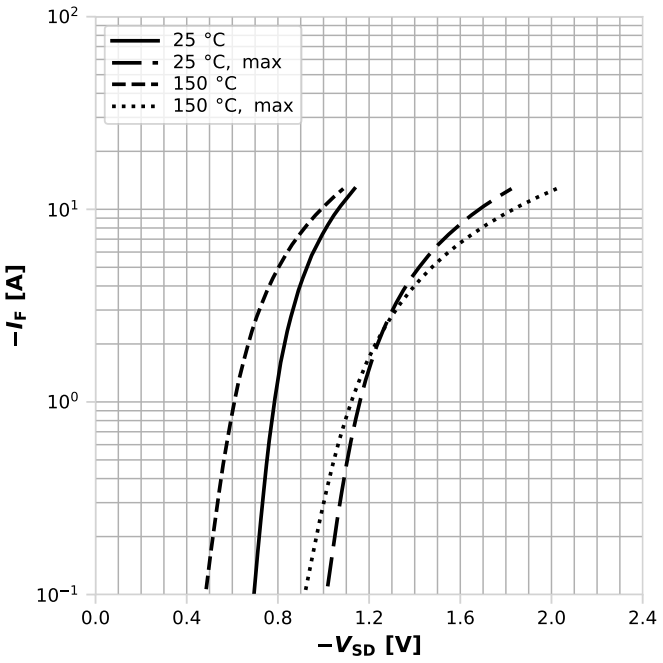
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

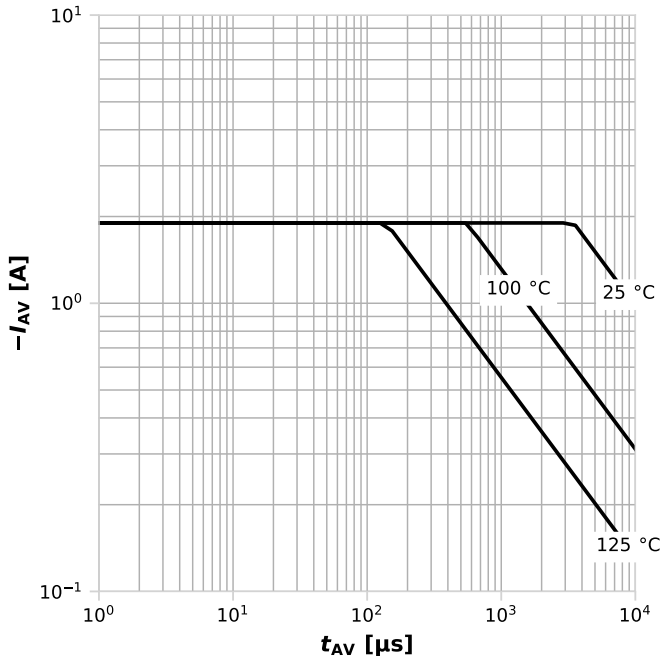
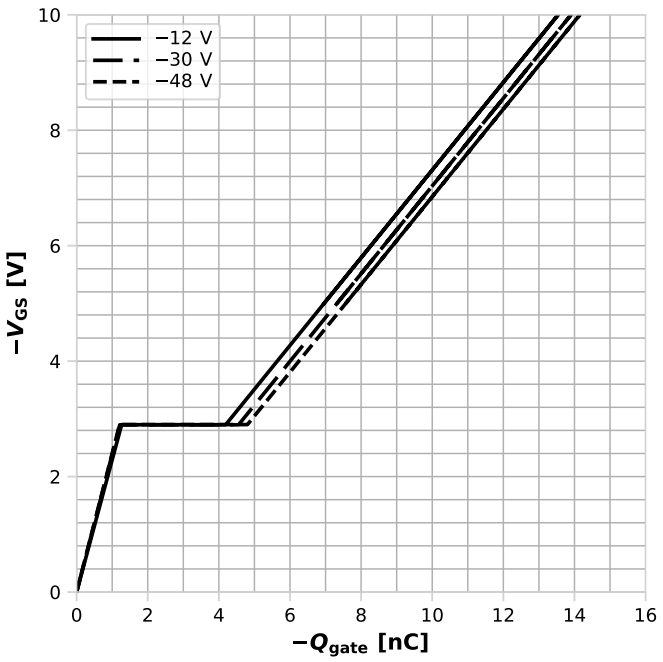
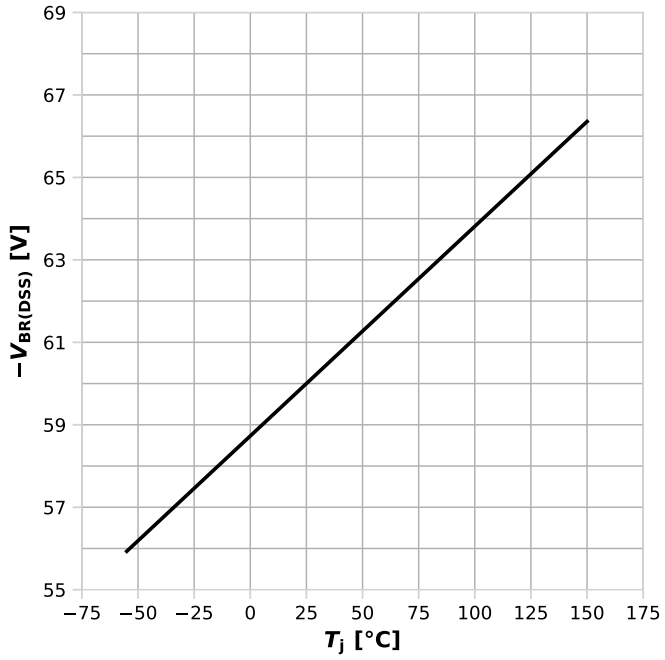
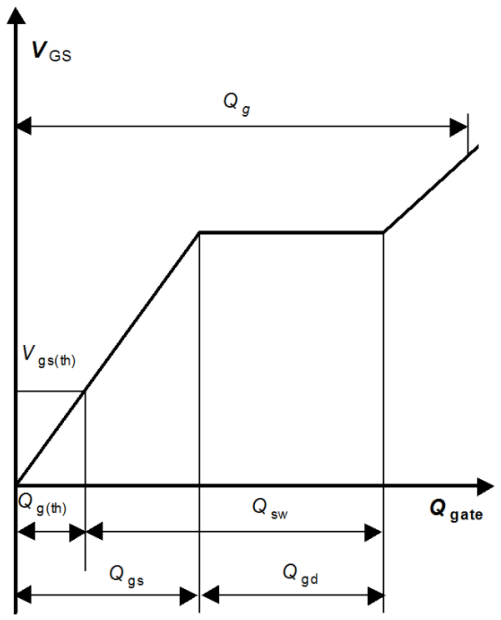
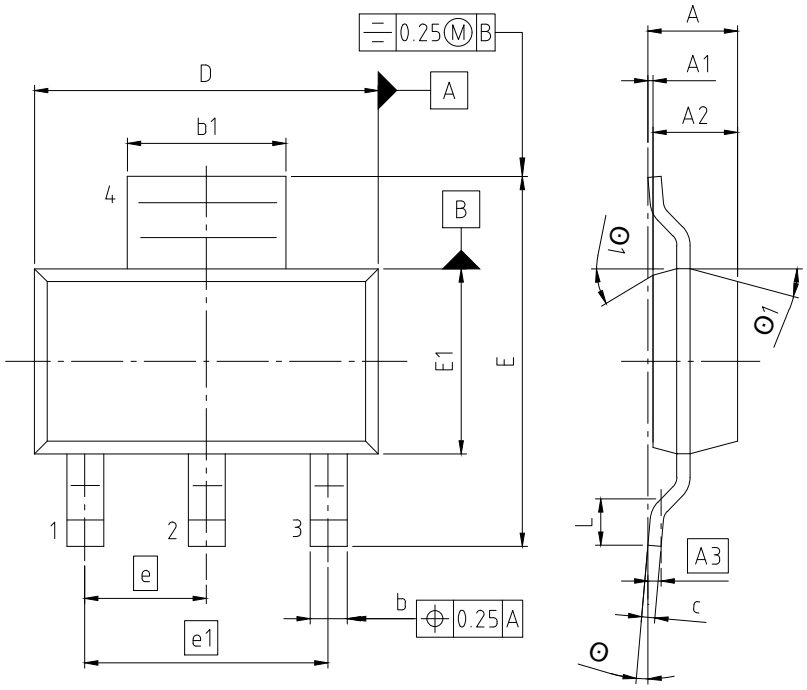
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=-1.9 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=-250 µA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-SOT223-4-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	1.40	1.80
A1	0.00	0.10
A2	1.50	1.70
A3	0.25	
b	0.60	0.80
b1	2.90	3.10
c	0.23	0.32
D	6.30	6.70
E	6.70	7.30
E1	3.30	3.70
N	4	
e	2.30	
e1	4.60	
L	0.5	---
Θ	0°	10°
Θ1	10°	15°

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH,
PROTRUSION OR GATE BURRS

Figure 1 Outline PG-SOT223, dimensions in mm

Revision history

BSP171I

Revision 2025-02-16, Rev. 2.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2025-02-16	Release of final datasheet

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