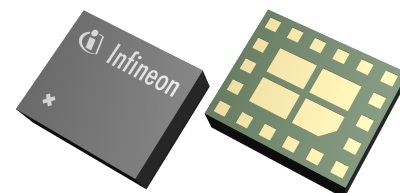


BGSX44MU18

4P4T antenna cross switch with MIPI RFFE control interface

Features

- High linearity up to 37 dBm peak power
- Fast switching time (max 2 μ s) for 5G SRS applications
- Low insertion loss and high port to port isolation up to 7.125 GHz
- Low power consumption allows to use MIPI RFFE supply
- MIPI RFFE 2.1 control interface
- Software and hardware programmable USID
- Ultra low profile lead-less plastic package (MSL-3, 260 °C per IPC/JEDEC J-STD-20)
- RoHS and WEEE compliant package



Potential applications

- 4P4T antenna routing/swapping for cellular mobile devices
- 4P4T antenna routing/swapping for 5G SRS application
- GSM, WCDMA, LTE and 5G FR1 applications
- 4x4 MIMO applications
- SAR reduction

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

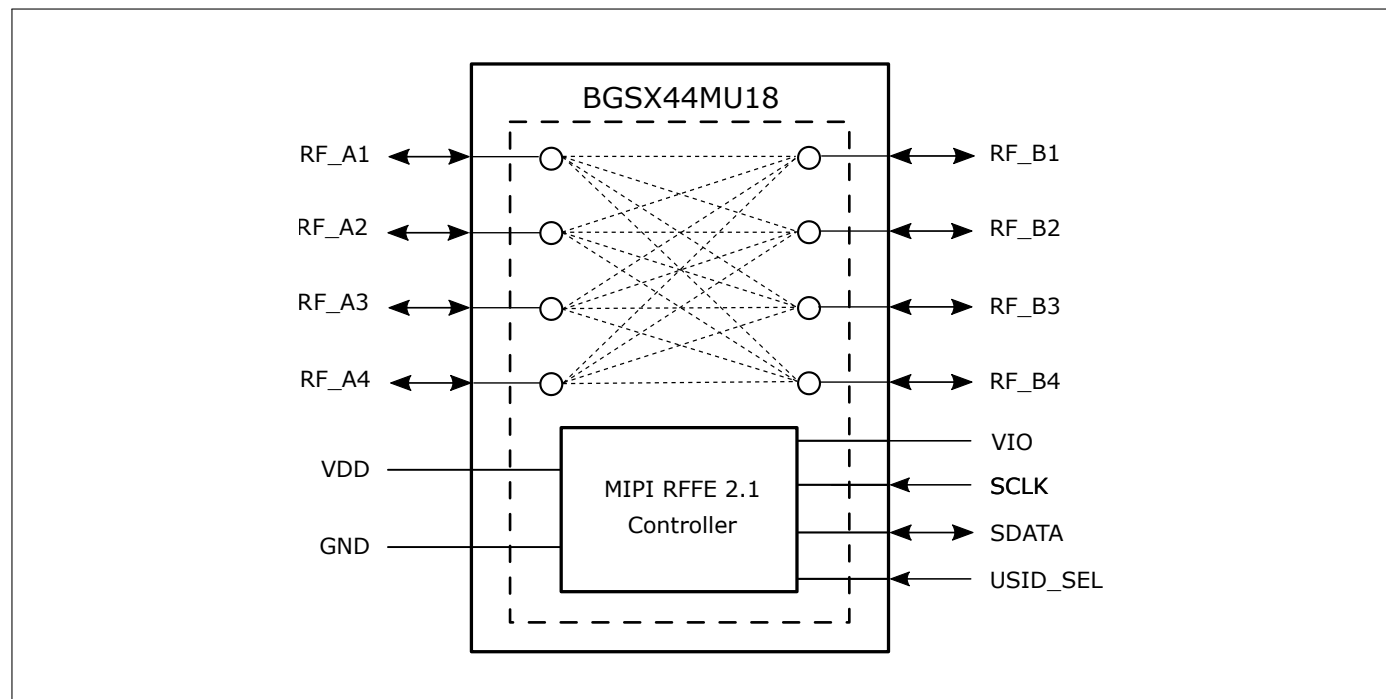
The BGSX44MU18 RF CMOS switch is specifically designed for LTE and 5G FR1 four-antenna applications. This 4P4T cross-switch offers low insertion loss and low harmonic generation.

The switch is controlled via a MIPI RFFE control interface. The on-chip controller allows power-supply voltages from 1.65 to 1.95 V. The switch features direct-connect-to-battery functionality and DC-free RF ports. Unlike GaAs technology, external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. The device has a very small size of only 2.0 mm x 2.4 mm and a thickness of 0.63 mm.

Table 1: Ordering information

Product type	Marking	Package
BGSX44MU18	X44A	PG-WLGA-18-1

Block diagram



BGSX44MU18

4P4T antenna cross switch with MIPI RFFE control interface

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Absolute maximum ratings

1 Absolute maximum ratings

Table 2: Absolute maximum ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	-0.3	–	3.9	V	–
Abs-Max RF input power	$P_{RF,max}$	–	–	38	dBm	Duty cycle of 25 %, frequency 0.4–7.125 GHz, VSWR 1:1
ESD robustness, HBM ¹⁾	$V_{ESD,HBM}$	-2	–	+2	kV	–
ESD robustness, CDM ²⁾	$V_{ESD,CDM}$	-1	–	+1	kV	–
Maximum DC-voltage on RF ports and RF-ground	V_{RFDC}	0	–	0	V	There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0 V
RFFE supply voltage	V_{IO}	-0.3	–	2.2	V	–
RFFE control voltage levels	$V_{SCLK},$ $V_{SDATA},$ V_{USID_SEL}	-0.3	–	$V_{IO} + 0.5$	V	–
Storage temperature range	T_{STG}	-55	–	150	$^\circ\text{C}$	–
Junction temperature	T_j	-40	–	125	$^\circ\text{C}$	–

¹⁾ Human Body Model ANSI/ESDA/JEDEC JS-001 ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$).

²⁾ Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

Warning: Stresses above the maximum values listed in Tab. 2 may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the maximum operation conditions specified in Tab. 3 may affect device reliability and life time. Functionality of the device might not be given under these conditions.

2 Operation ranges and general characteristics

Table 3: Operation ranges

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Max RF input power	$P_{RF,max}$	–	–	37	dBm	Peak envelope power of a 5G NR signal ¹⁾ , frequency 0.4–7.125 GHz, VSWR 1:1
		–	–	36	dBm	Pulsed RF input power, duty cycle of 25 % with $T_{period} = 4615 \mu s$, through-path, frequency 0.4–7.125 GHz, VSWR 1:1
Supply voltage	V_{DD}	1.6	1.8	3.6	V	For single supply operation ($V_{DD} = V_{IO}$ respectively V_{DD} connected to V_{IO}): $V_{DD,min} = 1.65 V$ and $V_{DD,max} = 1.95 V$
Ambient temperature	T_A	-40	25	85	°C	–

¹⁾MCS 27 (256 QAM) OFDM, 60 kHz sub carrier spacing, 100 MHz bandwidth, RMS power is 9 dB below peak power.

Table 4: General characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Supply current	I_{DD}	–	0.6	3.2	μA	Low-power mode
		–	26	50	μA	Active mode, $P_{RF} = 0 \text{ dBm}$
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage ¹⁾	V_{IH}	$0.7 \cdot V_{IO}$	–	V_{IO}	V	–
RFFE input low voltage ¹⁾	V_{IL}	0	–	$0.3 \cdot V_{IO}$	V	–
RFFE output high voltage ¹⁾	V_{OH}	$0.8 \cdot V_{IO}$	–	V_{IO}	V	–
RFFE output low voltage ¹⁾	V_{OL}	0	–	$0.2 \cdot V_{IO}$	V	–
RFFE control input capacitance	C_{Ctrl}	–	2	3	pF	at SCLK, SDATA, and USID_SEL
RFFE supply current	I_{IO}	–	0.04	6	μA	Idle mode without SCLK and SDATA activity/traffic

¹⁾Valid for SDATA, SCLK, and USID_SEL

RF characteristics

3 RF characteristics

Table 5: RF characteristics at $T_A = -40\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$, $P_{RF} = 0\text{ dBm}$, $V_{DD} = 1.6\text{ V} \dots 3.6\text{ V}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Insertion loss ¹⁾ at 25°C						
RF_Ax to RF_By all other paths off x,y={1,...,4}	I _L _{RF_Ax-RF_By}	–	0.46	0.54	dB	600–960 MHz
		–	0.50	0.57	dB	1160–1300 MHz
		–	0.54	0.63	dB	1400–1700 MHz
		–	0.58	0.72	dB	1700–2200 MHz
		–	0.65	0.80	dB	2200–2700 MHz
		–	0.79	1.00	dB	3300–4200 MHz
		–	0.91	1.20	dB	4400–5000 MHz
		–	1.12	1.64	dB	5150–5925 MHz
–	1.50	2.40	dB	5925–7125 MHz		
Insertion loss ¹⁾						
RF_Ax to RF_By all other paths off x,y={1,...,4}	I _L _{RF_Ax-RF_By}	–	0.46	0.63	dB	600–960 MHz
		–	0.50	0.67	dB	1160–1300 MHz
		–	0.54	0.73	dB	1400–1700 MHz
		–	0.58	0.81	dB	1700–2200 MHz
		–	0.65	0.88	dB	2200–2700 MHz
		–	0.79	1.19	dB	3300–4200 MHz
		–	0.91	1.41	dB	4400–5000 MHz
		–	1.12	1.80	dB	5150–5925 MHz
–	1.50	2.70	dB	5925–7125 MHz		
Return loss ¹⁾						
RF_Ax to RF_By all other paths off x,y={1,...,4}	R _L _{RF_Ax-RF_By}	22	30	–	dB	600–960 MHz
		20	28	–	dB	1160–1300 MHz
		18	26	–	dB	1400–1700 MHz
		15	23	–	dB	1700–2200 MHz
		14	20	–	dB	2200–2700 MHz
		10	17	–	dB	3300–4200 MHz
		9	15	–	dB	4400–5000 MHz
		7	12	–	dB	5150–5925 MHz
5	9	–	dB	5925–7125 MHz		
Isolation ¹⁾						
In-Out isolation: RF_Ax to RF_By x,y={1,...,4}	I _{SO} _{RF_Ax-RF_By}	35	43	–	dB	600–960 MHz
		32	39	–	dB	1160–1300 MHz
		30	37	–	dB	1400–1700 MHz
		28	35	–	dB	1700–2200 MHz
		27	34	–	dB	2200–2700 MHz
		24	31	–	dB	3300–4200 MHz
		23	30	–	dB	4400–5000 MHz
		21	29	–	dB	5150–5925 MHz
20	29	–	dB	5925–7125 MHz		

¹⁾ Measured on application board, without any external matching components at RF ports.

RF characteristics

Table 6: RF characteristics at $T_A = -40\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$, $P_{RF} = 0\text{ dBm}$, $V_{DD} = 1.6\text{ V} \dots 3.6\text{ V}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Isolation ¹⁾						
In-In/Out-Out isolation: RF_Ax to RF_Ay with x!=y RF_Bx to RF_By with x!=y x,y={1,...,4}	ISO _{RF_Ax-RF_Ay} ISO _{RF_Bx-RF_By}	35	44	–	dB	600–960 MHz
		33	40	–	dB	1160–1300 MHz
		31	39	–	dB	1400–1700 MHz
		29	37	–	dB	1700–2200 MHz
		28	35	–	dB	2200–2700 MHz
		22	32	–	dB	3300–4200 MHz
		19	30	–	dB	4400–5000 MHz
		15	29	–	dB	5150–5925 MHz
		12	27	–	dB	5925–7125 MHz
Harmonic generation ¹⁾ at CW, VSWR 1:1 / 50 Ω						
2 nd Harmonic	P _{H2}	–	-82	-70	dBm	LTE LB, 663–915 MHz, P _{RF} = 26 dBm
		–	-75	-67	dBm	LTE MB, 1710–2020 MHz, P _{RF} = 26 dBm
		–	-67	-59	dBm	LTE HB, 2300–2690 MHz, P _{RF} = 29 dBm
		–	-62	-55	dBm	N77 NR, 3300–4200 MHz, P _{RF} = 29 dBm
		–	-65	-53	dBm	N79 NR, 4400–5000 MHz, P _{RF} = 29 dBm
3 rd Harmonic	P _{H3}	–	-84	-76	dBm	LTE LB, 663–915 MHz, P _{RF} = 26 dBm
		–	-79	-70	dBm	LTE MB, 1710–2020 MHz, P _{RF} = 26 dBm
		–	-69	-61	dBm	LTE HB, 2300–2690 MHz, P _{RF} = 29 dBm
		–	-65	-57	dBm	N77 NR, 3300–4200 MHz, P _{RF} = 29 dBm
		–	-64	-53	dBm	N79 NR, 4400–5000 MHz, P _{RF} = 29 dBm
Harmonic generation ¹⁾ at 25 % duty cycle, VSWR 1:1 / 50 Ω						
2 nd Harmonic	P _{H2}	–	-63	-52	dBm	GSM LB, 824–915 MHz, P _{RF} = 35 dBm
		–	-62	-53	dBm	GSM HB, 1710–1910 MHz, P _{RF} = 33 dBm
3 rd Harmonic	P _{H3}	–	-55	-48	dBm	GSM LB, 824–915 MHz, P _{RF} = 35 dBm
		–	-56	-48	dBm	GSM HB, 1710–1910 MHz, P _{RF} = 33 dBm

¹⁾ Measured on application board, without any external matching components at RF ports.

RF characteristics

Table 7: RF characteristics at $T_A = -40\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$, $P_{RF} = 0\text{ dBm}$, $V_{DD} = 1.6\text{ V} \dots 3.6\text{ V}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Intermodulation distortion IMD2 ¹⁾						
Band 1 IMD2 high	IMD2	–	-124	-117	dBm	Test conditions, see Tab. 8
Band 1 IMD2 low		–	-120	-108	dBm	
Band 5 IMD2 high		–	-120	-113	dBm	
Band 5 IMD2 low		–	-109	-92	dBm	
Band 7 IMD2 high		–	-114	-108	dBm	
Band 7 IMD2 low		–	-108	-98	dBm	
Band 3 + 5 IMD2 ULCA		–	-92	-84	dBm	
Band 3 + N77 IMD2 ENDC		–	-90	-83	dBm	

¹⁾ Measured on application board, without any external matching components at RF ports.**Table 8: IMD2 testcases¹⁾**

Band	Symbol	In-band frequency (MHz)	Blocker frequency 1 (MHz)	Blocker power 1 (dBm)	Blocker frequency 2 (MHz)	Blocker power 2 (dBm)
Band 1	$B1_{\text{IMD2,high}}$	2140	1950	20	4090	-15
	$B1_{\text{IMD2,low}}$	2140	1950	20	190	-15
Band 5	$B5_{\text{IMD2,high}}$	881.5	836.5	20	1718	-15
	$B5_{\text{IMD2,low}}$	881.5	836.5	20	45	-15
Band 7	$B7_{\text{IMD2,high}}$	2655	2535	20	5190	-15
	$B7_{\text{IMD2,low}}$	2655	2535	20	120	-15
Band 3 + Band 5 ULCA	$B3B5_{\text{IMD2,ULCA}}$	881.5	836.5	23	1718	10
Band 3 + N77 ENDC	$B3N77_{\text{IMD2,ENDC}}$	1842.5	1747.5	23	3590	10

¹⁾ Both blockers applied to same RF path.

RF characteristics

Table 9: RF characteristics at $T_A = -40\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$, $P_{RF} = 0\text{ dBm}$, $V_{DD} = 1.6\text{ V} \dots 3.6\text{ V}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Intermodulation distortion IMD3 ¹⁾						
Band 1 IMD3 high	IMD3	–	-126	-113	dBm	Test conditions, see Tab. 10
Band 1 IMD3 mid		–	-124	-113	dBm	
Band 5 IMD3 high		–	-92	-82	dBm	
Band 5 IMD3 mid		–	-125	-114	dBm	
Band 7 IMD3 high		–	-125	-114	dBm	
Band 7 IMD3 mid		–	-90	-78	dBm	
Band 1 + Band 3 ULCA		–	-126	-101	dBm	
Band 5 + N78 ENDC		–	-121	-108	dBm	

¹⁾ Measured on application board, without any external matching components at RF ports.**Table 10: IMD3 testcases¹⁾**

Band	Symbol	In-band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{\text{IMD3,high}}$	2140	1950	20	6040	-15
	$B1_{\text{IMD3,mid}}$	2140	1950	20	1760	-15
Band 5	$B5_{\text{IMD3,high}}$	881.5	836.5	20	2554.5	-15
	$B5_{\text{IMD3,mid}}$	881.5	836.5	20	791.5	-15
Band 7	$B7_{\text{IMD3,high}}$	2655	2535	20	7725	-15
	$B7_{\text{IMD3,mid}}$	2655	2535	20	2415	-15
Band 1 + Band 3 ULCA	$B1B3_{\text{IMD3,ULCA}}$	2140	1950	23	1760	10
Band 5 + N78 ENDC	$B5N78_{\text{IMD3,ENDC}}$	2122	3780	26	829	10

¹⁾ Both blockers applied to same RF path.

BGSX44MU18

4P4T antenna cross switch with MIPI RFFE control interface

RF characteristics

Table 11: RF characteristics at $T_A = -40\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$, $P_{RF} = 0\text{ dBm}$, $V_{DD} = 1.6\text{ V} \dots 3.6\text{ V}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Switching time ¹⁾						
Power up settling time	t _{PUP}	–	10	25	μs	Time from power up plus switch command, 50 % last SCLK falling edge to 90 % RF signal
Switching time	t _{ST}	–	1	2	μs	Time to switch between RF states, 50 % last SCLK falling edge to 90 % RF signal

¹⁾ Measured on application board, without any external matching components.

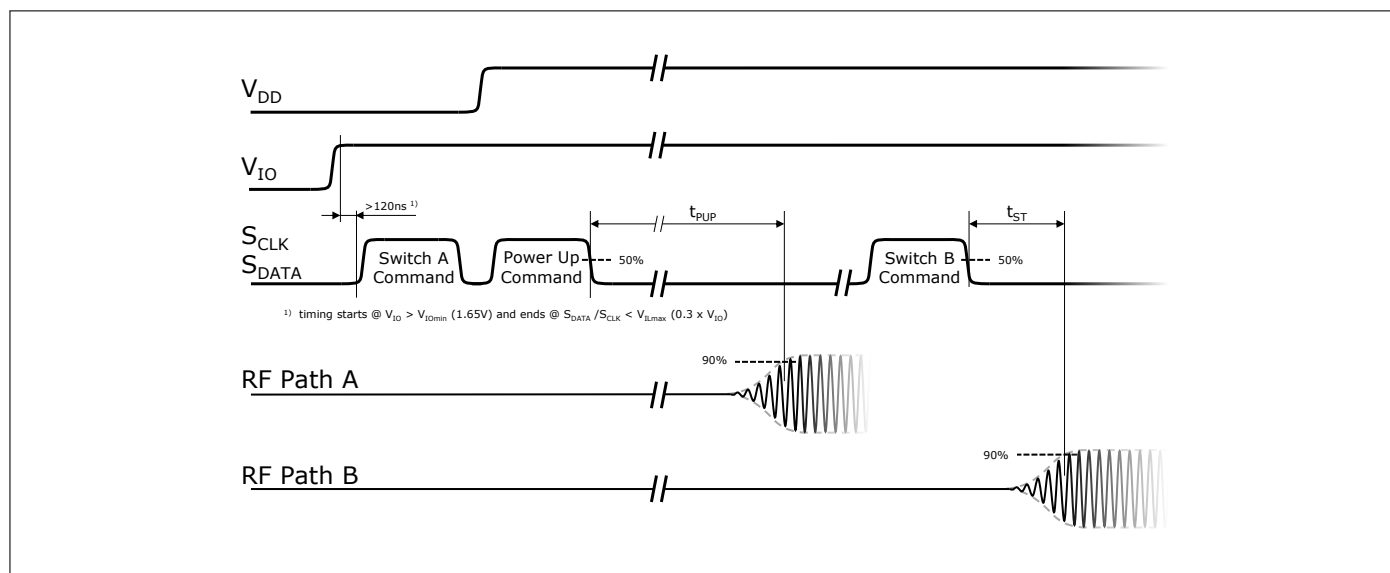


Figure 1: MIPI timing diagram

4 MIPI RFFE specification

The MIPI RFFE interface is implemented according to the following specifications and documents:

- MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017
- MIPI Alliance Errata 01 for MIPI RFFE Specification Version v2.1 - 24 February 2019
- Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)

Table 12: MIPI features, table I

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Standard reach RFFE bus length	Yes	RFFE Bus Length of up to 15 cm (standard)
Longer reach RFFE bus length feature (MIPI RFFE 2.1 optional feature)	Yes	Longer Reach allows for longer RFFE bus lengths. This requires a limitation to the Standard Frequency Range of RFFE plus additional timing requirements for all devices on the bus
Programmable driver strength (MIPI RFFE 2.x feature)	Yes	Allows to program MIPI device Bus driver strength (relevant for Read Back messages) up to 80 pF via BUS_LD-Register (0x2B); Default value: 50 pF
Register 0 write command sequence	Yes	Shortened Write Sequence for Register 0 Caution: only 7 LSBs in Reg 0 can be addressed
Register read and write command sequence	Yes	Standard Register Read/Write procedure addressing standard register space of 0x00 – 0x1F
Extended register read and write command sequence	Yes	Register Read/Write procedure addressing extended register space of 0x00 – 0xFF
Masked write command sequence (MIPI 2.1 optional feature)	Yes	Allow only certain bits in a register to be updated during a write command. Relevant Registers marked "MW" in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	SCLK range 32 kHz – 26 MHz for read and write commands
Support for extended frequency range operations for SCLK	Yes	SCLK range 26 MHz – 52 MHz for write commands
sRead (synchronous Read) full speed or half speed up to 26 MHz (MIPI 2.x feature)	Yes	Relaxed Slave setup time requirements as Master samples data on rising edge of SCLK signal
Regular read full speed or half speed up to 13 MHz (MIPI RFFE 1.10-2.x feature)	Yes	Stricter Slave setup time requirements as Master samples data on falling edge of SCLK signal
Product ID + extended product ID register	Yes	PRODUCT_ID (address 0x1D) and EXT_PRODUCT_ID (address 0x20) Registers

MIPI RFFE specification

Table 13: MIPI features, table II

Feature	Supported	Comment
Extended manufacturer ID (10->12 bit) (MIPI 2.1 optional feature)	Yes	The new 2 bits In MIPI 2.1 are placed in RFFE USID register at address 0x1F; value is 0 in IFX products
Revision ID register	Yes	This Register contains the Device Revision (address 0x21)
Programmable GSID (Group Slave Identifier)	Yes	RFFE 2.x GROUP_SID Register (at address 0x22); Only in case RFFE 1.1 backwards compatibility is supported: GROUP_SID0 bit-field access at address 0x1B (copy of GROUP_SID0)
Programmable USID (Unique Slave Identifier)	Yes	Device can be also explicitly addressed via combination of (old) USID, Manufacturer ID, and (extended) product ID to reprogram USID via (extended) Register Write sequence (see MIPI RFFE Spec v2.1 Chapter 6.2.1)
Trigger functionality	Yes	3 "standard" Triggers via PM_TRIG[5:0] consisting of 3 Mask- and 3 Trigger Bits
Ignored trigger handling in low power mode	Yes	When device is and stays in low power mode, write to trigger registers will be ignored (NOTE: when changing power mode, writing to trigger registers are not ignored)
Extended triggers and trigger masks (MIPI 2.1 optional feature)	Yes	additional eight Triggers and the associated Trigger Masks, have been added in MIPI 2.1 (registers at addresses 0x2D and 0x2E)
Broadcast / GSID write to PM TRIG register	Yes	The above mentioned Trigger Register (and extended trigger register) can be accessed via Broadcast/GSID writes to trigger several MIPI devices synchronously. NOTE: Trigger Mask bits are not changed with Broadcast/GSID writes
Reset	Yes	Reset is possible via VIO, PM TRIG or register SW_RST (0x23); NOTE: SW_RST only resets User Defined Registers, it does not reset the values of any reserved registers
Status / error sum register	Yes	RFFE 2.x ERR_SUM Register (address 0x24); only in case RFFE 1.1 backwards compatibility is supported: RFFE_STATUS Register access at address 0x1A (copy of ERR_SUM)
USID select pin	Yes	External pin (USID_SEL) for changing USID: see Tab. 14

Table 14: Default MIPI USID selection

External Condition (USID_SEL)	USID address
Ground	1010
VIO	1011

MIPI RFFE specification

Table 15: Register mapping, table I

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W		
0x00	SWITCH_CTRL_RF_A1	7:0	MODE_CTRL	Switch control of RF_A1; (see Tab. 18)	00000000	No	Yes Trigger 0-10	R/W MW		
0x01	SWITCH_CTRL_RF_A2	7:0	MODE_CTRL	Switch control of RF_A2 (see Tab. 18)	00000000	No	Yes Trigger 0-10	R/W MW		
0x02	SWITCH_CTRL_RF_A3	7:0	MODE_CTRL	Switch control of RF_A3 (see Tab. 18)	00000000	No	Yes Trigger 0-10	R/W MW		
0x03	SWITCH_CTRL_RF_A4	7:0	MODE_CTRL	Switch control of RF_A4 (see Tab. 18)	00000000	No	Yes Trigger 0-10	R/W MW		
0x1C	PM_TRIG	7	PWR_MODE(1) Operation mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W MW		
				1: Low power mode (LOW POWER)						
		6	PWR_MODE(0) State bit vector	0: No action (ACTIVE)	0					
				1: Powered reset (STARTUP to ACTIVE to LOW POWER)						
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No				
				1: Data not masked (ready for transfer to active REG)						
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0					
				1: Data not masked (ready for transfer to active REG)						
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0					
				1: Data not masked (ready for transfer to active REG)						
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes				
				1: Data transferred to active REG						
		1	TRIGGER_1	0: No action (data held in shadow REG)	0					
				1: Data transferred to active REG						
		0	TRIGGER_0	0: No action (data held in shadow REG)	0					
				1: Data transferred to active REG						
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	11101000	n/a	n/a	R		
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	n/a	n/a	R		
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001	n/a	n/a	R		
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID. These bits store the USID of the device.	See Tab. 14	No	No	R/W		

MIPI RFFE specification

Table 16: Register mapping, table II

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID	00000000	n/a	n/a	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision	0100	n/a	n/a	R
		3:0	SUB_REVISION	Chip sub revision	0001			
0x22	GSID	7:4	GSID0[3:0]	Primary group slave ID.	0000	No	No	R/W
		3:0	GSID1[3:0]	Secondary group slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	00000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	n/a	n/a	R
		6	COMMAND_FRAME_PARITY_ERR	Command sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:4	RESERVED	Reserved for future use	0x0	No	No	R/W
		3:0	BUS_LD[3:0]	Program the drive strength of the SDATA driver in readback modes. 0x0: 10pF 0x1: 20pF 0x2: 30pF 0x3: 40pF 0x4: 50pF 0x5: 60pF 0x6: 80pF 0x7: 80pF 0x8-0xF: reserved	0x4			

MIPI RFFE specification

Table 17: Register mapping, table III

Register address	Register name	Data Bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x2D	EXT_TRIG_MASK	7	EXT_TRIGGER_MASK_10	0: Data masked (held in shadow REG)	1	No	No	R/W MW
				1: Data not masked (ready for transfer to active REG)				
		6	EXT_TRIGGER_MASK_9	0: Data masked (held in shadow REG)	1			
				1: Data not masked (ready for transfer to active REG)				
		5	EXT_TRIGGER_MASK_8	0: Data masked (held in shadow REG)	1			
				1: Data not masked (ready for transfer to active REG)				
		4	EXT_TRIGGER_MASK_7	0: Data masked (held in shadow REG)	1			
				1: Data not masked (ready for transfer to active REG)				
		3	EXT_TRIGGER_MASK_6	0: Data masked (held in shadow REG)	1			
				1: Data not masked (ready for transfer to active REG)				
		2	EXT_TRIGGER_MASK_5	0: Data masked (held in shadow REG)	1			
				1: Data not masked (ready for transfer to active REG)				
		1	EXT_TRIGGER_MASK_4	0: Data masked (held in shadow REG)	1			
				1: Data not masked (ready for transfer to active REG)				
		0	EXT_TRIGGER_MASK_3	0: Data masked (held in shadow REG)	1			
				1: Data not masked (ready for transfer to active REG)				
0x2E	EXT_TRIG	7	EXT_TRIGGER_10	0: No action (data held in shadow REG)	0	Yes	No	R/W MW
				1: Data transferred to active REG				
		6	EXT_TRIGGER_9	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		5	EXT_TRIGGER_8	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		4	EXT_TRIGGER_7	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		3	EXT_TRIGGER_6	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		2	EXT_TRIGGER_5	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		1	EXT_TRIGGER_4	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	EXT_TRIGGER_3	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				

MIPI RFFE specification

Table 18: Modes of operation (truth table)

Mode	SWITCH_CTRL_RF_A1 Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
RF_A1-RF_B1 ISO	x	x	x	x	x	x	x	0
RF_A1-RF_B1	x	x	x	x	x	x	x	1
RF_A1-RF_B2 ISO	x	x	x	x	x	x	0	x
RF_A1-RF_B2	x	x	x	x	x	x	1	x
RF_A1-RF_B3 ISO	x	x	x	x	x	0	x	x
RF_A1-RF_B3	x	x	x	x	x	1	x	x
RF_A1-RF_B4 ISO	x	x	x	x	0	x	x	x
RF_A1-RF_B4	x	x	x	x	1	x	x	x

Mode	SWITCH_CTRL_RF_A2 Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
RF_A2-RF_B1 ISO	x	x	x	x	x	x	x	0
RF_A2-RF_B1	x	x	x	x	x	x	x	1
RF_A2-RF_B2 ISO	x	x	x	x	x	x	0	x
RF_A2-RF_B2	x	x	x	x	x	x	1	x
RF_A2-RF_B3 ISO	x	x	x	x	x	0	x	x
RF_A2-RF_B3	x	x	x	x	x	1	x	x
RF_A2-RF_B4 ISO	x	x	x	x	0	x	x	x
RF_A2-RF_B4	x	x	x	x	1	x	x	x

Mode	SWITCH_CTRL_RF_A3 Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
RF_A3-RF_B1 ISO	x	x	x	x	x	x	x	0
RF_A3-RF_B1	x	x	x	x	x	x	x	1
RF_A3-RF_B2 ISO	x	x	x	x	x	x	0	x
RF_A3-RF_B2	x	x	x	x	x	x	1	x
RF_A3-RF_B3 ISO	x	x	x	x	x	0	x	x
RF_A3-RF_B3	x	x	x	x	x	1	x	x
RF_A3-RF_B4 ISO	x	x	x	x	0	x	x	x
RF_A3-RF_B4	x	x	x	x	1	x	x	x

Mode	SWITCH_CTRL_RF_A4 Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
RF_A4-RF_B1 ISO	x	x	x	x	x	x	x	0
RF_A4-RF_B1	x	x	x	x	x	x	x	1
RF_A4-RF_B2 ISO	x	x	x	x	x	x	0	x
RF_A4-RF_B2	x	x	x	x	x	x	1	x
RF_A4-RF_B3 ISO	x	x	x	x	x	0	x	x
RF_A4-RF_B3	x	x	x	x	x	1	x	x
RF_A4-RF_B4 ISO	x	x	x	x	0	x	x	x
RF_A4-RF_B4	x	x	x	x	1	x	x	x

BGSX44MU18 features a truth table shown in Tab. 18 which allows to connect multiple RF_Ax ports to any RF_Bx port by combining individual states. As an example, all RF_Ax ports can be connected to RF_B1 by combining states RF_A1-RF_B1, RF_A2-RF_B1, RF_A3-RF_B1, and RF_A4-RF_B1 by following register settings: SWITCH_CTRL_RF_A1 = 'xx000001', SWITCH_CTRL_RF_A2 = 'xx000001', SWITCH_CTRL_RF_A3 = 'xx000001', and SWITCH_CTRL_RF_A4 = 'xx000001'.

5 Application information

Pin configuration and function

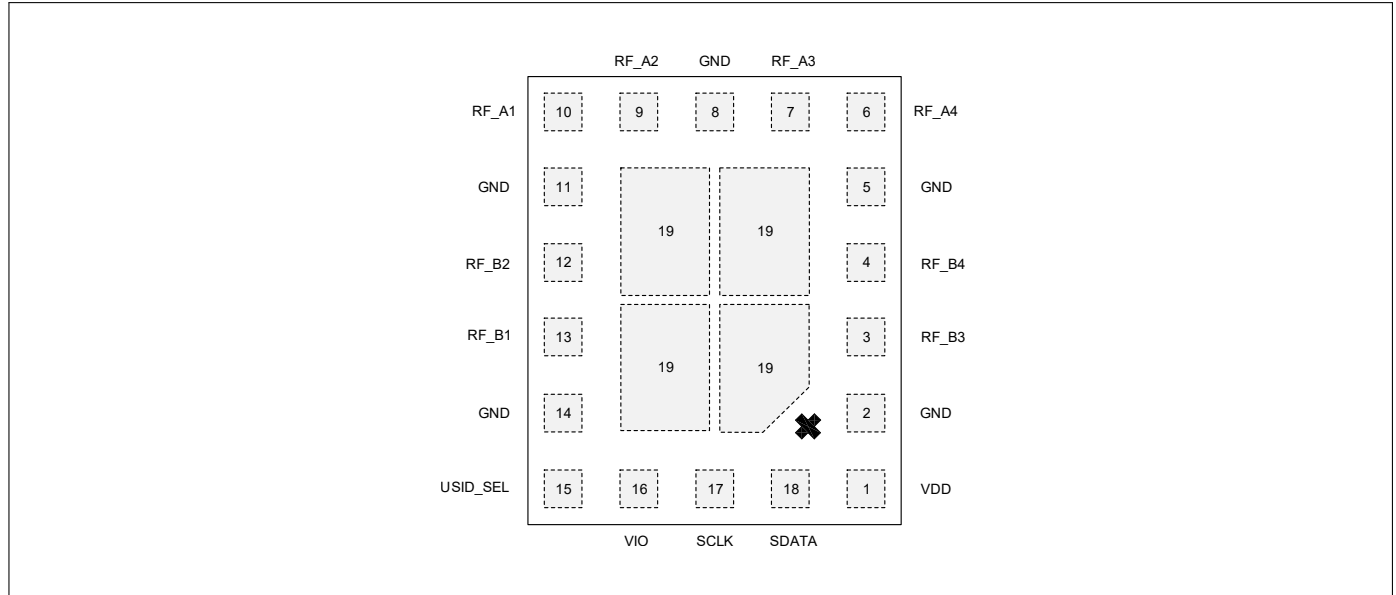


Figure 2: Footprint (top view)

Table 19: Pin definition and function

Pin No.	Name	Function
1	VDD	Power supply
2	GND	RF ground
3	RF_B3	RF antenna port 3
4	RF_B4	RF antenna port 4
5	GND	RF ground
6	RF_A4	RF TRX port 4
7	RF_A3	RF TRX port 3
8	GND	RF ground
9	RF_A2	RF TRX port 2
10	RF_A1	RF TRX port 1
11	GND	RF ground
12	RF_B2	RF antenna port 2
13	RF_B1	RF antenna port 1
14	GND	RF ground
15	USID_SEL	MIPI USID select port (to be connected to VIO or GND)
16	VIO	MIPI RFFE power supply
17	SCLK	MIPI RFFE clock
18	SDATA	MIPI RFFE data
19	GND	RF center ground

BGSX44MU18

4P4T antenna cross switch with MIPI RFFE control interface

Application information

Application board configuration

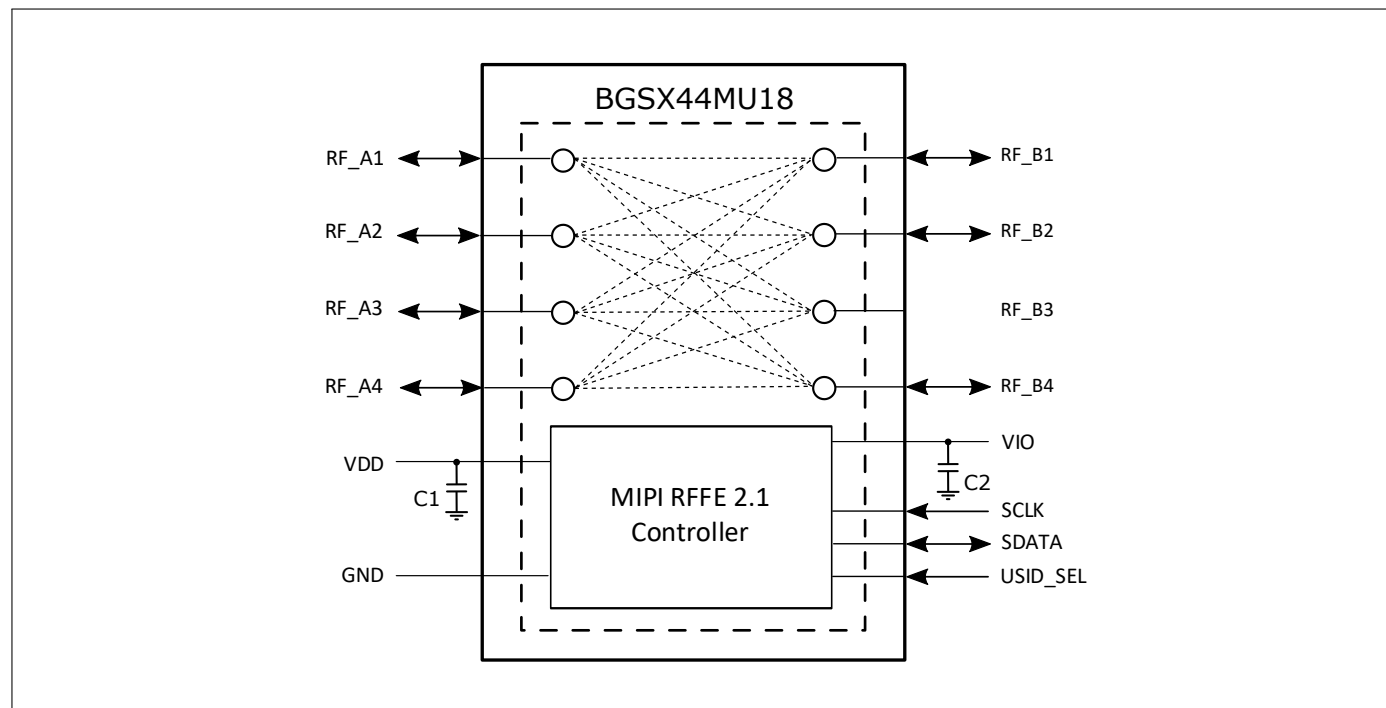


Figure 3: BGSX44MU18 application schematic

Table 20: Bill of materials table

Name	Value	Package	Manufacturer	Function
C1	10 nF	0201	Various	DC coupling
C2	10 nF	0201	Various	DC coupling

6 Package information

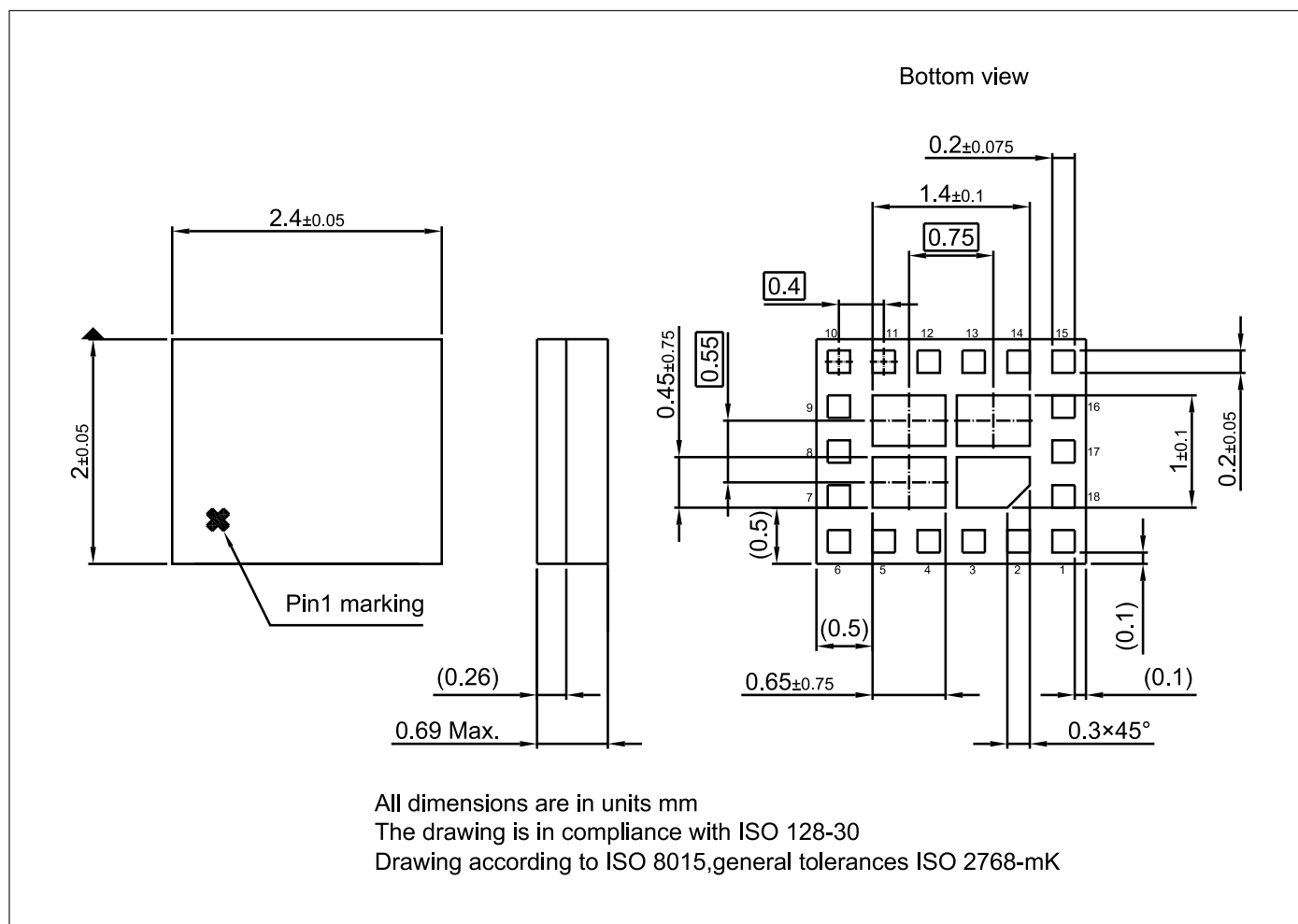


Figure 4: PG-WLGA-18-1 package outline (top, side and bottom views)

BGSX44MU18
4P4T antenna cross switch with MIPI RFFE control interface
Package information

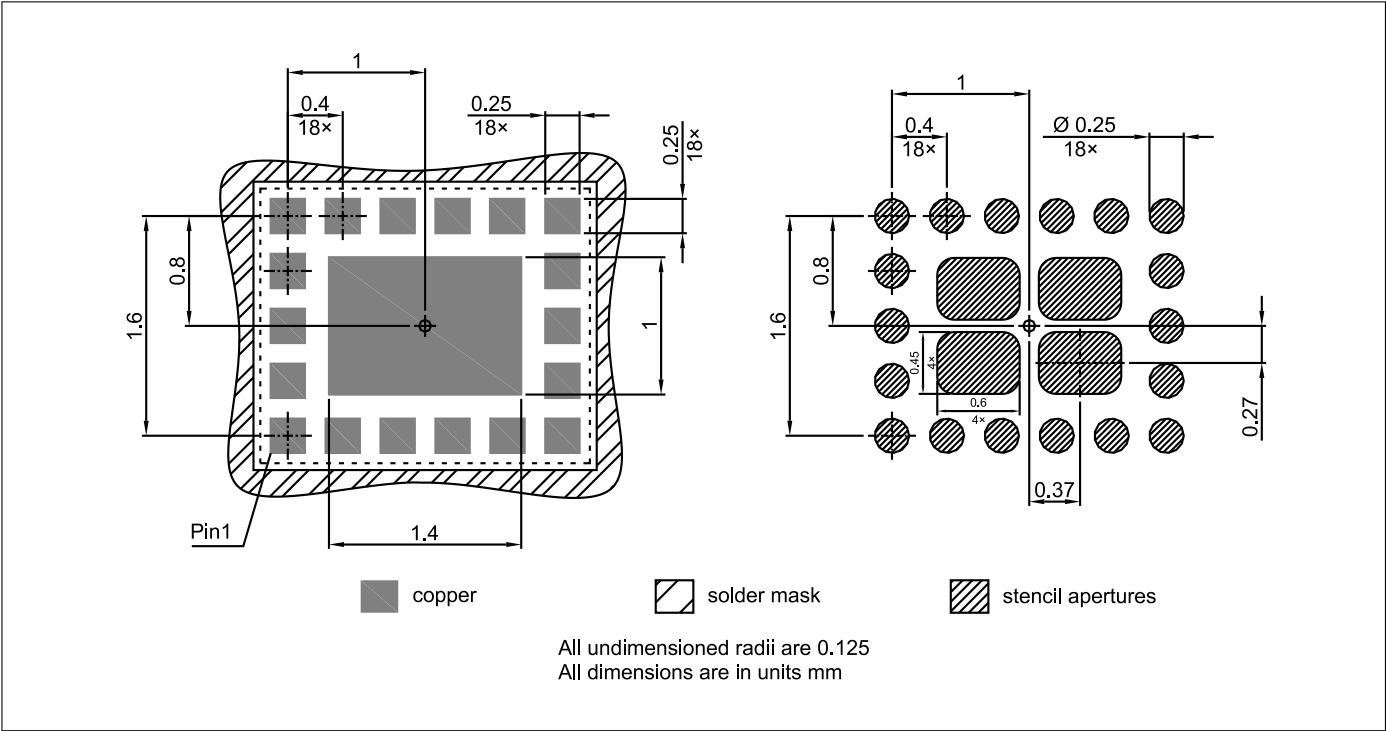


Figure 5: Footprint recommendation

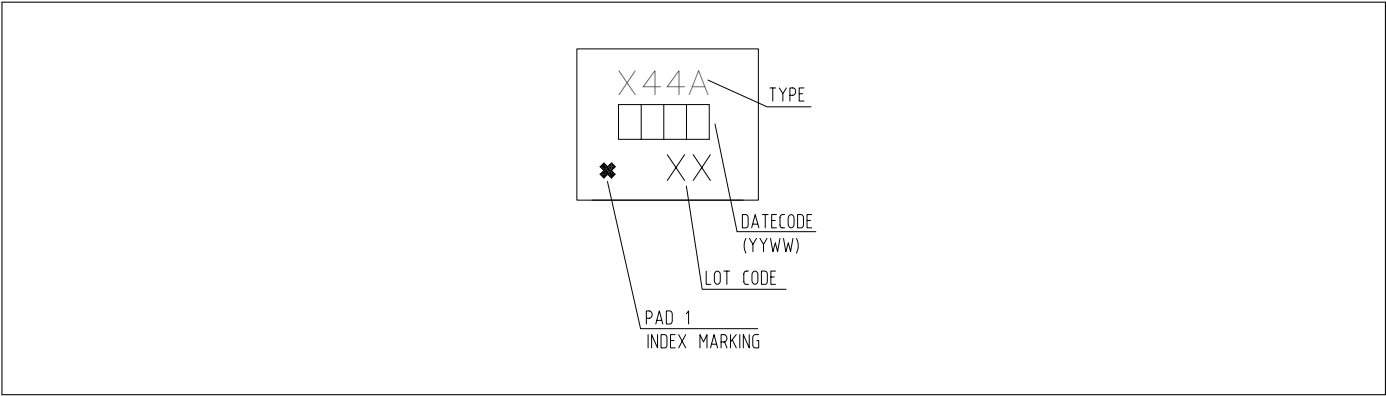


Figure 6: Marking specification (top view; first datecode digits YY indicate year of manufacture and second digits WW indicate calendar week of manufacture)

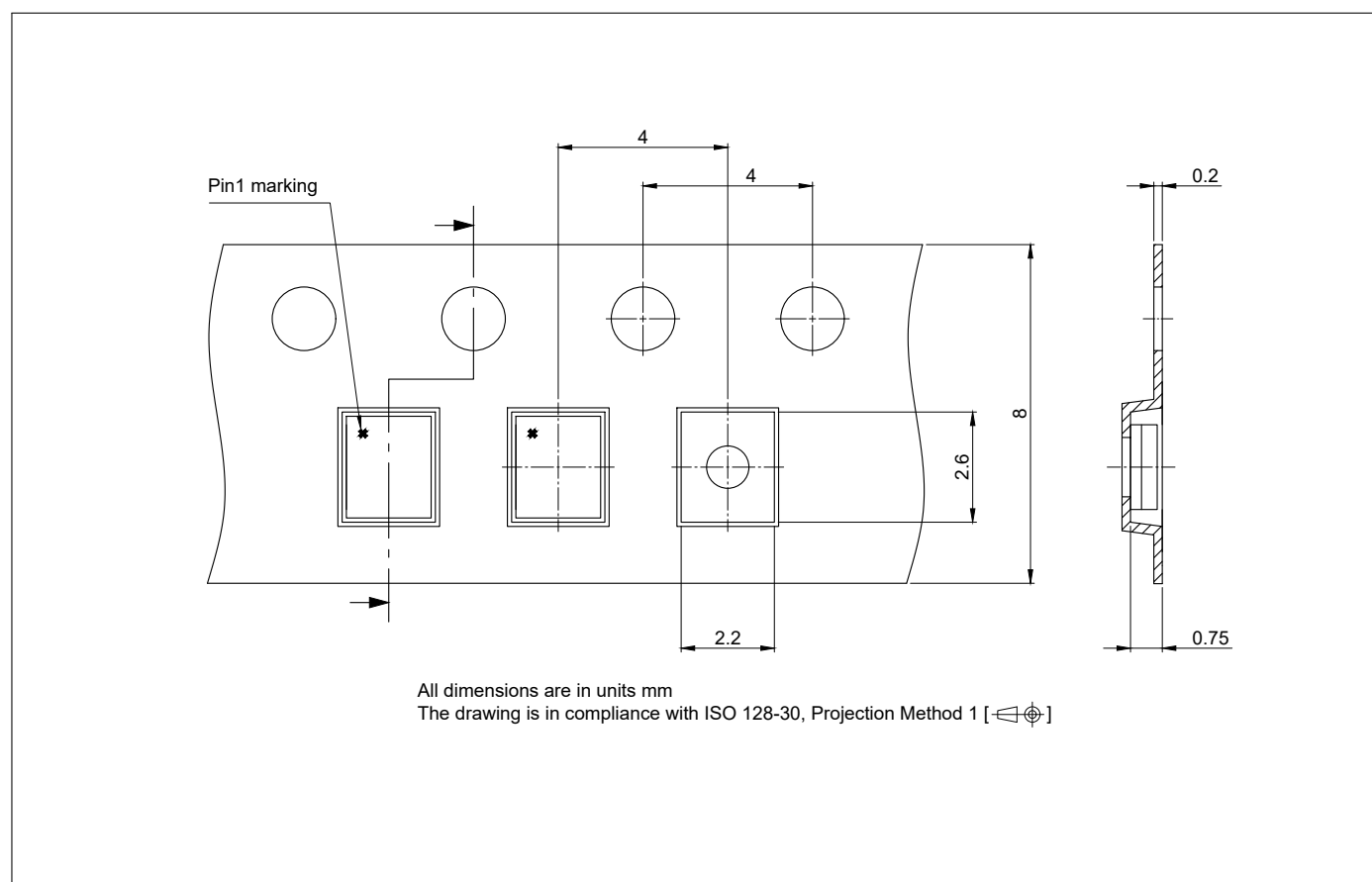


Figure 7: PG-WLGA-18-1 carrier tape drawing (top and side views)

Revision History

Revision v2.1 - 2021.09.14

Page or Item	Subjects (major changes since previous revision)
Revision 2.2, 2023-05-30	
5	RFFE supply current max values updated in table 4
19	Package outline drawing updated in figure 4, table 21 as redundant information removed

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