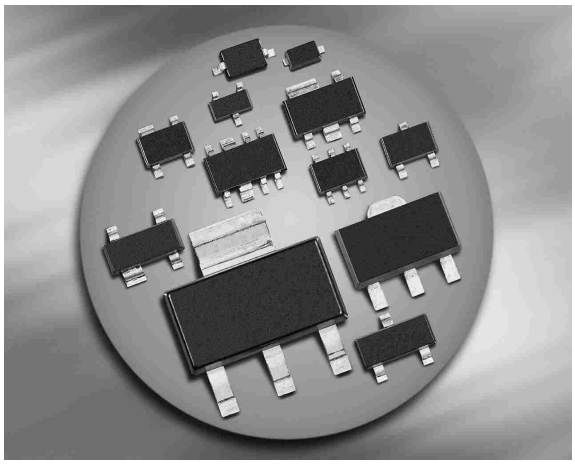
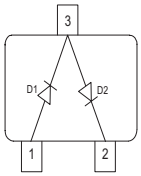
**Silicon PIN Diode Array**

- Surge protection device
- Designed for surge overvoltage clamping in antiparallel connection
- Pb-free (RoHS compliant) package

RoHS



**BAR66**




| Type | Package | Configuration | $L_S$(nH) | Marking |
|---|---|---|---|---|
| BAR66 | SOT23 | series | 1.8 | PMs |

**Maximum Ratings** at $T_A$ = 25°C, unless otherwise specified

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Diode reverse voltage | $V_R$ | 150 | V |
| Forward current | $I_F$ | 200 | mA |
| Total power dissipation<br>$T_s \leq 25$ °C | $P_{tot}$ | 250 | mW |
| ESD contact discharge[1)] | $V_{ESD}$ | 25 | kV |
| Peak pulse current ($t_p$ = 8 / 20 µs)[2)] | $I_{pp}$ | 12 | A |
| Junction temperature | $T_j$ | 150 | °C |
| Operating temperature range | $T_{op}$ | -55 ... 125 | |
| Storage temperature | $T_{stg}$ | -55 ... 150 | |

**Thermal Resistance**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction - soldering point[3)], BAR 66 | $R_{thJS}$ | ≤ 290 | K/W |

[1] $V_{ESD}$ according to IEC61000-4-2, only valid if pin 1 and pin 2 are connected

[2] $I_{pp}$ according to IEC61000-4-5, only valid if pin 1 and pin 2 are connected

[3] For calculation of $R_{thJA}$ please refer to Application Note Thermal Resistance

**Electrical Characteristics** at $T_A$ = 25°C, unless otherwise specified

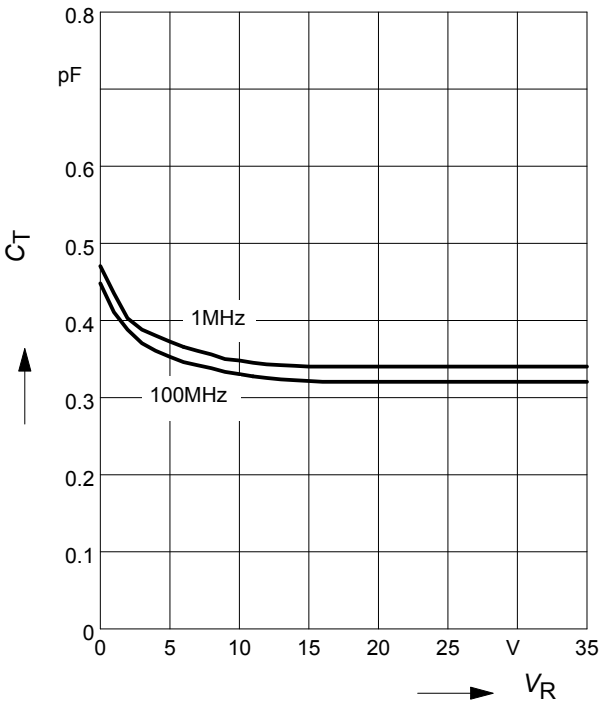
| Parameter | Symbol | Values | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| **DC Characteristics** | | | | | |
| Breakdown voltage<br>$I_{(BR)}$ = 5 µA | $V_{(BR)}$ | 150 | - | - | V |
| Reverse current<br>$V_R$ = 100 V | $I_R$ | - | - | 20 | nA |
| Forward voltage<br>$I_F$ = 50 mA | $V_F$ | - | 0.95 | 1.2 | V |
| Clamping voltage<br>$V_{ESD}$ = ± 15 kV (contact)[1)]<br>$I_{PP}$ = 12 A, $t_p$ = 8/20 µs[2)] | $V_{CL}$ | <br>-<br>- | <br>tbd<br>7 | <br>-<br>- | |
| **AC Characteristics** | | | | | |
| Diode capacitance<br>$V_R$ = 35 V, $f$ = 1 MHz<br>$V_R$ = 0 V, $f$ = 100 MHz | $C_T$ | <br>-<br>- | <br>0.4<br>0.35 | <br>0.6<br>0.9 | pF |
| Zero bias conductance<br>$V_R$ = 0 V, $f$ = 1 GHz | $g_P$ | - | 220 | - | µS |
| Forward resistance<br>$I_F$ = 5 mA, $f$ = 100 MHz | $r_f$ | - | 1.5 | 1.8 | Ω |
| Charge carrier life time<br>$I_F$ = 10 mA, $I_R$ = 6 mA, measured at $I_R$ = 3 mA,<br>$R_L$ = 100 Ω | $\tau_{rr}$ | - | 0.7 | - | µs |

[1] $V_{ESD}$ according to IEC61000-4-2, only valid if pin 1 and pin 2 are connected

[2] $I_{pp}$ according to IEC61000-4-5, only valid if pin 1 and pin 2 are connected

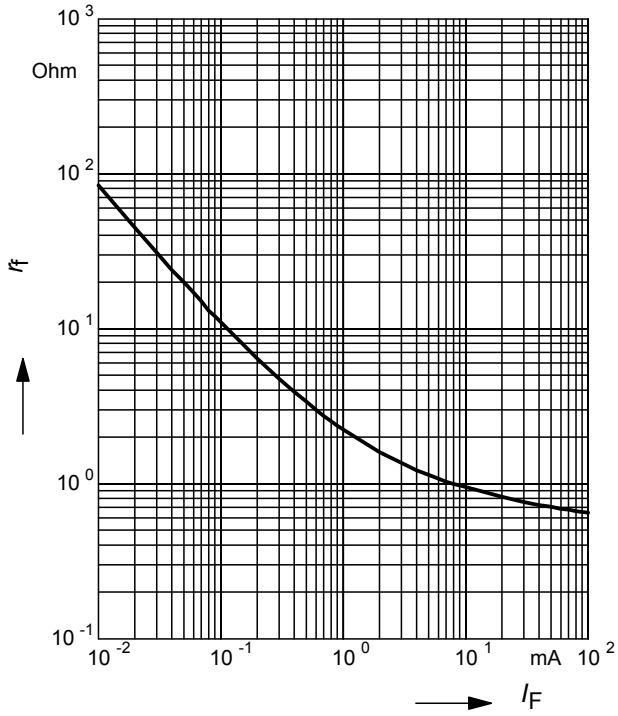
**Diode capacitance $C_T = f(V_R)$**

$f$ = Parameter



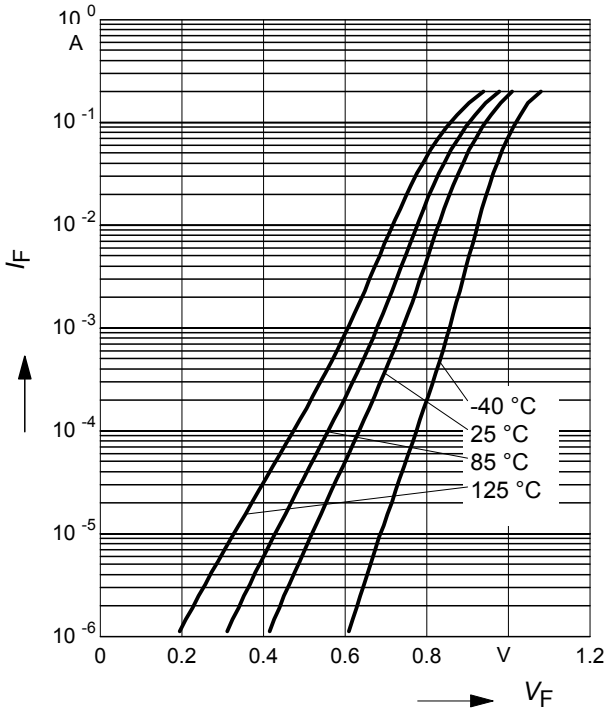

**Forward resistance $r_f = f(I_F)$**

$f$ = 100MHz



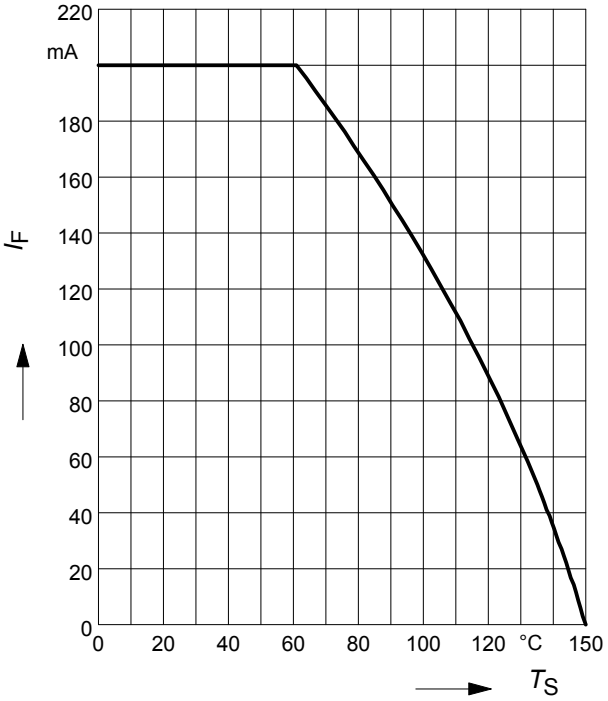

**Forward current $I_F = f(V_F)$**

$T_A$ = Parameter



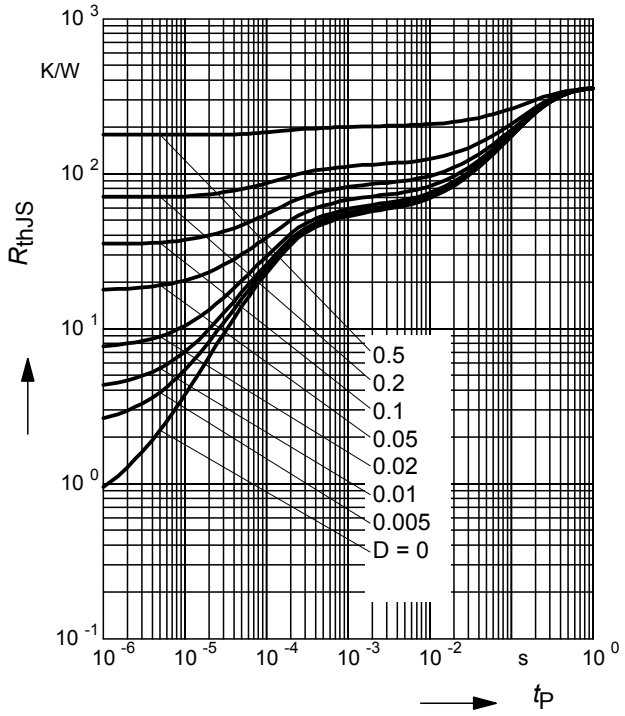

**Forward current $I_F = f(T_S)$**

BAR66



**Permissible Puls Load** $R_{thJS} = f(t_p)$

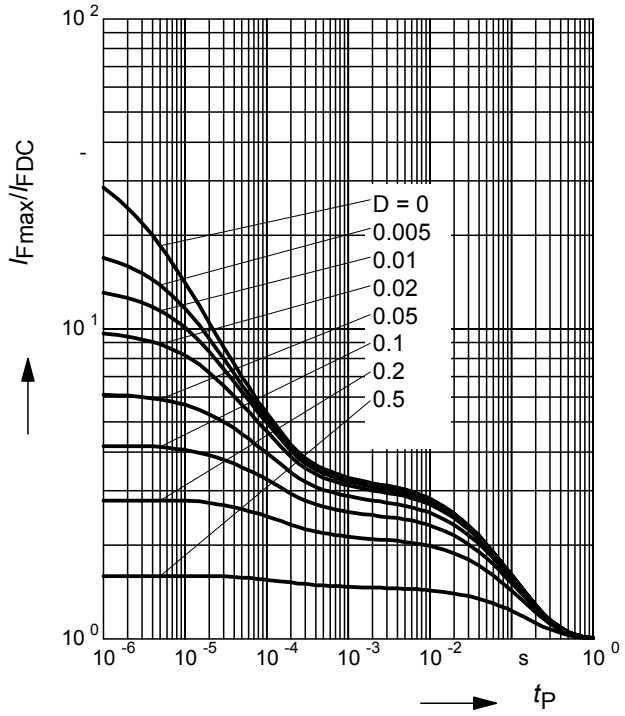
BAR66



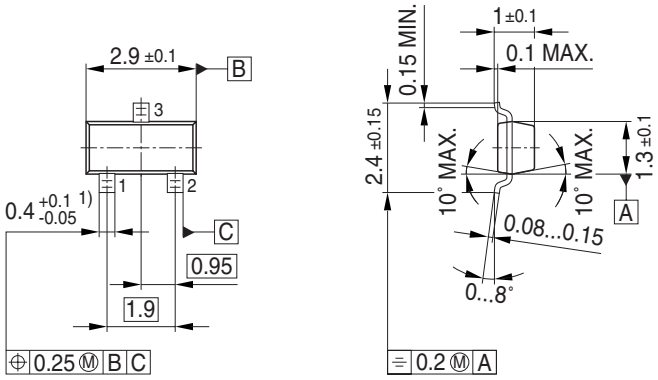

**Permissible Pulse Load**

$I_{Fmax}/I_{FDC} = f(t_p)$

BAR66

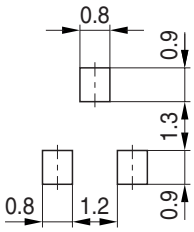


## Package Outline

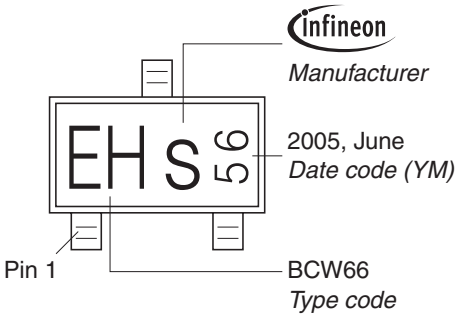



1) Lead width can be 0.6 max. in dambar area

## Foot Print

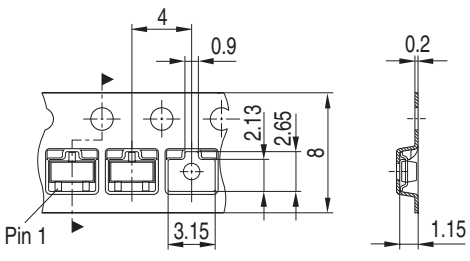



## Marking Layout (Example)




## Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



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