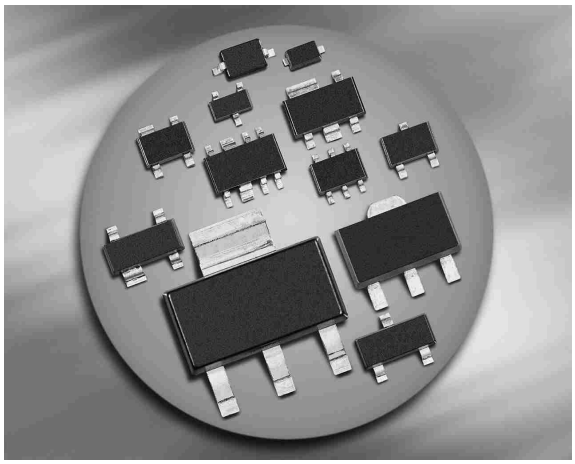
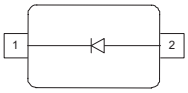
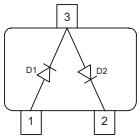
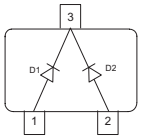
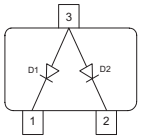
Silicon PIN Diodes

- PIN diode for high speed switching of RF signals
- Very low forward resistance (low insertion loss)
- Very low capacitance (high isolation)
- For frequencies up to 3GHz
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101[1)]



AEC Qualified RoHS

BAR63-02.. BAR63-03W	BAR63-04 BAR63-04W	BAR63-05 BAR63-05W	BAR63-06 BAR63-06W
			

Type	Package	Configuration	L_S(nH)	Marking
BAR63-02L*	TSLP-2-1	single, leadless	0.4	G
BAR63-02V	SC79	single	0.6	G
BAR63-02W	SCD80	single	0.6	GG
BAR63-03W	SOD323	single	1.8	white G
BAR63-04	SOT23	series	1.8	G4s
BAR63-04W	SOT323	series	1.4	G4s
BAR63-05	SOT23	common cathode	1.8	G5s
BAR63-05W	SOT323	common cathode	1.4	G5s
BAR63-06	SOT23	common anode	1.8	G6s
BAR63-06W	SOT323	common anode	1.4	G6s

[1]*BAR63-02L is not qualified according AEC Q101

Maximum Ratings at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	50	V
Forward current	I_F	100	mA
Total power dissipation	P_{tot}		mW
BAR63-02L, $T_S \leq 118°C$		250	
BAR63-02V, -02W, BAR63-03W, $T_S \leq 115°C$		250	
BAR63-04...BAR63-06, $T_S \leq 55°C$		250	
BAR63-04S, $T_S \leq 115°C$		250	
BAR63-04W...BAR63-06W, $T_S \leq 105°C$		250	
Junction temperature	T_j	150	°C
Operating temperature range	T_{op}	-55 ... 125	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point[1)]	R_{thJS}		K/W
BAR63-02L		≤ 125	
BAR63-02V, BAR63-02W		≤ 140	
BAR63-03W		≤ 155	
BAR63-04...BAR63-06		≤ 380	
BAR63-04S		≤ 180	
BAR63-04W...BAR63-06W		≤ 180	

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Breakdown voltage $I_{(BR)}$ = 5 µA	$V_{(BR)}$	50	-	-	V
Reverse current V_R = 35 V	I_R	-	-	10	nA
Forward voltage I_F = 100 mA	V_F	-	0.95	1.2	V

[1]For calculation of R_{thJA} please refer to the Technical Information

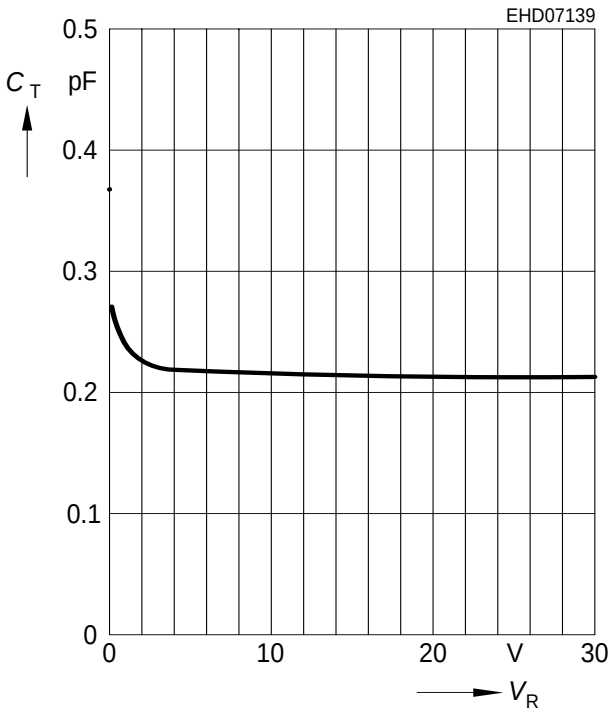
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics					
Diode capacitance	C_T				pF
V_R = 5 V, f = 1 MHz		-	0.21	0.3	
V_R = 0 V, 100 MHz ... 1.8 GHz		-	0.3	-	
Reverse parallel resistance	R_P				kΩ
V_R = 0 V, f = 100 MHz		-	500	-	
V_R = 0 V, f = 1 GHz		-	15	-	
V_R = 0 V, f = 1.8 GHz		-	5	-	
Forward resistance	r_f				Ω
I_F = 5 mA, f = 100 MHz		-	1.2	2	
I_F = 10 mA, f = 100 MHz		-	1	-	
Charge carrier life time I_F = 10 mA, I_R = 6 mA, measured at I_R = 3 mA, R_L = 100 Ω	τ_{rr}	-	75	-	ns
I-region width	W_I	-	4.5	-	µm
Insertion loss[1]	I_L				dB
I_F = 1 mA, f = 1.8 GHz		-	0.15	-	
I_F = 5 mA, f = 1.8 GHz		-	0.11	-	
I_F = 10 mA, f = 1.8 GHz		-	0.1	-	
Isolation[1]	I_{SO}				
V_R = 0 V, f = 0.9 GHz		-	17.9	-	
V_R = 0 V, f = 1.8 GHz		-	12.3	-	
V_R = 0 V, f = 2.45 GHz		-	10	-	
Series inductance	L_S	-	-	-	

[1]BAR63-02L in series configuration, Z = 50Ω

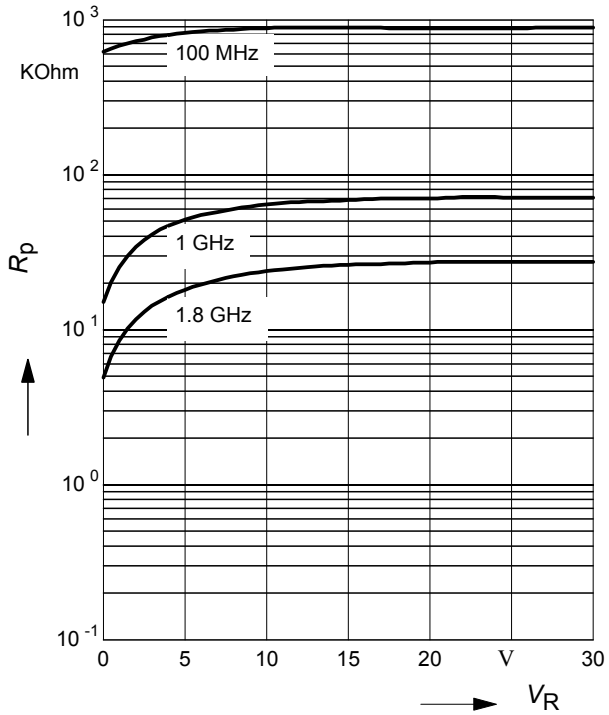
Diode capacitance $C_T = f(V_R)$

f = 1MHz - 1.8GHz



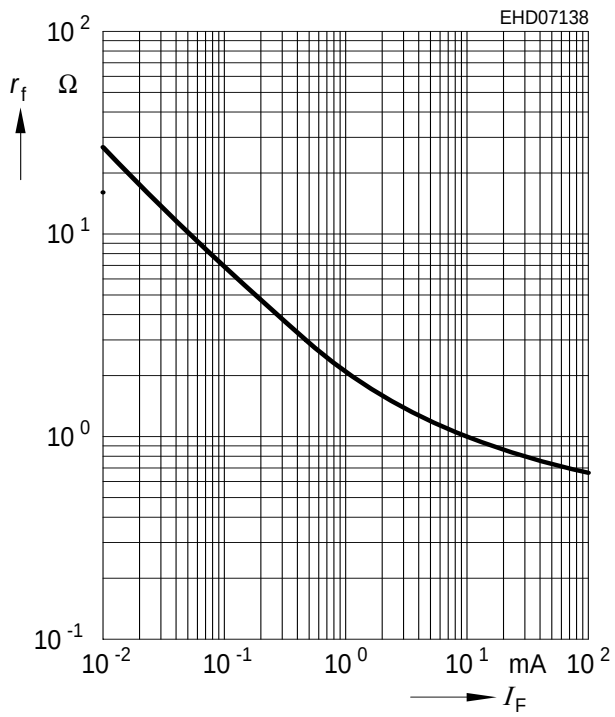
Reverse parallel resistance $R_P = f(V_R)$

f = Parameter



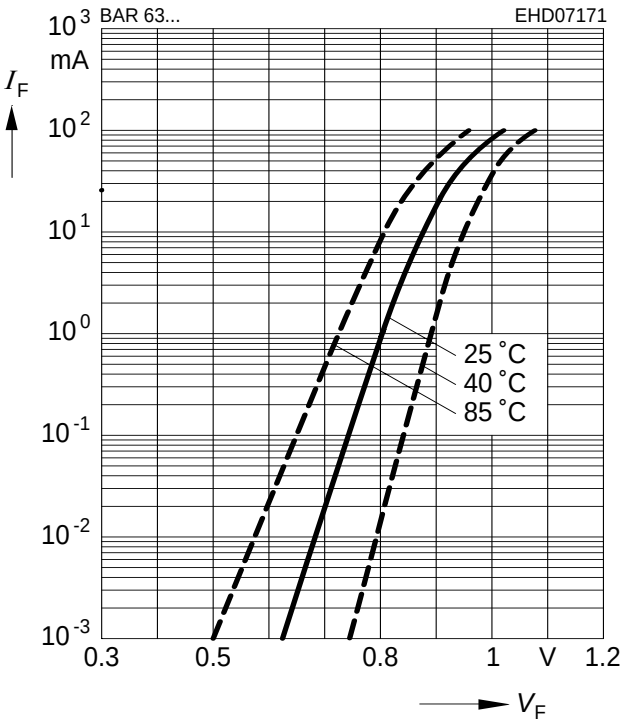
Forward resistance $r_f = f(I_F)$

f = 100MHz

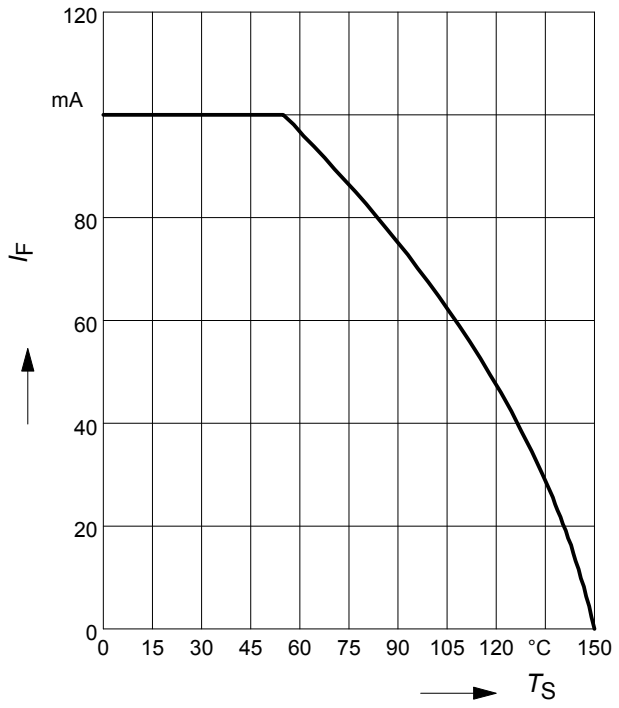


Forward current $I_F = f(V_F)$

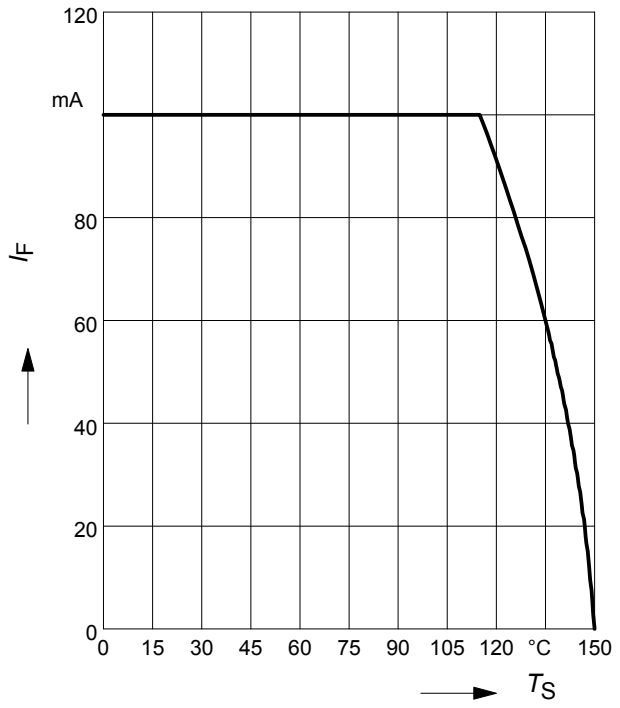
T_A = Parameter



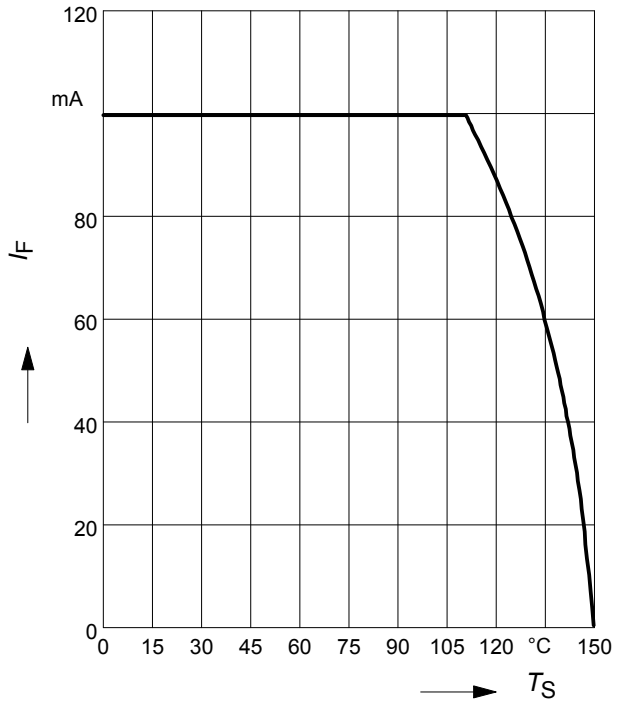
Forward current $I_F = f(T_S)$
BAR63-04...BAR63-06



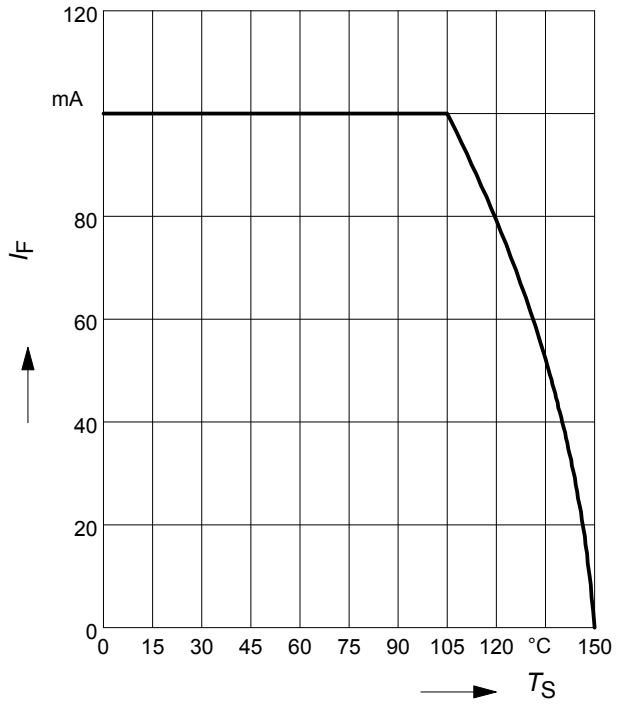
Forward current $I_F = f(T_S)$
BAR63-02V, BAR63-02W



Forward current $I_F = f(T_S)$
BAR63-03W

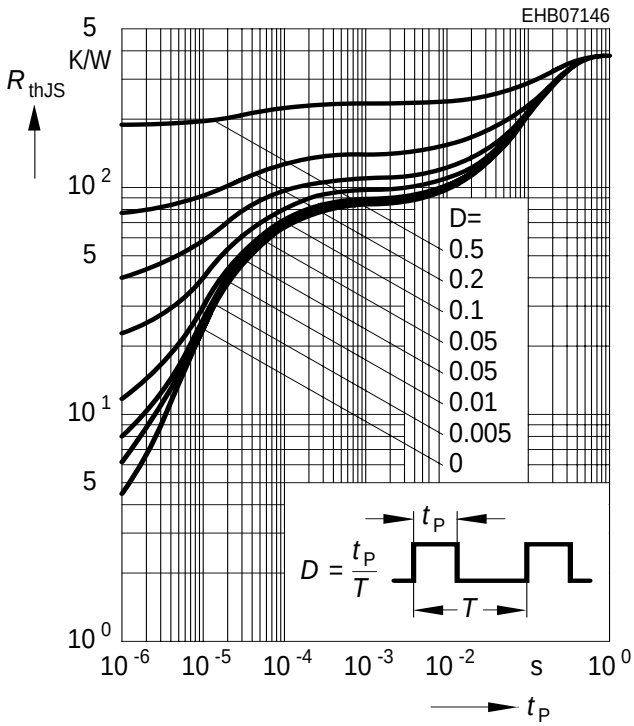


Forward current $I_F = f(T_S)$
BAR63-04W...BAR63-06W



Permissible Puls Load $R_{thJS} = f(t_p)$

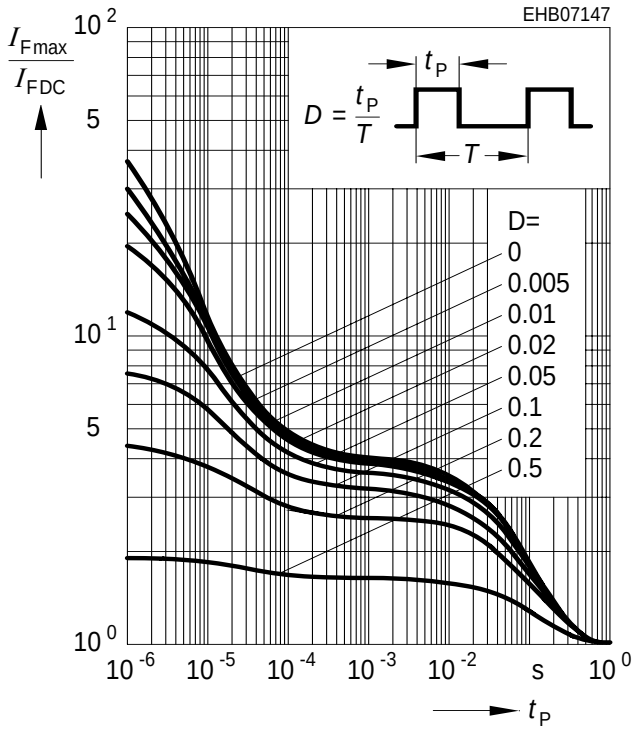
BAR63-04...BAR63-06



Permissible Pulse Load

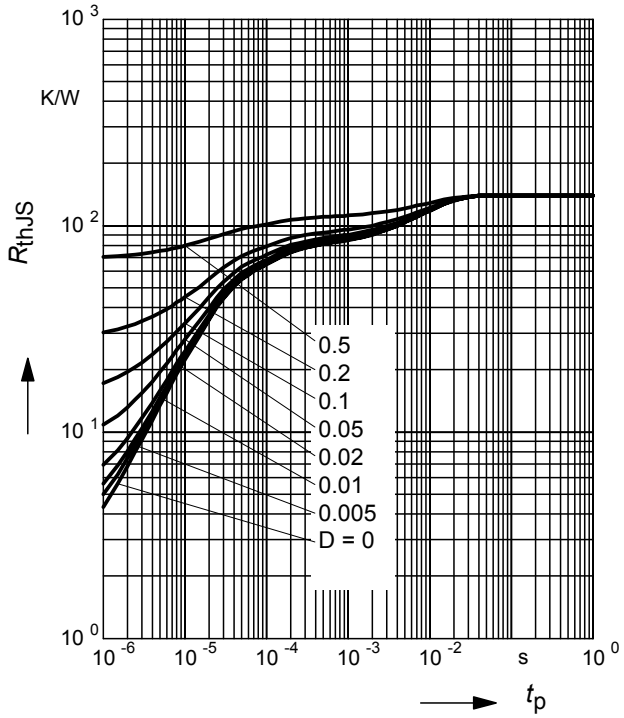
$I_{Fmax}/I_{FDC} = f(t_p)$

BAR63-04...BAR63-06



Permissible Puls Load $R_{thJS} = f(t_p)$

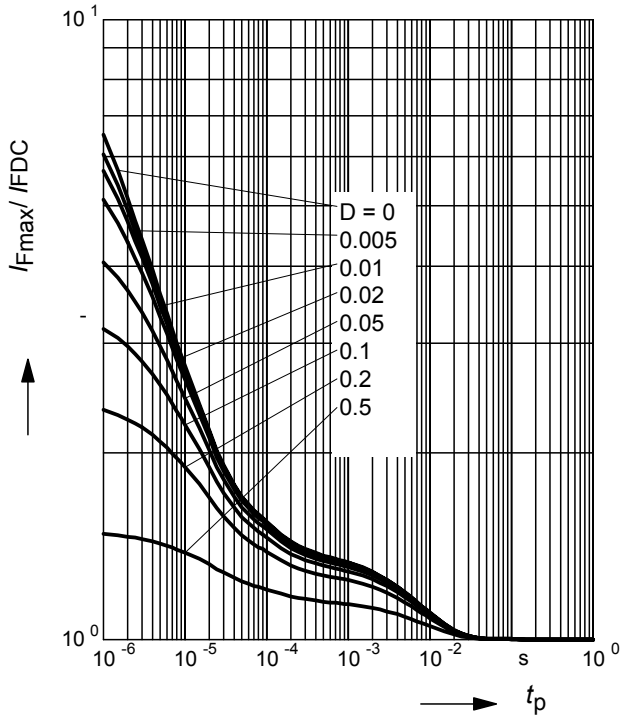
BAR63-02V, BAR63-02W



Permissible Pulse Load

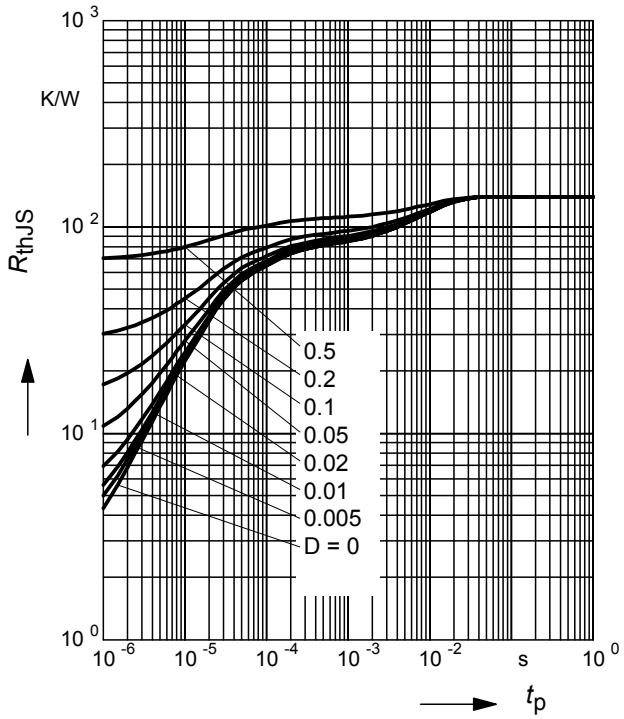
$I_{Fmax}/I_{FDC} = f(t_p)$

BAR63-02V, BAR63-02W



Permissible Puls Load $R_{thJS} = f(t_p)$

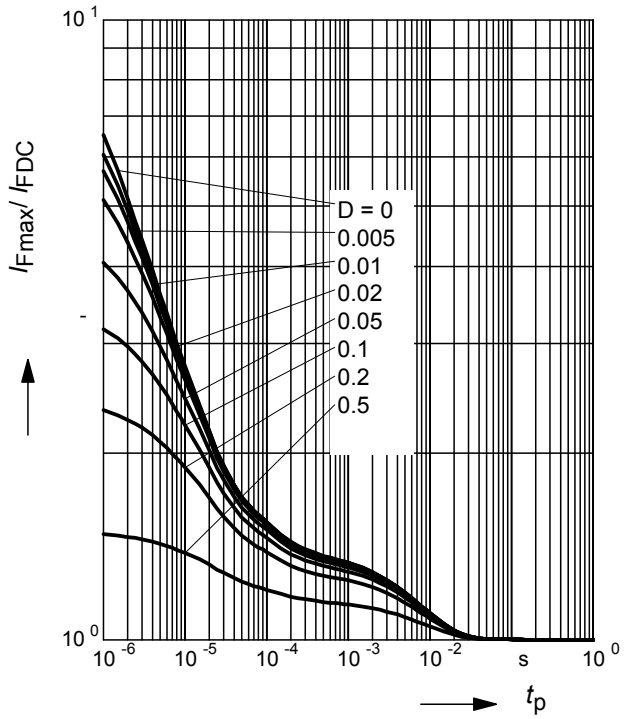
BAR63-03W



Permissible Pulse Load

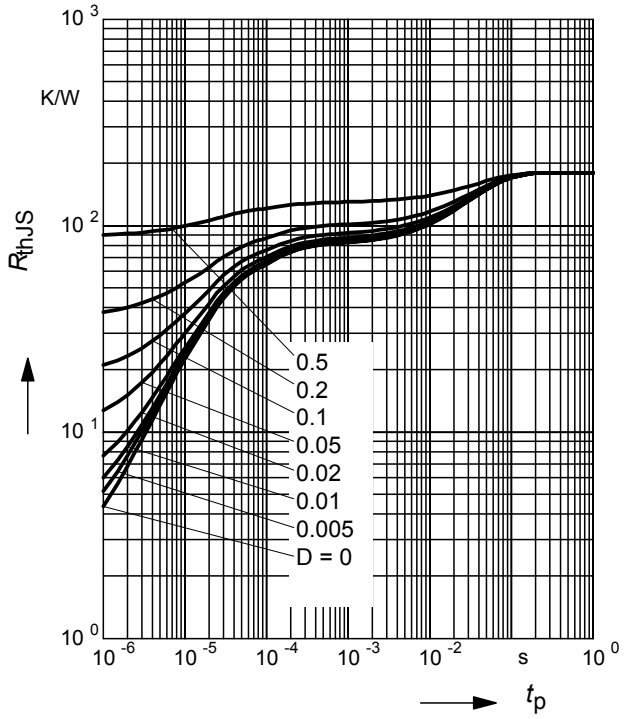
$I_{Fmax}/I_{FDC} = f(t_p)$

BAR63-03W



Permissible Puls Load $R_{thJS} = f(t_p)$

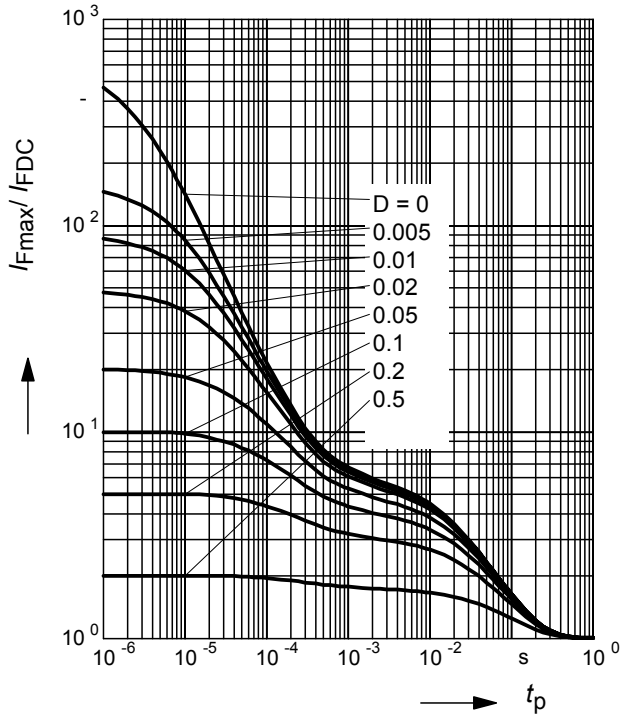
BAR63-04W...BAR63-06W



Permissible Pulse Load

$I_{Fmax}/I_{FDC} = f(t_p)$

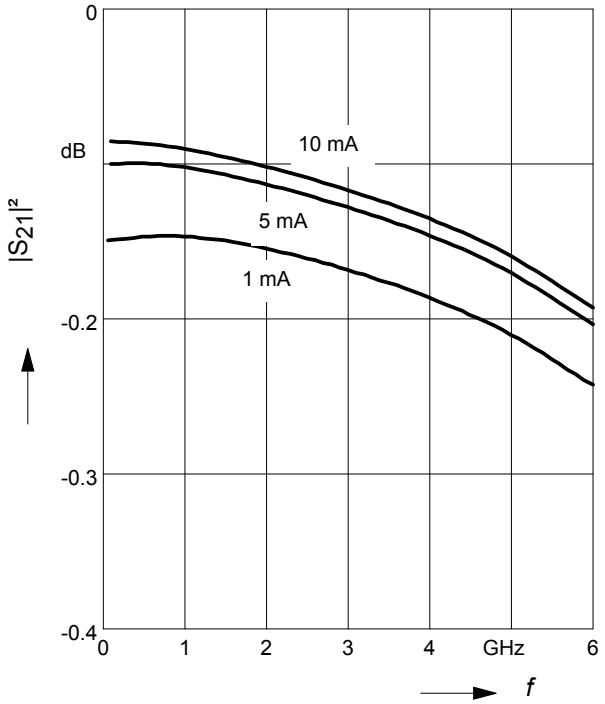
BAR63-04W...BAR63-06W



Insertion loss $I_L = -|S_{21}|^2 = f(f)$

I_F = Parameter

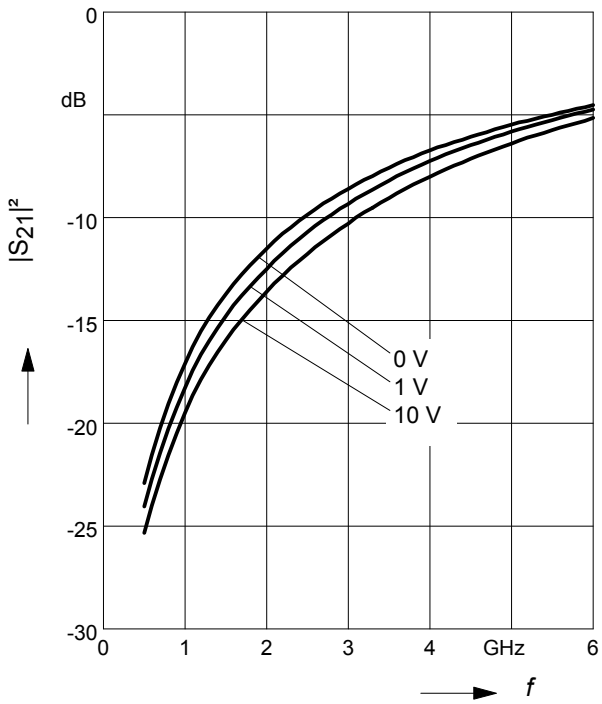
BAR63-02L in series configuration, $Z = 50\Omega$



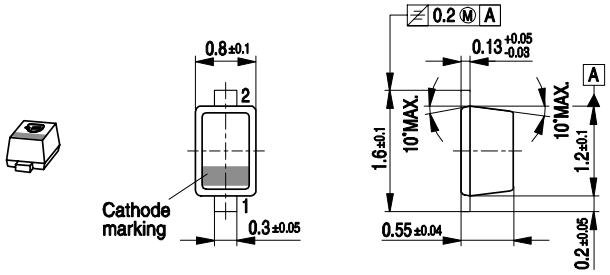
Isolation $I_{SO} = -|S_{21}|^2 = f(f)$

V_R = Paramter

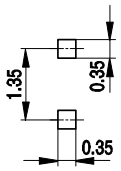
BAR63-02L in series configuration, $Z = 50\Omega$



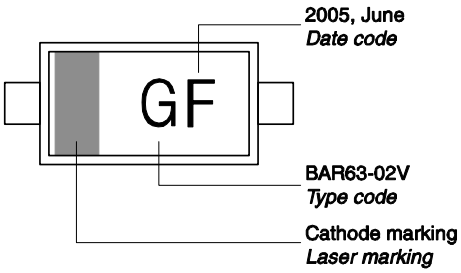
Package Outline



Foot Print

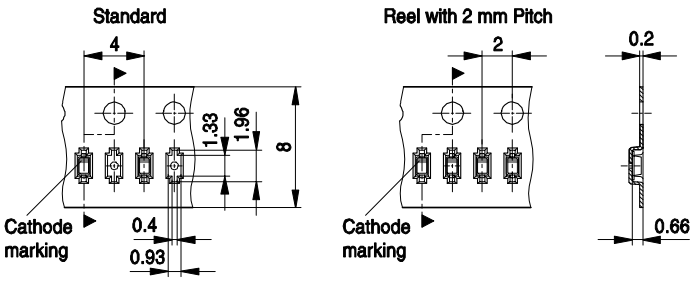


Marking Layout (Example)

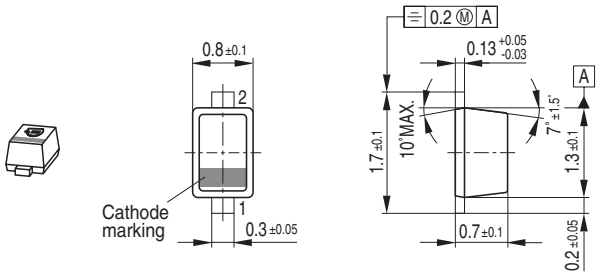


Standard Packing

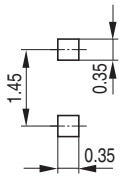
Reel ø180 mm = 3.000 Pieces/Reel
Reel ø180 mm = 8.000 Pieces/Reel (2 mm Pitch)
Reel ø330 mm = 10.000 Pieces/Reel



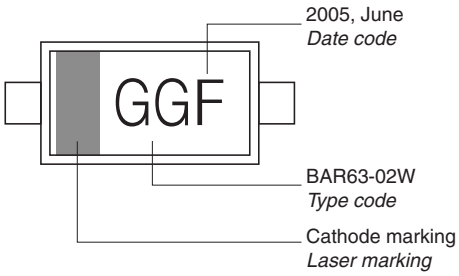
Package Outline



Foot Print



Marking Layout (Example)



Standard Packing

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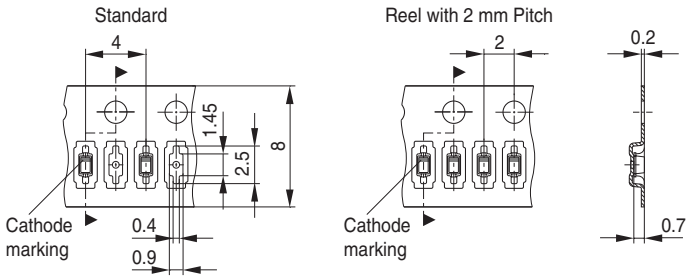
Reel ø330 mm = 10.000 Pieces/Reel

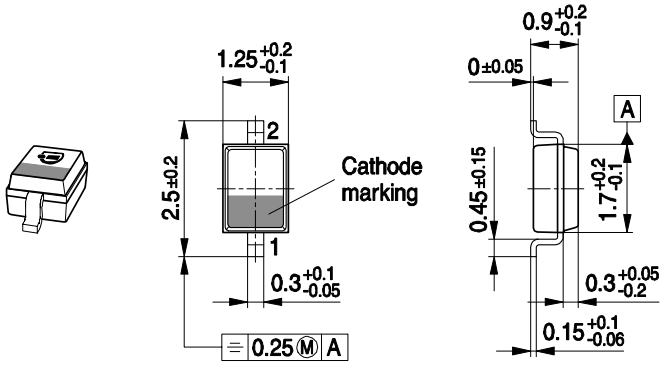


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75[1]) CES-Code

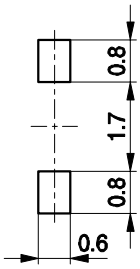
Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

1) New Marking Layout for SC75, implemented at October 2005.

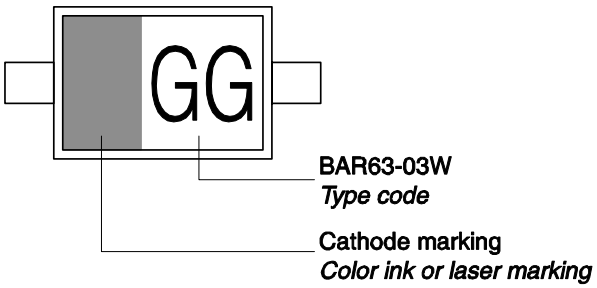
Package Outline



Foot Print

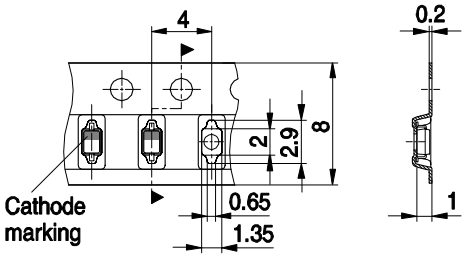


Marking Layout (Example)

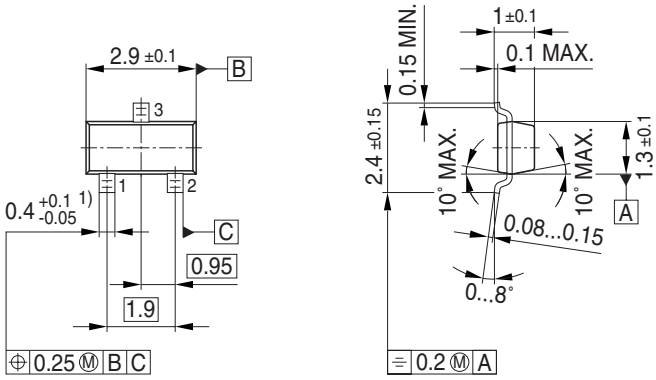


Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel

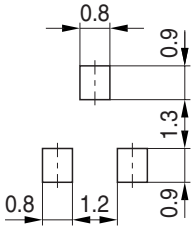


Package Outline

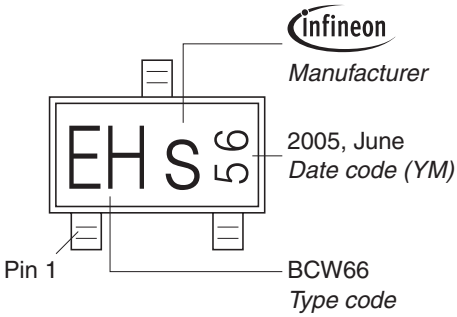


1) Lead width can be 0.6 max. in dambar area

Foot Print

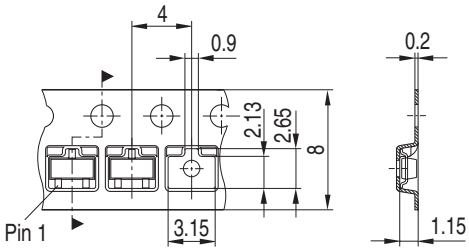


Marking Layout (Example)

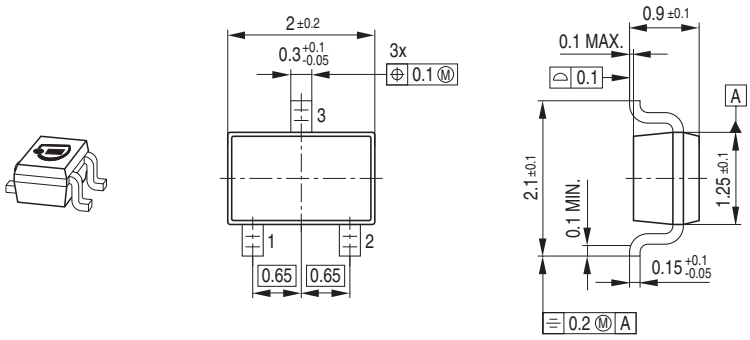


Standard Packing

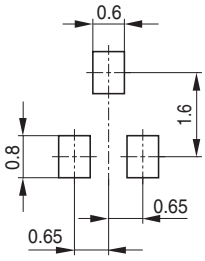
Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



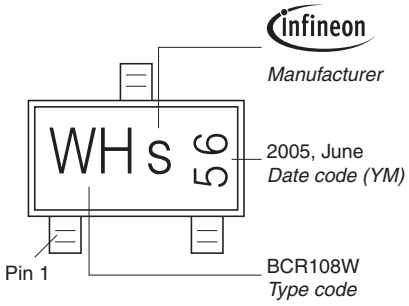
Package Outline



Foot Print

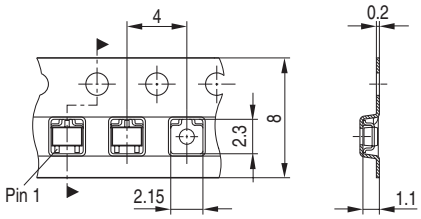


Marking Layout (Example)

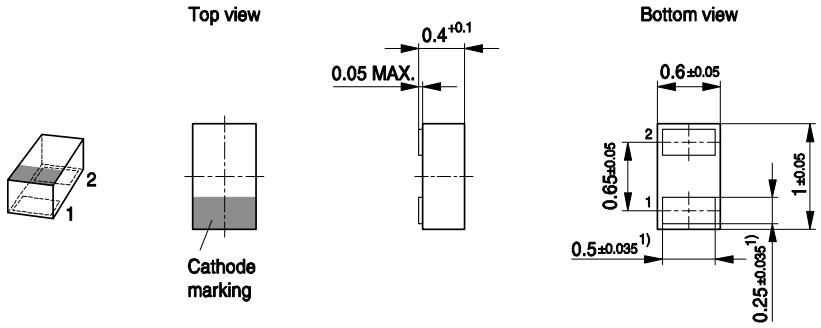


Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



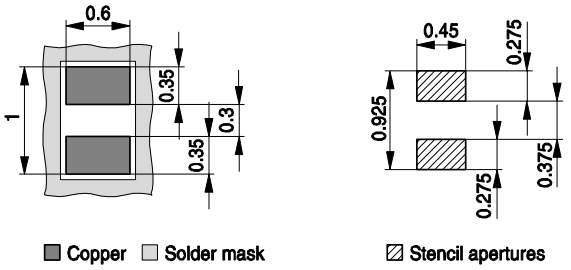
Package Outline



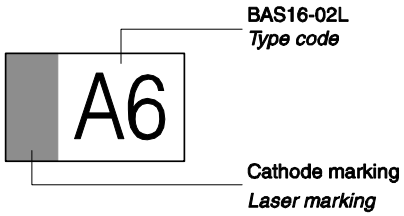
1) Dimension applies to plated terminal

Foot Print

For board assembly information please refer to Infineon website "Packages"

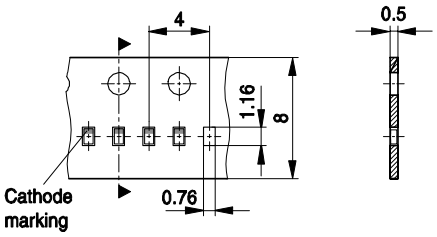


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel
Reel ø330 mm = 50.000 Pieces/Reel (optional)



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