# Low-side MOSFET driver with fast over-current protection (negative current sense) and fault/enable

## 1ED44173N01B Technical description

## About this document

### Scope and purpose

This application note describes the features and key advantages of using Infineon's 1ED44173N01B gate driver. This document will help the designer use the device within the recommended operating range by explaining how to select the current-sensing shunt resistor ($R_{CS}$), resistor and capacitor (RC) filter for overcurrent protection (OCP) and short-circuit protection (SCP), resistor and capacitor for fault clear time, and how to design the interfacing circuitry with the controller. A simple adapter board to evaluate 1ED44173N01B and the test result of the adapter board for one PFC demo board are also included. This application note provides detailed information to help speed up design time and avoid circuit problems that can occur due to incorrect usage of the driver.

### Intended audience

This document is intended for people and designers who are looking to reduce their system cost and space while increasing the power density of their design with 1ED44173N01B.

### Ordering information

| Base Part Number | Package | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| EVAL-1ED44173N01B | EVAL | Boxed | 1 | EVAL1ED44173N01BTOBO1 |
| 1ED44173N01B | PG-SOT23-6 | Tape and Reel | 3000 | 1ED4473N01BXTSA1 |
| IPW65R045C7 | PG-TO 247-3 | Tube | 240 | IPW65R045C7FKSA1 |

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# 1 Product overview

## 1.1 Internal block diagram and features

Figure 1 illustrates the internal block diagram of the 1ED44173N01B.

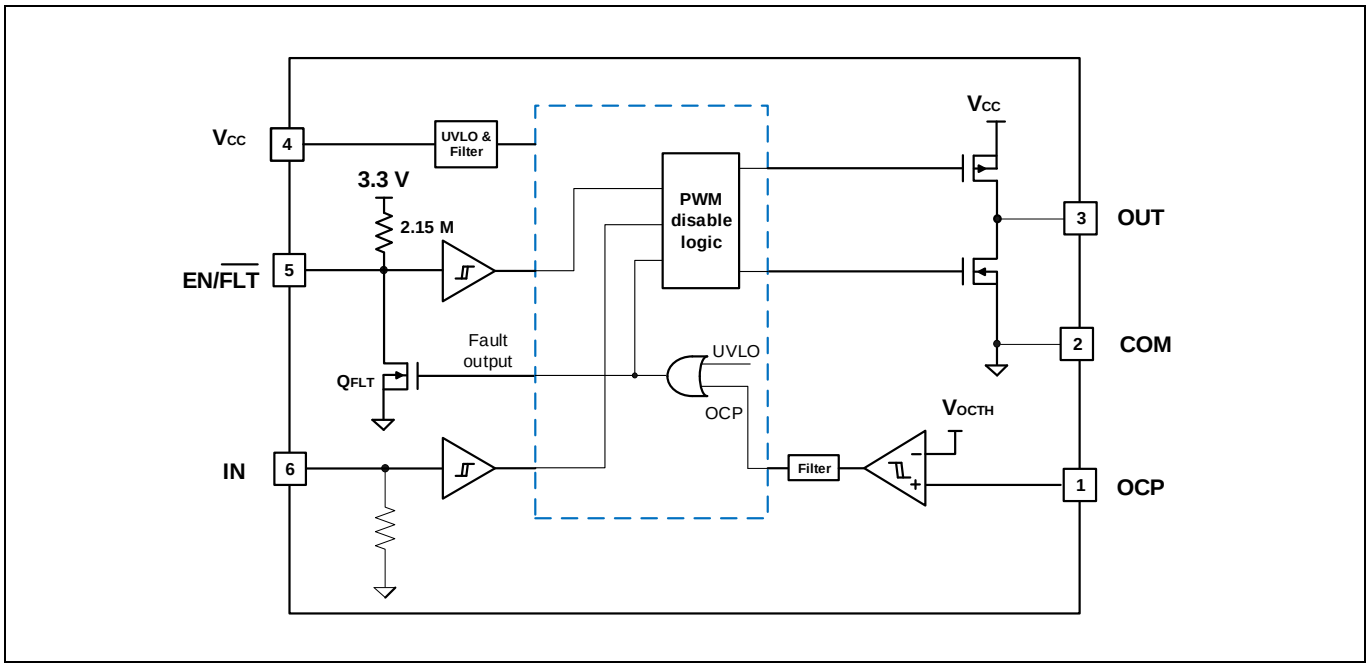



**Figure 1 Internal block diagram**

## 1.2 The detailed features and integrated functions of 1ED44173N01B

### 1.2.1 Features

- Overcurrent detection with negative voltage input
- -246 mV overcurrent threshold with accurate ±5% tolerance
- Single pin enable control and fault output indications
- Programmable fault clear time
- Undervoltage lockout for MOSFETs
- CMOS Schmitt-triggered inputs
- 3.3 V, 5 V and 15 V input logic-compatible
- 25 V $V_{CC}$ voltage supply support (max)
- Output in phase with input
- 3 kV ESD HBM

### 1.2.2 Functions

- Overcurrent shutdown
- UVLO
- Fault output and Enable
- The OUT keeps “low” during protection time
- Active-high input signal logic

## 1.3 Maximum electrical ratings

**Table 1 Detailed description of absolute maximum ratings**

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Fixed supply voltage | | – 0.3 | 25 | V |
| $V_O$ | Output voltage (OUT) | | – 0.3 | $V_{CC}$ + 0.3 | |
| $V_{OCP}$ | Voltage at current sense pin (OCP) | | – 10 | $V_{CC}$ +0.3 | |
| $V_{EN/\overline{FLT}}$ | Voltage at enable and fault reporting pin ($EN/\overline{FLT}$) | | – 0.3 | $V_{CC}$ + 0.3 | |
| $V_{IN}$ | Logic input voltage ( IN ) | | – 10 | $V_{CC}$ + 0.3 | |
| $P_D$ | Package power dissipation @ $T_A \leq 25°C$ | PG-SOT-23-6 | — | 0.5 | W |
| $R_{thJA}$ | Thermal resistance, junction to ambient | | — | 250 | °C/W |
| $T_J$ | Junction temperature | | – 40 | 150 | °C |
| $T_S$ | Storage temperature | | – 55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 260 | |

Table 1: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board-mounted and still-air conditions.

## 1.4 Description of the input and output pins

Table 2 defines the 1ED44173N01B input and output pins. The detailed functional descriptions are as follows:

**Table 2 Pin descriptions of 1ED44173N01B**

| Pin number | Pin name | Pin description |
|---|---|---|
| 1 | OCP | Current sense input |
| 2 | COM | Ground |
| 3 | OUT | Gate drive output |
| 4 | $V_{CC}$ | Supply voltage |
| 5 | $EN/\overline{FLT}$ | Enable, fault reporting and fault clear time program pin, three functions:<br>1. Logic input to enable I/O functionality. I/O logic functions when enable is high.<br>2. Fault reporting function like overcurrent or undervoltage lockout, this pin has negative logic and an open-drain output.<br>3. Fault clear time program with external resistor and capacitor. |
| 6 | IN | Logic input for gate driver output (OUT), in phase |

### Overcurrent detection pin

Pin 1: OCP

- The $R_{CS}$ should be connected between the pin of system ground and the input power return to detect short-circuit current (refer to Figure 5). An RC filter needs to be connected between the shunt resistor and the OCP pin if the internal blanking time is not sufficient to eliminate the noise.
- The integrated comparator is triggered if the voltage of the OCP pin ($V_{OCP}$) is less than -246 mV. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at pin $\mathrm{EN}/\overline{\mathrm{FLT}}$ is pulled down to low.
- The connection length between the $R_{CS}$ and OCP pin should be minimized.

### Common supply ground pin

Pin 2: COM

- This pin connects the control ground for the internal circuit of the driver.

### Gate drive output pin

Pin 3: OUT

- The pin is connected to the gate of the MOSFET by the gate resistor to turn the power device on or off.
- To prevent oscillations, a gate resistor is needed to be in series with the pin and the gate of MOSFET.

### Bias voltage pin

Pin 4: $V_{CC}$

- This is the control supply pin for the internal IC.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality filter capacitor with low equivalent series resistance (ESR) and low equivalent series inductance (ESL) should be mounted very close to this pin and COM pin.

### Fault output and enable pin

Pin 5: $\mathrm{EN}/\overline{\mathrm{FLT}}$

- This is a multifunctional pin. One function is the fault output. An active low output is given on this pin for a fault state condition in the 1ED44173N01B. The fault conditions are overcurrent detection and $V_{CC}$ undervoltage operation. The $\mathrm{EN}/\overline{\mathrm{FLT}}$ output is open-drain configured. The $\mathrm{EN}/\overline{\mathrm{FLT}}$ signal line should be pulled up to the logic power supply (5 V or 3.3 V) with proper resistance.
- The second function is enabled. Externally pulling down the pin can disable the output. For normal operation, the pin needs to be pulled up.
- The third function is fault clear time program with external resistor and capacitor.

### Signal input pin

Pin 6: IN

- This is the pin to control the operation of the external device.
- It is activated by voltage input signals. The terminal is internally connected to a Schmitt-trigger circuit.
- The signal logic of the pin is active-high. The device associated with the pin will be turned on when a sufficient logic voltage is applied to the pin.
- The wiring of the input should be as short as possible to protect the 1ED44173N01B against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 3.

## 1.5 Outline drawings

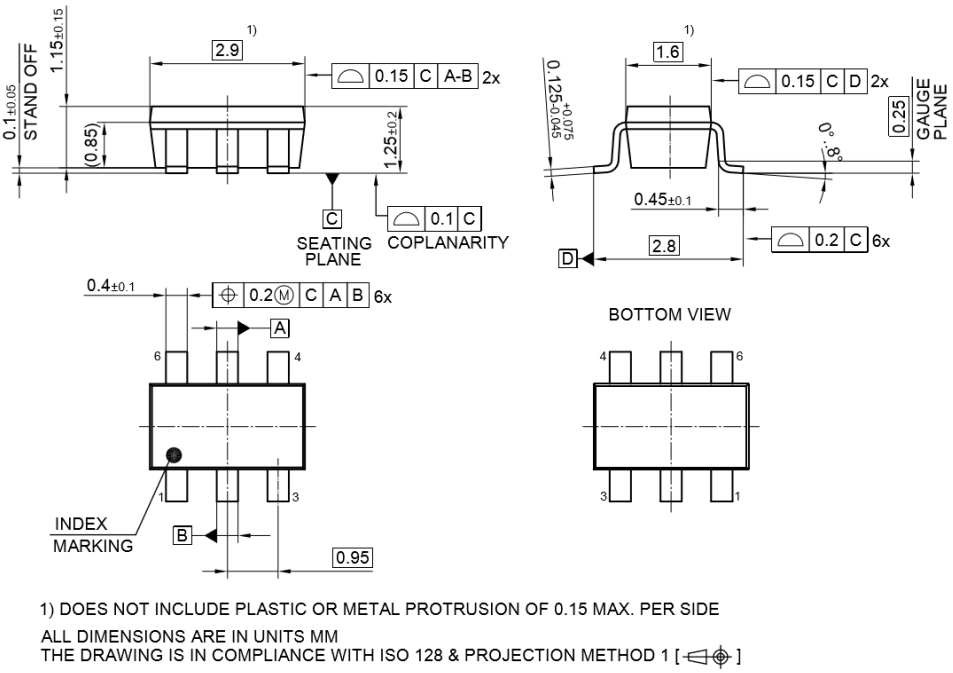



**Figure 2 Package outline dimensions**

# 2 Interface circuit and layout guide

## 2.1 Input/Output signal connection

Figure 3 shows the I/O interface circuit between a microcontroller (µC) or digital signal processing (DSP) unit and the 1ED44173N01B. The 1ED44173N01B input logic is active-high. The $\mathrm{EN}/\overline{\mathrm{FLT}}$ output is an open-drain configuration. This signal should be pulled up to high by an external logic power supply with a pull-up resistor. RC (1 KΩ / 100 pF) is recommended for the input pin to prevent input noise.

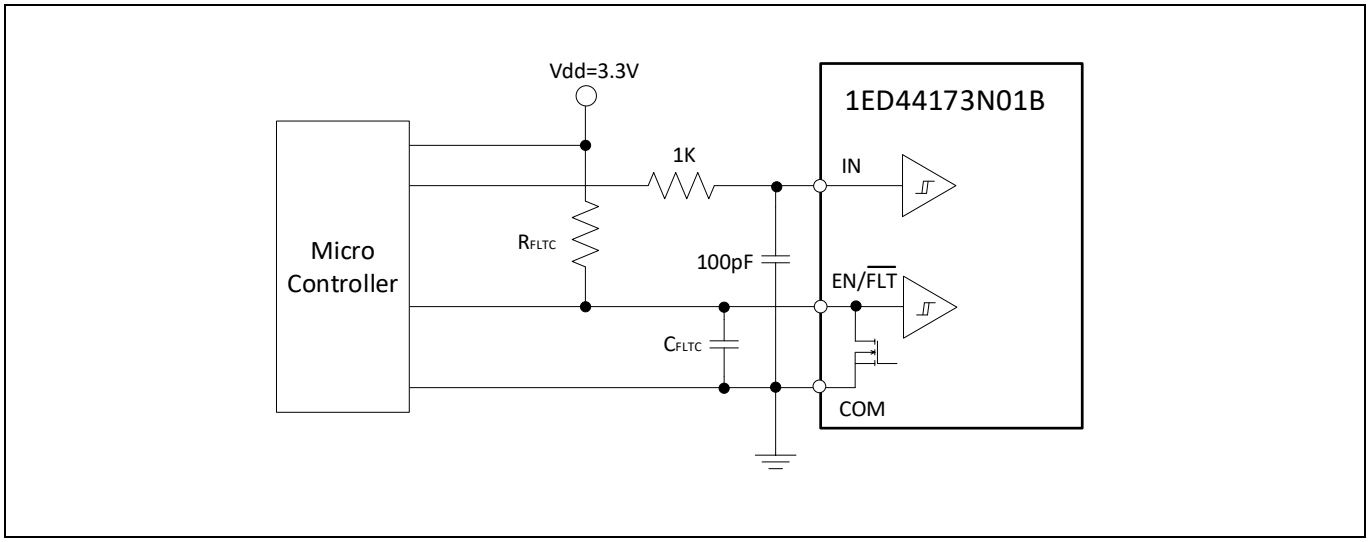



**Figure 3 Recommended microcontroller I/O interface circuit**

**Table 3 Maximum ratings of IN and $\mathrm{EN}/\overline{\mathrm{FLT}}$ pins**

| Item | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Fixed supply voltage | $V_{CC}$ | Applied between $V_{CC}$ – COM | 25 | V |
| Logic input voltage | IN | Applied between IN – COM | -10 ~ $V_{CC}$ + 0.3 | V |
| Voltage at enable and fault reporting pin | $\mathrm{EN}/\overline{\mathrm{FLT}}$ | Applied between $\mathrm{EN}/\overline{\mathrm{FLT}}$ – COM | -0.3 ~ $V_{CC}$ + 0.3 | V |

The input and fault output maximum rating voltages are listed in Table 3. Since the fault output is open-drain configured and its rating is $V_{CC}$ + 0.3 V, a 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 3.3 V logic power supply, which is similar to the input signal.

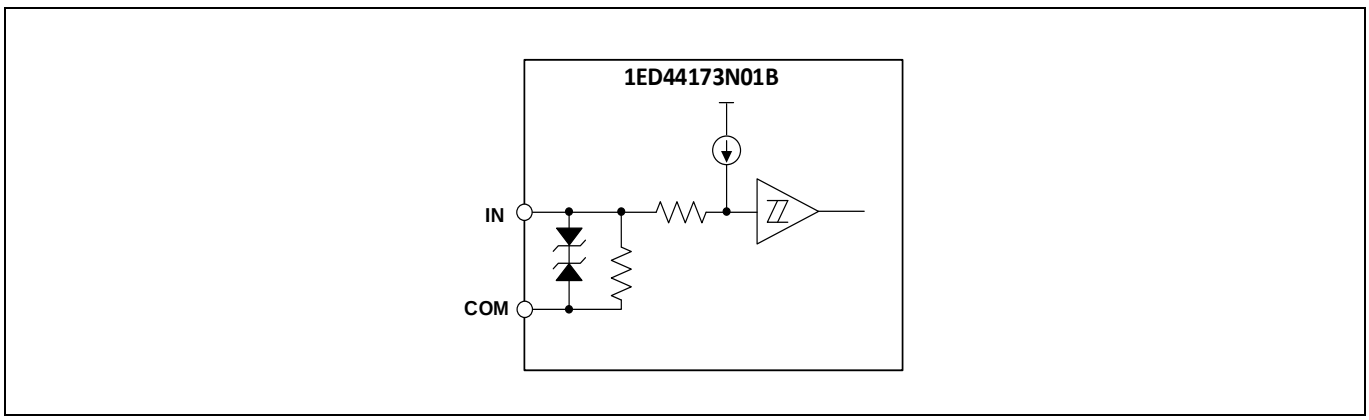



**Figure 4 Simplified input structure diagram of 1ED44173N01B**

The 1ED44173N01B input pin is internally clamped to COM by Zener diodes. It also includes a pull-down resistor and an input Schmitt trigger for better noise immunity. The input pin has the capability to process input voltage up to supply voltage of the driver, and is also compatible with 3.3 V µC or DSP. Table 4 shows the logic input threshold.

**Table 4 Input threshold voltage (at $V_{CC}$ = 15 V, $T_J$ = 25 ℃)**

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Logic "1" input voltage (IN) | $V_{INH}$ | IN – COM | 1.9 | 2.1 | 2.3 | V |
| Logic "0" input voltage (IN) | $V_{INL}$ | | 0.8 | 1.0 | 1.2 | V |

As shown in Figure 4, the 1ED44173N01B input signal section integrates a pull-down resistor. Therefore, when using an external filtering resistor between the microcontroller output and 1ED44173N01B input, pay attention to the signal voltage drop at the 1ED44173N01B input terminal. It should fulfill the logic "1" input voltage requirement. For instance, R = 1 kΩ and C = 100 pF are recommeded for the parts shown in Figure 3.

## 2.2 General interface circuit example

Figure 5 shows a typical application circuit of 1ED44173N01B for the interface schematic with control signals connected directly to a XMC™ µC.

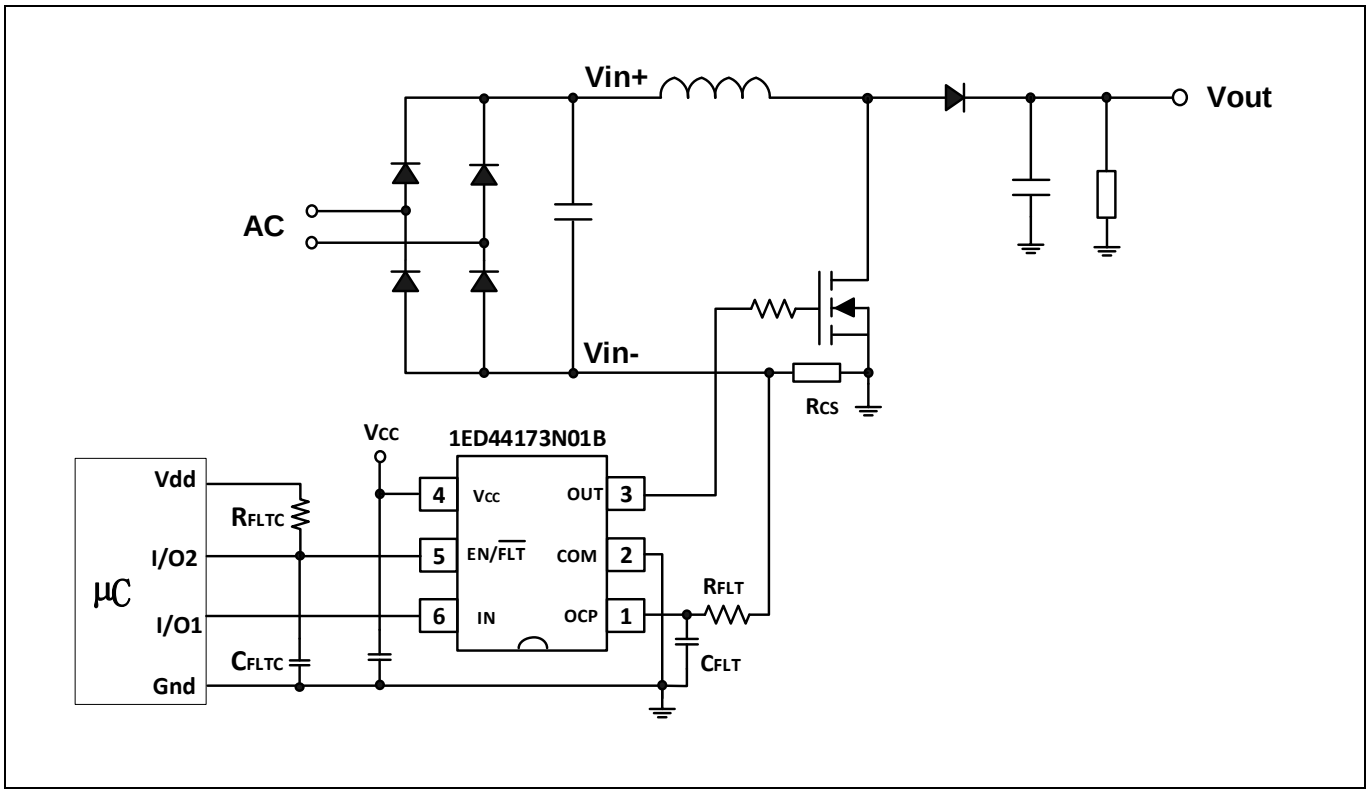



**Figure 5 Application circuit example of active power factor correction (APFC) with $R_{CS}$ for OCP**

*Note:*

1. *The input signal is active-high configured. There is an internal pull-down resistor from the input signal line to COM. When employing an RC coupling circuit between microcontroller and 1ED44173N01B, the RC values should be properly selected so that the input signal is compatible with the 1ED44173N01B logic "1"/logic "0" input voltages.*
2. *To avoid malfunction, the wiring of the input should be as short as possible (less than 2-3 cm).*
3. *The input of 1ED44173N01B can be directly connected to the microcontroller terminal without any opto-coupler or transformer isolation.*
4. *$EN/\overline{FLT}$ output is an open-drain output. This signal line should be pulled up to the positive side of the 5 V or 3.3 V logic power supply with a pull-up resistor. The fault clear program parts are $R_{FLTC}$ and $C_{FLTC}$. The wiring of the two parts should be placed as close to $EN/\overline{FLT}$ and COM pins as possible.*
5. *To prevent protection function errors, the $R_{FLT}$ and $C_{FLT}$ wiring between OCP and power ground should be as short as possible. $C_{FLT}$ wiring should be placed as close to OCP and COM pins as possible.*
6. *Each capacitor should be mounted as close to the pins of the 1ED44173N01B as possible.*
7. *It is recommended to connect the ground pin of the microcontroller directly to the COM pin.*

## 2.3 Recommended layout pattern for overcurrent protection (OCP) & short-circuit protection (SCP) functions

As shown in Figure 6, it is recommended that the OCP filter capacitor connections to the 1ED44173N01B pins be as short as possible. It is also recommended to keep the current sense loop, which is shown in Figure 6, as small as possible for better noise immunity. External current-sensing resistors are applied to detect overcurrent. A high ESL $R_{CS}$ or a long wiring pattern between the $R_{CS}$ and low-side MOSFET will cause excessive surges that might damage the 1ED44173N01B and current detection components. This may also distort the sensing signals. To decrease the parasitic inductance, the wiring between the $R_{CS}$ and emitter of low-side MOSFET should be as short as possible. **Low ESL film resistors** are strongly recommended for the **$R_{CS}$**.

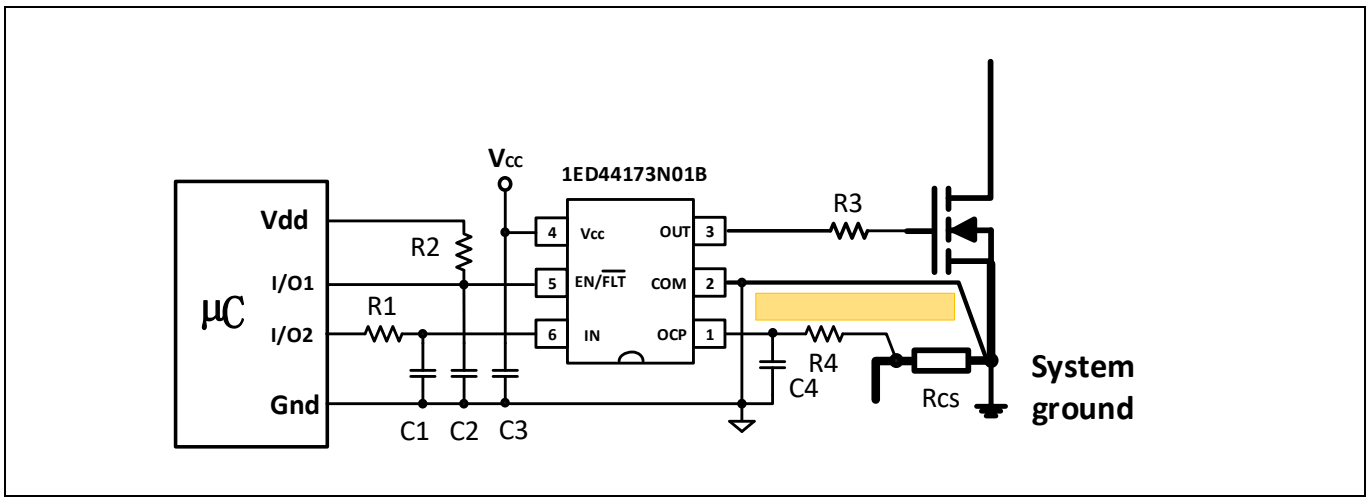



**Figure 6 Recommended layout pattern for OCP & SCP function**

## 2.4 Recommended wiring of the bypass capacitors

It is recommended to place a low ESL ceramic bypass capacitor (C3) exceeding 1 µF connected between $V_{CC}$ and COM directly. Also connect the ground of the capacitor (C1,C2,C4) to COM. Finally, connect COM to system ground at $R_{CS}$. The signal ground and power ground at $R_{CS}$ are connected at only one point. It is also recommended to keep the driver output return loop, which is shown in Figure 7, as small as possible.

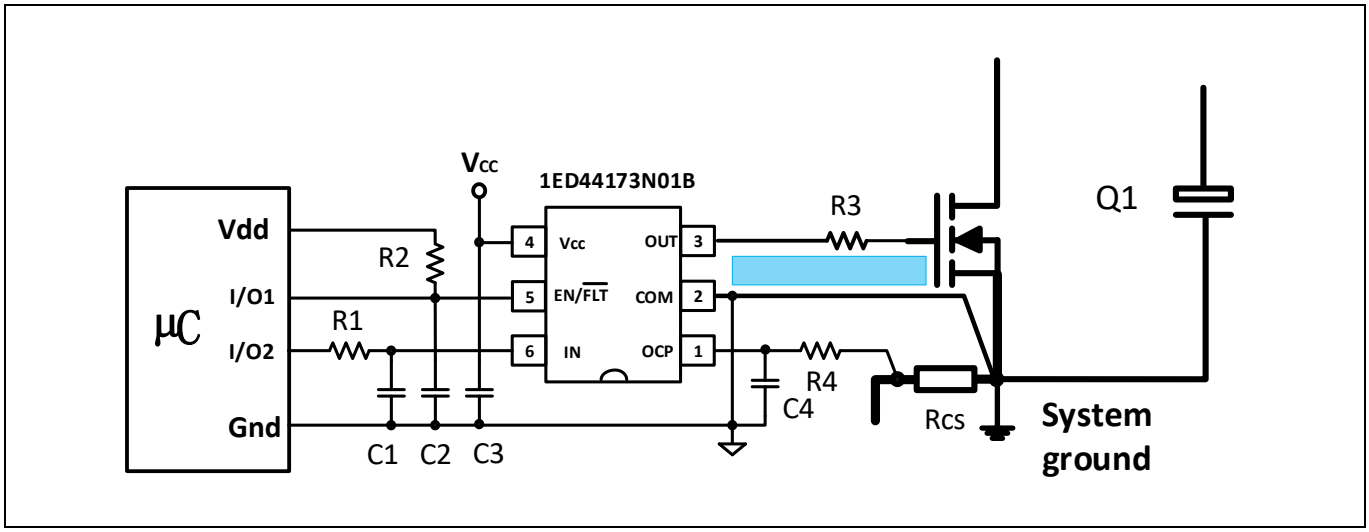


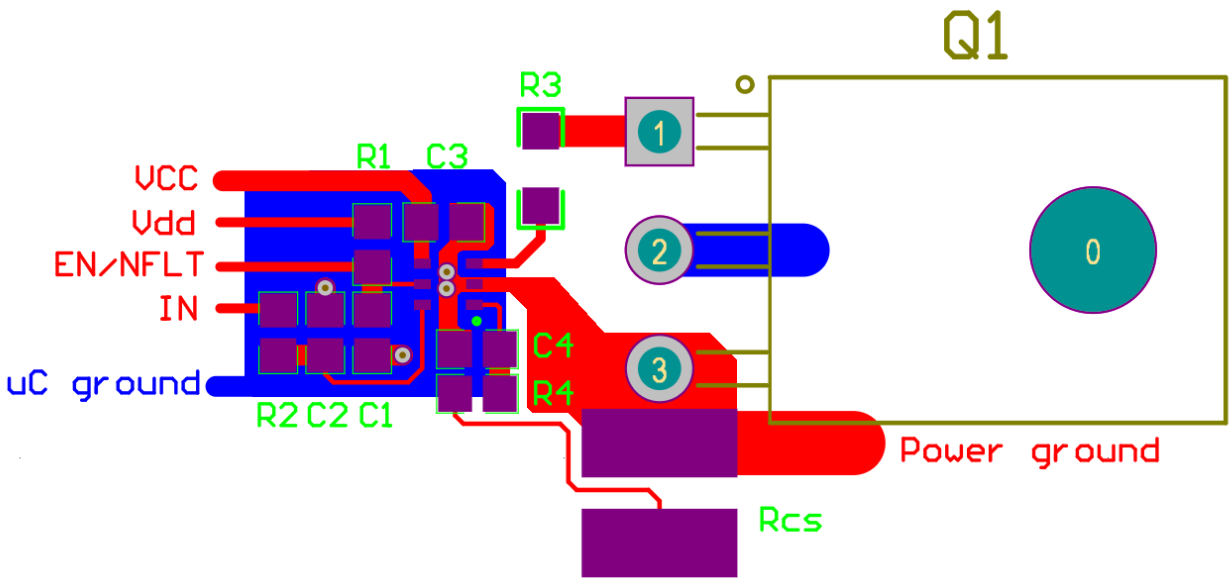

**Figure 7 Recommended wiring of bypass capacitors**

## 2.5 Recommended PCB layout

Proper PCB layout is important in high-current, fast-switching circuits to provide proper device operation and robustness of the design. Improper component and placement may cause errant switching, excessive voltage ringing or circuit latch-up.
Here is the recommended PCB layout:

1. PCB trace loop area and inductance must be minimized.
   - This is accomplished by placing the 1ED44173N01B directly at the power switch (MOSFET).
   - Placing the bypass capacitor (C3) directly at $V_{CC}$ and COM.
   - Locating ground planes or ground return traces directly above or beneath 1ED44173N01B can reduce trace inductance.
2. A ground plane also helps as a radiated noise shield, and provides some heat sinking for power dissipated within the device.

Figure 8 is the example of the PCB layout for the schematic of Figure 7.




(Blue: Bottom layer, Red: Top layer)

**Figure 8 Example of the PCB layout for the schematic of Figure 7**

# 3 Protection features

## 3.1 Undervoltage lockout protection (UVLO)

The 1ED44173N01B has an internal UVLO protection feature on the $V_{CC}$ pin supply circuit blocks. Table 5 shows the UVLO threshold.
Upon power-up, if the $V_{CC}$ voltage fails to reach the $V_{CCUV+}$ threshold, the driver cannot turn on. Additionally, if the $V_{CC}$ voltage decreases below the $V_{CCUV-}$ threshold and the $V_{CC}$ bias voltage remains lower than the $V_{CCUV-}$ threshold exceeding UVLO filter time ($t_{VCCUV}$) during operation, the undervoltage lockout circuitry will recognize a fault condition and shut down the drive output. The EN/$\overline{\text{FLT}}$ will then pull down to inform the controller of the fault condition, regardless of the status of the IN input pin. The $t_{VCCUV}$ about 2 µs helps to suppress noise from the UVLO circuit, so that negative-going voltage spikes at the supply pin will avoid parasitic UVLO events.

**Table 5 $V_{CC}$ UVLO threshold voltage ($T_J$ = 25 ℃)**

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ supply undervoltage positive-going threshold | $V_{CCUV+}$ | Applied between $V_{CC}$ – COM | 7.4 | 8.0 | 8.6 | V |
| $V_{CC}$ supply undervoltage negative-going threshold | $V_{CCUV-}$ | | 6.7 | 7.3 | 7.8 | |
| $V_{CC}$ supply undervoltage lockout hysteresis | $V_{CCUVH}$ | | — | 0.7 | — | |

When $V_{CC}$ is higher than $V_{CCUV+}$ and longer than $t_{FLTC}$, EN/$\overline{\text{FLT}}$ becomes high and the 1ED44173N01B is enabled. (Figure 9 shows the UVLO protection.) The UVLO function is latched up. 1ED44173N01B will wait for a new input signal on IN before it activates the output stage.

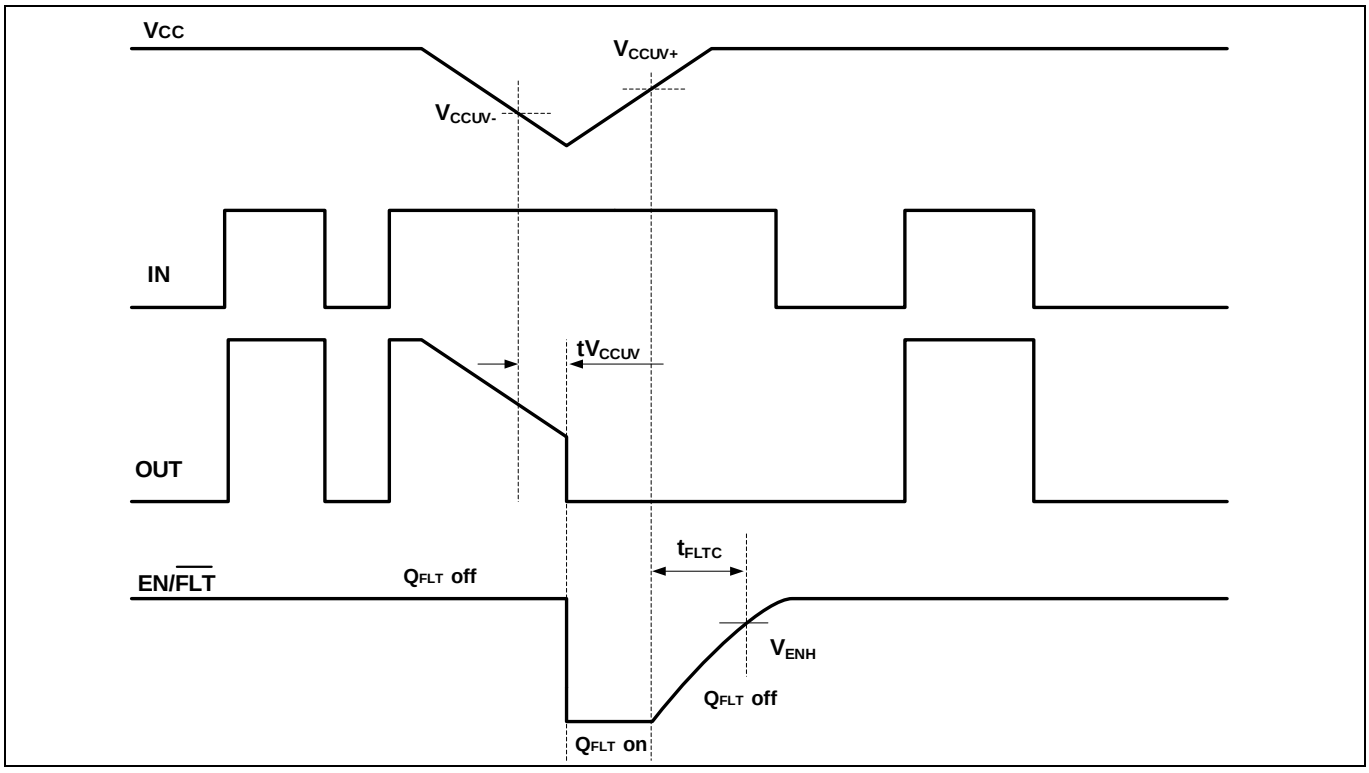



**Figure 9 $V_{CC}$ undervoltage protection**

## Protection features

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power device could be driven with a low voltage, resulting in the power device conducting current while the channel impedance is high. This could result in very high conduction losses within the power device, and lead to power device failure.

The $V_{CC}$ power for the 1ED44173N01B is normally provided by a single 15 V supply that is connected to the $V_{CC}$ and COM terminals. The $V_{CC}$ power supply should be well filtered with a low-impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the 1ED44173N01B pins. High-frequency noise on the supply might cause the internal control circuit to malfunction and to generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ±1 V.

## 3.2 Overcurrent protection (OCP)

### 3.2.1 Timing chart of OCP

The 1ED44173N01B has a fast overcurrent shutdown function. Its internal comparator monitors the voltage of the OCP pin. If this voltage exceeds the OCP threshold ($V_{OCTH}$), which is specified in Table 6, a fault signal is activated and the OUT is turned off. The tolerance of the OCP threshold is ±5%, which keeps the accurate OCP in the system design.

**Table 6 Current limit threshold voltage (at $V_{CC}$ = 15 V, $T_J$ = 25 ℃)**

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Current limit threshold voltage | $V_{OCTH}$ | OCP – COM | -259 | -246 | -233 | mV |

Typically, the maximum short-circuit current magnitude of the MOSFET is gate-voltage dependent. A higher gate voltage results in a larger short-circuit current. Generally, the maximum overcurrent trip level is set to below 2 times the nominal rated collector current. The overcurrent protection timing chart is shown in Figure 10.

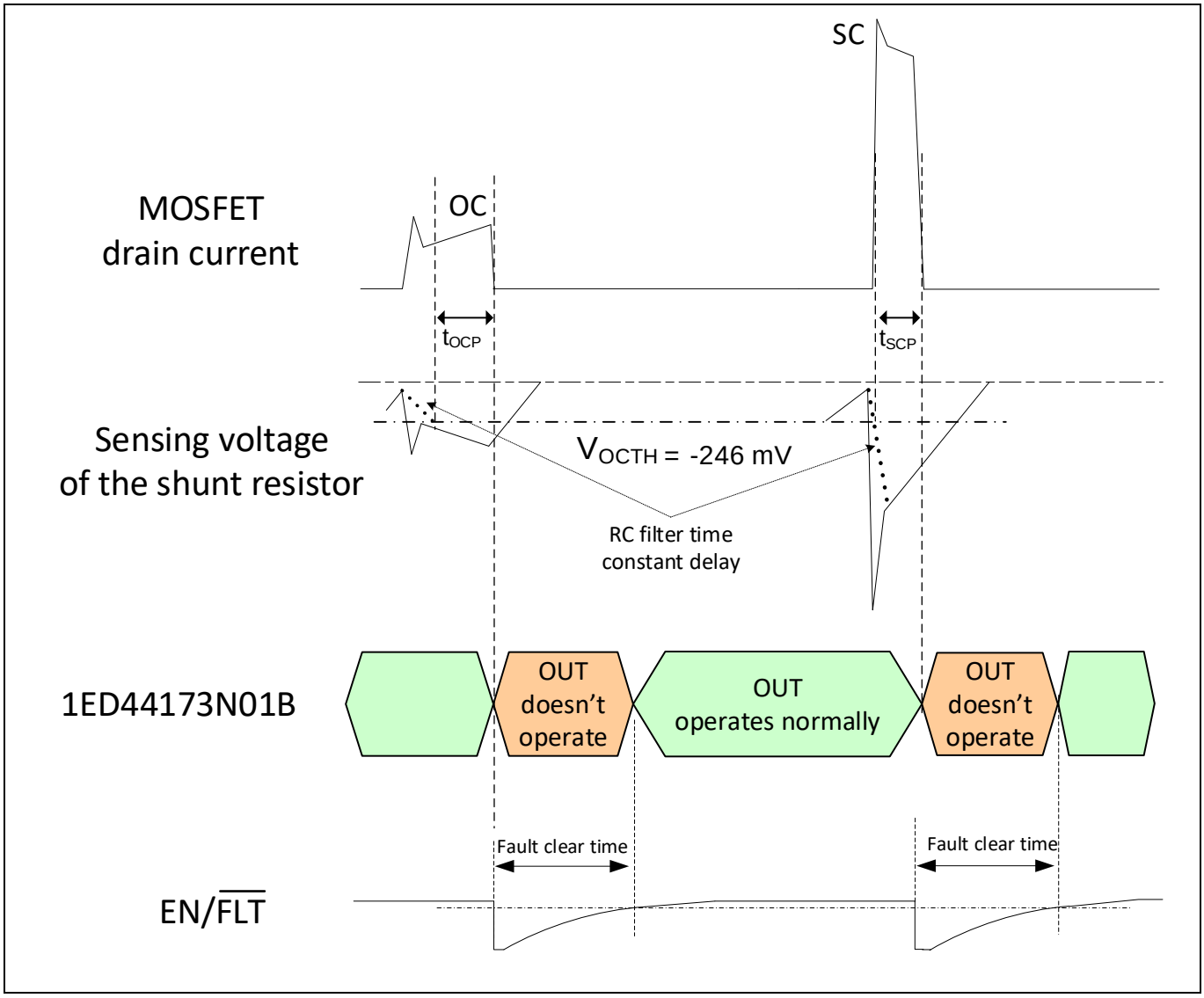



**Figure 10 Timing chart of OCP**

### 3.2.2 Selecting $R_{CS}$

The value of the $R_{CS}$ is calculated by the following equation:

$$R_{CS} = \frac{V_{OCTH}}{I_{OC}} \quad (1)$$

Where $I_{OC}$ is the current of the overcurrent (OC) detection level.

The maximum value of the OC protection level should be set lower than the repetitive peak collector current in the datasheet considering the tolerance of $R_{CS}$.

For example, if the OCP is 25 A, the recommended value of the $R_{CS}$ is calculated as

$$R_{CS(min)} = \frac{0.25}{25} = 10\ m\Omega$$

For the power rating of the $R_{CS}$, the following list should be considered:

- Maximum load current (Irms)
- $R_{CS}$ value at Tc = 25 °C
- Power derating ratio of $R_{CS}$ at $T_C$ = 100 °C according to the manufacturer's datasheet
- Safety margin

The $R_{CS}$ power rating is calculated by the following equation:

$$P_{SC} = \frac{I_{rms}^2 \times R_{SC} \times margin}{derating\ ratio} \quad (2)$$

For example, If $R_{SC}$ = 10 mΩ:

- Max. load current: 4 A (rms)
- Power derating ratio of $R_{CS}$ at $T_C$ = 100 °C : 80%
- Safety margin : 50%

$$P_{SC} = \frac{4^2 x\ 0.01\ x\ 1.5}{0.8} = 0.3\ W$$

A proper power rating of $R_{CS}$ is over 0.3 W, e.g. 0.5 W.

A proper resistance and power rating higher than the minimum value should be chosen considering the OCP level required in the application.

### 3.2.3 OCP delay time

The internal OCP blanking time ($t_{BLK,}$ Table 7 shows the specification) is necessary in the OC sensing circuit to prevent malfunction of the OCP caused by noise. If the internal blanking time is not sufficient to suppress the noise, an additional external RC filter is necessary. The RC time constant is determined by considering the noise duration and the short-circuit withstand time capability of the MOSFET.

The sensing voltage on $R_{CS}$ is applied to the OCP pin of 1ED44173N01B via the RC filter. The filter delay time ($t_{FILTER}$) that the input voltage of OCP pin decreases to the OCP minus threshold voltage ($V_{OCTH}$ = - 246 mV) is caused by RC filter time constant.

In addition there is a shutdown propagation delay of OCP ($t_{OCPDEL}$, the time from OCP happening to output shutdown). Please refer to Table 8.

**Table 7 Specification of OCP blanking time**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Overcurrent protection blanking time $t_{BLK}$ | 30 | 50 | 80 | ns |

**Table 8 Specification of OCP to output shutdown propagation delay**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| OCP to output shutdown propagation delay $t_{OCPDEL}$ | — | 97 | 140 | ns |

Therefore, the total delay time from OCP threshold ($V_{OCTH}$) to the shutdown of the MOSFET becomes:

$$t_{TOTAL} = t_{FILTER} + t_{OCPDEL} \quad (3)$$

Shutdown propagation delay is inversely proportional to the current rating, therefore the $t_{TOTAL}$ is reduced at higher current conditions. The total delay must be less than the short-circuit withstanding time ($t_{SC}$) of the MOSFET in the datasheet. If the $t_{SC}$ = 1 µs, the RC time constant should be set in the range of 0.5 µs. Recommended values for the filter components are R = 470 Ω and C = 1 nF.

## 3.3 Fault output circuit and fault clear time setup

The 1ED44173N01B provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the driver to report a fault via the EN/$\overline{FLT}$ pin. The first is an undervoltage condition of $V_{CC}$ and the second is if the OCP pin recognizes a fault. Once the fault condition occurs, the EN/$\overline{FLT}$ pin is internally pulled to COM. The EN/$\overline{FLT}$ output stays in the low state until the fault condition has been removed and the internal pull down MOSFET $Q_{FLT}$ turns off, then the voltage on the EN/$\overline{FLT}$ pin is charged up with internal and external pull-up voltage.

The length of the fault clear time period ($t_{FLTC}$) is determined by exponential charging characteristics of the capacitor where the time constant is set by $R_{FLTC}$ and $C_{FLTC}$. Figure 11 and Figure 5 show that $R_{FLTC}$ is connected between the external supply ($V_{dd}$ = 3.3 V) and the EN/$\overline{FLT}$ pin, while $C_{FLTC}$ is placed between the EN/$\overline{FLT}$ and COM pins. Actually the EN/$\overline{FLT}$ pin is pulled up to 3.3 V with a 2.15 MΩ pull-up resistor internally.

If the $V_{dd}$=3.3 V, the length of the fault clear time period can be determined by using the formula below.

$$t_{FLTC} = -\left(\frac{R_{FLTC} \times 2.15M}{R_{FLTC} + 2.15M}\right) \times C_{FLTC} \times \ln\left(1 - \frac{V_{ENH}}{V_{dd}}\right) \quad (4)$$

Where $V_{ENH}$ is fault clear threshold voltage (typical 2.1 V).

The sample of $t_{FLTC}$ setup:

If $C_{FLTC}$ = 150 pF, $R_{FLTC}$ = 1 MΩ, $V_{dd}$ = 3.3 V, then

$$t_{FLTC} = -\left(\frac{1M \times 2.15M}{1M + 2.15M}\right) \times 150pF \times \ln\left(1 - \frac{2.1V}{3.3V}\right) = 103us$$

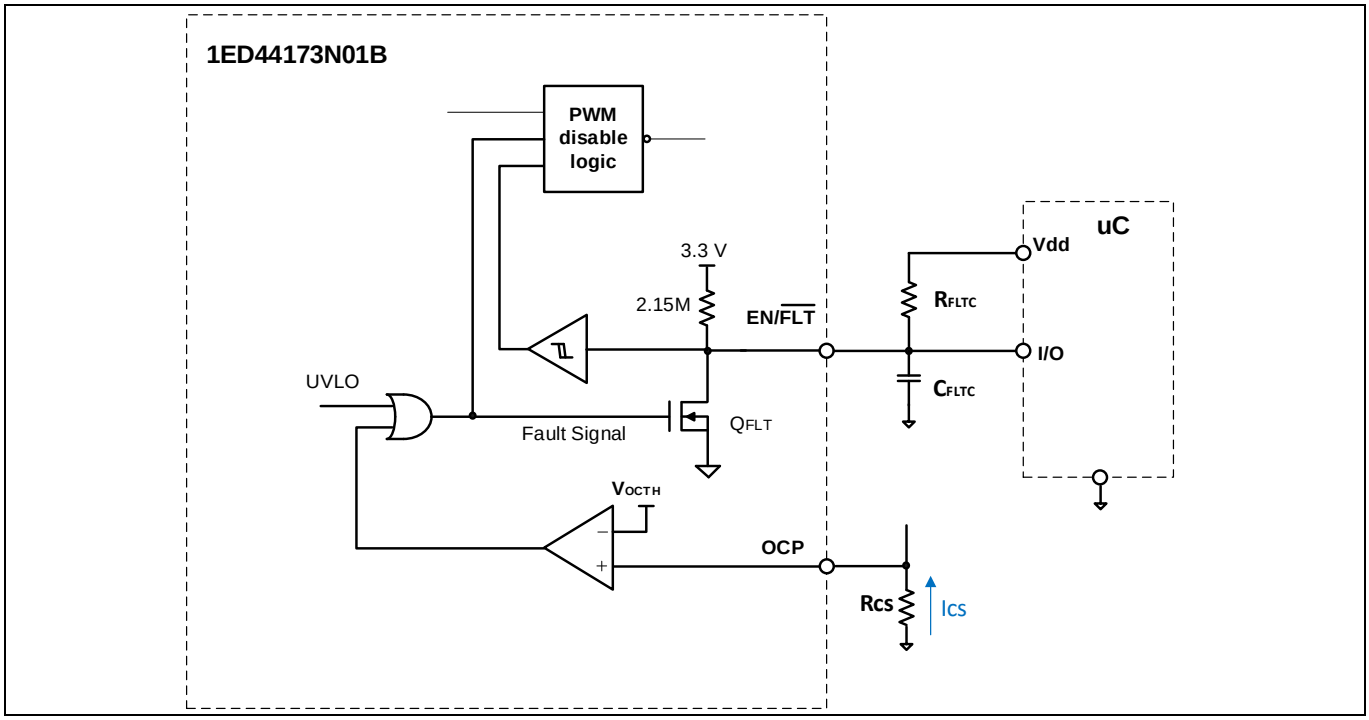



**Figure 11 Diagram of the fault output circuit and fault clear time setup**

If the $C_{FLTC}$ is not connected, and $R_{FLTC}$ is pulled up to $V_{CC}$ with 10 kΩ resistor, the gate driver can implement overcrrent protection cycle by cycle. The feature of OCP with cycle by cycle can limit the peak inductor current in low-line voltage and prevent the saturation of the PFC inductor.

## 3.4 Enable input circuit

1ED44173N01B provides an enable functionality that allows you to shut down or to enable the output. When EN/$\overline{\text{FLT}}$ is pulled up (the enable voltage is higher than $V_{ENH}$), the output is able to operate normally, pulling EN/$\overline{\text{FLT}}$ low (the enable voltage is lower than $V_{ENL}$), the output is disabled. The enable function is latched up. After a disable event, 1ED44173N01B will wait for a new input signal on IN before it activates the output stage. See the threshold voltage of $V_{ENH}$ and $V_{ENL}$ in Table 9 and Figure 12.

**Table 9 EN/$\overline{\text{FLT}}$ input threshold voltage (at $V_{CC}$ = 15 V, $T_J$ = 25 ℃)**

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Logic "1" input voltage (EN/$\overline{\text{FLT}}$) | $V_{ENH}$ | EN/$\overline{\text{FLT}}$ – COM | 1.9 | 2.1 | 2.3 | V |
| Logic "0" input voltage (EN/$\overline{\text{FLT}}$) | $V_{ENL}$ | | 0.8 | 1 | 1.2 | V |

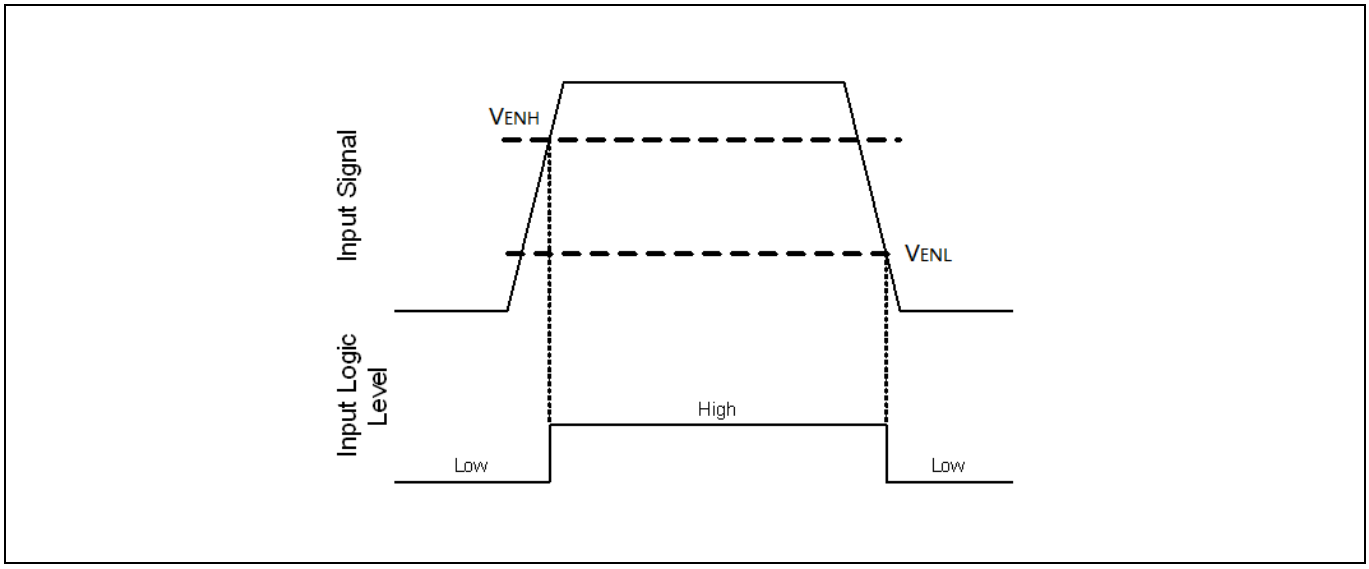



**Figure 12 Enable input thresholds**

The relationships between the input (IN), output (OUT) and enable (EN/$\overline{\text{FLT}}$) signals of the 1ED44173N01B are illustrated below in Figure 13.

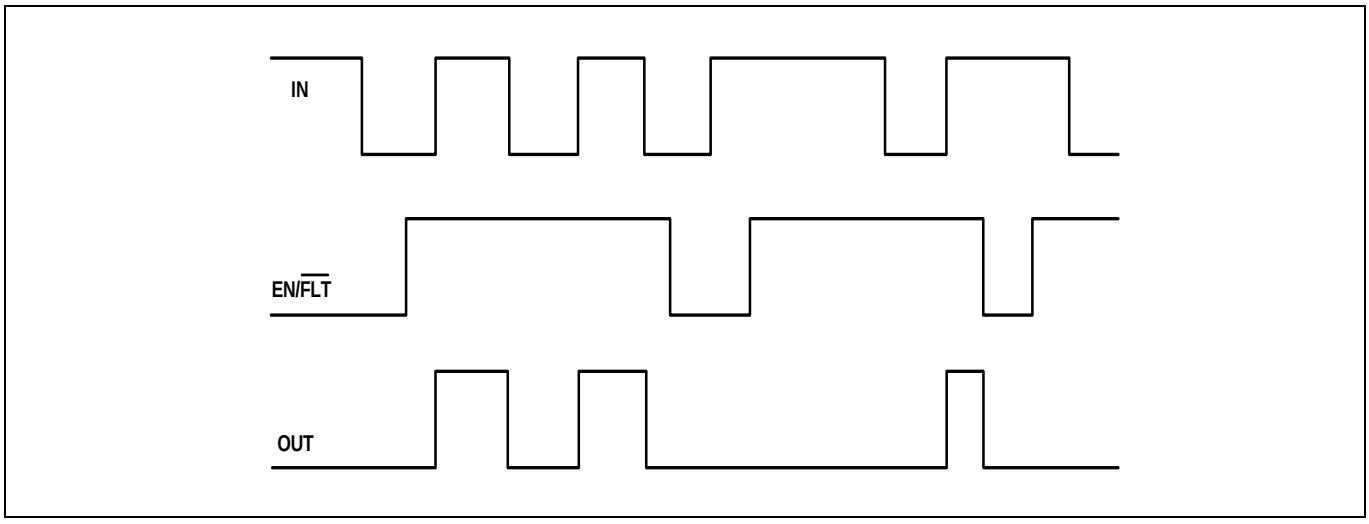



**Figure 13 Input/output/enable pins timing diagram**

From Figure 14, we can see the definitions of the timing parameter ($t_{DISA}$) associated with this device. $t_{DISA}$ is the delay time from the enable signal pulling down to output shutting down. Please refer to Table 10.

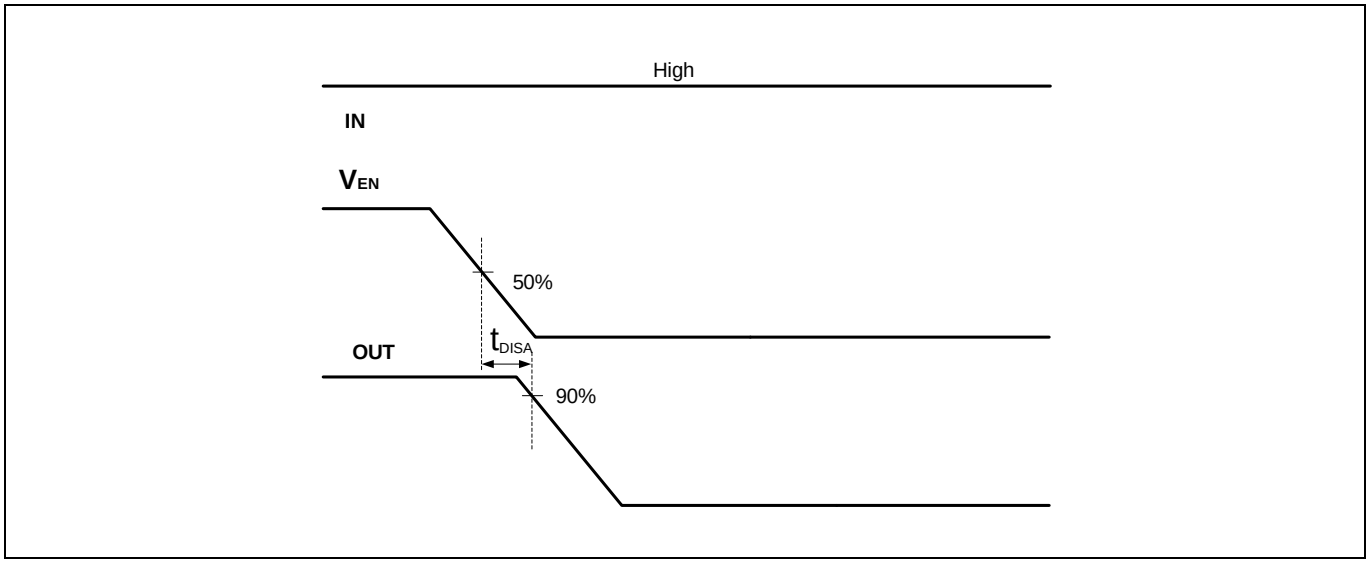



**Figure 14 EN pin switching time waveform**

**Table 10 Specification of disable delay time**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Enable propagation delay $t_{DISA}$ | 27 | 34 | 45 | ns |

# 4 Driving capability

## 4.1 $I_{O+}$ and $I_{O-}$

The 1ED44173N01B provides minimum 2 A source or sink-driving capability (see Table 11) which is large enough to drive most discrete PFC switches, e.g. the MOSFET.

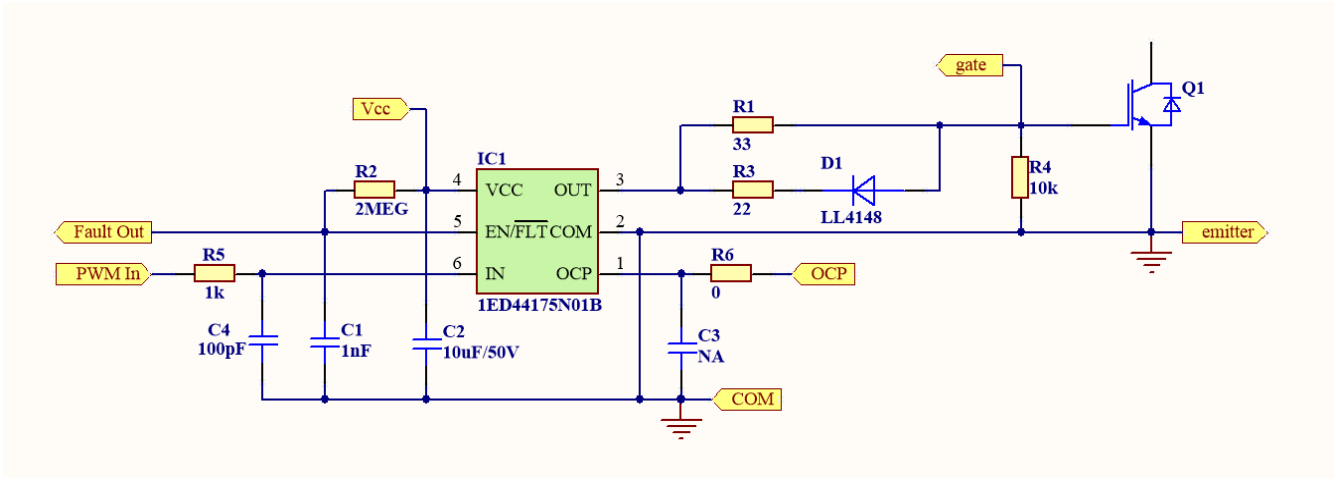
**Table 11 $I_{O+}$ and $I_{O-}$ (at $V_{CC}$ = 15 V, $T_J$ = 25 ℃)**

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output sourcing short-circuit pulsed current | $I_{O+}$ | $V_O$ = 0 V<br>PW ≤ 2 µs | 2 | 2.6 | — | A |
| Output sinking short-circuit pulsed current | $I_{O-}$ | $V_O$ = 15 V<br>PW ≤ 2 µs | 2 | 2.6 | — | |

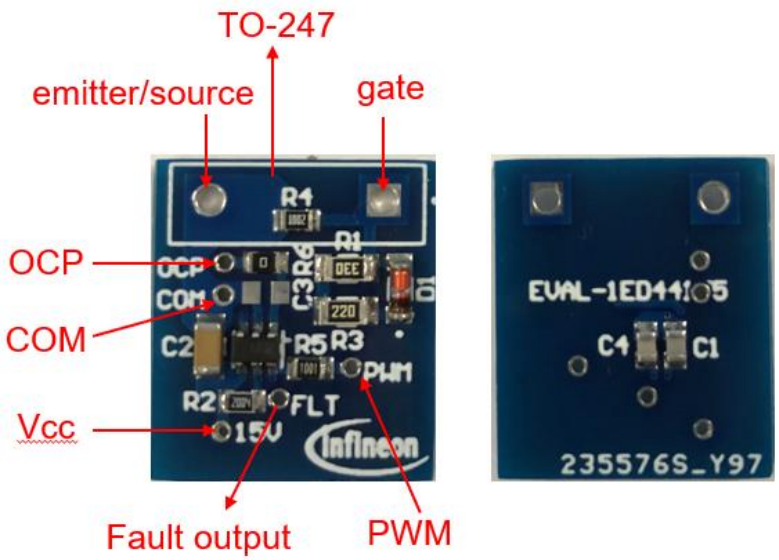
# 5 EVAL-1ED44175N01B adapter board

A small, dual purpose adapter board (EVAL-1ED44175N01B, see Figure 15 ) is available for testing the 1ED44173N01B inside an actual switched-mode application.

The 1ED44173N01B MOSFET low-side driver is pin-to-pin compatible with the 1ED44175N01B low-side IGBT driver. The board includes a footprint that can support either the 1ED44173N01B or 1ED44175N01B SOT-236 low-side drivers with OCP and enable/fault output, TO-247 footprint of gate and emitter for IGBT or gate and source for MOSFET, and other SMD components. The adapter board can be easily connected to an existing switched-mode power circuit for fast in-circuit evaluation.




**Schematic (1ED44175N01B can be replaced with 1ED44173N01B)**

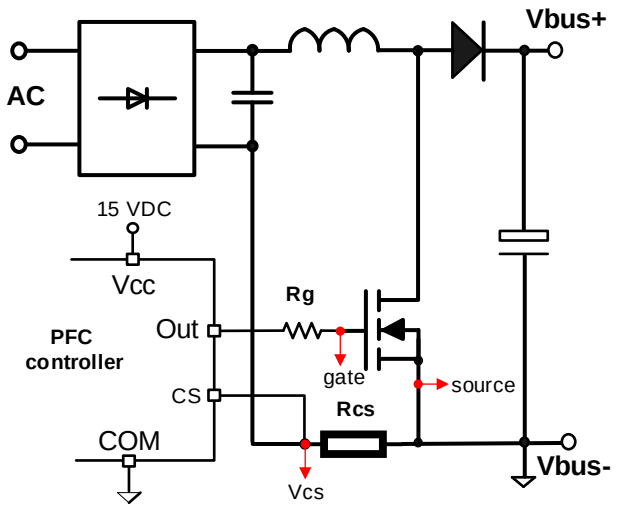



**Board profile**

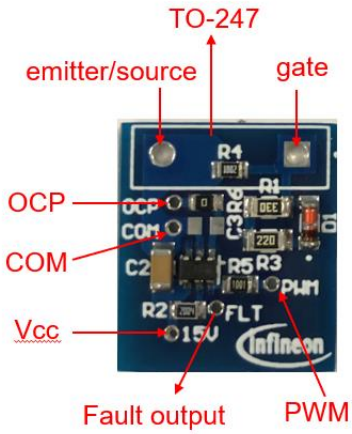
**Figure 15 EVAL-1ED44175 adapter board**

## 5.1 The evaluation of 1ED44173N01B on the PFC board

### 5.1.1 The connection between the adapter board and PFC board




**Block diagram of the PFC board**

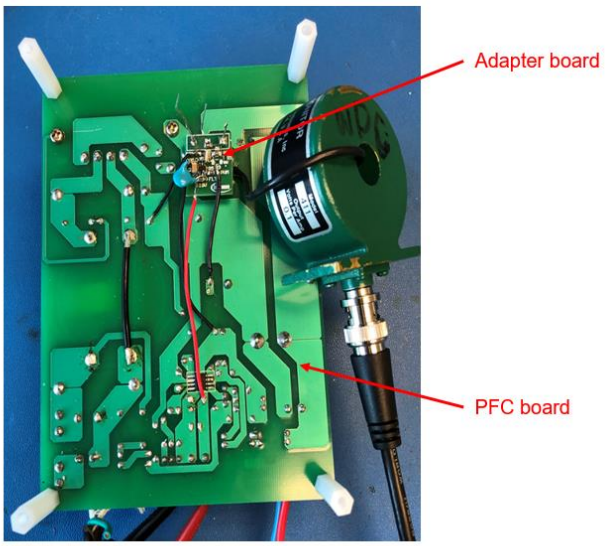



**Adapter board**

- Disconnect $R_g$ on the PFC board
- Having the following connections between PFC board and adapter board:

| PFC board | Adapter board |
|---|---|
| 15 $V_{DC}$ | $V_{CC}$ |
| COM | COM |
| $V_{CS}$ | OCP |
| Out | PWM |
| gate | gate |
| source | emitter/source |

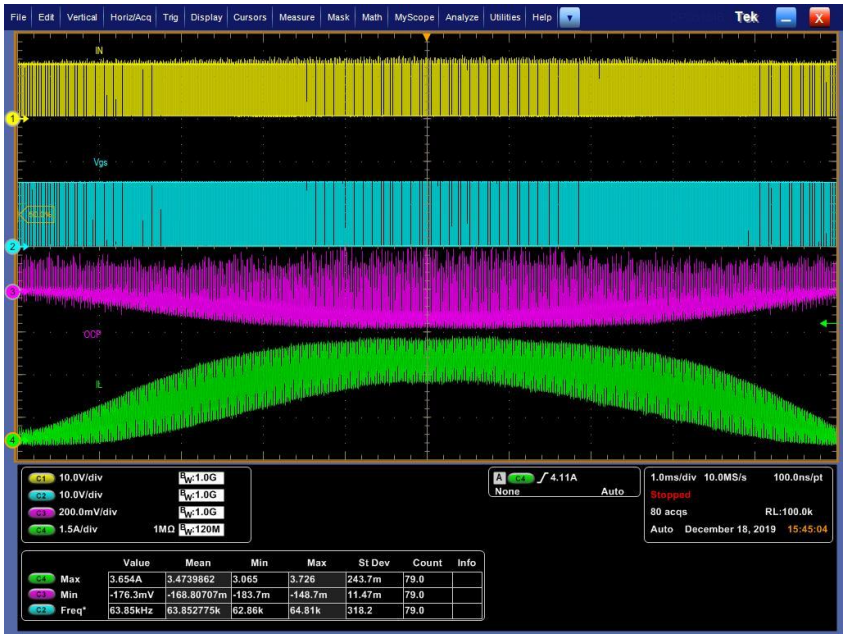
Top




Bottom

**Figure 16 Connection between PFC board and adapter board**

### 5.1.2 Normal operation



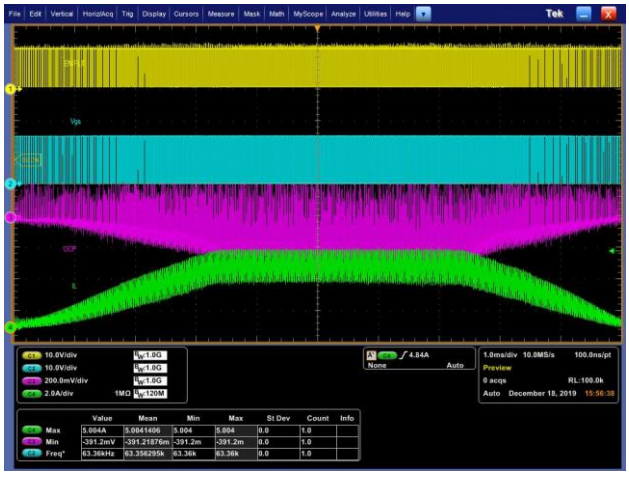

- Channel 1 (yellow): PWM input voltage
- Channel 2 ( blue): Gate voltage of PFC MOSFET
- Channel 3 ( purple ): Voltage of OCP pin
- Channel 4 ( green): Current of PFC inductor

Working condition:

- PFC inductor = 750 uH, $R_{cs}$ = 0.05Ω
- PFC MOSFET : IPP60R199CP
- Frequency = 64 kHz, $V_{in}$ = 220 $V_{ac}$, $V_{bus}$ = 400 V
- $P_{out}$ = 400 W

**Figure 17 Normal operation**

### 5.1.3 OCP




Zoom out


Zoom in

- $V_{in}$ = 175 $V_{ac}$, $V_{bus}$ = 400 V, $P_{out}$ = 500 W, (R2 = 10 kΩ, C1: not connected)
- Cycle by cycle OCP

**Figure 18 OCP**

### 5.1.4 Short PFC inductor test


- Channel 1 (yellow): PWM voltage
- Channel 2 ( blue): Gate voltage of PFC MOSFET
- Channel 3 ( purple ): Voltage of OCP
- Channel 4 ( green): Current of the cable to short the PFC indcutor

- PFC MOSFET: IPP60R199CP
- Rg = 68 Ω, $R_{CS}$ = 0.05 Ω
- OCP pin: with external filter (R6 = 330 Ω, C3 = 1 nF)
- Vin = 400Vdc
- Short PFC inductor test with 125 mm cable
- The protection time is less than **200 ns** (fast enough to protect most power MOSFETs, including SiC MOSFETs)

**Figure 19 Short PFC inductor test**

# 6 Recommended related products

The 1ED44173N01B can be used to drive up to 75 A/650 V CoolMOS™ from Infineon at a frequency of up to 100 kHz for PFC applications. The power rating is up to 3 kW. If the higher frequency is required for the application, Infineon's CoolSiC™ SiC MOSFET is a good choice. Some parts of the CoolMOS™, CoolSiC™, rapid switching emitter-controlled diode and silicon carbide CoolSiC™ Schottky diode from Infineon in PFC applications are recommended in Table 12,Table 13, and Table 14.

**Table 12 Infineon's CoolMOS™ C7 superjunction MOSFET**

| Part Number | Voltage level | Package | RDS (on) | ID @ 25°C max | ID, pulse @ 25°C max |
|---|---|---|---|---|---|
| IPW(Z)65R019C7 | 650 V | PG-TO 247-3(4) | 19 mΩ | 75 A | 496 A |
| IPW(Z)65R045C7 | 650 V | PG-TO 247-3(4) | 45 mΩ | 46 A | 212 A |
| IPW(Z)65R065C7 | 650 V | PG-TO 247-3(4) | 65 mΩ | 33 A | 145 A |
| IPW(Z)65R095C7 | 650 V | PG-TO 247-3(4) | 95 mΩ | 24 A | 100 A |
| IPW65R125C7 | 650 V | PG-TO 247 | 125 mΩ | 18 A | 75 A |
| IPW65R190C7 | 650 V | PG-TO 247 | 190 mΩ | 13 A | 49 A |

For more options visit www.infineon.com/MOSFET

**Table 13 Infineon's CoolSiC™ SiC MOSFETs**

| Part Number | Voltage level | Package | RDS (on) | ID @ 25°C max | ID, pulse @ 25°C max |
|---|---|---|---|---|---|
| IMW(ZA)65R027M1H | 650 V | PG-TO 247-3(4) | 27 mΩ | 47(59) A | 184 A |
| IMW(ZA)65R048M1H | 650 V | PG-TO 247-3(4) | 48 mΩ | 39 A | 100 A |
| IMW(ZA)65R072M1H | 650 V | PG-TO 247-3(4) | 72 mΩ | 26(28) A | 69 A |
| IMW(ZA)65R107M1H | 650 V | PG-TO 247-3(4) | 107 mΩ | 20 A | 48 A |

For more options visit https://www.infineon.com/SiC MOSFET

**Table 14 Infineons RAPID 1 diode**

| Part Number | Voltage level | Package | VF @ 25°C max | IF @ 100°C max | IF @ 25°C max |
|---|---|---|---|---|---|
| IDW30E65D1 | 650 V | PG-TO247-3 | 1.7 V (IF=30 A) | 30 A | 60 A |
| IDW40E65D1(E) | 650 V | PG-TO247-3(-AI) | 1.7 V (IF=40 A) | 40 A | 80 A |
| IDW60C65D1 | 650 V | PG-TO247-3 | 1.7 V (IF=30 A) | 30 A | 60 A |
| IDW80C65D1 | 650 V | PG-TO247-3 | 1.7 V (IF=40 A) | 40 A | 80 A |

For more options visit www.infineon.com/rapiddiodes

## Recommended related products

**Table 15 Infineon's silicon carbide CoolSiC™ Schottky diode**

| Part Number | Voltage level | Package | VF @ $T_j$=25°C max | IF @ $T_C$ < 120°C | $I_{F,SM}$ @ $T_C$=25°C $t_p$=10 ms max |
|---|---|---|---|---|---|
| IDW20G65C5 | 650 V | TO-247 | 1.7 V (IF=20 A) | 20 A | 103 |
| IDW32G65C5B | 650 V | TO-247 | 1.7 V (IF=16 A) | 2 x 16 A | 95 A |
| IDW40G65C5B | 650 V | TO-247 | 1.7 V (IF=20 A) | 2 x 20 A | 103 A |
| IDW30G65C5 | 650 V | TO-247 | 1.7 V (IF=30 A) | 30 A ($T_C$ < 115°C) | 165 A |
| IDW40G65C5 | 650 V | TO-247 | 1.7 V (IF=40 A) | 40 A ($T_C$ < 110°C) | 182 A |

For more options visit CoolSiC™ Schottky Diode

# 7 References

1. Datasheet of 1ED44173N01B, Rev 1.0
2. 1ED44175N01B - Low-side IGBT driver with over-current protection and fault/enable - Technical description

# 8 Revision history

Major changes since the last revision

| Version number | Revision date | Revision description |
|---|---|---|
| 1.0 | 2020-04-22 | Initial release |
| 1.1 | 2020-06-16 | Add OPN of EVAL-1ED44173N01B on first page |
| 1.2 | 2024-01-16 | Page 21 figure 15 and page 22 figure 16, Correct the gate and emitter/source pins of the evaluation board. On page 25, chapter 6, Add missing table. |

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