

## SP000923326, SP001328238

## Unipolar Hall Switch

## Features

- 3.0 V to 32 V operating supply voltage
- Operation from unregulated power supply
- Reverse polarity protection (-18 V)
- Overvoltage capability up to 42 V without external resistor
- Output overcurrent and overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 0.35  $\mu$ s)
- High ESD performance
- Small SMD package PG-SOT23-3-15



## Target applications

Target applications for the TLE496x Hall Switch family are all applications which require a high precision Hall Switch with an operating temperature range from  $-40^{\circ}\text{C}$  to  $170^{\circ}\text{C}$ . Its superior supply voltage range from 3.0 V to 32 V with overvoltage capability (e.g. load-dump) up to 42 V without external resistor makes it ideally suited for automotive and industrial applications.

The TLE4964-1M is a unipolar switch with a typical operating point BOP = 18 mT and a hysteresis of  $B_{\text{HYS}} = 5.5$  mT. It is ideally suited for various position detection applications.

## Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100.

## Description

Table 1 Overview

Characteristic	Supply Voltage	Supply Current	Sensitivity	Interface	Temperature
Unipolar Hall Effect Switch	3.0 V ~ 32 V	1.6 mA	Low $B_{\text{OP}}$ : 18 mT $B_{\text{RP}}$ : 12.5 mT	Open Drain Output	$-40^{\circ}\text{C}$ to $170^{\circ}\text{C}$

Table 2 Ordering information

Product name	Product type	Ordering code	Package
TLE4964-1M	Unipolar Hall Switch	SP000923326 (3k) SP001328238 (10k)	PG-SOT23-3-15

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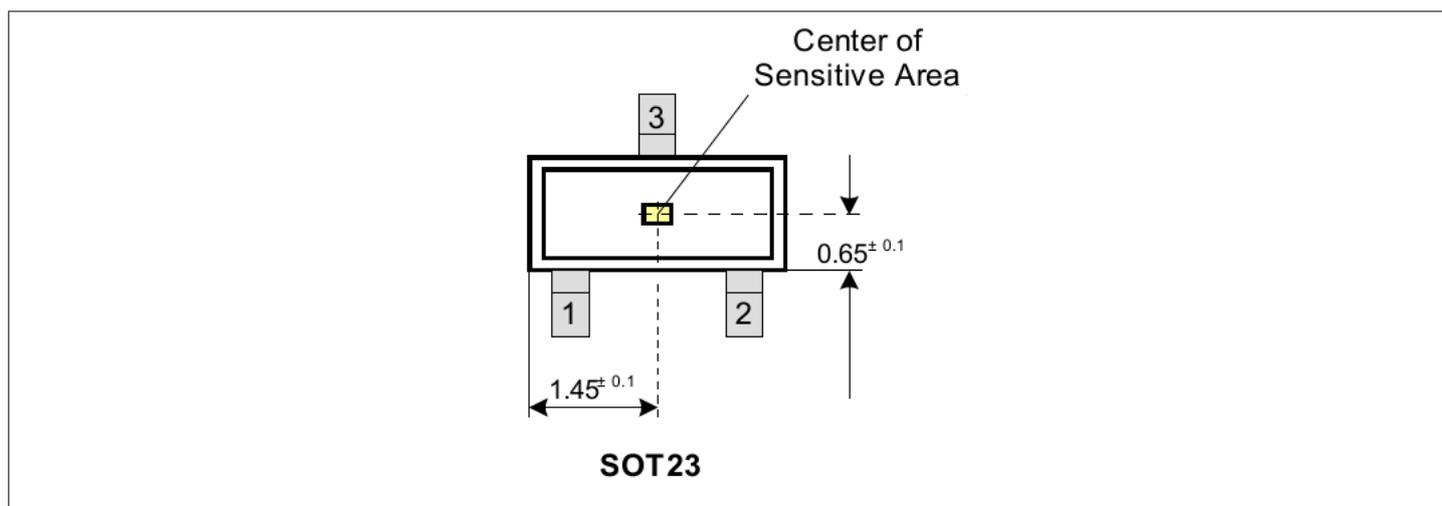
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## 1 Functional description

### 1.1 General

The TLE4964-1M is an integrated Hall effect switch designed specifically for highly accurate applications with superior supply voltage capability, operating temperature range and temperature stability of the magnetic thresholds.

### 1.2 Pin configuration (top view)



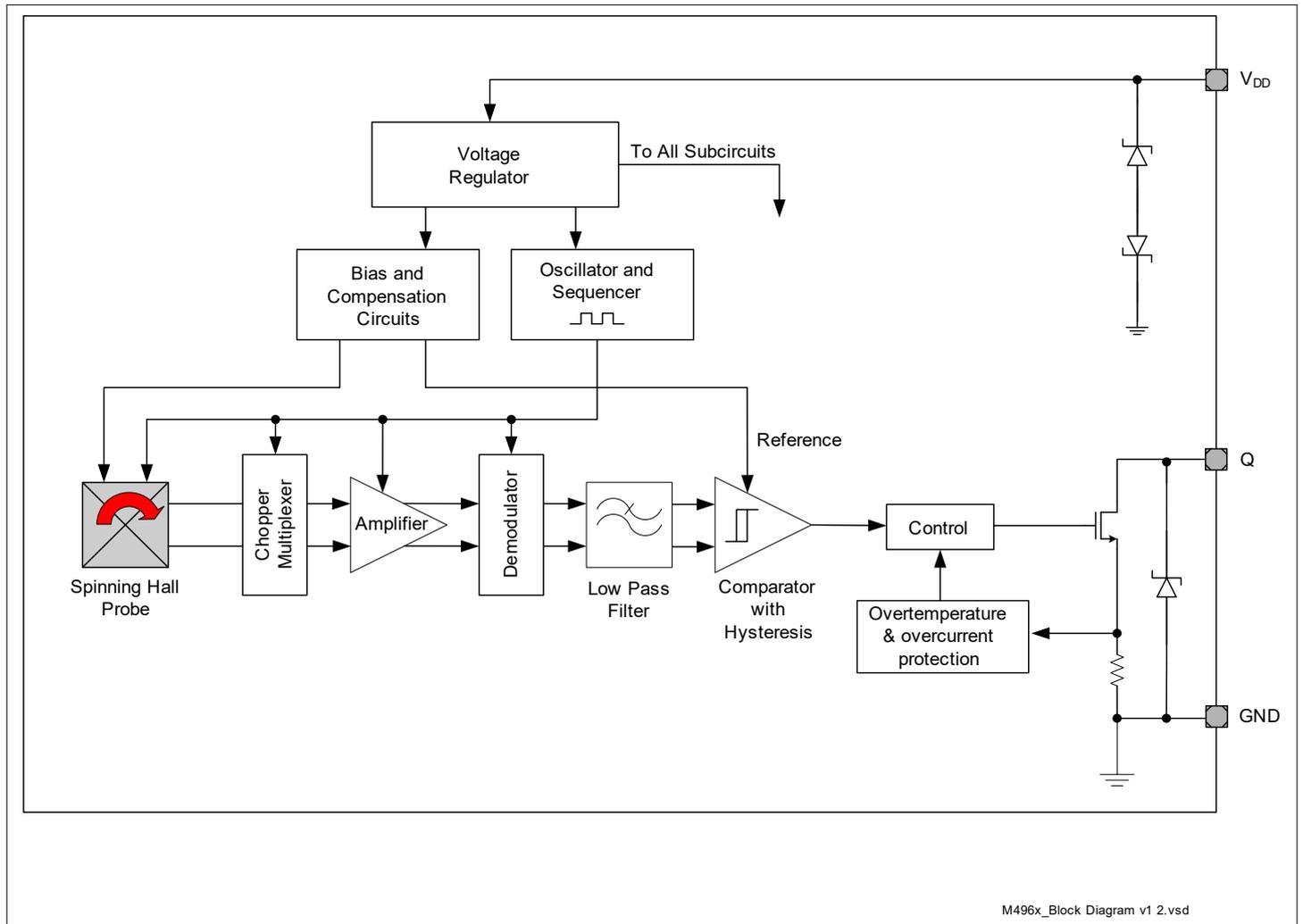
**Figure 1** Pin configuration and center of sensitive area

### 1.3 Pin description

**Table 3** Pin description PG-SOT23-3-15

Pin no.	Symbol	Function
1	VDD	Supply voltage
2	Q	Output
3	GND	Ground

**1.4 Block diagram**



M496x\_Block Diagram v1 2.vsd

**Figure 2 Functional block diagram TLE4964-1M**

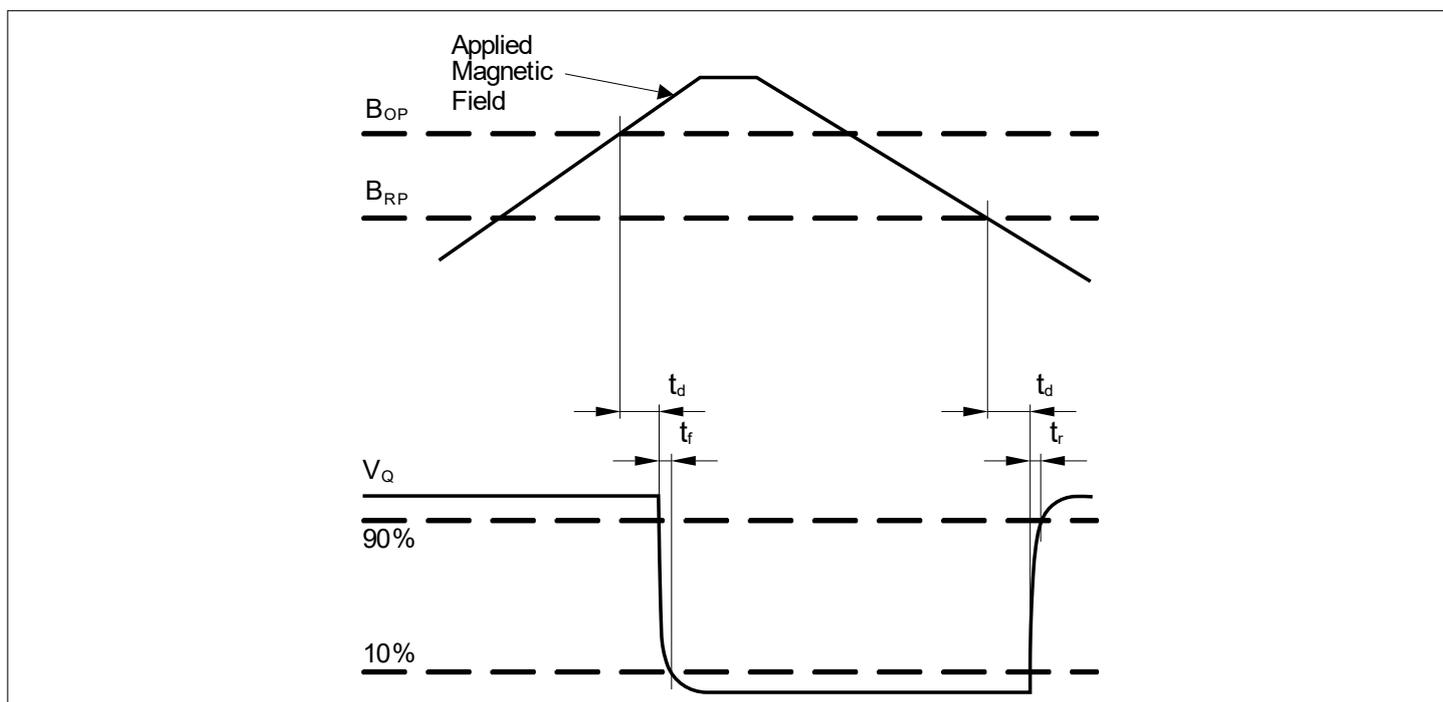
## 1.5 Functional block description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

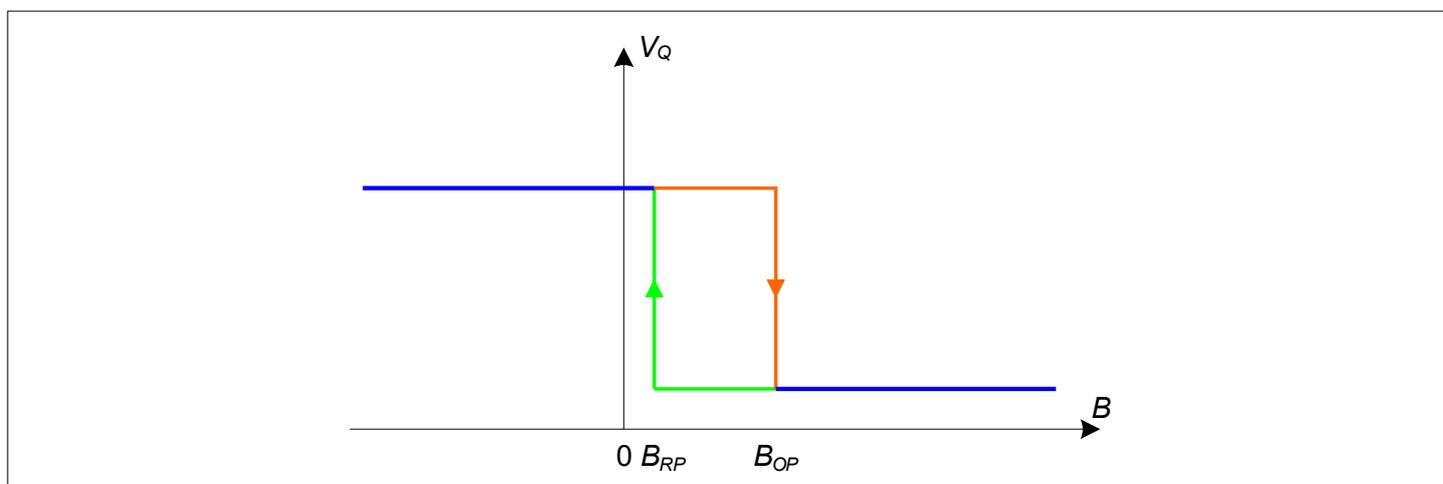
The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.



**Figure 3** Timing diagram TLE4964-1M



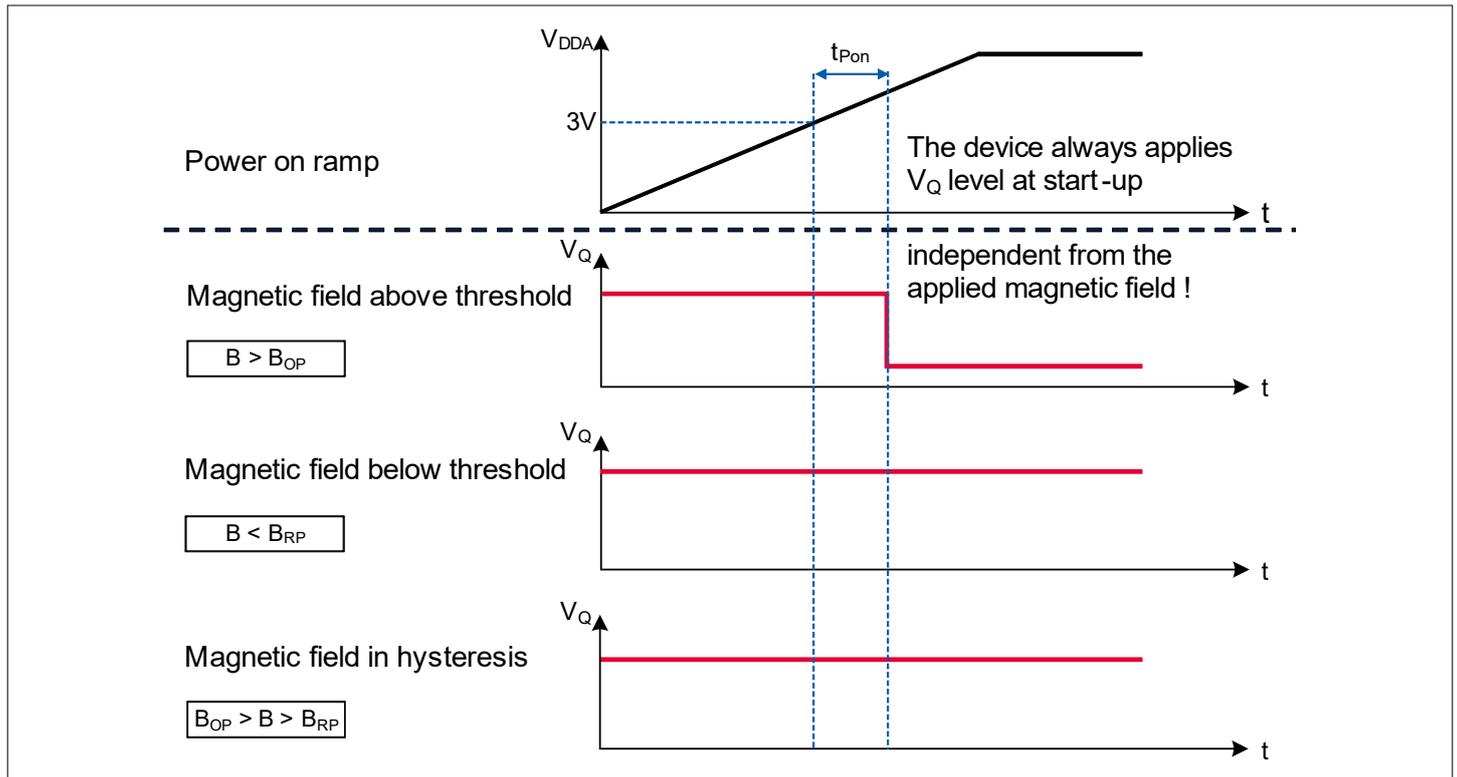
**Figure 4** Output signal TLE4964-1M

### 1.6 Default start-up behavior

The magnetic thresholds exhibit a hysteresis  $B_{HYS} = B_{OP} - B_{RP}$ . In case of a power-on with a magnetic field  $B$  within hysteresis ( $B_{OP} > B > B_{RP}$ ) the output of the sensor is set to the pull up voltage level ( $V_Q$ ) per default. After the first crossing of  $B_{OP}$  or  $B_{RP}$  of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

$V_{DDA}$  is the internal supply voltage which is following the external supply voltage  $V_{DD}$ .

This means for  $B > B_{OP}$  the output is switching, for  $B < B_{RP}$  and  $B_{OP} > B > B_{RP}$  the output stays at  $V_Q$ .



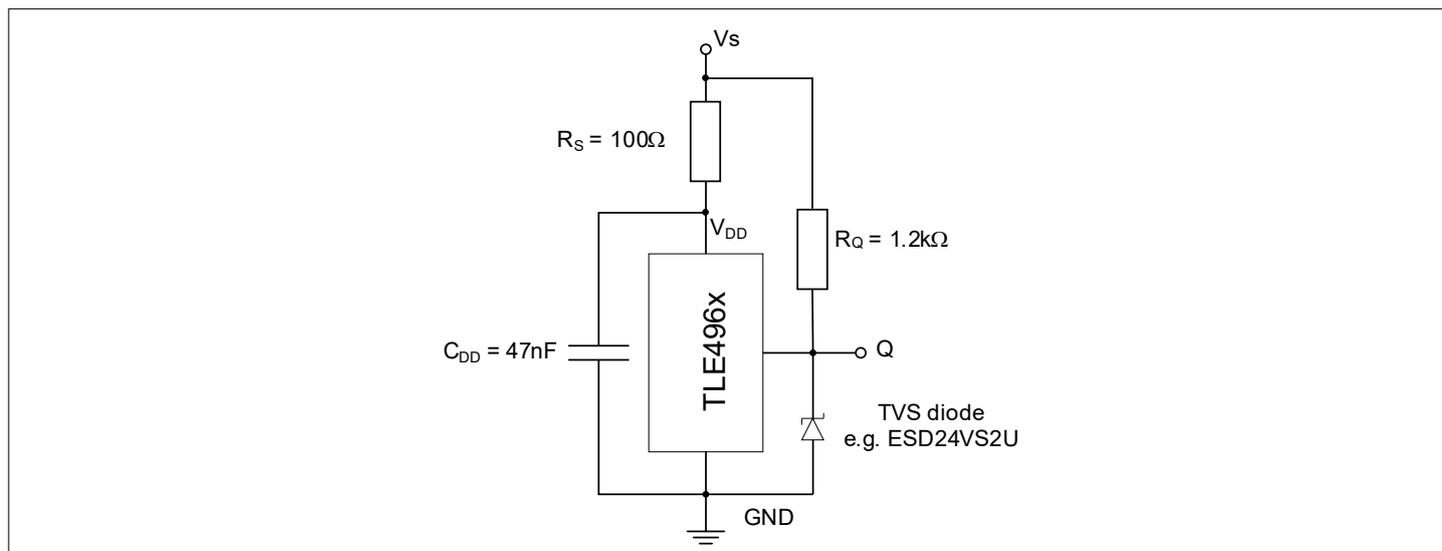
**Figure 5 Start-up behavior of the TLE4964-1M**

## 2 Specification

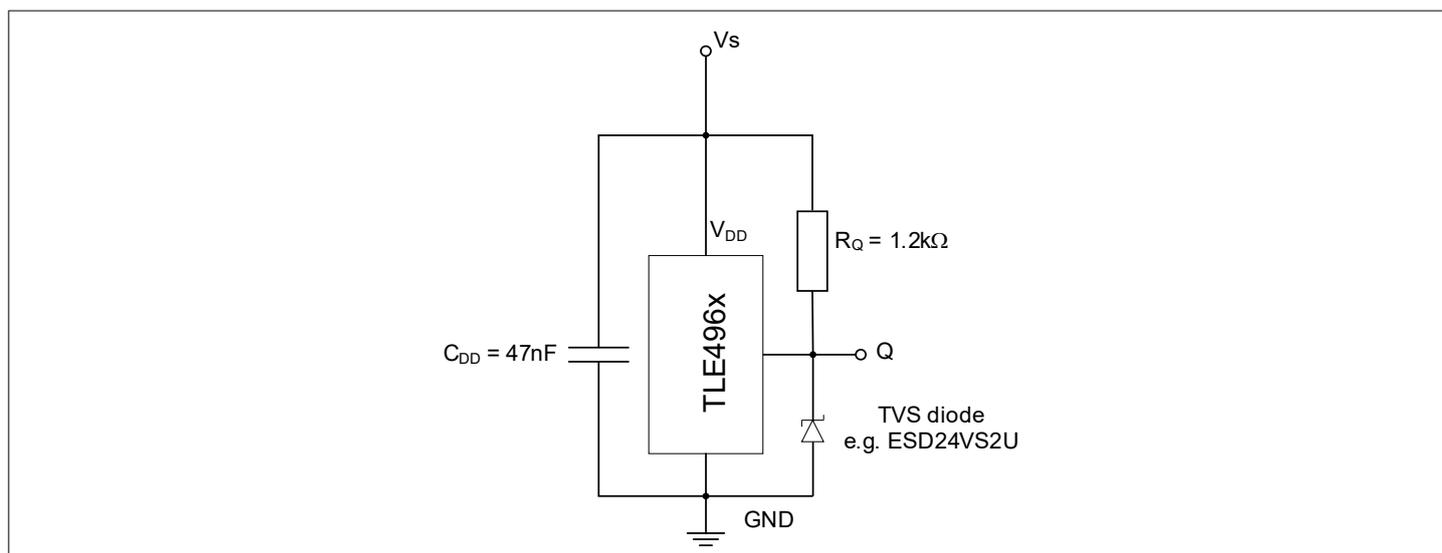
### 2.1 Application circuit

The following [Figure 6](#) shows one option of an application circuit. As explained above the resistor  $R_S$  can be left out (see [Figure 7](#)). The resistor  $R_Q$  has to be in a dimension to match the applied  $V_S$  to keep  $I_Q$  limited to the operating range of maximum 25 mA.

e.g.:  $V_S = 12\text{ V}$ ;  $I_Q = 12\text{ V}/1200\ \Omega = 10\text{ mA}$



**Figure 6** Application circuit 1: with external resistor



**Figure 7** Application circuit 2: without external resistor

## 2.2 Absolute maximum ratings

**Table 4** Absolute maximum rating parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage <sup>1)</sup>	V <sub>DD</sub>	-18	-	32	V	-
				42		10h, no external resistor required
Output voltage	V <sub>Q</sub>	-0.5	-	32	V	-
Reverse output current	I <sub>Q</sub>	-70	-	-	mA	-
Junction temperature <sup>1)</sup>	T <sub>J</sub>	-40	-	155	°C	for 2000h (not additive)
				165		for 1000h (not additive)
				175		for 168h (not additive)
				195		for 3 x 1h (additive)
Storage temperature	T <sub>S</sub>	-40	-	150	°C	-
Thermal resistance Junction ambient	R <sub>thJA</sub>	-	-	300	K/W	for PG-SOT23-3-15 (2s2p)
Thermal resistance Junction lead	R <sub>thJL</sub>	-	-	100	K/W	for PG-SOT23-3-15

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Calculation of the dissipated power P<sub>DIS</sub> and junction temperature T<sub>J</sub> of the chip (SOT23 example):

e.g. for: V<sub>DD</sub> = 12 V, I<sub>S</sub> = 2.5 mA, V<sub>QSAT</sub> = 0.5 V, I<sub>Q</sub> = 20 mA

Power dissipation: P<sub>DIS</sub> = 12 V x 2.5 mA + 0.5 V x 20 mA = 30 mW + 10 mW = 40 mW

Temperature ΔT = R<sub>thJA</sub> x P<sub>DIS</sub> = 300 K/W x 40 mW = 12 K

For T<sub>A</sub> = 150°C: T<sub>J</sub> = T<sub>A</sub> + ΔT = 150°C + 12 K = 162°C

**Table 5** ESD protection<sup>1)</sup> (T<sub>A</sub> = 25°C)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM) <sup>2)</sup>	V <sub>ESD</sub>	-7	-	7	kV	R = 1.5 kΩ, C = 100 pF

(table continues...)

**Table 5** (continued) ESD protection<sup>1)</sup> ( $T_A = 25^\circ\text{C}$ )

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage (CDM) <sup>3)</sup>	$V_{\text{ESD}}$	-1	–	1	kV	–
ESD voltage (system level) <sup>4)</sup>	$V_{\text{ESD}}$	-15	–	15	kV	with circuit shown in Figure 6 and Figure 7

- 1) Characterization of ESD is carried out on a sample basis, not subject to production test.  
 2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.  
 3) Charge device model (CDM) tests according to JESD22-C101.  
 4) Gun test (2 k $\Omega$  / 330 pF or 330  $\Omega$  / 150 pF) according to ISO 10605-2008.

### 2.3 Operating range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4964-1M. All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned. The maximum tested magnetic field is 600 mT.

**Table 6** Operating conditions parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{\text{DD}}$	3.0	–	32 <sup>1)</sup>	V	–
Output voltage	$V_{\text{Q}}$	-0.3	–	32	V	–
Junction temperature	$T_{\text{J}}$	-40	–	170	$^\circ\text{C}$	–
Output current	$I_{\text{Q}}$	0	–	25	mA	–
Magnetic signal input frequency <sup>2)</sup>	$f_{\text{SW}}$	0	–	10	kHz	–

- 1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.  
 2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3dB corner frequency of the internal low-pass filter in the signal path.

### 2.4 Electrical and magnetic characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to  $V_{\text{DD}} = 12\text{ V}$  and  $T_A = 25^\circ\text{C}$ . The below listed specification is valid in combination with the application circuit shown in Figure 6 and Figure 7.

**Table 7** General electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply current	$I_{\text{S}}$	1.1	1.6	2.5	mA	–
Reverse current	$I_{\text{SR}}$	–	0.05	1	mA	for $V_{\text{DD}} = -18\text{ V}$

(table continues...)

**Table 7 (continued) General electrical characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output saturation voltage	V <sub>QSAT</sub>	-	0.2	0.5	V	I <sub>Q</sub> = 20 mA
		-	0.24	0.6	V	I <sub>Q</sub> = 25 mA
Output leakage current	I <sub>QLEAK</sub>	-	-	10	μA	-
Output current limitation	I <sub>QLIMIT</sub>	30	56	70	mA	internally limited and thermal shutdown
Output fall time <sup>1)</sup>	t <sub>f</sub>	0.17	0.4	1	μs	1.2 kΩ / 50 pF, see Figure 3
Output rise time <sup>1)</sup>	t <sub>r</sub>	0.4	0.5	1	μs	1.2 kΩ / 50 pF, see Figure 3
Output jitter <sup>1) 2)</sup>	t <sub>QJ</sub>	-	0.35	1	μs	for square wave signal with 1 kHz
Delay time <sup>1) 3)</sup>	t <sub>d</sub>	12	15	30	μs	see Figure 3
Power-on time <sup>1) 4)</sup>	t <sub>PON</sub>	-	80	150	μs	V <sub>DD</sub> = 3 V, B ≤ B <sub>RP</sub> - 0.5 mT or B ≥ B <sub>OP</sub> + 0.5 mT
Chopper frequency <sup>1)</sup>	f <sub>OSC</sub>	-	350	-	kHz	-

- 1) Not subject to production test, verified by design/characterization.  
2) Output jitter is the 1σ value of the output switching distribution.  
3) Systematic delay between magnetic threshold reached and output switching.  
4) Time from applying V<sub>DD</sub> = 3.0 V to the sensor until the output is valid.

**Table 8 Magnetic characteristics**

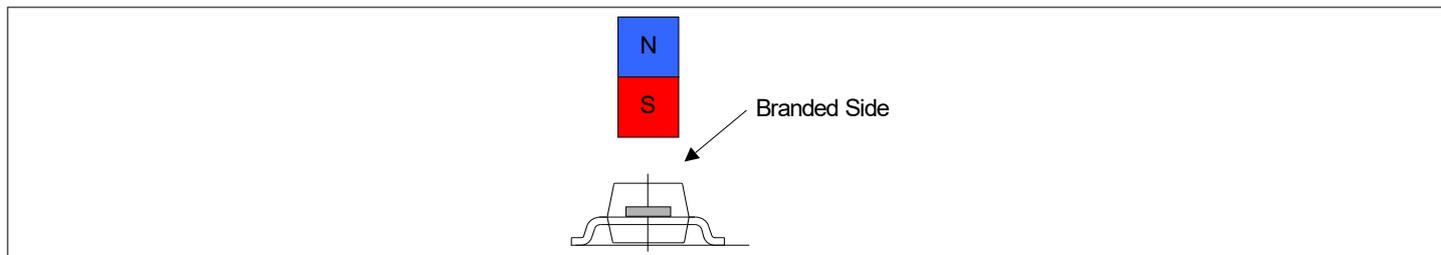
Parameter	Symbol	T (°C)	Values			Unit	Note or Test Condition
			Min.	Typ.	Max.		
Operating point	B <sub>OP</sub>	-40	13.5	19.4	25.3	mT	-
		25	12.5	18.0	23.5		
		170	10.2	14.9	19.6		
Release point	B <sub>RP</sub>	-40	9.1	13.5	17.9	mT	-
		25	8.4	12.5	16.6		
		170	6.7	10.3	13.9		
Hysteresis	B <sub>HYS</sub>	-40	4.4	5.9	8.0	mT	-
		25	4.1	5.5	7.5		
		170	3.4	4.6	6.3		
Effective noise value of the magnetic switching points <sup>1)</sup>	B <sub>Neff</sub>	25	-	62	-	μT	-
Temperature compensation of magnetic thresholds <sup>2)</sup>	T <sub>C</sub>	-	-	-1200	-	ppm/K	-

**2 Specification**

- 1) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents the rms-value and corresponds therefore to a  $1\sigma$  probability of normal distribution. Consequently a  $3\sigma$  value corresponds to 99.7% probability of appearance.
- 2) Not subject to production test, verified by design/characterization.

**Field direction definition**

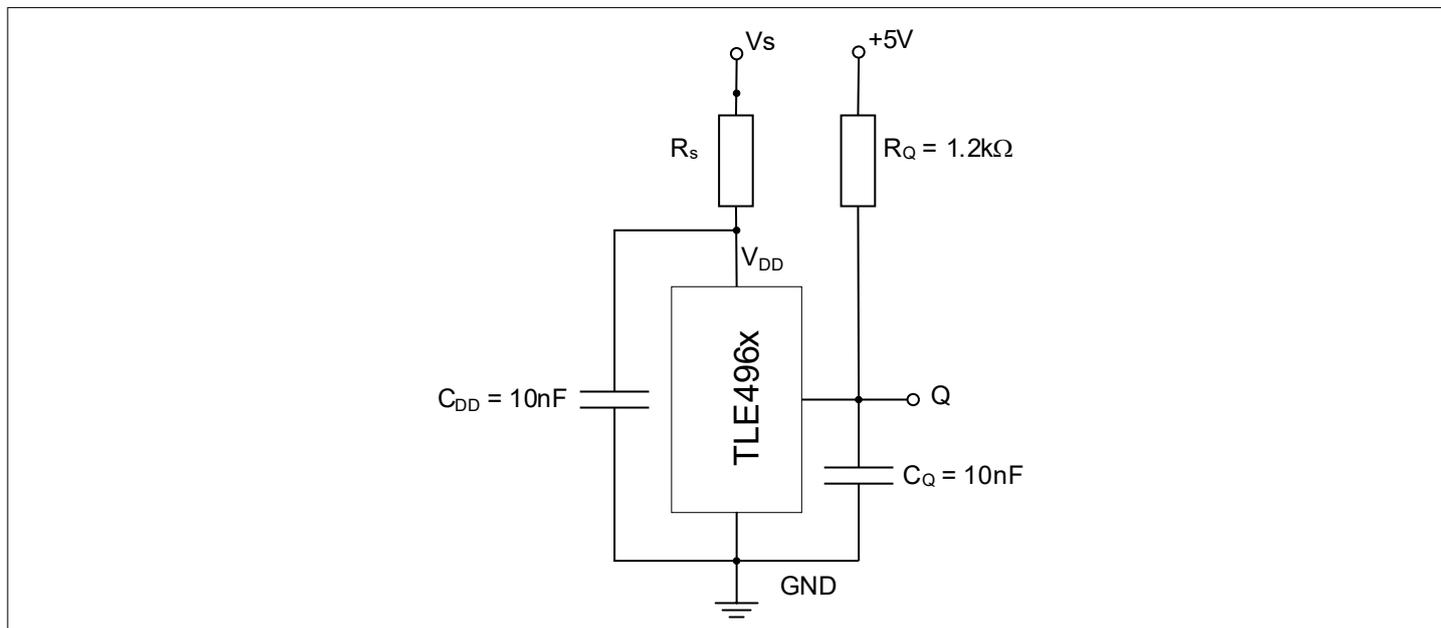
Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.



**Figure 8** Definition of magnetic field direction PG-SOT23-3-15

**2.5 Electro magnetic compatibility**

Characterization of electro magnetic compatibility is carried out on a sample basis from one qualification lot. Not all specification parameters have been monitored during EMC exposure.



**Figure 9** EMC test circuit

Ref: ISO 7637-2 (Version 2004), test circuit [Figure 9](#) (with external resistor,  $R_S = 100\ \Omega$ )

**Table 9** Magnetic compatibility

Parameter	Symbol	Level/Type	Status
Testpulse 1	$V_{EMC}$	-100 V	C
Testpulse 2a <sup>1)</sup>		60 V/110 V	A/C
Testpulse 2b		10 V	C

**(table continues...)**

**Table 9** (continued) **Magnetic compatibility**

Parameter	Symbol	Level/Type	Status
Testpulse 3a		-150 V	A
Testpulse 3b		100 V	A
Testpulse 4 <sup>2)</sup>		-7 V/-5.5 V	A
Testpulse 5b <sup>3)</sup>		$U_S = 86.5 \text{ V}/U_S^* = 28.5 \text{ V}$	A

- 1) ISO 7637-2 (2004) describes internal resistance = 2 Ω (former 10 Ω).  
 2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V ±0.2 V.  
 3) A central load dump protection of 42 V is used.  $U_S^* = 42 \text{ V} - 13.5 \text{ V}$ .

Ref: ISO 7637-2 (Version 2004), test circuit [Figure 9](#) (without external resistor,  $R_S = 0 \text{ Ω}$ )

**Table 10** **Electro magnetic compatibility**

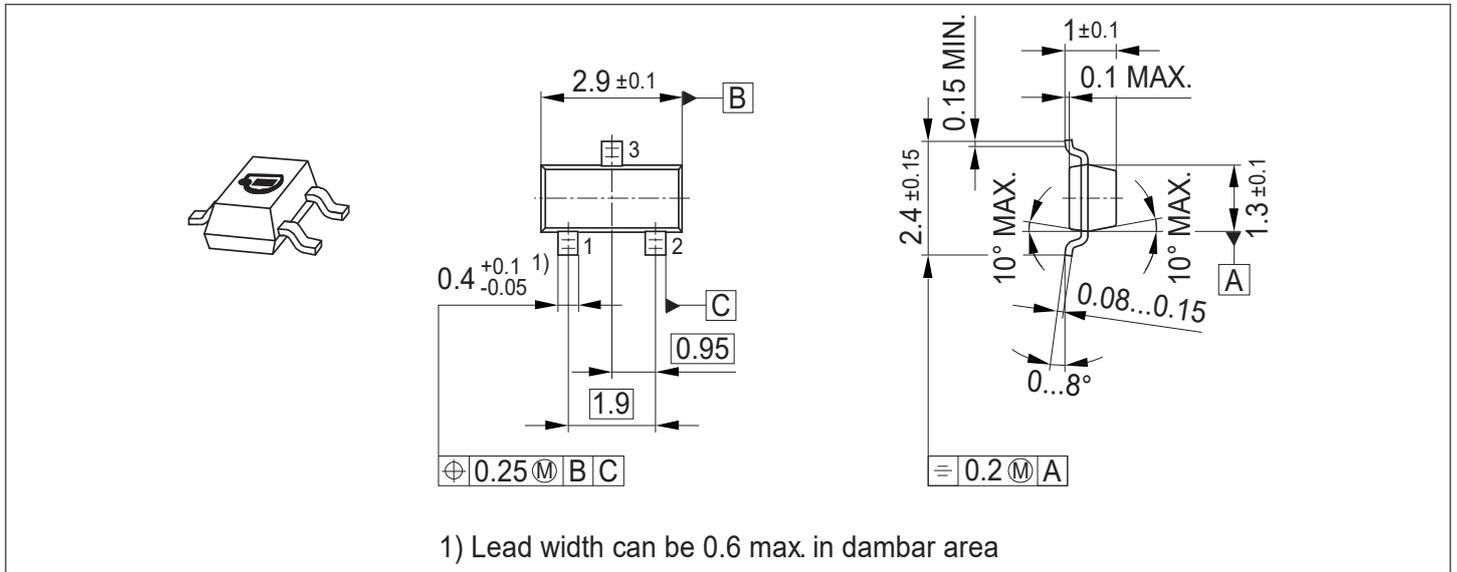
Parameter	Symbol	Level/Type	Status
Testpulse 1	$V_{EMC}$	-50 V	C
Testpulse 2a <sup>1)</sup>		50 V	A
Testpulse 2b		10 V	C
Testpulse 3a		-150 V	A
Testpulse 3b		100 V	A
Testpulse 4 <sup>2)</sup>		-7 V/5.5 V	A
Testpulse 5b <sup>3)</sup>		$U_S = 86.5 \text{ V}/U_S^* = 28.5 \text{ V}$	A

- 1) ISO 7637-2 (2004) describes internal resistance = 2 Ω (former 10 Ω).  
 2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V ±0.2 V.  
 3) A central load dump protection of 42 V is used.  $U_S^* = 42 \text{ V} - 13.5 \text{ V}$ .

### 3 Package information

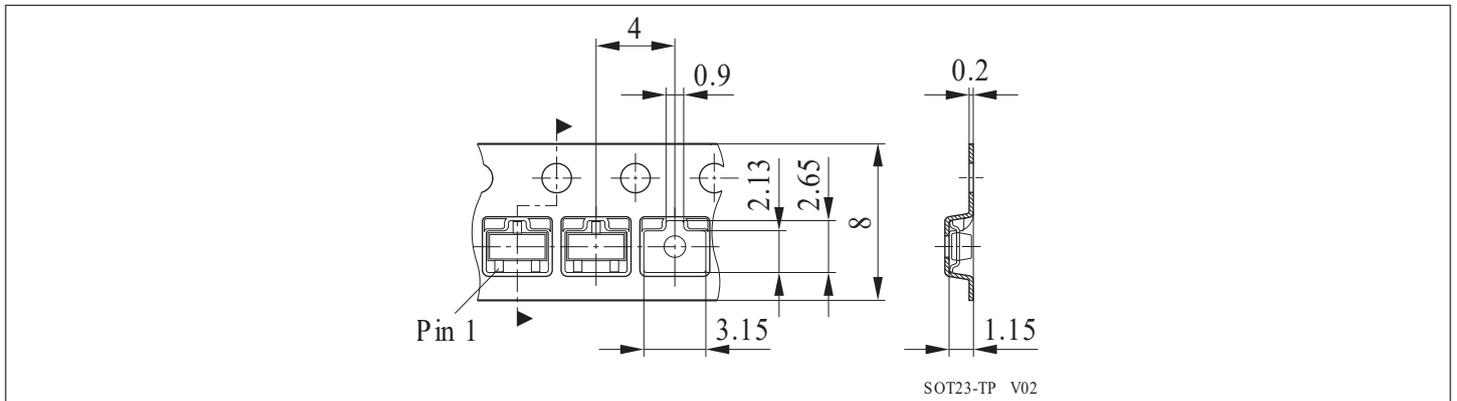
The TLE4964-1M is available in the small halogen-free SMD package PG-SOT23-3-15.

#### 3.1 Package outline PG-SOT23-3-15



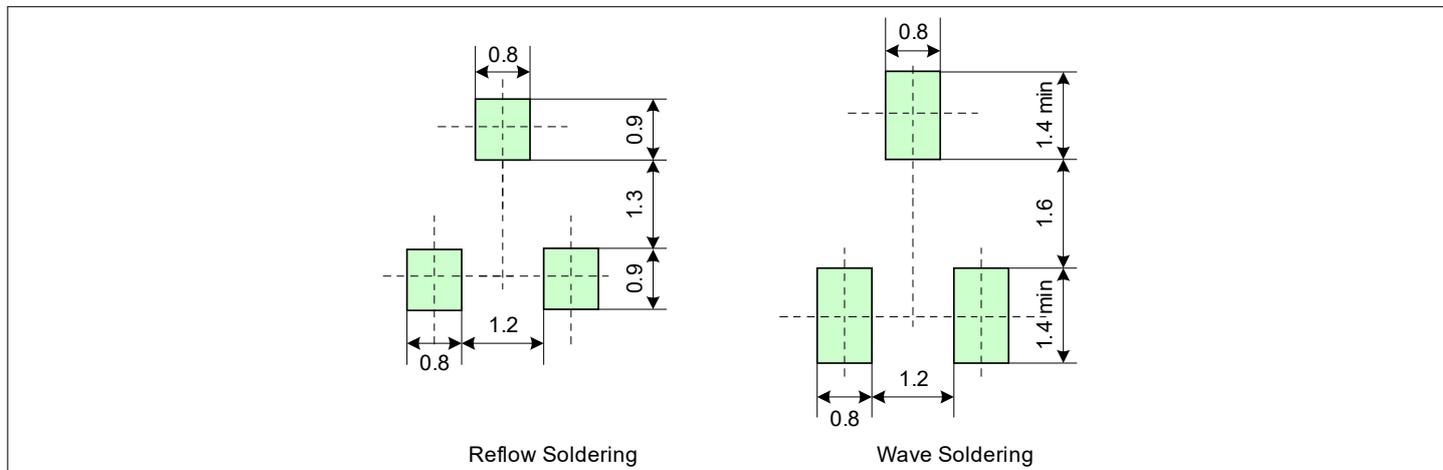
**Figure 10 PG-SOT23-3-15 package outline (all dimensions in mm)**

#### 3.2 Packing information PG-SOT23-3-15



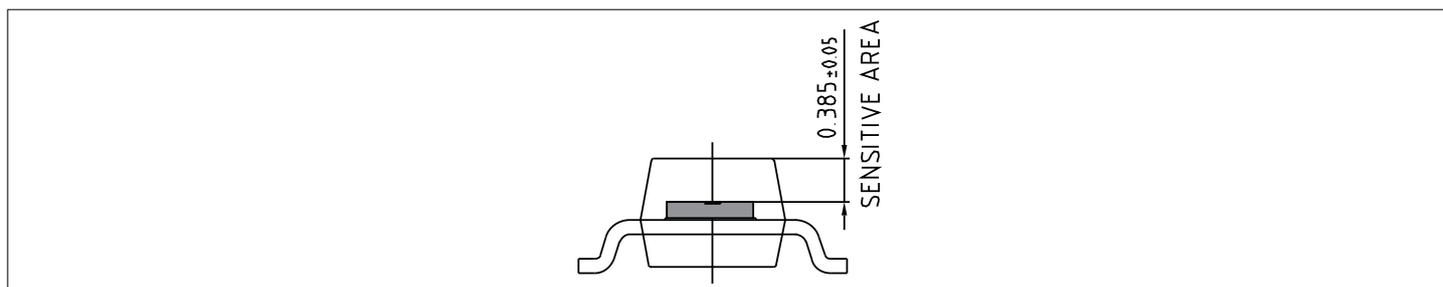
**Figure 11 Packing of the PG-SOT23-3-15 in a tape**

### 3.3 Footprint PG-SOT23-3-15



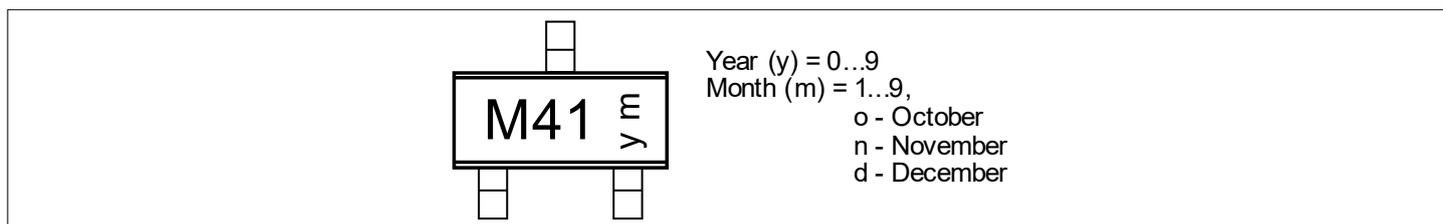
**Figure 12** Footprint PG-SOT23-3-15

### 3.4 PG-SOT23-3-15 distance between chip and package



**Figure 13** Distance between chip and package

### 3.5 Package marking



**Figure 14** Marking of TLE4964-1M

## 4 Graphs of the magnetic parameters

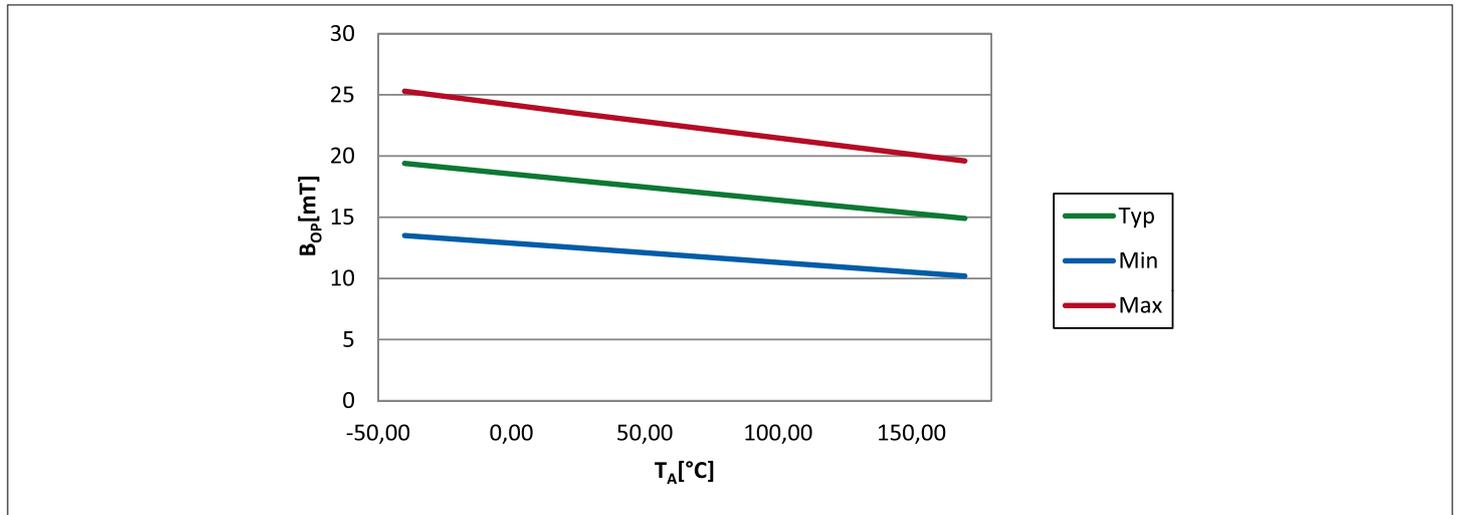


Figure 15 Operating point (B<sub>OP</sub>) of the TLE4964-1M over temperature

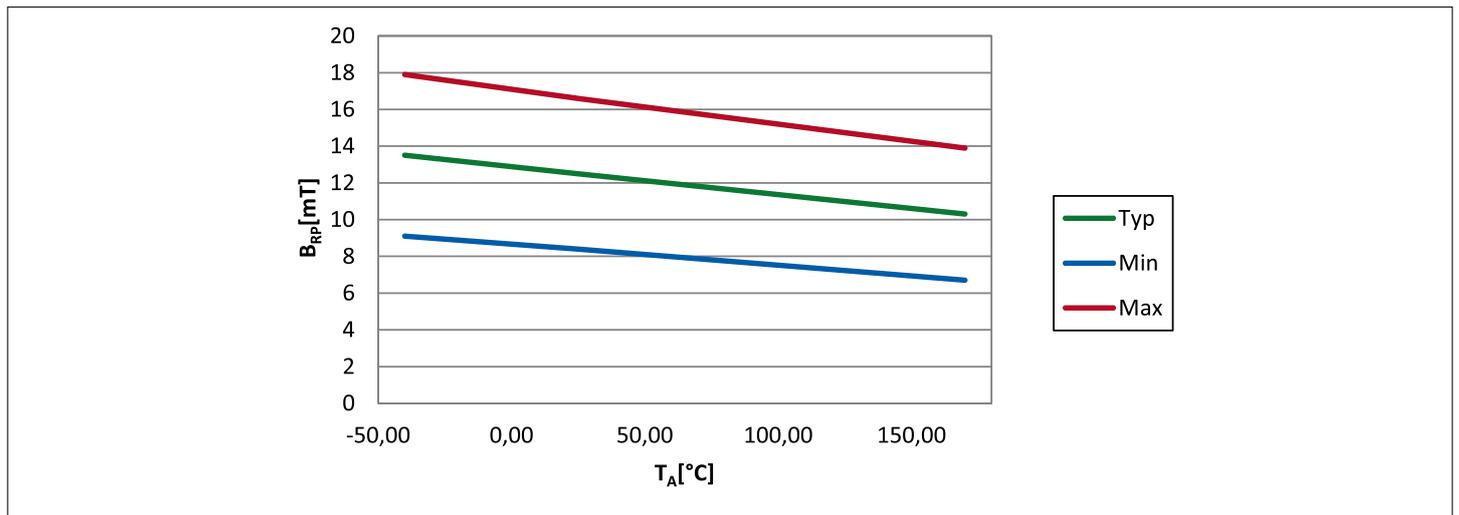


Figure 16 Release point (B<sub>RP</sub>) of the TLE4964-1M over temperature

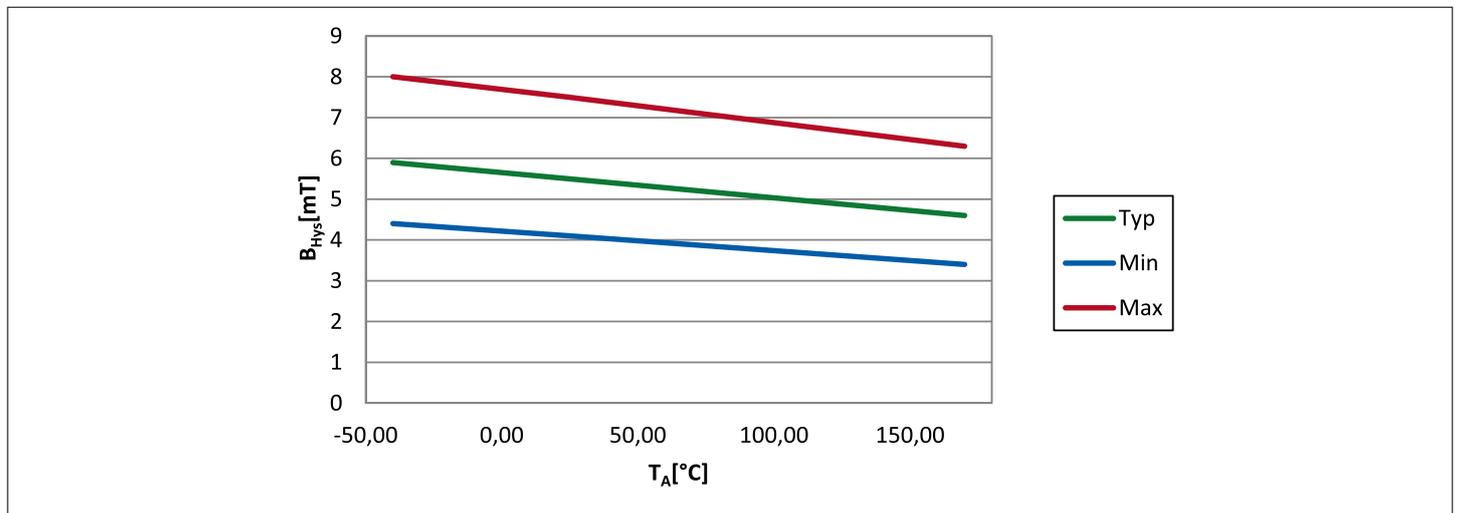
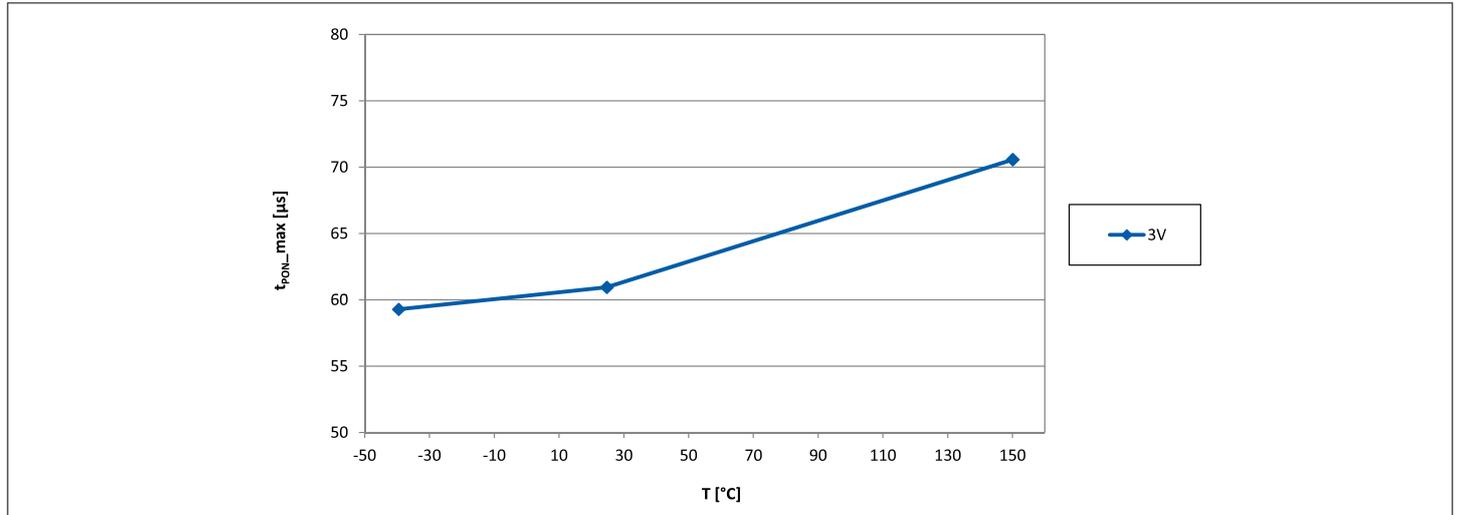
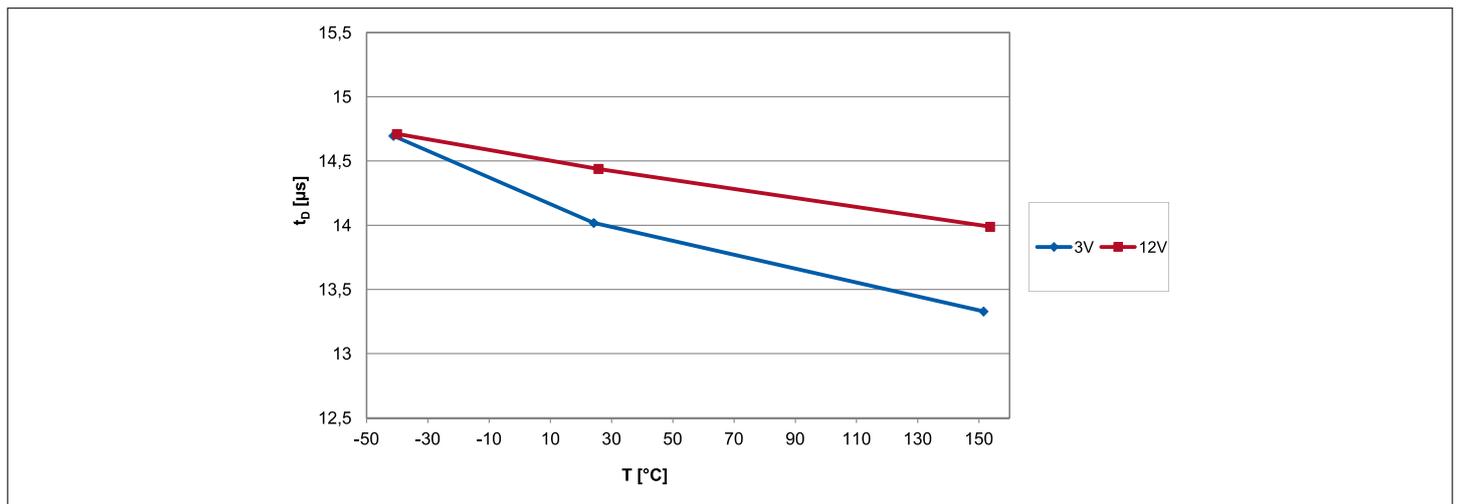


Figure 17 Hysteresis (B<sub>Hys</sub>) of the TLE4964-1M over temperature

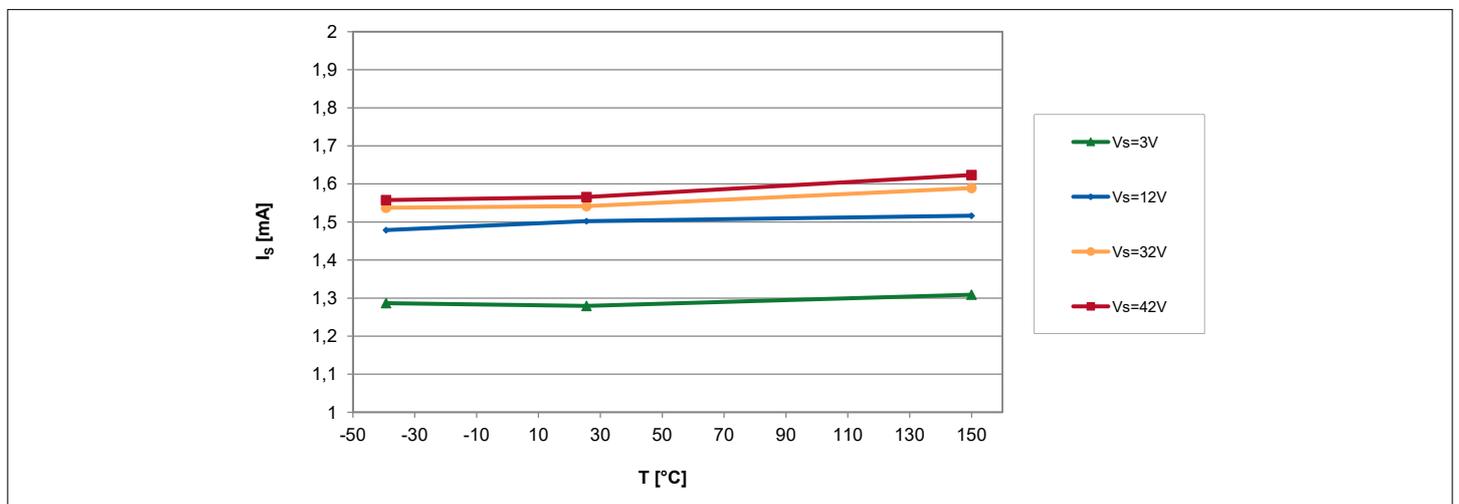
## 5 Graphs of the electrical parameters



**Figure 18** Power on time  $t_{PON}$  of the TLE4964-1M over temperature

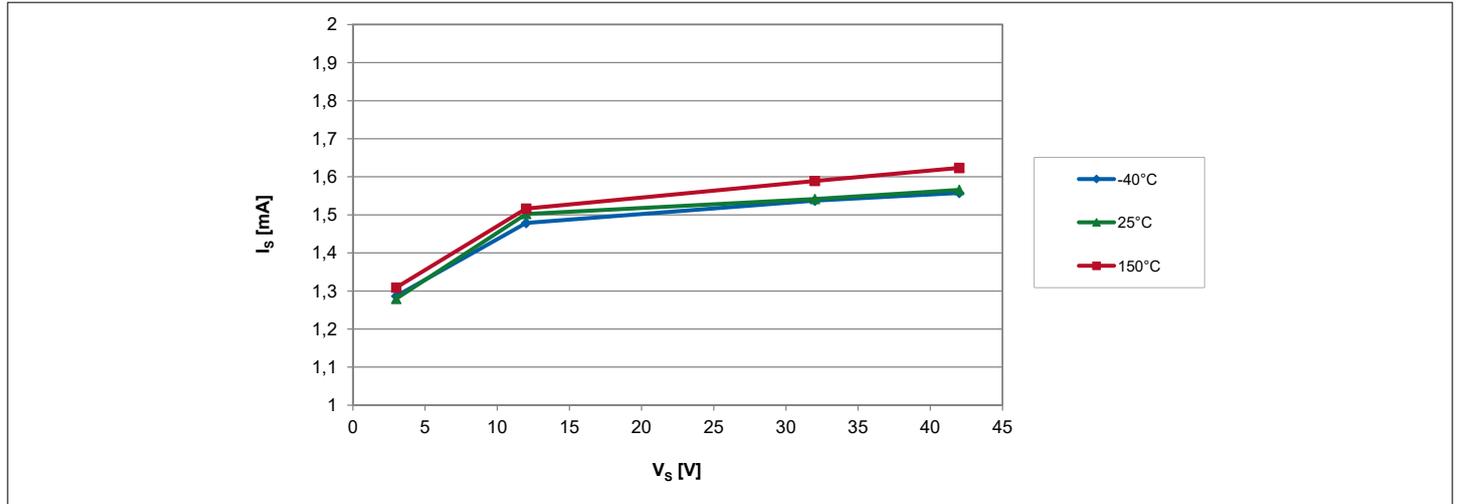


**Figure 19** Signal delay time of the TLE4964-1M over temperature

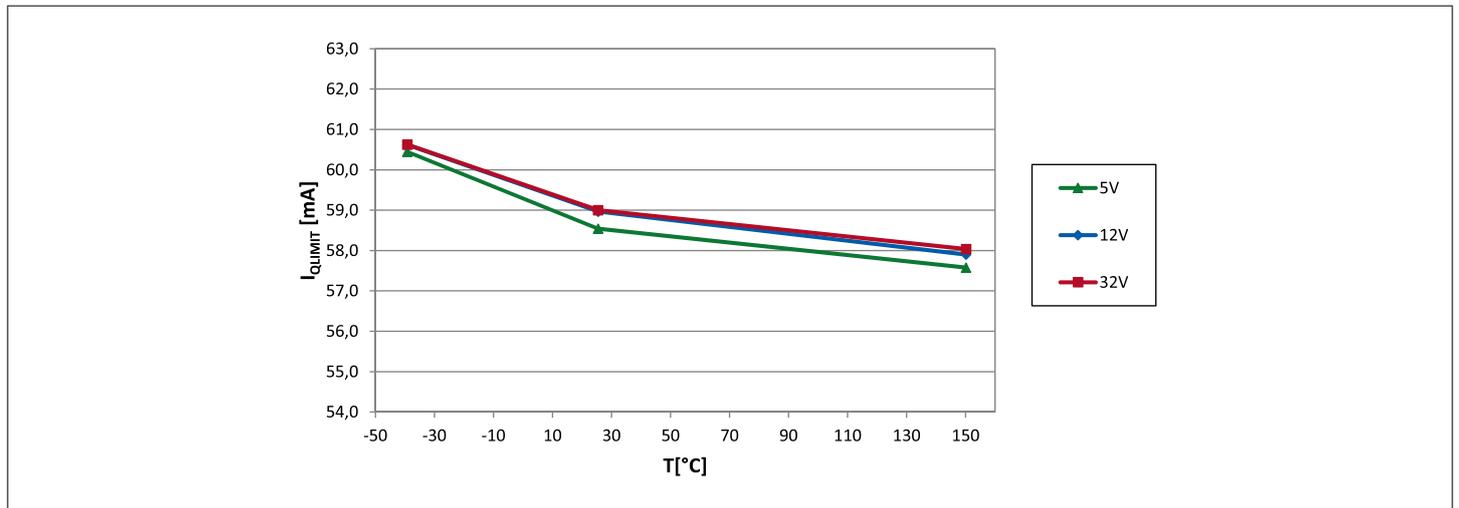


**Figure 20** Supply current of the TLE4964-1M over temperature

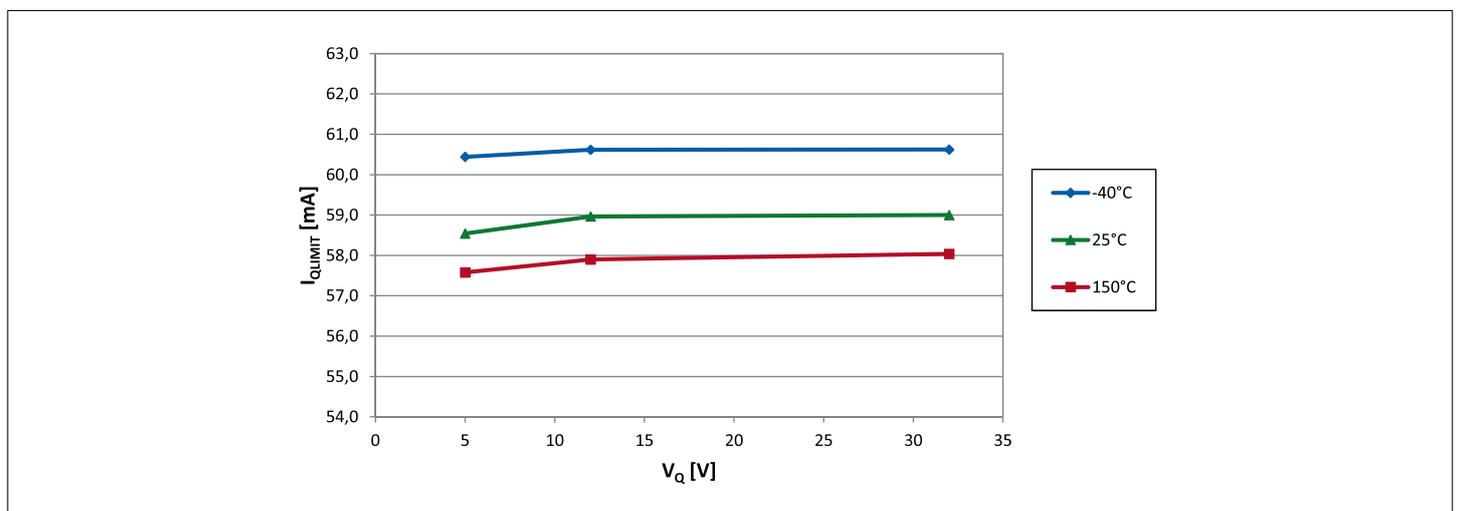
5 Graphs of the electrical parameters



**Figure 21** Supply current of the TLE4964-1M over supply voltage

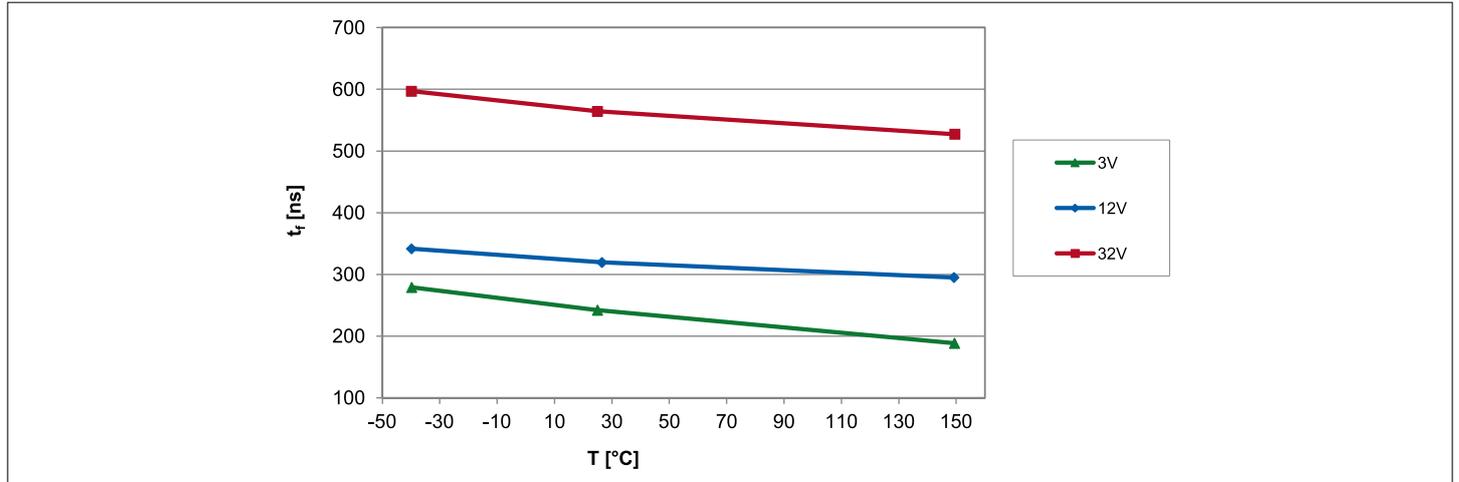


**Figure 22** Output current limit of the TLE4964-1M over temperature

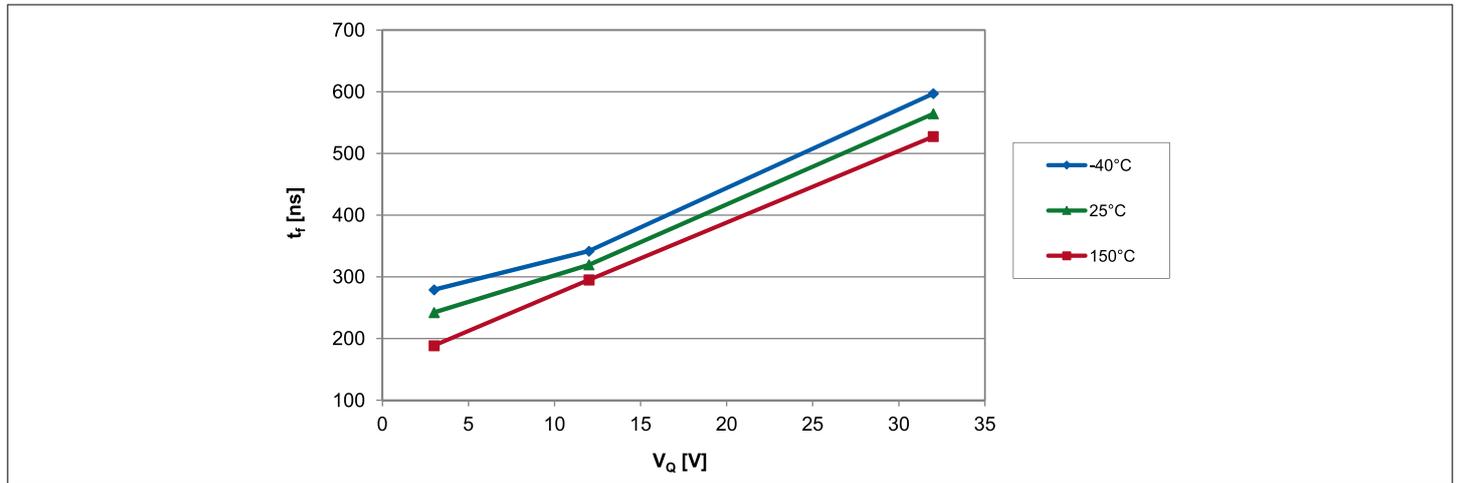


**Figure 23** Output current limit of the TLE4964-1M over applied pull-up voltage

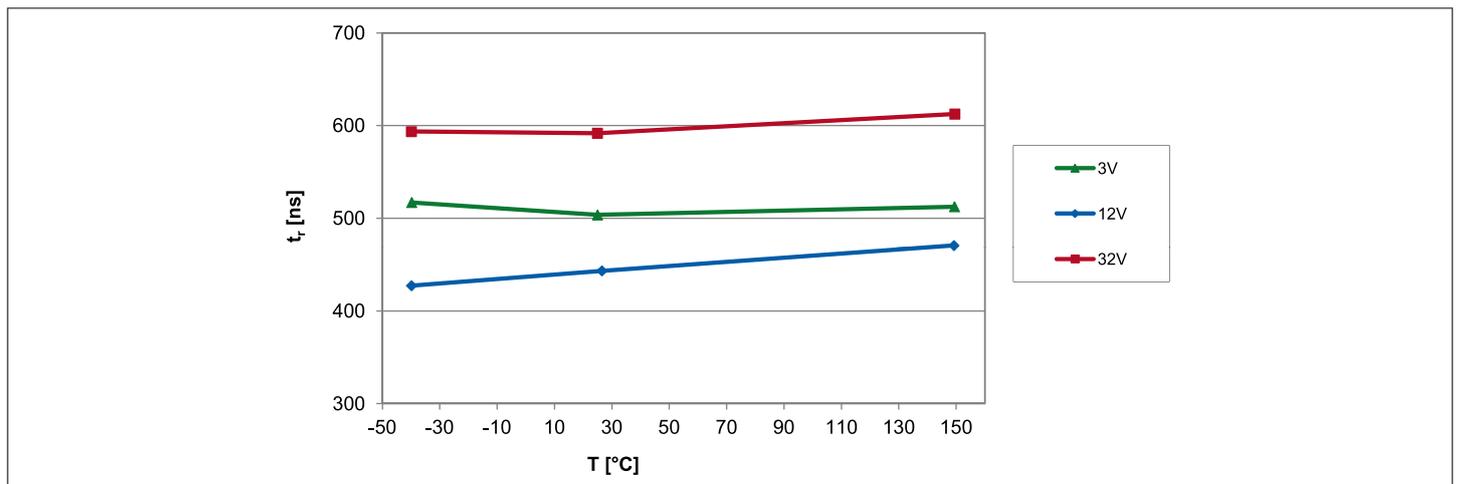
5 Graphs of the electrical parameters



**Figure 24** Output fall time of the TLE4964-1M over temperature

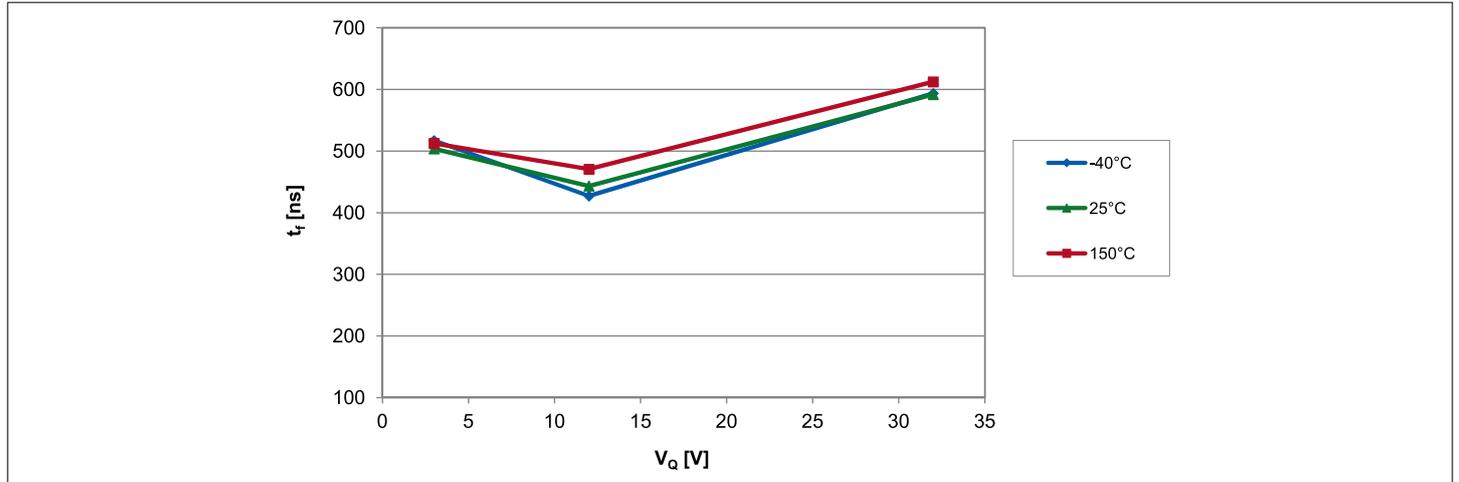


**Figure 25** Output fall time of the TLE4964-1M over applied pull-up voltage

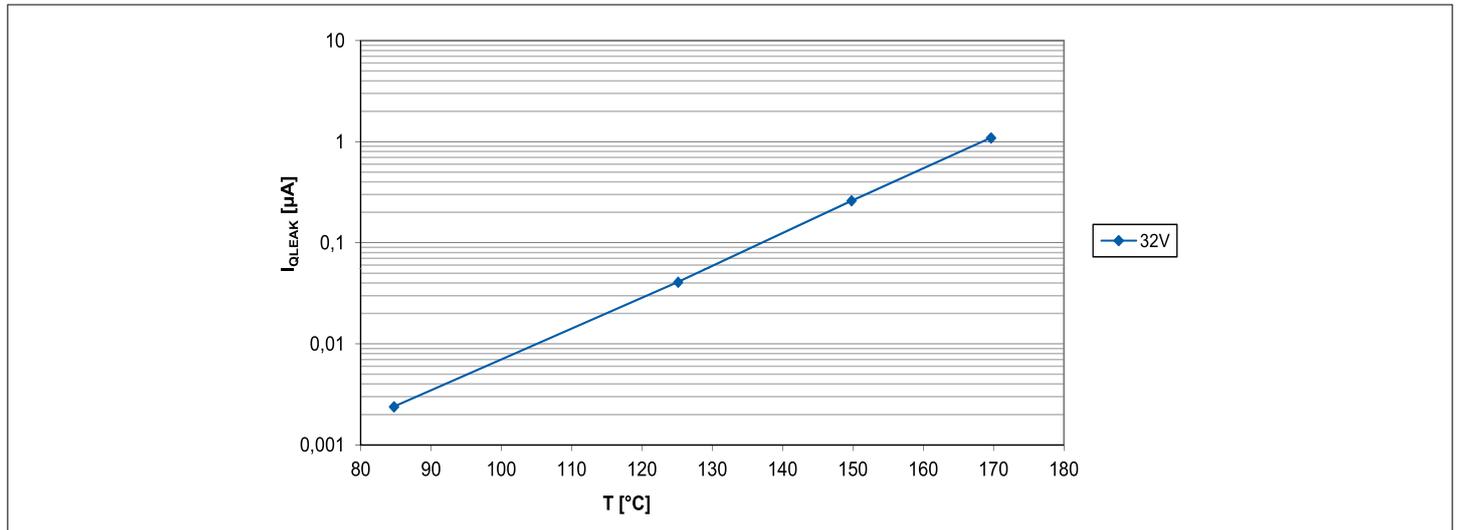


**Figure 26** Output rise time of the TLE4964-1M over temperature

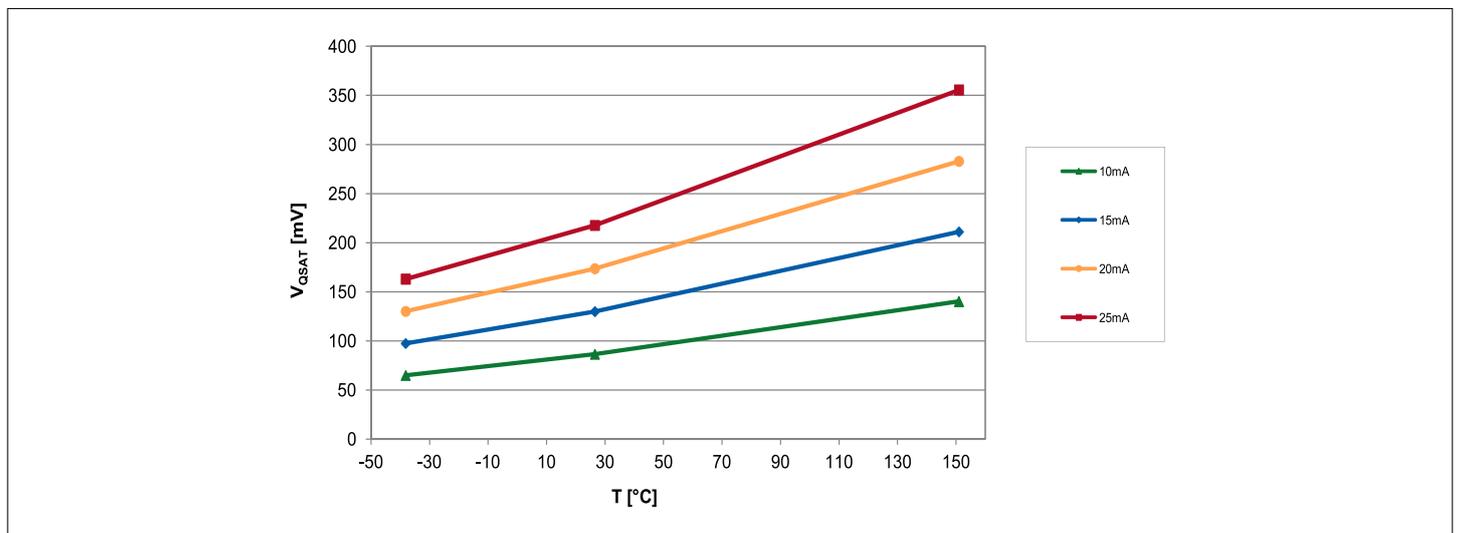
5 Graphs of the electrical parameters



**Figure 27** Output rise time of the TLE4964-1M over applied pull-up voltage

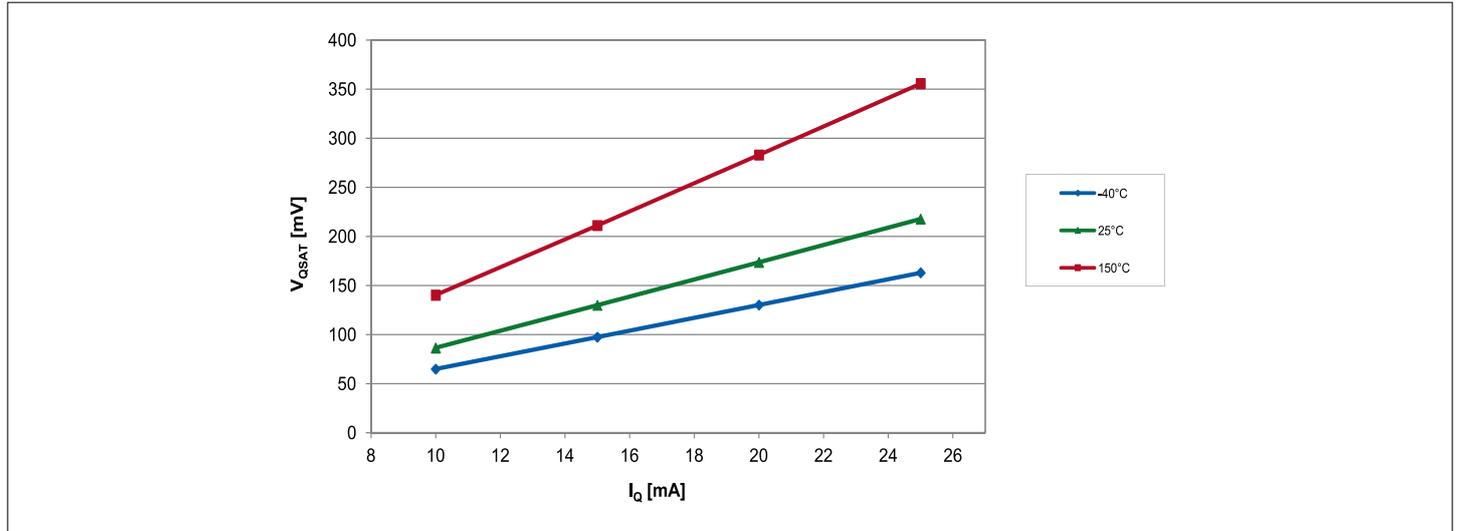


**Figure 28** Output leakage current of the TLE4964-1M over temperature

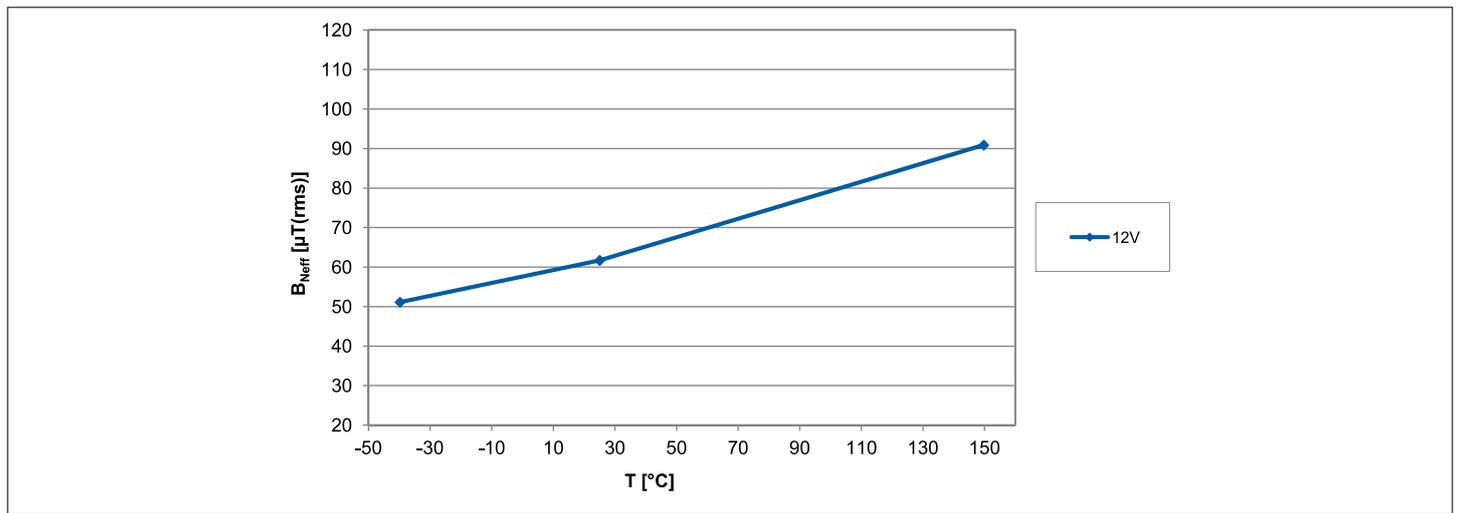


**Figure 29** Saturation voltage of the TLE4964-1M over temperature

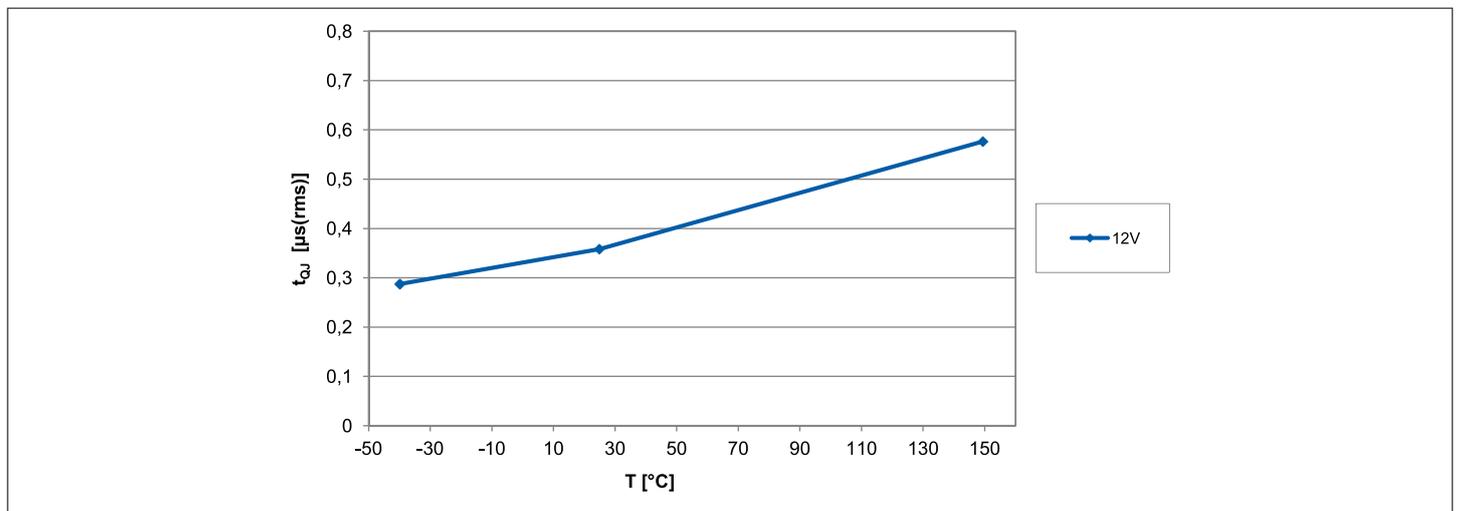
5 Graphs of the electrical parameters



**Figure 30** Saturation voltage of the TLE4964-1M over output current



**Figure 31** Effective noise of the TLE4964-1M thresholds over temperature



**Figure 32** Output signal jitter of the TLE4964-1M over temperature

## Revision history

Document version	Date of release	Description of changes
Revision 1.3	2025-05-20	<ul style="list-style-type: none"><li>Added ordering code SP001328238 (10k) in <a href="#">Ordering information</a></li></ul>
Revision 1.2	2019-12-20	<ul style="list-style-type: none"><li>Updated text and figure in <a href="#">Default start-up behavior</a></li><li>Updated standards in <a href="#">Table 5</a></li><li>Added maximum tested magnetic field in <a href="#">Operating range</a></li><li>Editorial changes</li></ul>
Revision 1.0	2013-07-20	<ul style="list-style-type: none"><li>Initial release</li></ul>

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