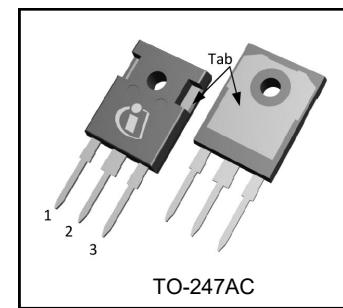
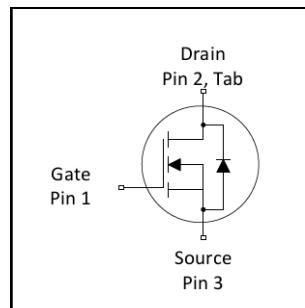


V_{DSS}	60V
R_{DS(on)} typ.	2.1mΩ
max.	2.5mΩ
I_D (Silicon Limited)	270A①
I_D (Package Limited)	195A



Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and di/dt Capability
- Lead-Free

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP3006PbF	TO-247AC	Tube	25	IRFP3006PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	270①	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V(Silicon Limited)	190①	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Wire Bond Limited)	195	
I _{DM}	Pulsed Drain Current ②	1080	
P _D @ T _C = 25°C	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	10	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf.in (1.1N.m)	

Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	320	mJ
I _{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E _{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑧	—	0.4	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface	0.24	—	
R _{θJA}	Junction-to-Ambient	—	40	

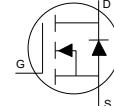
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5\text{mA}$ ②
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	2.1	2.5	$\text{m}\Omega$	$V_{GS} = 10\text{V}$, $I_D = 170\text{A}$ ⑤
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
		—	—	-100		$V_{GS} = -20\text{V}$
R_G	Internal Gate Resistance	—	2.0	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

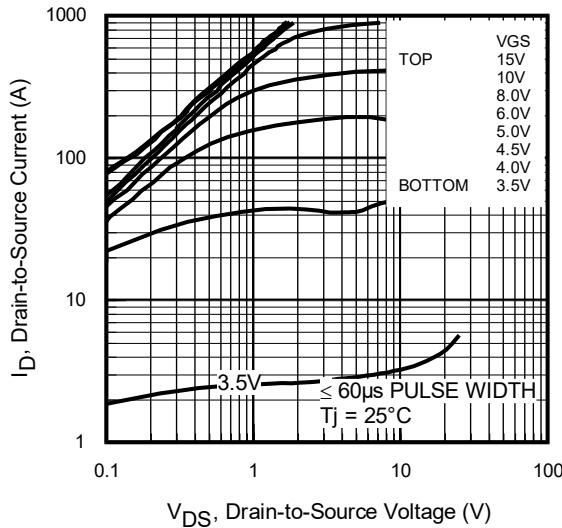
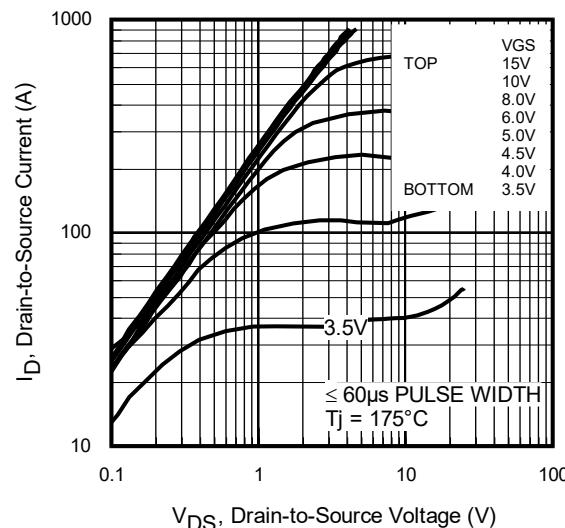
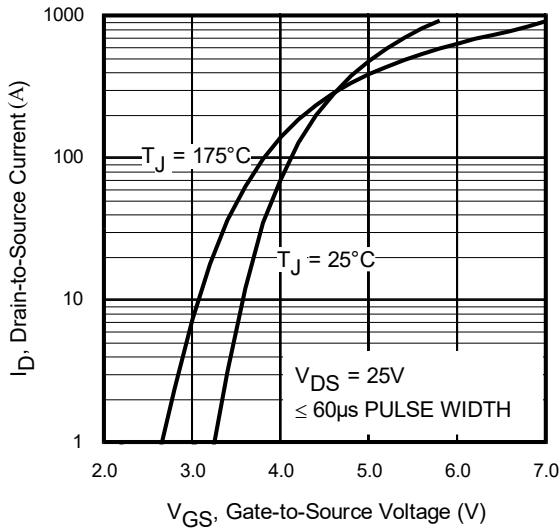
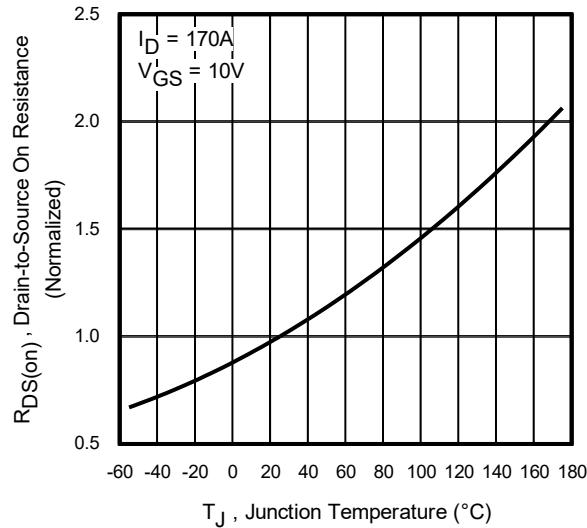
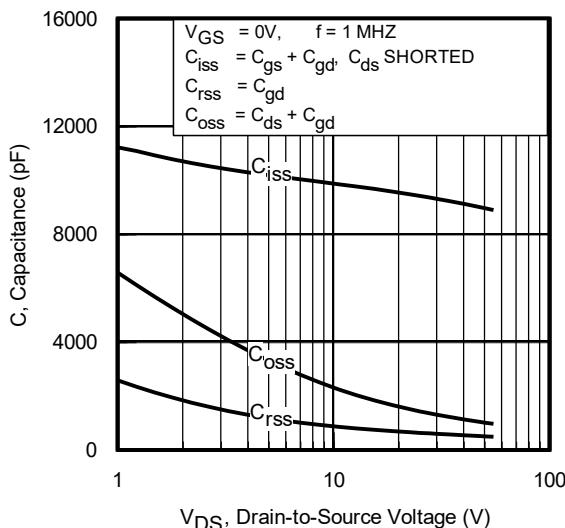
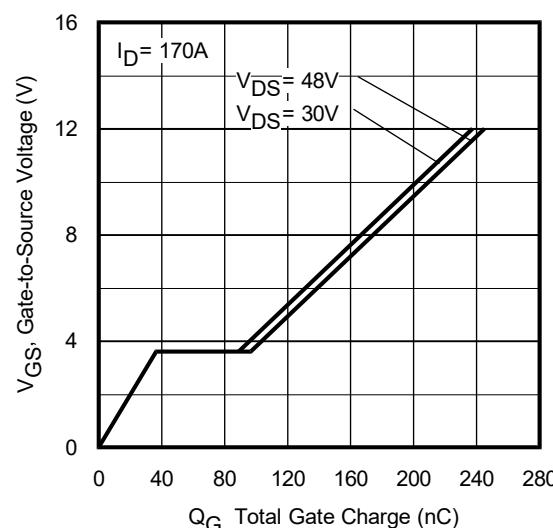
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	280	—	—	S	$V_{DS} = 25\text{V}$, $I_D = 170\text{A}$
Q_g	Total Gate Charge	—	200	300	nC	$I_D = 170\text{A}$
Q_{gs}	Gate-to-Source Charge	—	37	—		$V_{DS} = 30\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	60	—		$V_{GS} = 10\text{V}$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	140	—		$I_D = 170\text{A}$, $V_{DS} = 0\text{V}$, $V_{GS} = 10\text{V}$
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 39\text{V}$
t_r	Rise Time	—	182	—		$I_D = 170\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	118	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	189	—		$V_{GS} = 10\text{V}$ ⑤
C_{iss}	Input Capacitance	—	8970	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output Capacitance	—	1020	—		$V_{DS} = 50\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	534	—		$f = 1.0 \text{ MHz}$, See Fig. 5
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	1480	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 48V ⑦ See Fig. 11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	1920	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 48V ⑧

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	—	—	257 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{sM}	Pulsed Source Current (Body Diode) ②	—	—	1028		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_s = 170\text{A}$, $V_{GS} = 0\text{V}$ ⑤
t_{rr}	Reverse Recovery Time	—	44	—	ns	$T_J = 25^\circ\text{C}$
		—	48	—		$T_J = 125^\circ\text{C}$
Q_{rr}	Reverse Recovery Charge	—	63	—	nC	$T_J = 25^\circ\text{C}$ $V_R = 51\text{V}$
		—	77	—		$T_J = 125^\circ\text{C}$ $I_F = 170\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ ⑤
I_{RRM}	Reverse Recovery Current	—	2.4	—	A	$T_J = 25^\circ\text{C}$

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. Junction temperature.
- ③ Limited by $T_{J\text{max}}$, starting $T_J = 25^\circ\text{C}$, $L = 0.022\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 170\text{A}$, $V_{GS} = 10\text{V}$. Part not Recommended for use above this value.
- ④ $ISD \leq 170\text{A}$, $di/dt \leq 1360\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_0 is measured at T_J approximately 90°C .
- * All spec data and curves based on (TO-220 Pak -IRFB3006PbF) Datasheet.

**Fig 1.** Typical Output Characteristics**Fig 2.** Typical Output Characteristics**Fig 3.** Typical Transfer Characteristics**Fig 4.** Normalized On-Resistance vs. Temperature**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

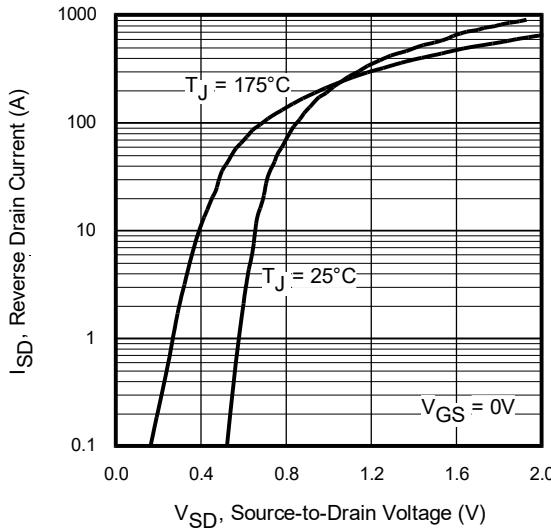


Fig 7. Typical Source-to-Drain Diode Forward Voltage

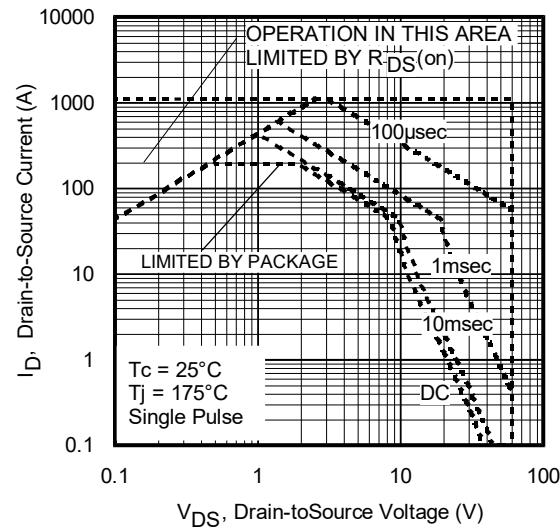


Fig 8. Maximum Safe Operating Area

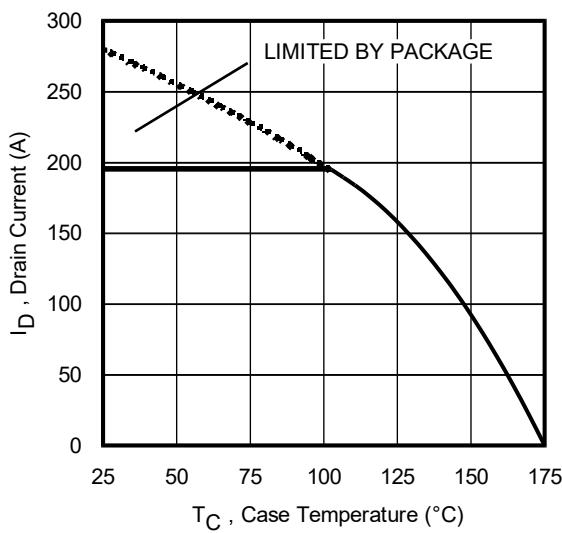


Fig 9. Maximum Drain Current vs. Case Temperature

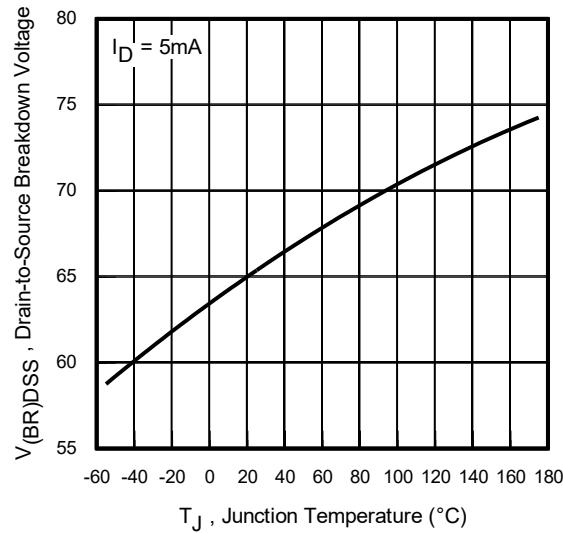


Fig 10. Drain-to-Source Breakdown Voltage

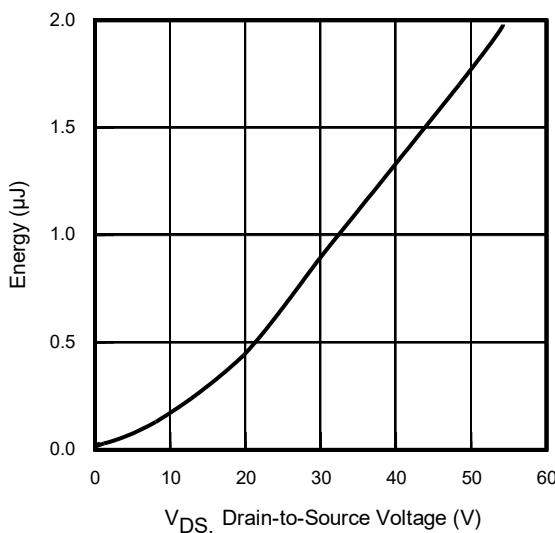


Fig 11. Typical Coss Stored Energy

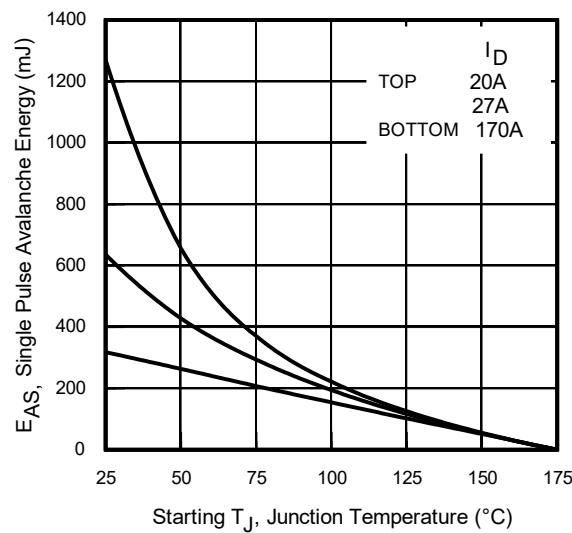


Fig 12. Maximum Avalanche Energy vs. Drain Current

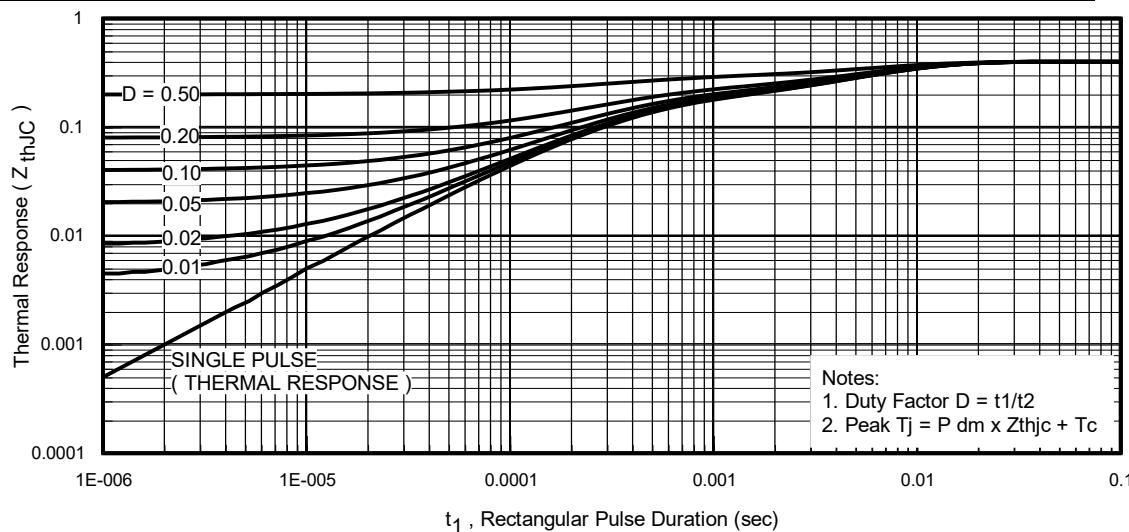


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

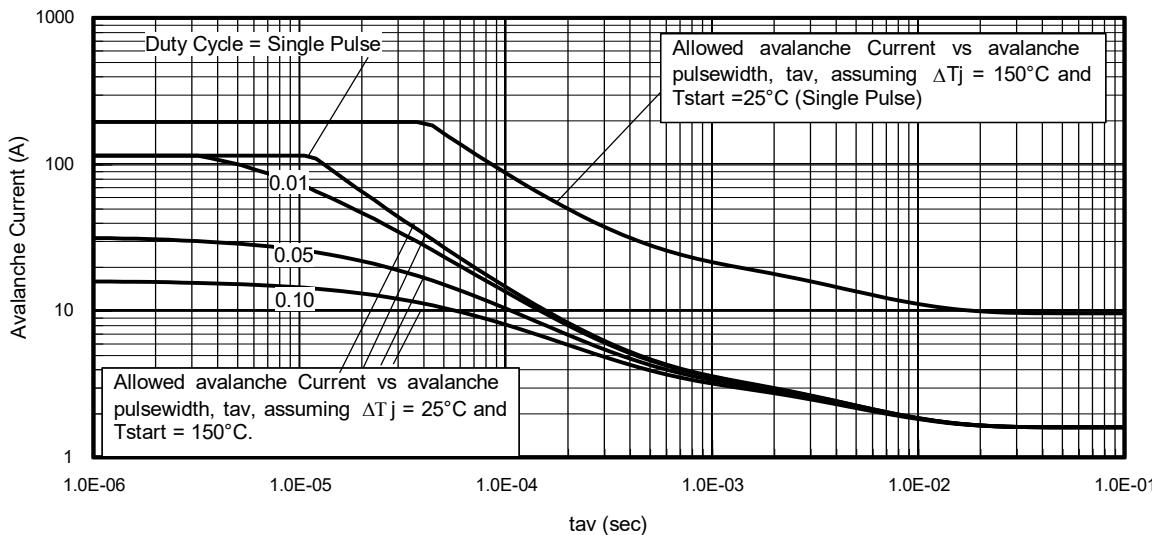
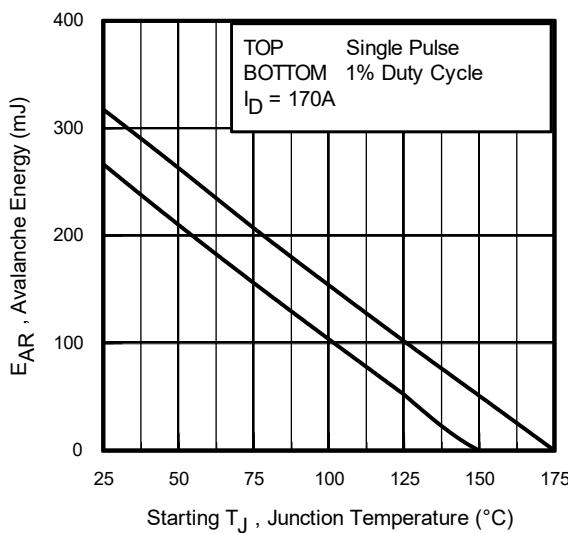


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 14, 15: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
 2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
 3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
 4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
 6. I_{av} = Allowable avalanche current.
 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as $25^\circ C$ in Figure 14, 15).
- t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

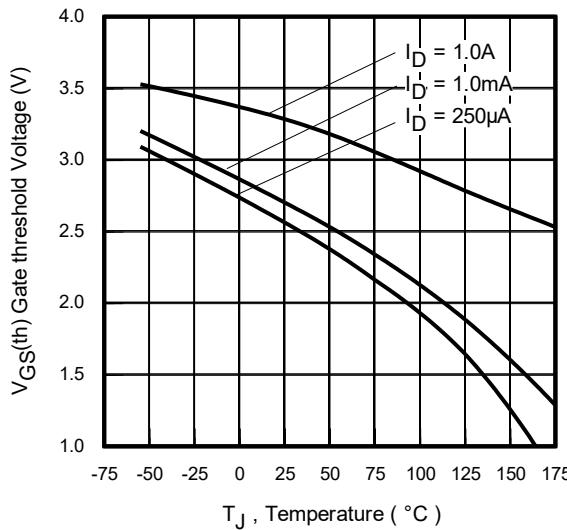
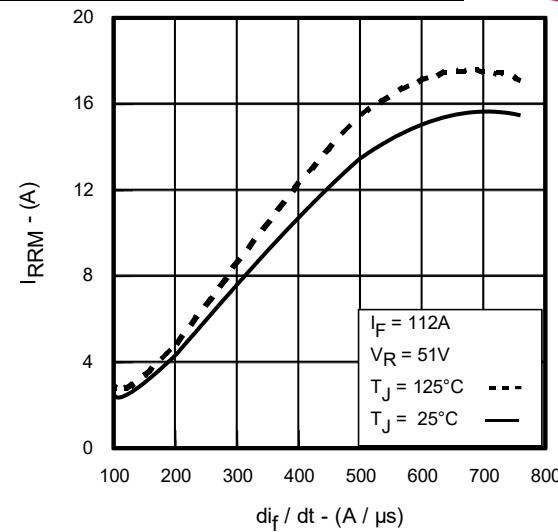
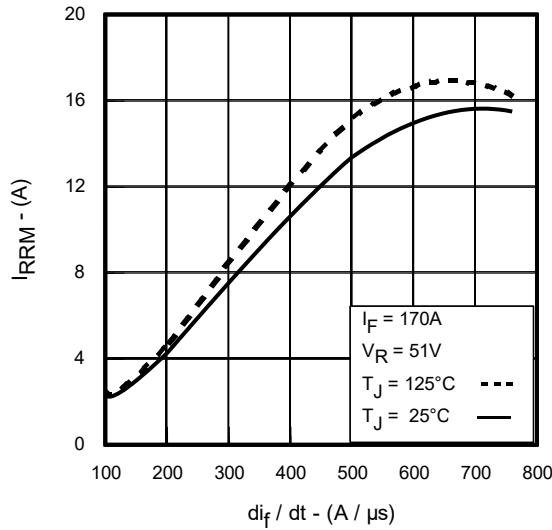
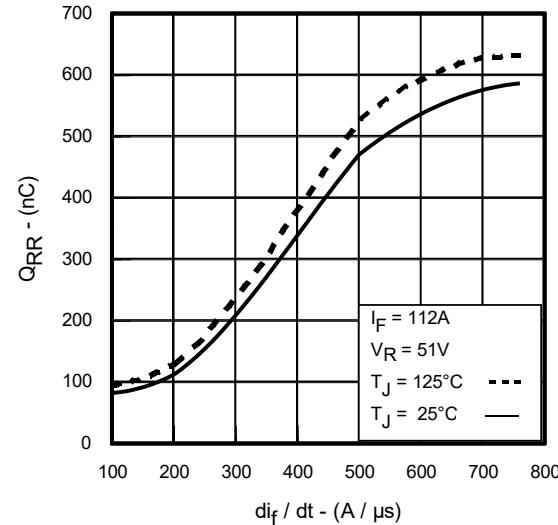
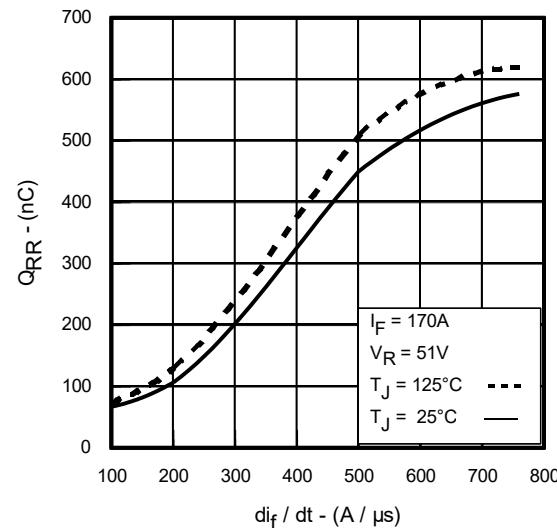
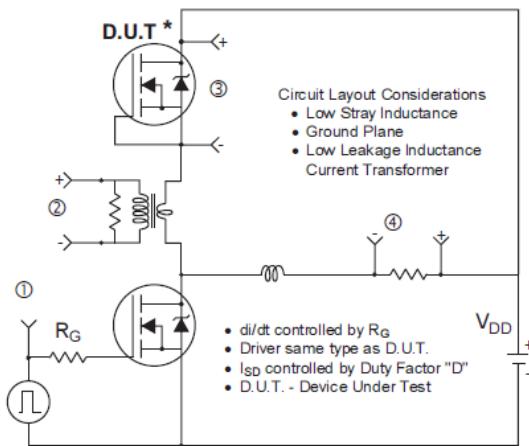
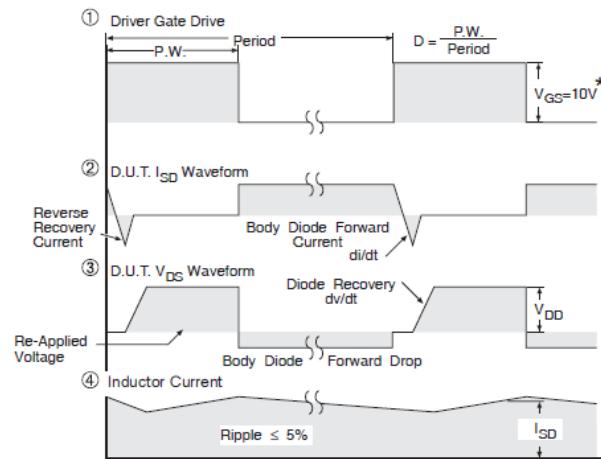


Fig. 16 Threshold Voltage vs. Temperature

Fig. 17 Typical Recovery Current vs. di_f/dtFig 18. Typical Recovery Current vs. di_f/dtFig 19. Typical Stored Charge vs. di_f/dtFig 20. Typical Stored Charge vs. di_f/dt



* Reverse Polarity of D.U.T for P-Channel



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

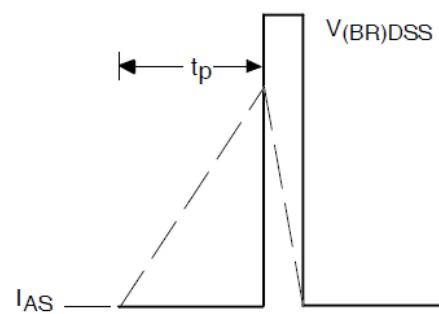
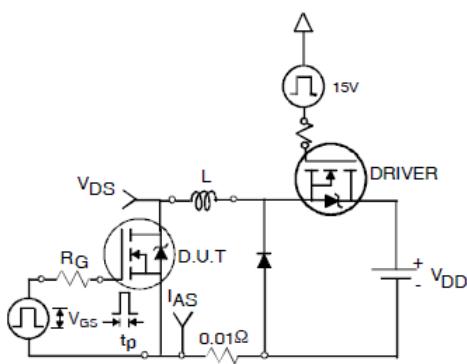


Fig 22a. Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

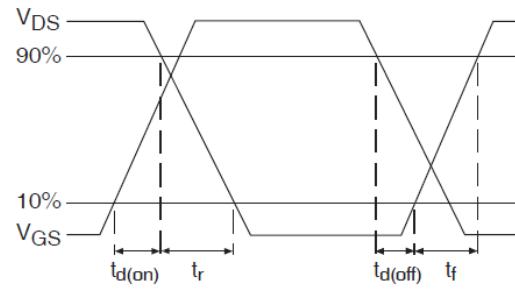
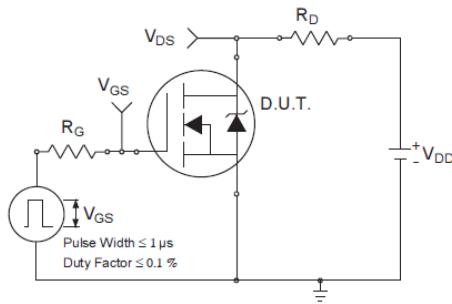


Fig 23a. Switching Time Test Circuit

Fig 23b. Switching Time Waveforms

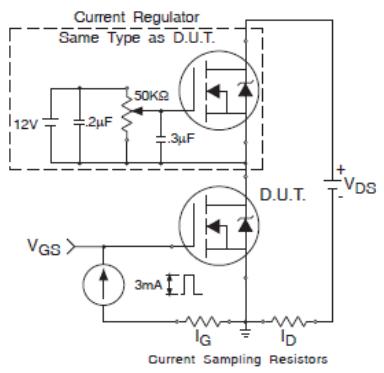


Fig 24a. Gate Charge Test Circuit

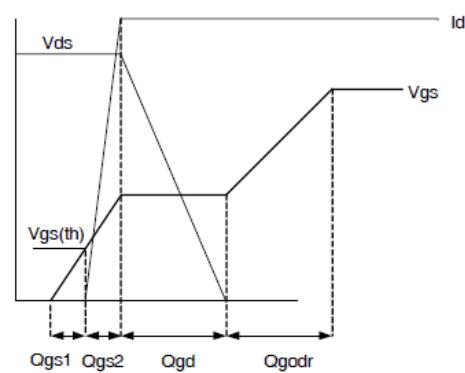
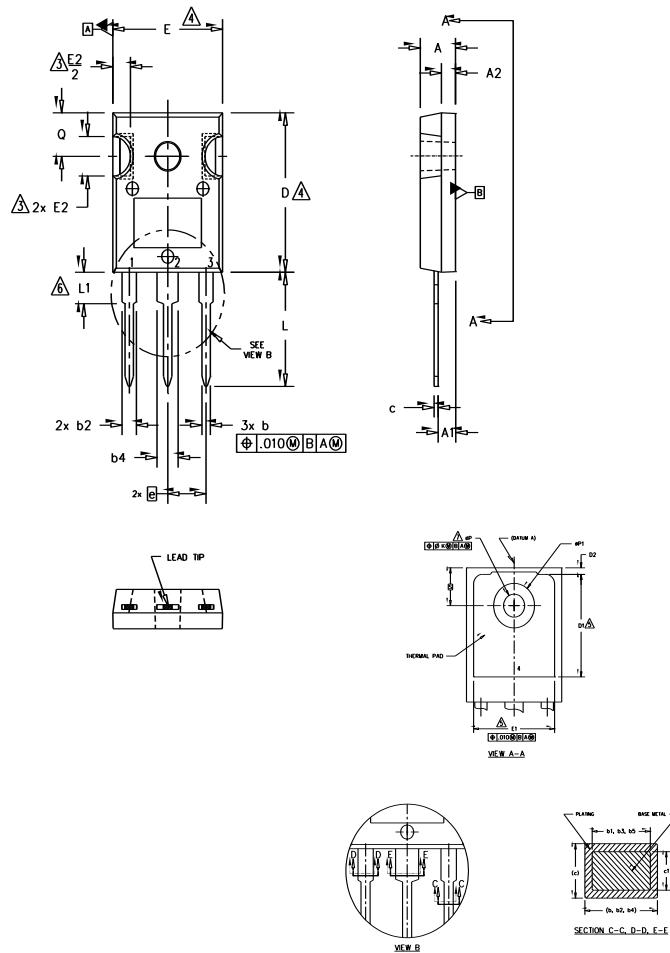


Fig 24b. Gate Charge Waveform

TO-247AC Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES	
	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.		
A	.183	.209	4.65	5.31		
A1	.087	.102	2.21	2.59		
A2	.059	.098	1.50	2.49		
b	.039	.055	0.99	1.40		
b1	.039	.053	0.99	1.35		
b2	.065	.094	1.65	2.39		
b3	.065	.092	1.65	2.34		
b4	.102	.135	2.59	3.43		
b5	.102	.133	2.59	3.38		
c	.015	.035	0.38	0.89		
c1	.015	.033	0.38	0.84		
D	.776	.815	19.71	20.70	4	
D1	.515	—	13.08	—	5	
D2	.020	.053	0.51	1.35		
E	.602	.625	15.29	15.87	4	
E1	.530	—	13.46	—		
E2	.178	.216	4.52	5.49		
e	.215 BSC		5.46 BSC			
e _k	.010		0.25			
L	.559	.634	14.20	16.10		
L1	.146	.169	3.71	4.29		
øP	.140	.144	3.56	3.66		
øP1	—	.291	—	7.39		
O	.209	.224	5.31	5.69		
S	.217 BSC		5.51 BSC			

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

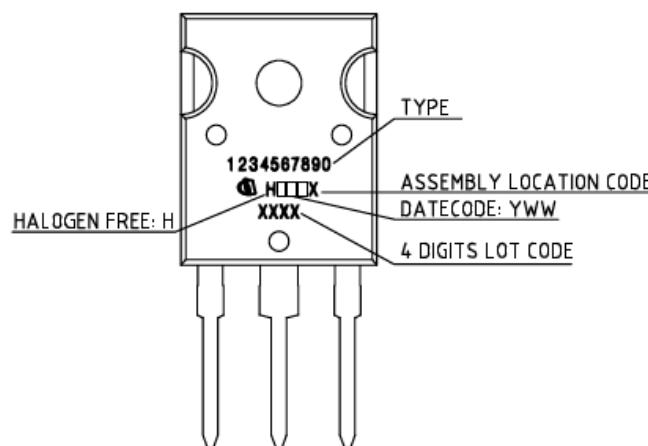
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter
- 4.- COLLECTOR

DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.

Qualification information[†]

Qualification level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	TO-247AC	N/A
RoHS compliant	Yes	

[†] Qualification standards can be found at Infineon web site: <https://www.infineon.com/>

^{††} Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Rev.	Comments
2013-09-06	2.0	<ul style="list-style-type: none">• Final data sheet
2024-11-25	2.1	<ul style="list-style-type: none">• Update datasheet to Infineon format• Updated Part marking –page 8• Added disclaimer on last page.

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