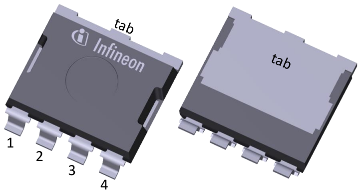
MOSFET

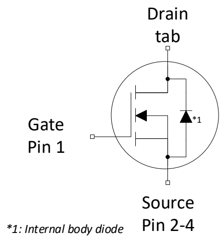
OptiMOS™ 5 Linear FET 2, 100 V

PG-HSOG-4



Features

- Ideal for hot-swap and e-fuse applications
- Very low on-resistance $R_{DS(on)}$
- Wide safe operating area SOA
- Low $V_{gs(th)}$ spread
- Improved current sharing
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	1.85	mΩ
I_D	285	A
I_{pulse} (V_{DS}=56 V, t_p=10 ms)	12	A

Part number	Package	Marking	Related links
IPM018N10NM5LF2	PG-HSOG-4	18N10LF2	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	285	A	V_{GS}=10 V, T_C=25 °C
				204		V_{GS}=10 V, T_C=100 °C
				213		V_{GS}=15 V, T_C=100 °C
				30		V_{GS}=10 V, T_A=25 °C, R_{thJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1140	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	807	mJ	I_D=100 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	349	W	T_C=25 °C
				3.8		T_A=25 °C, R_{thJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

2) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3) See Diagrams 3 and 4 for more detailed information

4) See Diagram 14 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.43	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5]	R_{thJA}			40		
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}			62		

5) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.85	3.15	3.45	V	V_{DS}=V_{GS}, I_D=240 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.4	1.7	mΩ	V_{GS}=15 V, I_D=100 A
			1.6	1.85		V_{GS}=10 V, I_D=100 A
Gate resistance	R_G	-	1.4	2.1	Ω	-
Transconductance	g_{fs}	65	130	-	S	$\lvert V_{DS}\rvert \geq 2\lvert I_D\rvert R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [6)]	C_{iss}	-	11000	14000	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [6)]	C_{oss}		1600	2100		
Reverse transfer capacitance [6)]	C_{rss}		61	110		
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		23			
Turn-off delay time	$t_{d(off)}$		36			
Fall time	t_f		16			

6) Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7)]

<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="3">Values</th><th rowspan="2">Unit</th><th rowspan="2">Note / Test condition</th></tr>
<tr><th>Min.</th><th>Typ.</th><th>Max.</th></tr>
<tr><td>Gate to source charge</td><td>Q_{gs}</td><td rowspan="6">-</td><td>74</td><td>-</td><td>nC</td><td rowspan="6">V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V</td></tr>
<tr><td>Gate charge at threshold</td><td>$Q_{g(th)}$</td><td>35</td><td>-</td><td>nC</td></tr>
<tr><td>Gate to drain charge [8)]</td><td>Q_{gd}</td><td>25</td><td>38</td><td>nC</td></tr>
<tr><td>Switching charge</td><td>Q_{sw}</td><td>64</td><td>-</td><td>nC</td></tr>
<tr><td>Gate charge total [8)]</td><td>Q_g</td><td>142</td><td>178</td><td>nC</td></tr>
<tr><td>Gate plateau voltage</td><td>$V_{plateau}$</td><td>6.6</td><td>-</td><td>V</td></tr>
<tr><td>Gate charge total, sync. FET</td><td>$Q_{g(sync)}$</td><td>-</td><td>128</td><td>-</td><td>nC</td><td>V_{DS}=0.1 V, V_{GS}=0 to 10 V</td></tr>
<tr><td>Output charge [8)]</td><td>Q_{oss}</td><td>-</td><td>181</td><td>241</td><td>nC</td><td>V_{DS}=50 V, V_{GS}=0 V</td></tr>
</table>

7) See "Gate charge waveforms" for parameter definition
8) Defined by design. Not subject to production test.

Table 7 Reverse diode

<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="3">Values</th><th rowspan="2">Unit</th><th rowspan="2">Note / Test condition</th></tr>
<tr><th>Min.</th><th>Typ.</th><th>Max.</th></tr>
<tr><td>Diode continuous forward current</td><td>I_S</td><td rowspan="2">-</td><td rowspan="2">-</td><td>285</td><td rowspan="2">A</td><td rowspan="2">T_C=25 °C</td></tr>
<tr><td>Diode pulse current</td><td>$I_{S,pulse}$</td><td>1140</td></tr>
<tr><td>Diode forward voltage</td><td>V_{SD}</td><td>-</td><td>0.84</td><td>1.0</td><td>V</td><td>V_{GS}=0 V, I_F=100 A, T_j=25 °C</td></tr>
<tr><td>Reverse recovery time [9)]</td><td>t_{rr}</td><td rowspan="2">-</td><td>58</td><td>116</td><td>ns</td><td rowspan="2">V_R=50 V, I_F=100 A, di_F/dt=100 A/µs</td></tr>
<tr><td>Reverse recovery charge [9)]</td><td>Q_{rr}</td><td>118</td><td>236</td><td>nC</td></tr>
</table>

9) Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

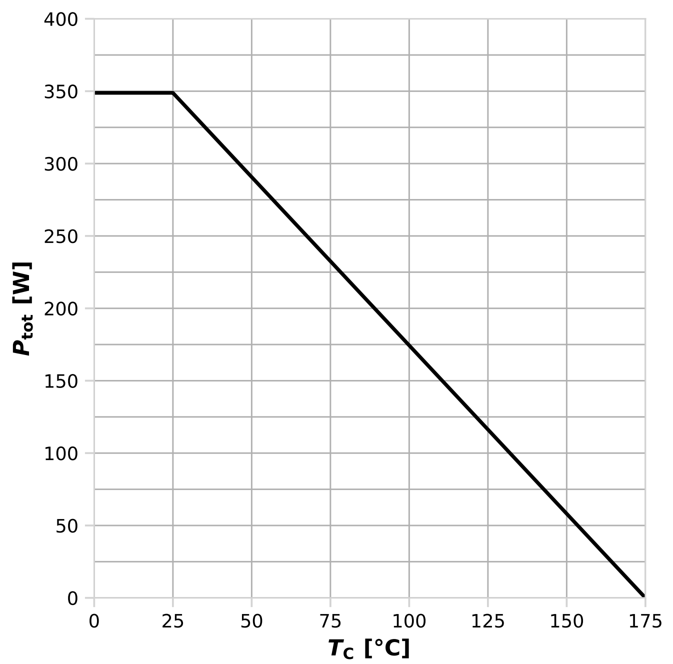
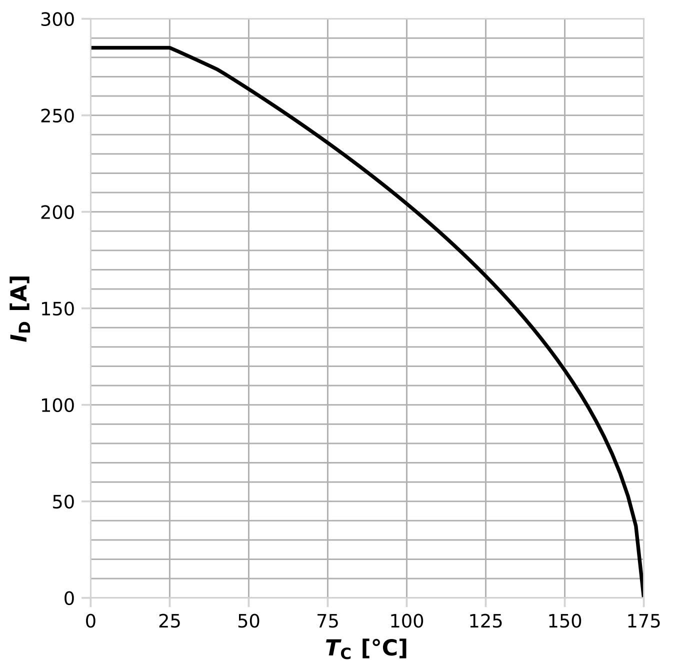
Diagram 1: Power dissipation	Diagram 2: Drain current
	
P_{tot}=f(T_C)	I_D=f(T_C); V_{GS}≥10 V

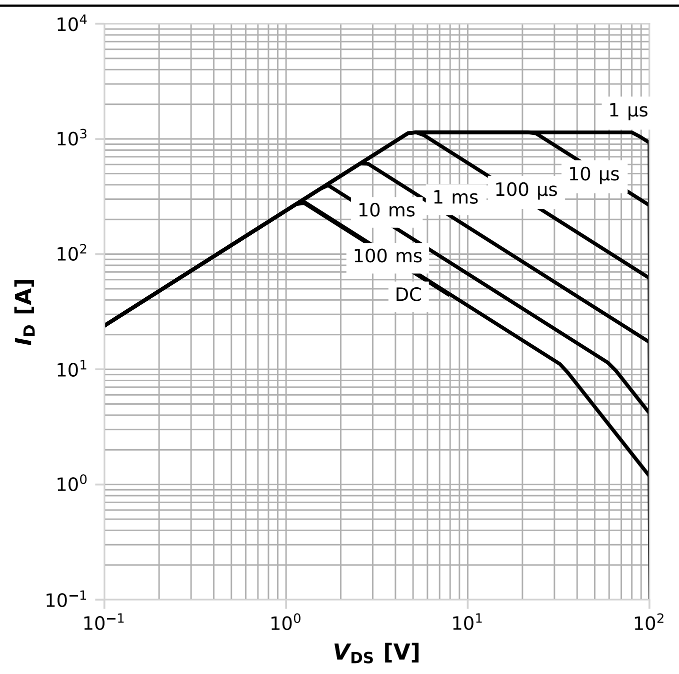
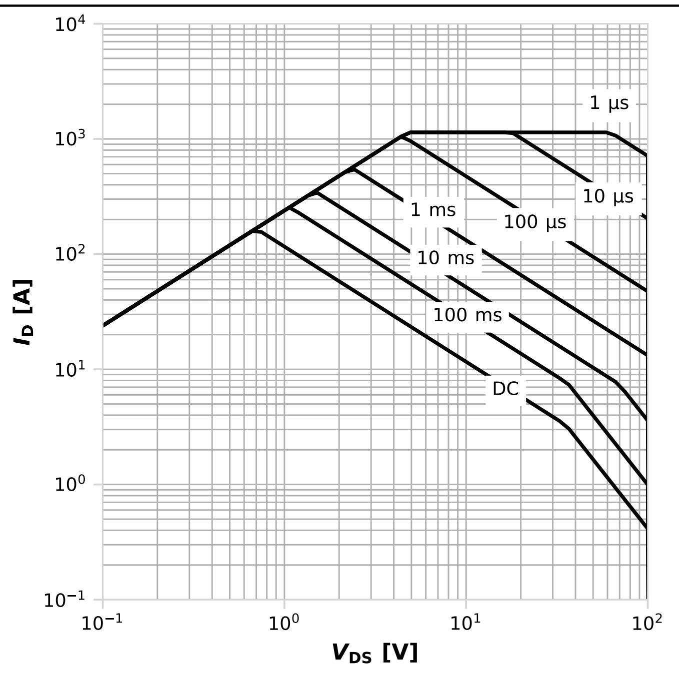
Diagram 3: Safe operating area	Diagram 4: Safe operating area
	
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p	I_D=f(V_{DS}); T_C=125 °C; D=0; parameter: t_p

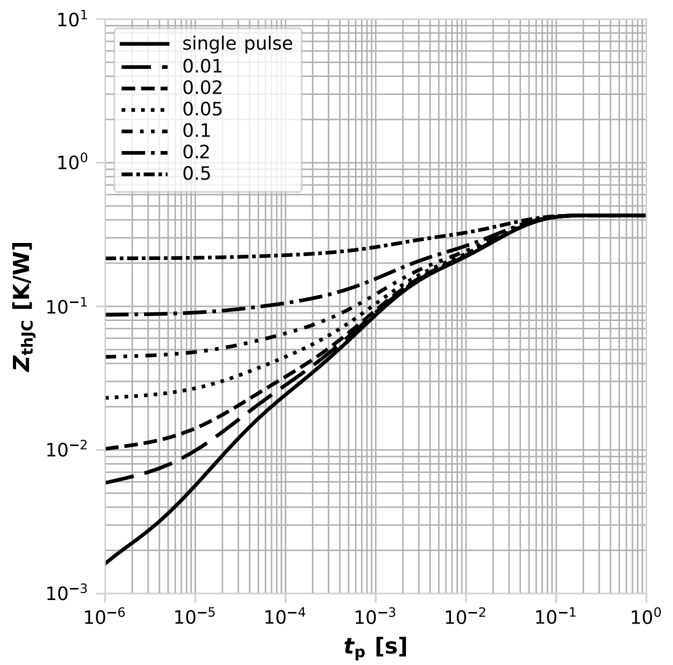
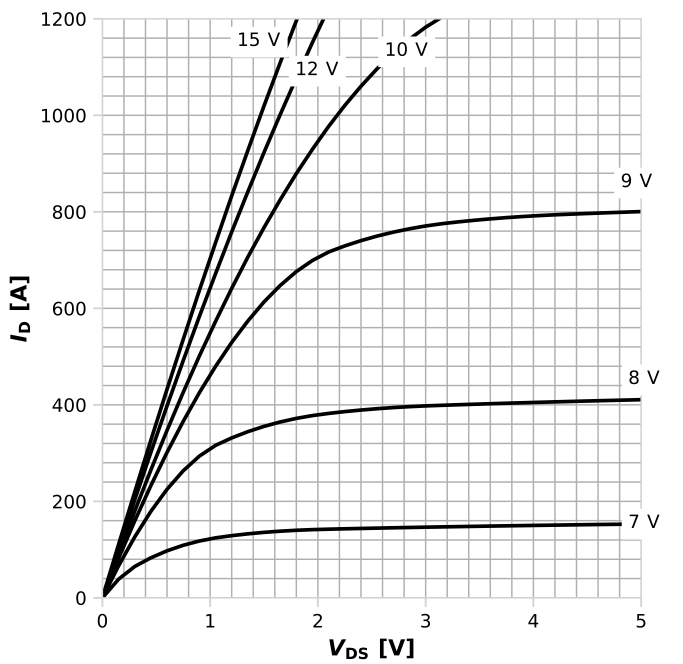
Diagram 5: Max. transient thermal impedance	Diagram 6: Typ. output characteristics
	
Z_{thJC}=f(t_p); parameter: D=t_p/T	I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

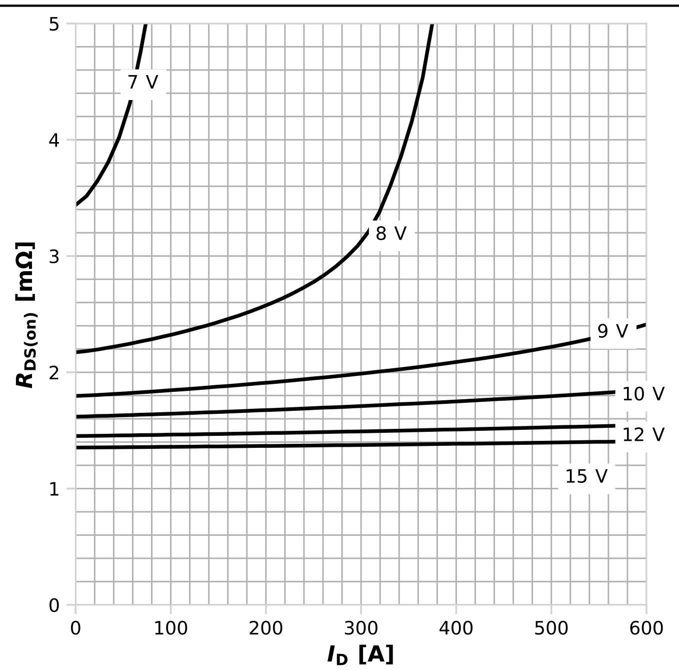
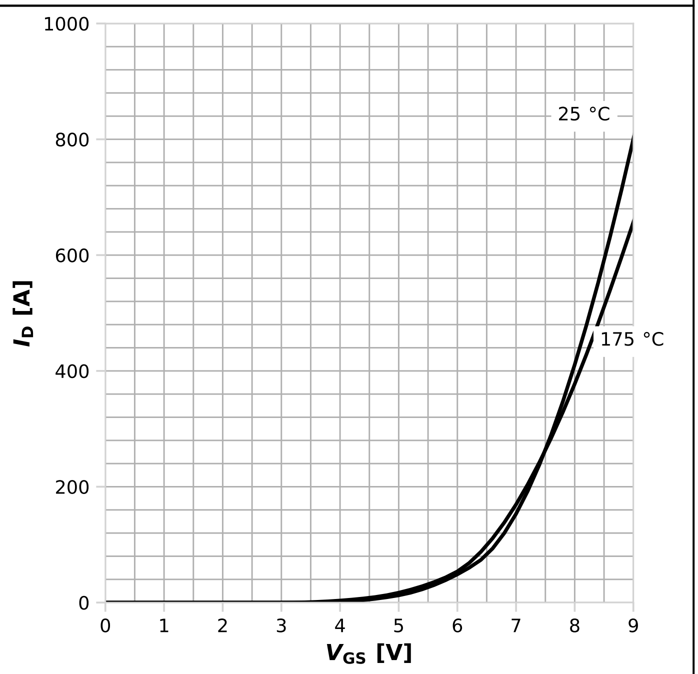
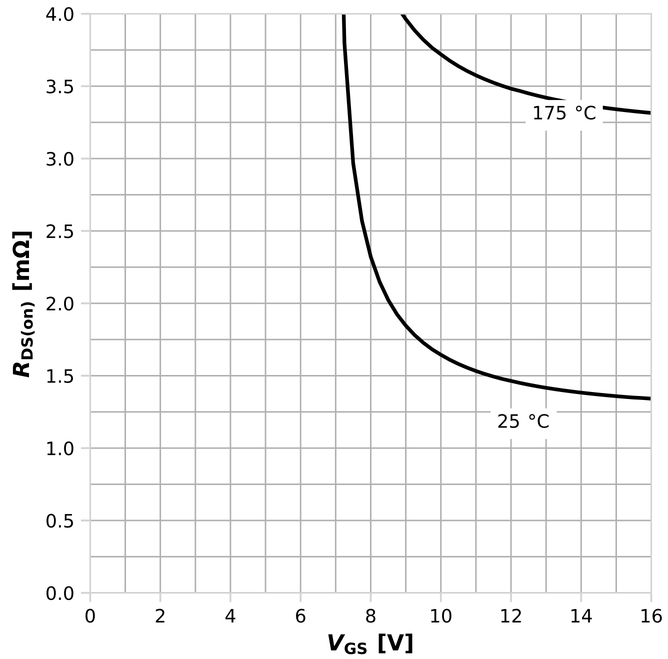
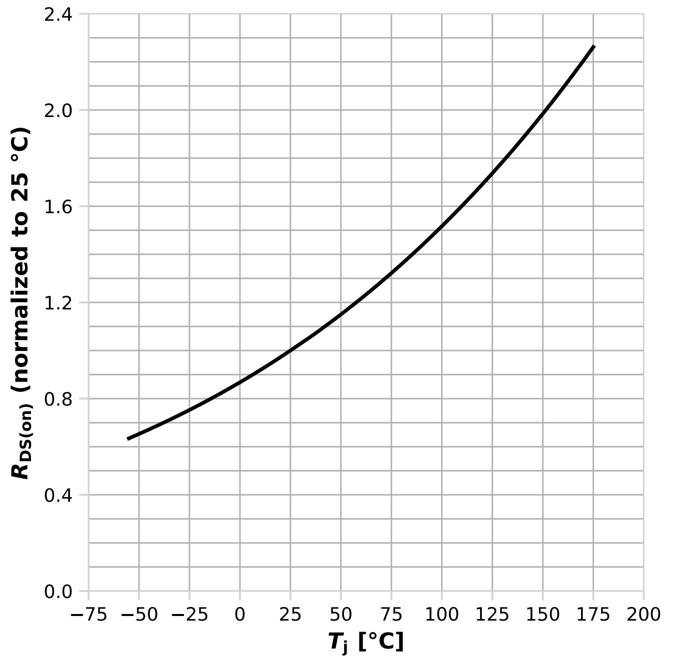
Diagram 7: Typ. drain-source on resistance	Diagram 8: Typ. transfer characteristics
	
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}	I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 9: Typ. drain-source on resistance



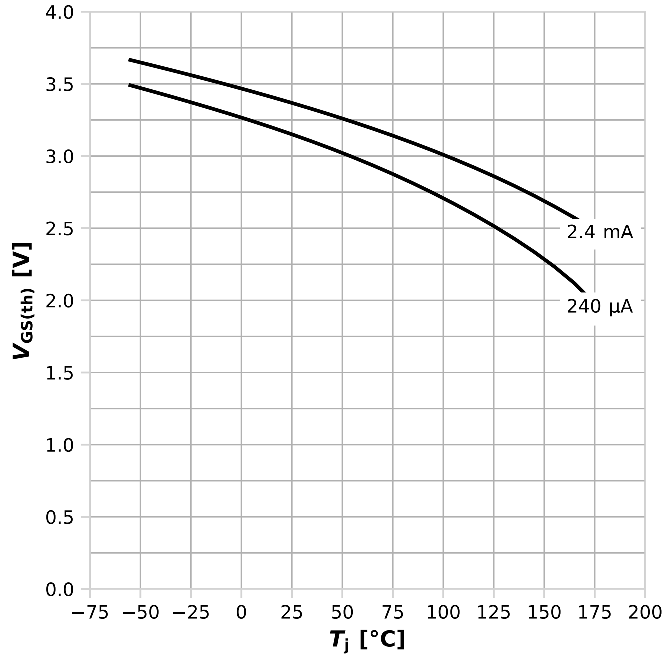
$R_{DS(on)}$=f(V_{GS}), I_D=100 A; parameter: T_j

Diagram 10: Normalized drain-source on resistance



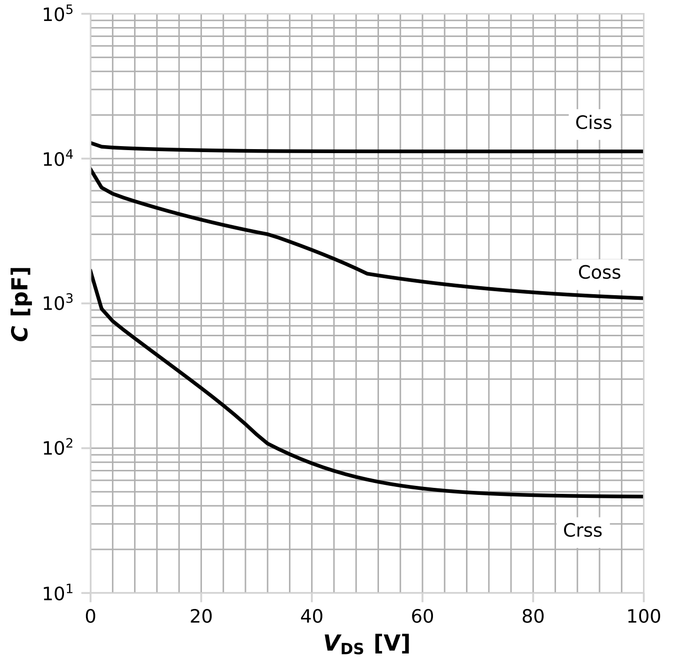
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V

Diagram 11: Typ. gate threshold voltage



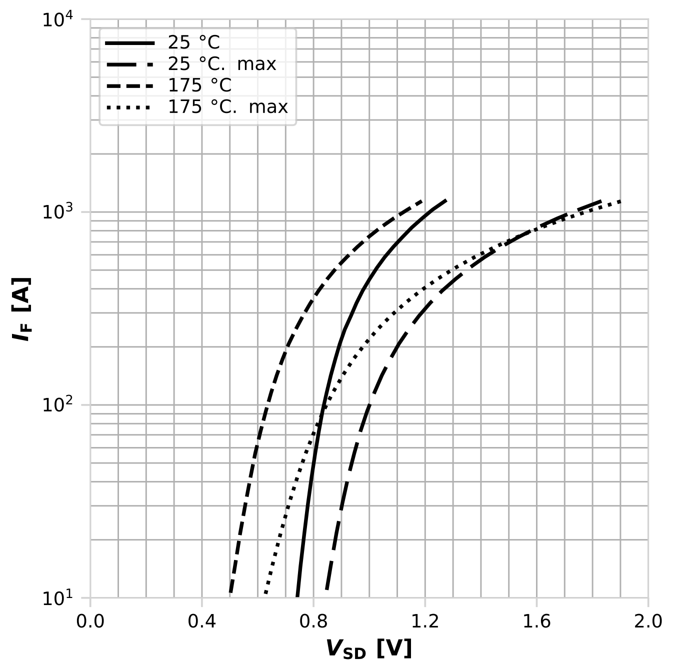
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 12: Typ. capacitances



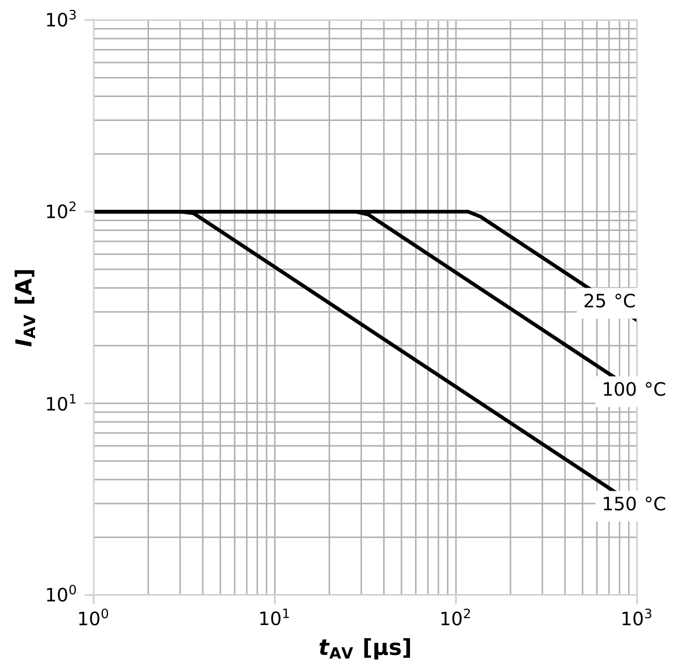
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 13: Forward characteristics of reverse diode



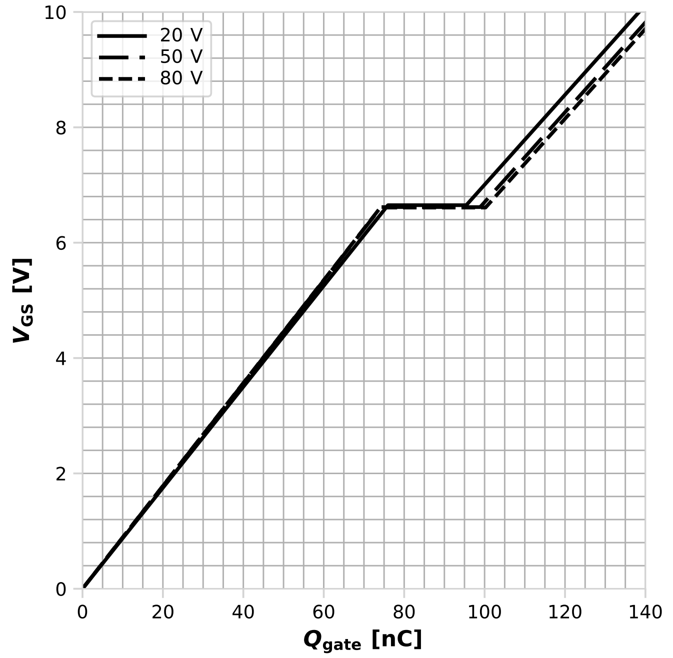
$I_F=f(V_{SD})$; parameter: T_j

Diagram 14: Avalanche characteristics



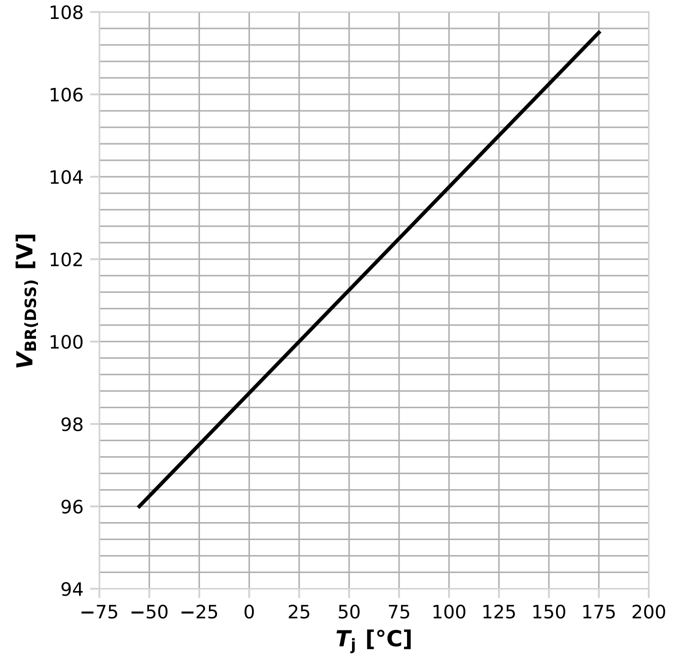
$I_{AS}=f(t_{AV})$; R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 15: Typ. gate charge

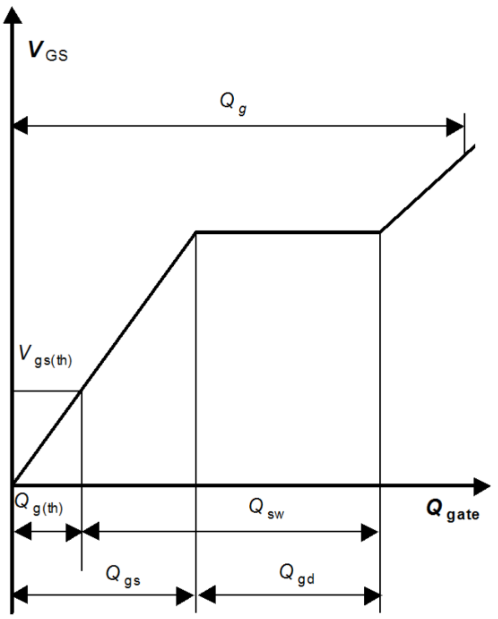


$V_{GS}=f(Q_{gate})$, I_D=100 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 16: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; I_D=1 mA

Gate charge waveforms

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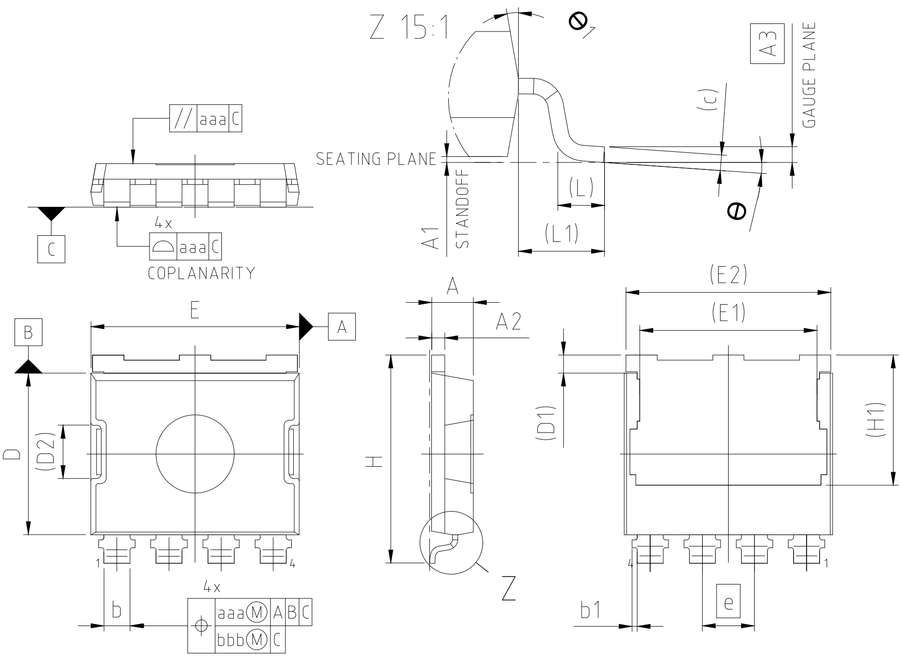
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-HSOG-4-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	1.50	1.70
A1	0.00	0.15
A2	0.40	0.60
A3	0.20	
b	0.90	1.10
b1	0.00	0.25
c	0.20	
D	6.10	6.40
D1	0.70	
D2	2.04	
E	7.80	8.20
E1	6.80	
E2	7.86	

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
e	2.00	
H	7.80	8.20
H1	5.00	
L	0.60	
L1	1.10	
N	4	
Θ	0°	8°
Θ1	8°	12°
aaa	0.10	
bbb	0.05	

NOTES: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
N IS THE NUMBER OF LEADS

Figure 1 Outline PG-HSOG-4, dimensions in mm

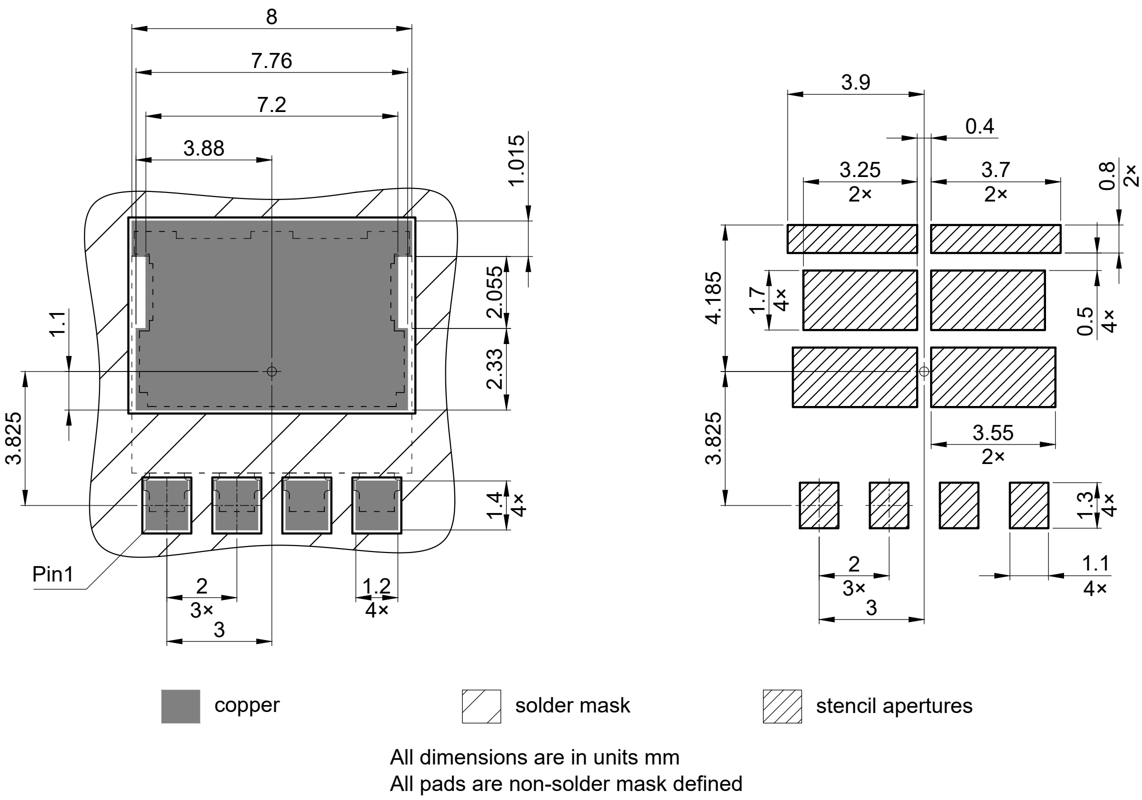


Figure 2 Footprint drawing PG-HSOG-4, dimensions in mm

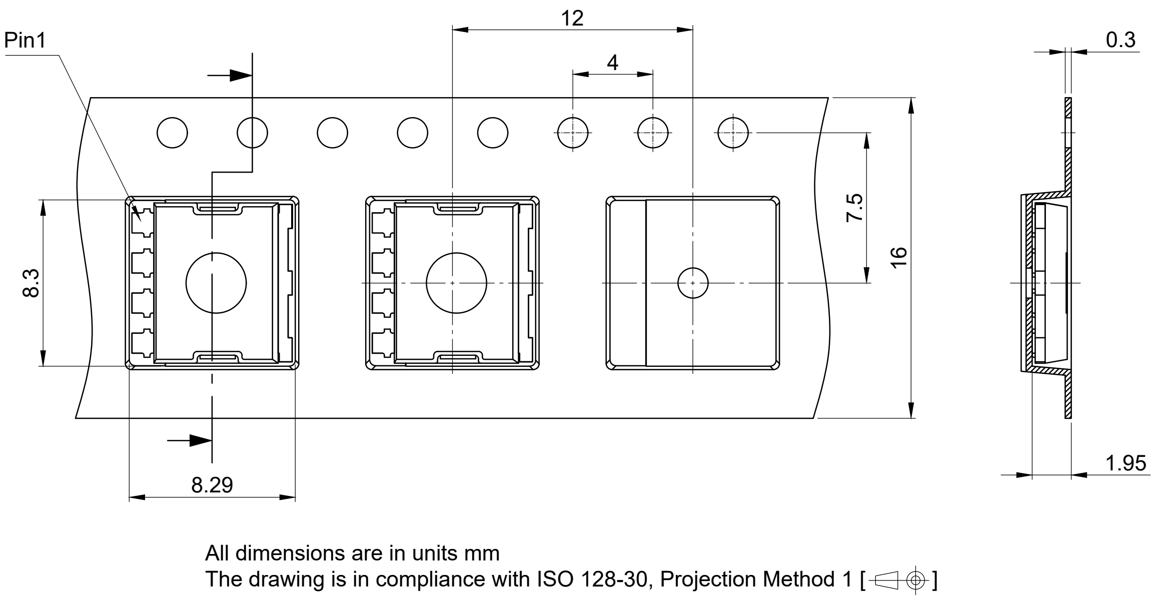


Figure 3 Packaging variant PG-HSOG-4, dimensions in mm

Revision history

IPM018N10NM5LF2

Revision 2025-03-07, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-03-07	Release of final datasheet

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