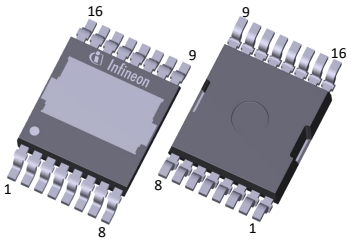
SiC MOSFET

CoolSiC™ MOSFET 650 V G2

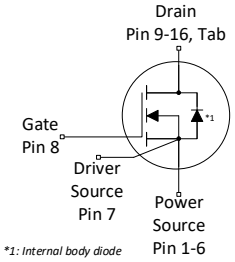
TOLT



Built on Infineon's robust 2nd generation Silicon Carbide trench technology, the 650 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

Features

- Ultra-low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.5 V
- Robust against parasitic turn-on even with 0 V turn-off gate voltage
- Flexible driving voltage and compatible with bipolar driving scheme
- Robust body diode operation under hard commutation events
- .XT interconnection technology for best-in-class thermal performance



Benefits

- Enables high efficiency and high power density designs
- Facilitates great ease of use and integration
- Provides the best price performance ratio compared to Industry's most ambitious roadmaps
- Reduces the size, weight and bill of materials of the systems
- Enhances system robustness and reliability

Potential applications

- SMPS
- Solar PV inverters
- Energy storage and battery formation
- UPS
- EV charging infrastructure
- Motor drives

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DSS} over full $T_{j,range}$	650	V
$R_{DS(on),typ}$	60	mΩ
$R_{DS(on),max}$	73	mΩ
$Q_{G,typ}$	18	nC
$I_{D,pulse}$	96	A
Q_{oss} @ 400 V	36	nC
E_{oss} @ 400 V	4.8	µJ

Part number	Package	Marking	Related links
IMLT65R060M2H	PG-HDSOP-16	65R060M2	see Appendix A

Table of contents

1 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous DC drain current [1]	I_{DDC}	-	-	40	A	T_c = 25 °C
				28		T_c = 100 °C
Peak drain current [2]	I_{DM}	-	-	96	A	T_c = 25 °C, V_{GS} = 18 V
Avalanche energy, single pulse	E_{AS}	-	-	89	mJ	I_D = 3.4 A, V_{DD} = 50 V; see table 11
Avalanche energy, repetitive	E_{AR}			0.44		
Avalanche current, single pulse	I_{AS}	-	-	3.4	A	-
MOSFET *dv/dt* ruggedness	*dv/dt*	-	-	200	V/ns	V_{DS}= 0...400 V
Gate source voltage (static) [3]	V_{GS}	-7	-	23	V	-
Gate source voltage (transient)	V_{GS}	-10	-	25	V	t_p ≤ 500 ns, duty cycle ≤ 1 %
Power dissipation	P_{tot}	-	-	200	W	T_c = 25 °C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55		175	°C	
Mounting torque	-	-		-	Ncm	
Continuous reverse drain current [1]	I_{SDC}	-	-	40	A	V_{GS} = 18 V, T_c = 25 °C
				28		V_{GS} = 0 V, T_c = 25 °C
Peak reverse drain current [2]	I_{SM}	-	-	96	A	T_c = 25 °C, t_p ≤ 250 ns
				29		T_c = 25 °C
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_c = 25 °C, t = 1 min

[1] Limited by $T_{j,max}$.

[2] Pulse width t_{pulse} limited by $T_{j,max}$.

[3] The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	-	0.75	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$		0			

4 Electrical characteristics

at T_j = 25 °C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DSS}	650	-	-	V	V_{GS} = 0 V, I_D = 0.31 mA
Gate threshold voltage [4]	$V_{GS(th)}$	3.5	4.5	5.6	V	V_{DS} = V_{GS}, I_D = 3.1 mA
Zero gate voltage drain current	I_{DSS}	-	1	75	µA	V_{DS} = 650 V, V_{GS} = 0 V, T_j = 25 °C
			3	-		V_{DS} = 650 V, V_{GS} = 0 V, T_j = 175 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS} = 20 V, V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	78	-	mΩ	V_{GS} = 15 V, I_D = 15.4 A, T_j = 25 °C
			60	73		V_{GS} = 18 V, I_D = 15.4 A, T_j = 25 °C
			55	-		V_{GS} = 20 V, I_D = 15.4 A, T_j = 25 °C
			98	-		V_{GS} = 18 V, I_D = 15.4 A, T_j =175 °C
Internal gate resistance	$R_{G,int}$	-	5.1	-	Ω	f = 1 MHz

[4] Tested after 1 ms pulse at V_{GS} = +20 V. “Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	669	-	pF	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz
Reverse transfer capacitance	C_{rss}		4.1	-		
Output capacitance [5]	C_{oss}		50	65		
Output charge [5]	Q_{oss}	-	36	46	nC	calculation based on C_{oss}
Effective output capacitance, energy related [6]	$C_{o(er)}$	-	60	-	pF	V_{GS} = 0 V, V_{DS} = 0...400 V
Effective output capacitance, time related [7]	$C_{o(tr)}$	-	89	-	pF	I_D = constant, V_{GS} = 0 V, V_{DS} = 0... 400 V
Turn-on delay time	$t_{d(on)}$	-	6.3	-	ns	V_{DD} = 400 V, V_{GS} = 0/18 V, I_D = 15.4 A, $R_{G,ext}$ = 1.8 Ω; see table 10
Rise time	t_r		5.6			
Turn-off delay time	$t_{d(off)}$		13.7			
Fall time	t_f		4.8			

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Turn-ON switching losses [8]	E_{on}	-	26	-	µJ	V_{DD} = 400 V, V_{GS} = 0/18 V, I_D = 15.4 A, $R_{G,ext}$ = 1.8 Ω
Turn-OFF switching losses [8]	E_{off}		13			
Total switching losses [8]	E_{tot}		39			

[5] Maximum specification is defined by calculated six sigma upper confidence bound

[6] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

[7] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

[8] MOSFET used in half-bridge configuration without external diode

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	4.9	-	nC	V_{DD} = 400 V, I_D = 15.4 A, V_{GS} = 0 to 18 V
Gate to drain charge	Q_{GD}		3.4			
Total gate charge	Q_G		18			

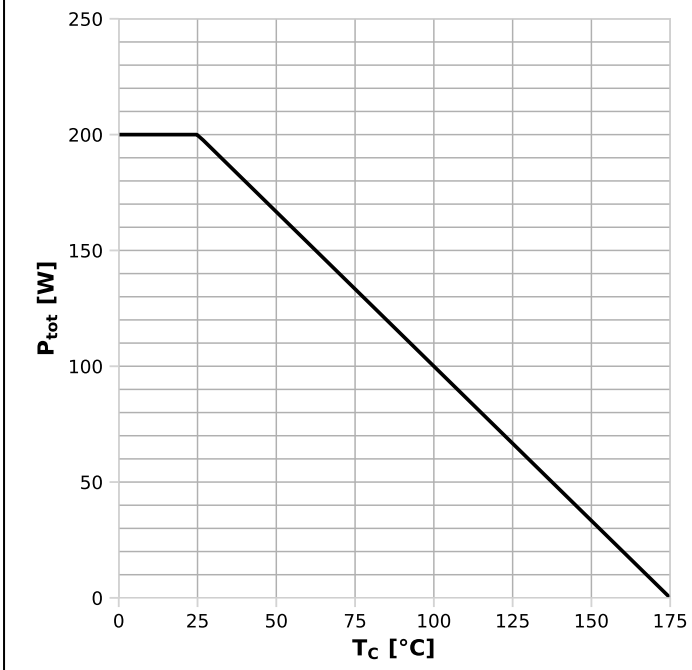
Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	V_{SD}	-	4.3	-	V	V_{GS} = 0 V, I_S = 15.4 A, T_j = 25 °C
MOSFET forward recovery time	t_{fr}	-	9.3	-	ns	V_{DD} = 400 V, I_S = 15.4 A, di_S/dt = 1000 A/µs; see table 9
			5.1			V_{DD} = 400 V, I_S = 15.4 A, di_S/dt = 4000 A/µs; see table 9
MOSFET forward recovery charge [9]	Q_{fr}	-	38	-	nC	V_{DD} = 400 V, I_S = 15.4 A, di_S/dt = 1000 A/µs; see table 9
			50			V_{DD} = 400 V, I_S = 15.4 A, di_S/dt = 4000 A/µs; see table 9
MOSFET peak forward recovery current	I_{frm}	-	8.2	-	A	V_{DD} = 400 V, I_S = 15.4 A, di_S/dt = 1000 A/µs; see table 9
			19.7			V_{DD} = 400 V, I_S = 15.4 A, di_S/dt = 4000 A/µs; see table 9

[9] Q_{fr} includes Q_{oss}

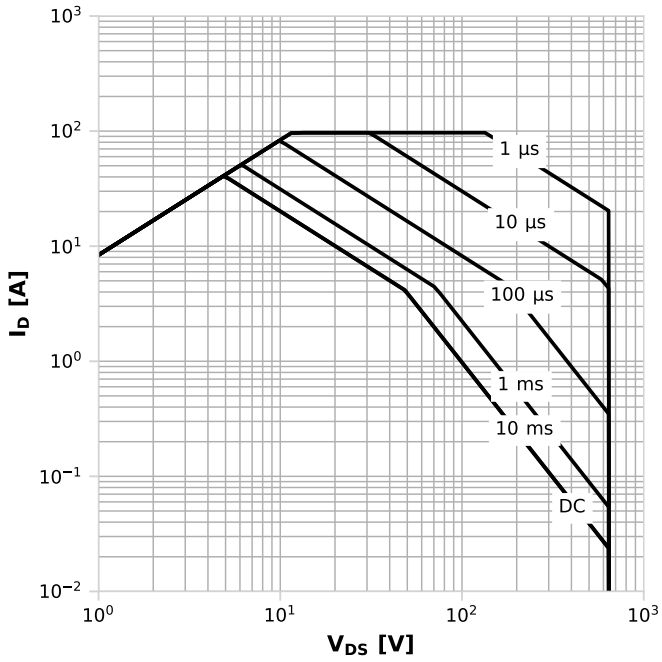
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



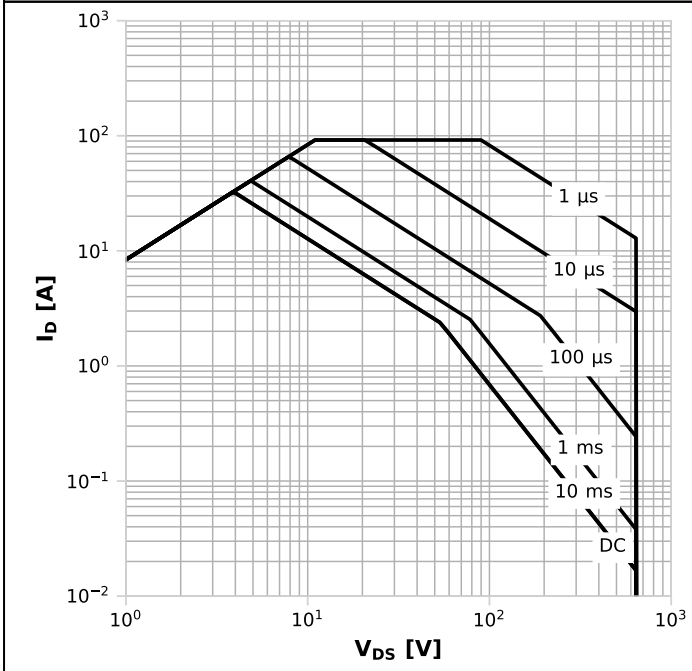
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



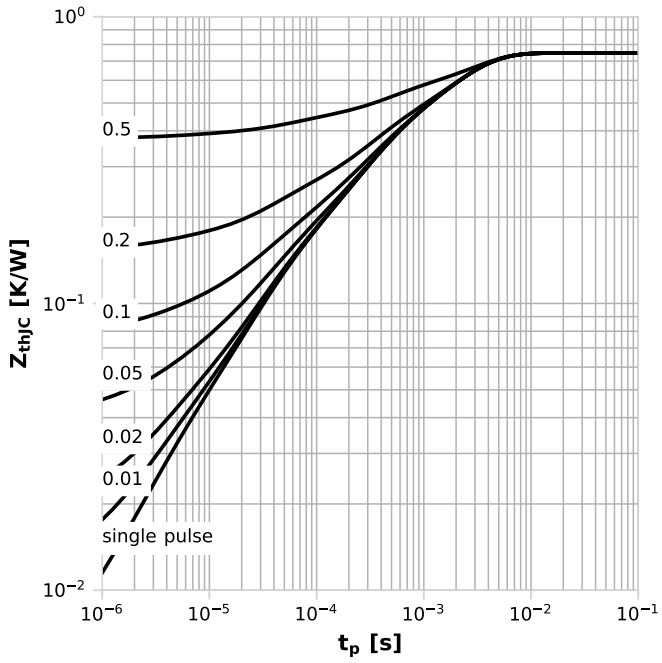
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

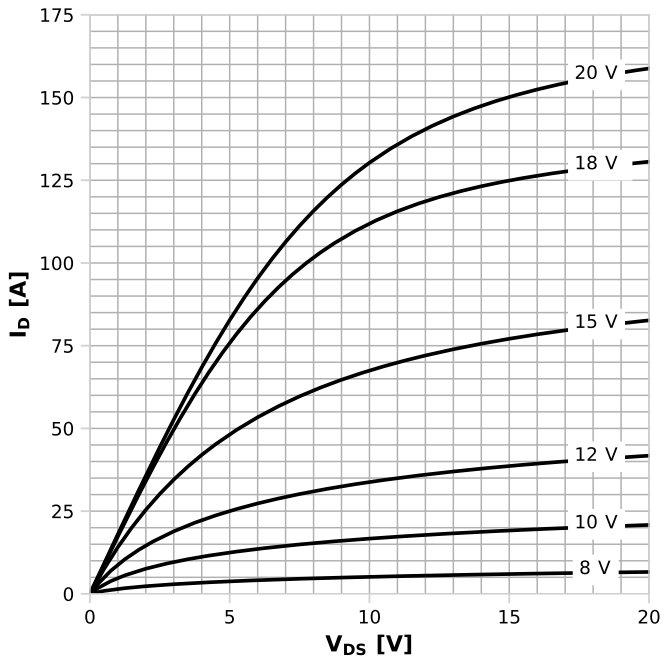
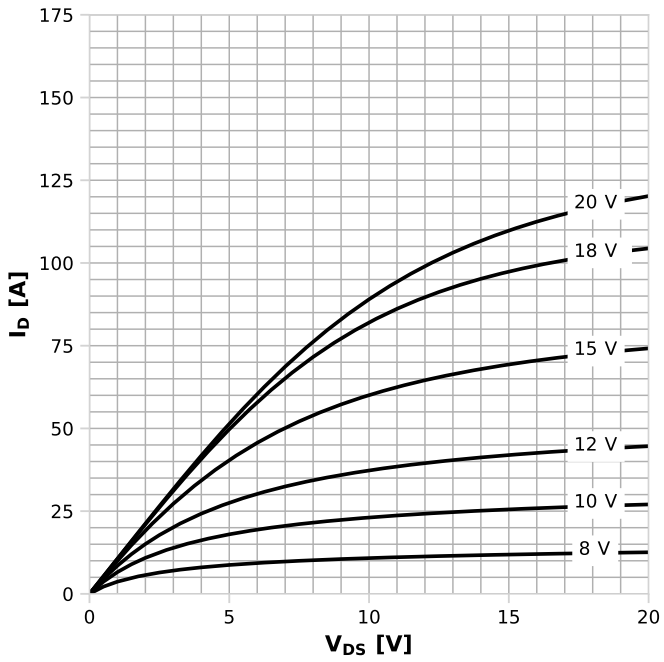
Diagram 5: Typ. output characteristics	Diagram 6: Typ. output characteristics
	
$I_D=f(V_{DS})$; T_j=25 °C; parameter: V_{GS}	$I_D=f(V_{DS})$; T_j=175 °C; parameter: V_{GS}

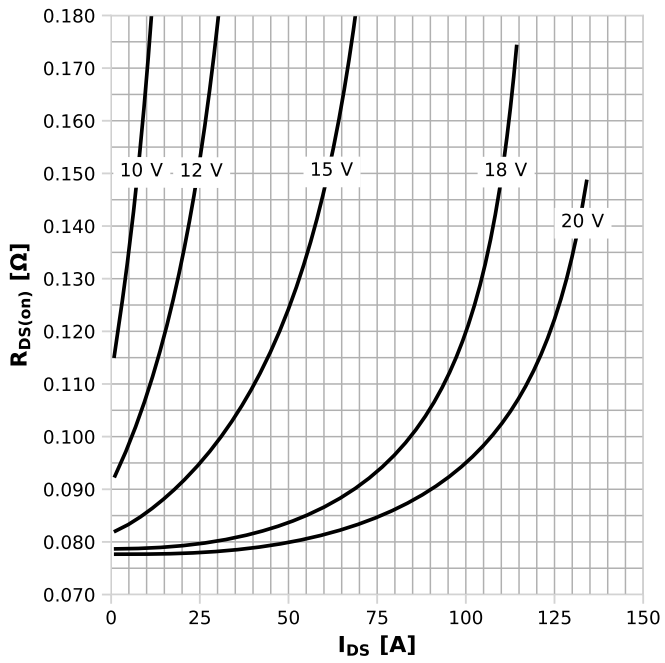
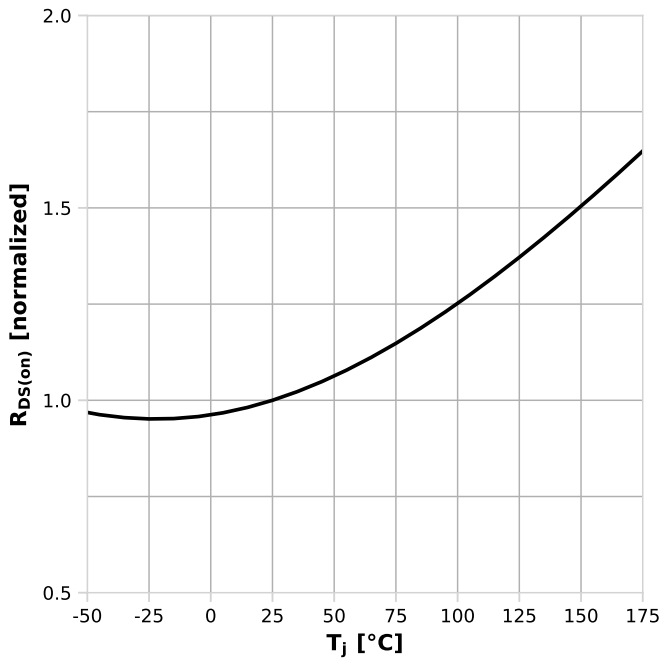
Diagram 7: Typ. drain-source on-state resistance	Diagram 8: Drain-source on-state resistance
	
$R_{DS(on)}=f(I_{DS})$; T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}=f(T_j)$; I_D=15.4 A; V_{GS}=18 V

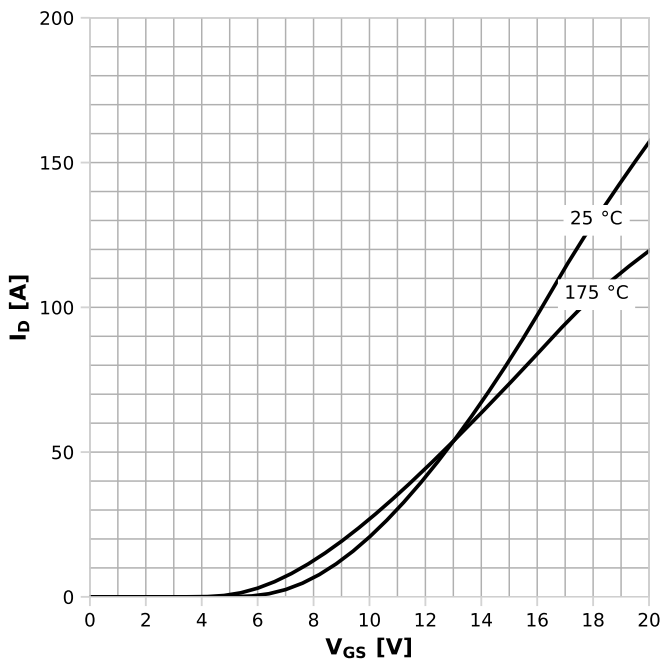
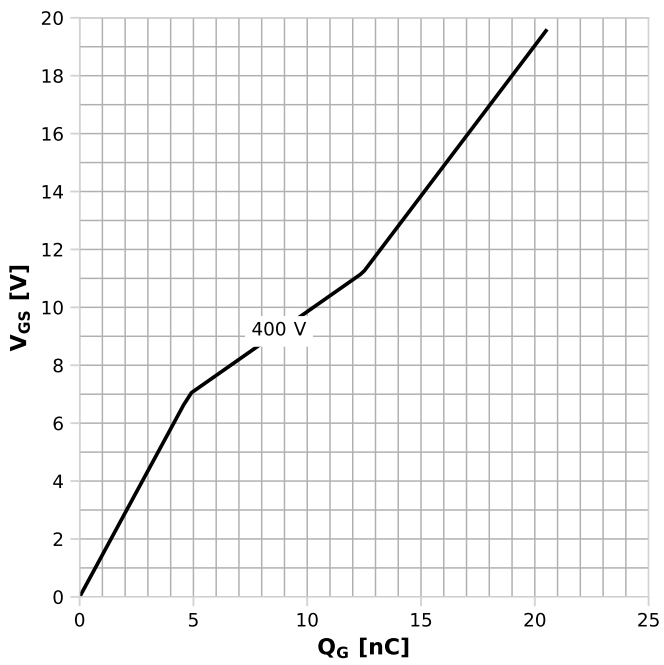
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j	$V_{GS}=f(Q_{gate})$; I_D=15.4 A pulsed; parameter: V_{DD}

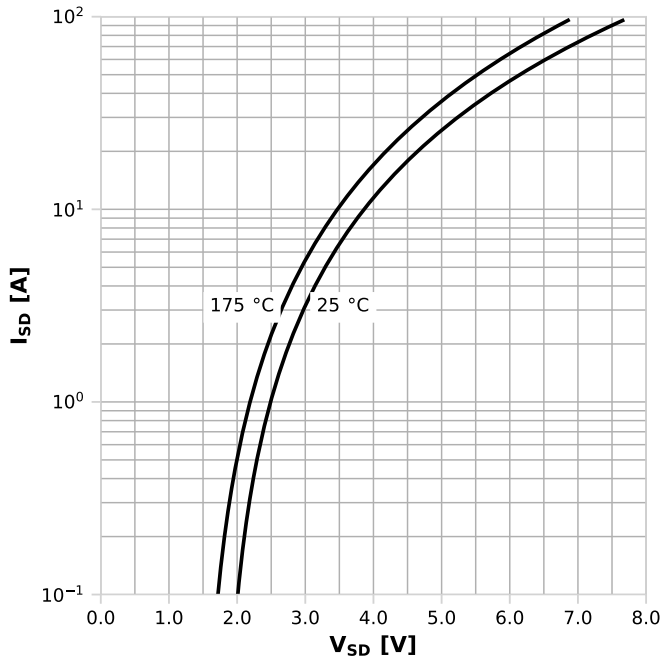
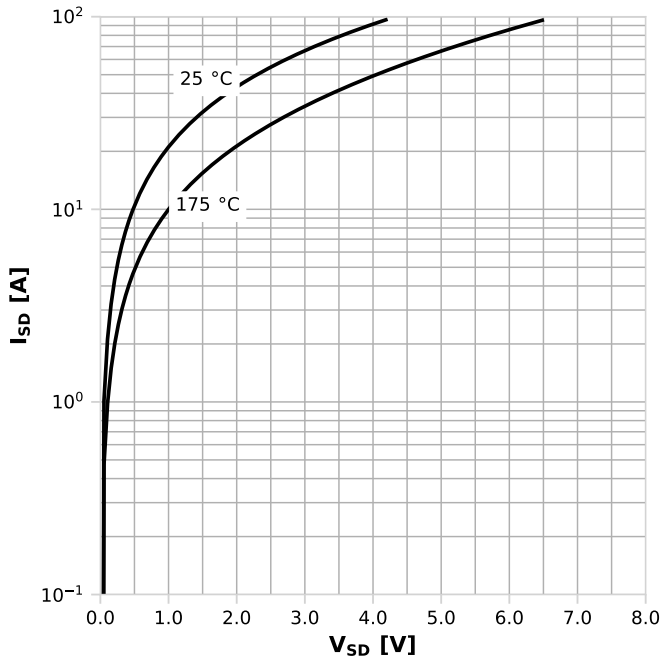
Diagram 11: Typ. reverse characteristics	Diagram 12: Typ. reverse characteristics
	
$I_{SD}=f(V_{SD})$; V_{GS}=0 V; parameter: T_j	$I_{SD}=f(V_{SD})$; V_{GS}=18 V; parameter: T_j

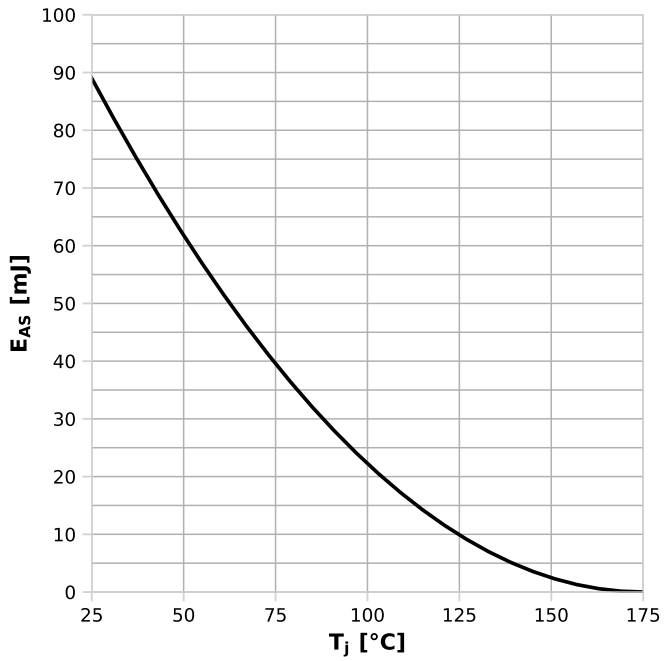
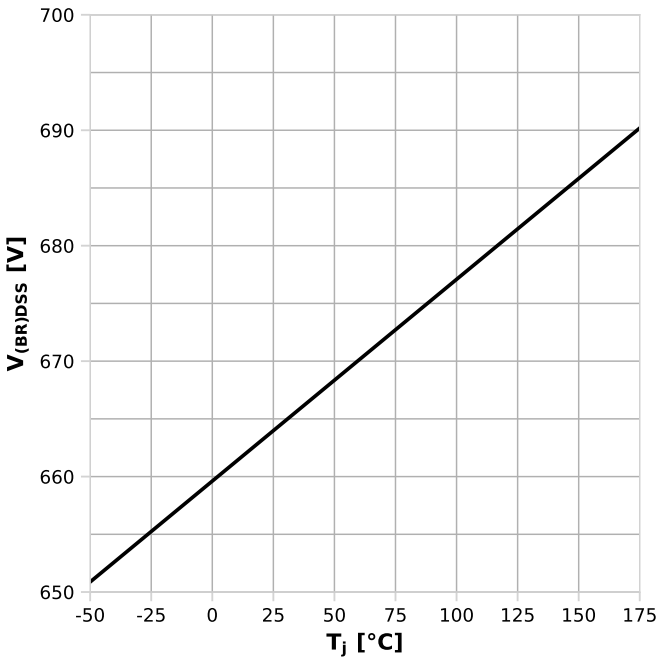
Diagram 13: Avalanche energy	Diagram 14: Drain-source breakdown voltage
	
$E_{AS}=f(T_j)$; I_D=3.4 A; V_{DD}=50 V	$V_{(BR)DSS}=f(T_j)$; I_D=0.31 mA

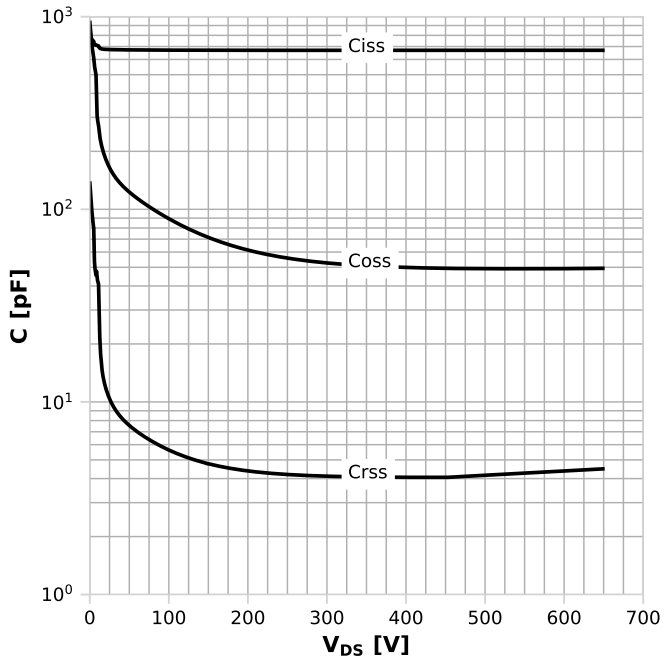
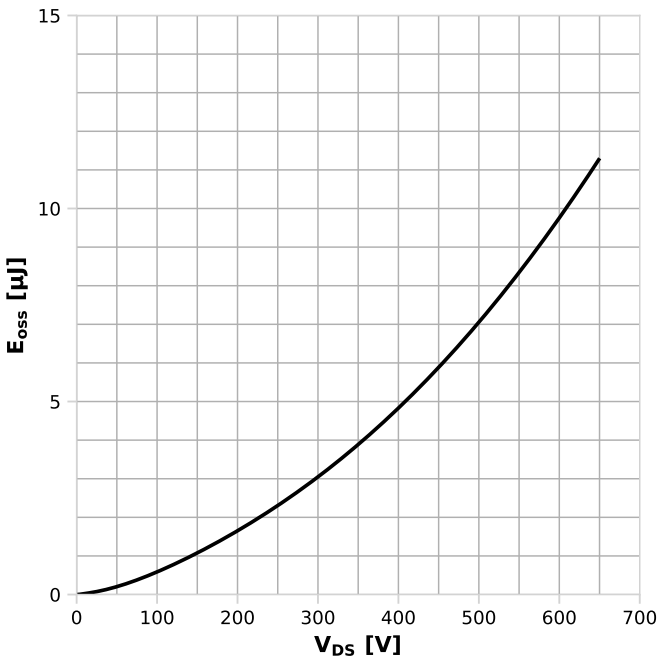
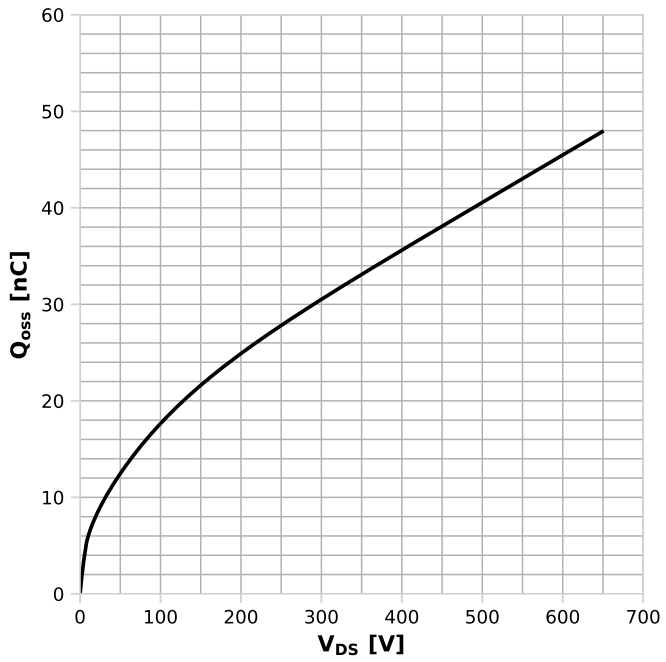
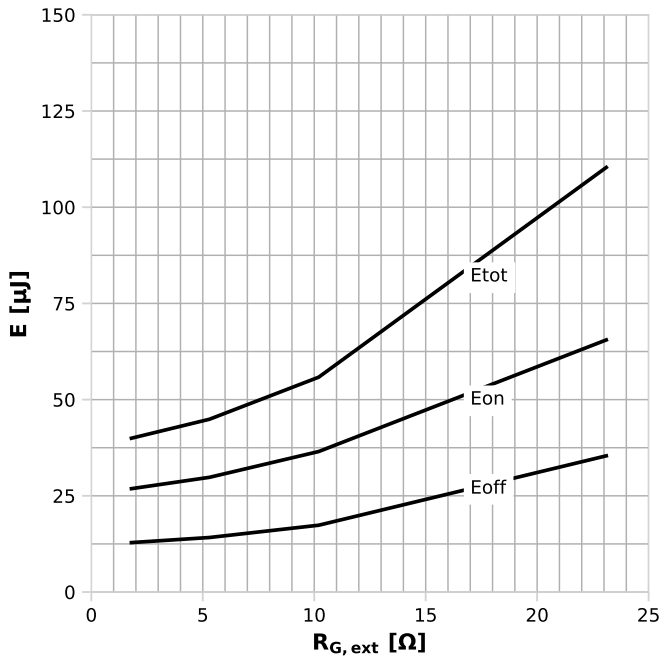
Diagram 15: Typ. capacitances	Diagram 16: Typ. Coss stored energy
	
$C=f(V_{DS})$; V_{GS}=0 V; f=250 kHz	$E_{oss}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge



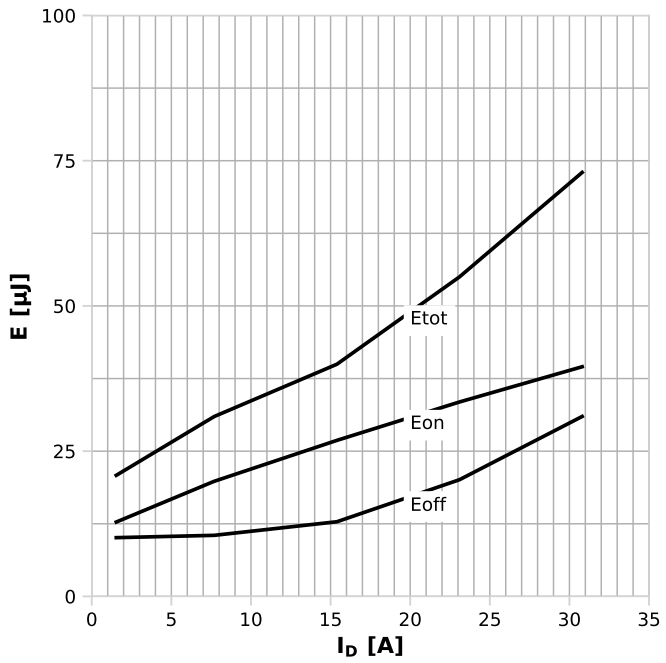
$Q_{oss}=f(V_{DS})$

Diagram 18: Typ. Switching Losses vs $R_{G,ext}$



$E=f(R_{G,ext})$; V_{DD}=400 V; V_{GS}=0-18 V; I_D=15.4 A

Diagram 19: Typ. Switching Losses vs switching current



$E=f(I_D)$; V_{DD}=400 V; V_{GS}=0-18 V; $R_{G,ext}$=1.8 Ω

6 Test circuits

Table 9 Body diode characteristics

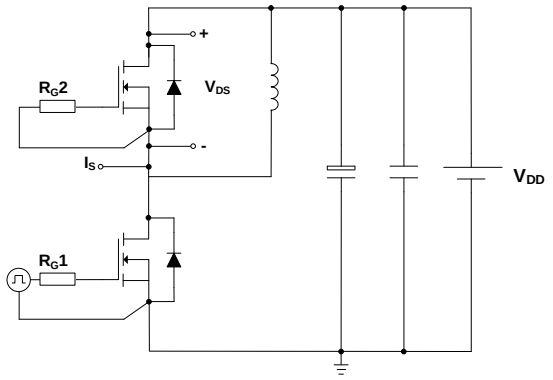
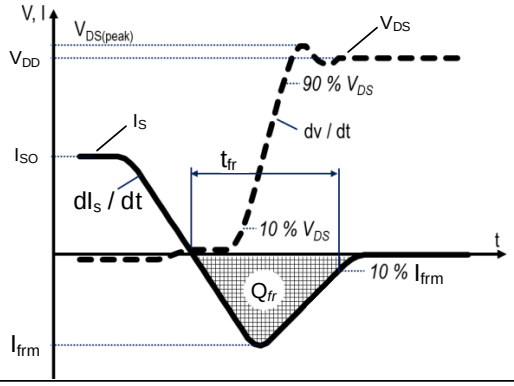
Test circuit for body diode characteristics	Body diode recovery waveform
	

Table 10 Switching times

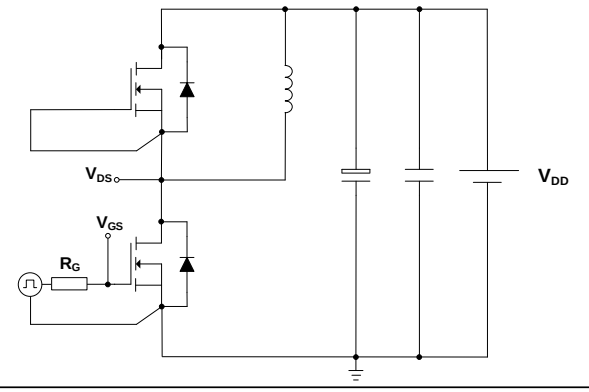
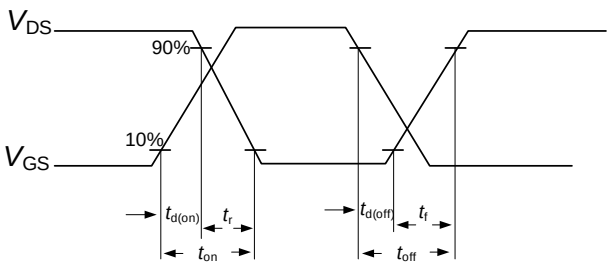
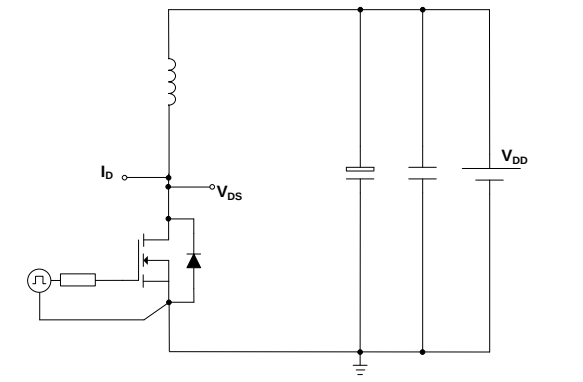
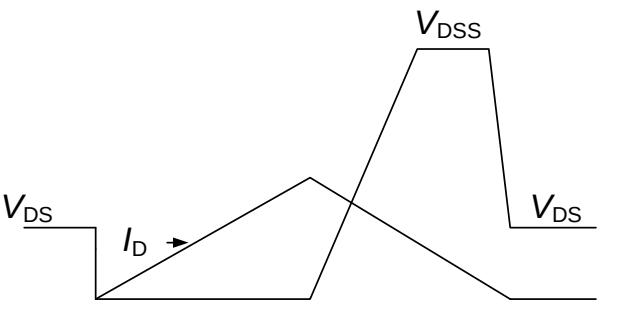
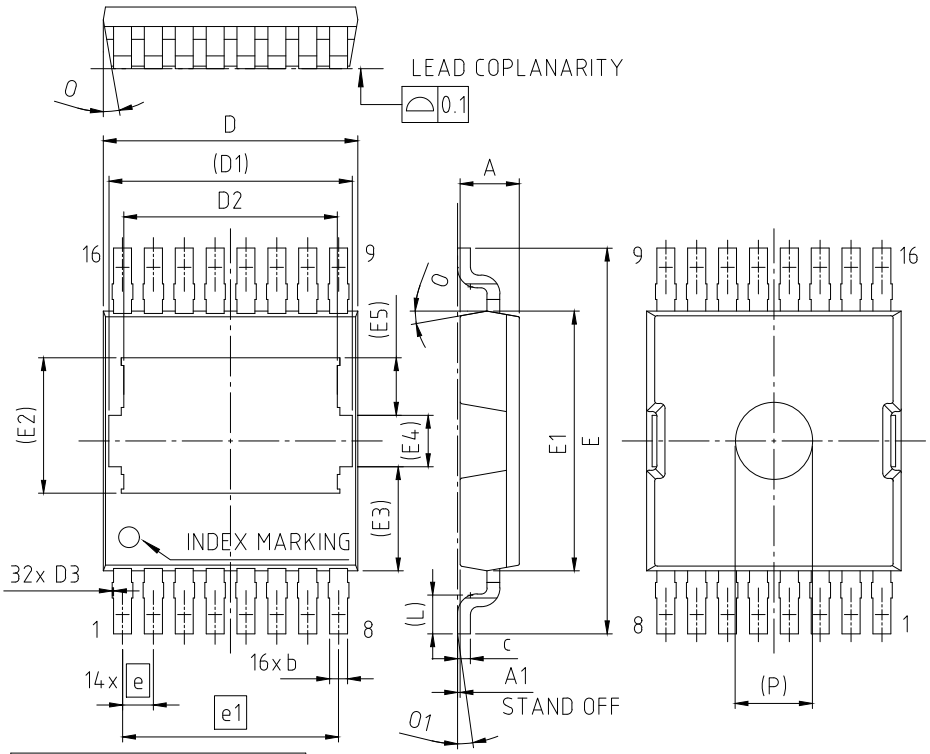
Switching times test circuit for inductive load	Switching times waveform
	

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package outlines



PACKAGE - GROUP NUMBER: **PG-HDSOP-16-U02**

DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	2.25	2.35	**e**	1.20	
A1	0.00	0.15	**e1**	8.40	
b	0.60	0.80	**L**	1.50	
c	0.40	0.60	**P**	3.00	
D	9.70	10.10	**O**	10°	
D1	9.46		**O1**	0.00°	8°
D2	8.20	8.40			
D3	0.15				
E	14.80	15.20			
E1	10.00	10.30			
E2	5.27				
E3	4.05				
E4	2.00				
E5	2.24				

NOTES:
ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT
DIMENSIONS DO NOT INCLUDE MOLD FLASH,
PROTRUSION OR GATE BURRS

Figure 1 Outline PG-HDSOP-16, dimensions in mm

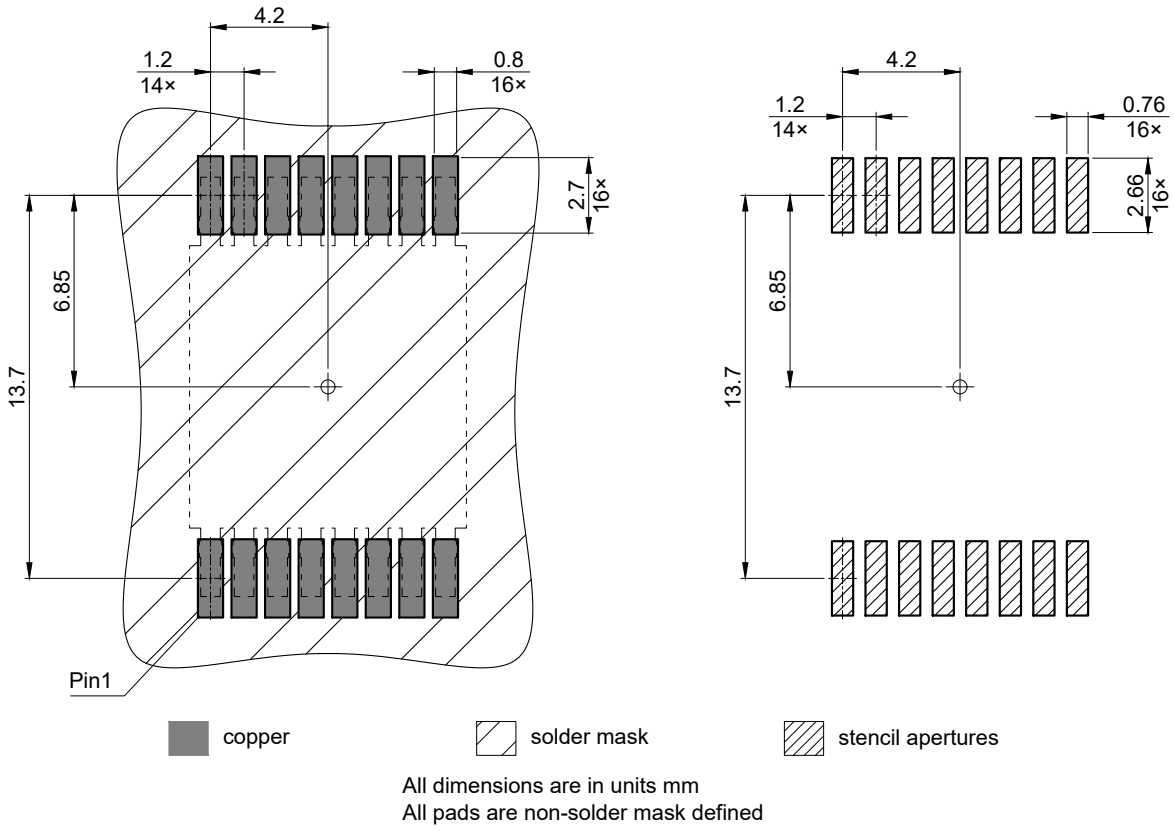


Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm

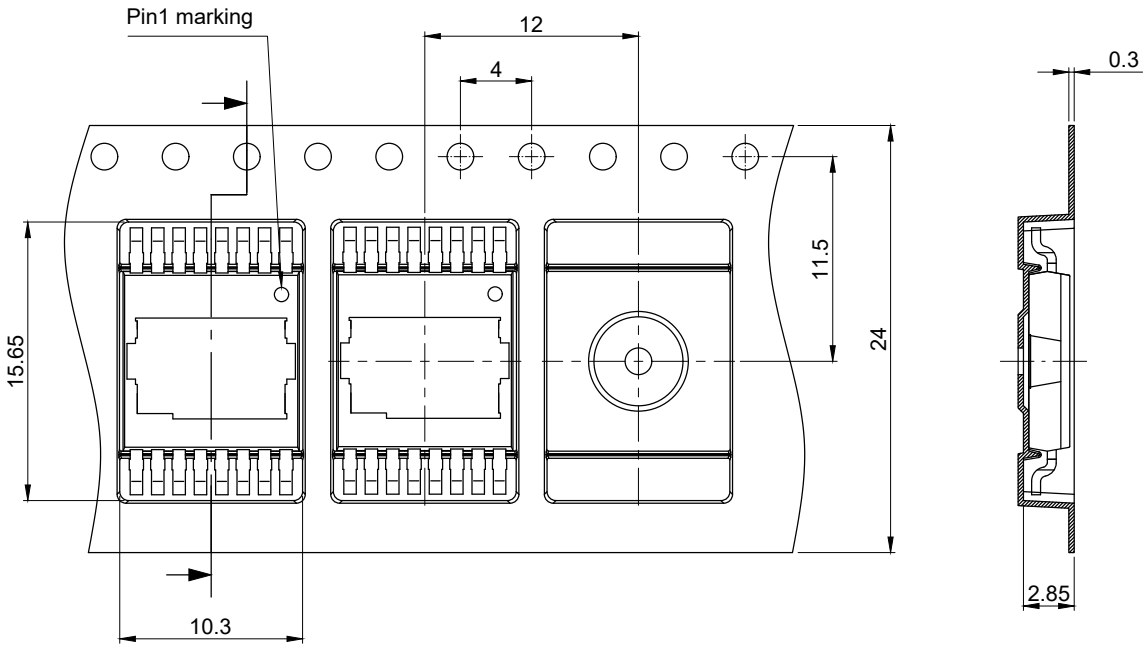


Figure 3 Packaging variant PG-HDSOP-16, dimensions in mm

8 Appendix A

Table 12 Related links

- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Webpage
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Application Note
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Simulation Model
- IFX Design tools

Revision history

IMLT65R060M2H

Revision 2025-03-17, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2024-05-03	Release of final
2.1	2024-11-20	update of reverse diode characteristics
2.2	2025-03-17	Revision of reverse diode characteristics

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: **erratum@infineon.com**

Published by
Infineon Technologies AG
81726 München, Germany

Important notice
The products which may also include samples and may be comprised of hardware or software or both ("Product") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Product or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

If the Product includes security features:
Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:
The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software. If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).