IAUTN15S6N025T

Automotive MOSFET

OptiMOS™ 6 Power-Transistor

RoHS

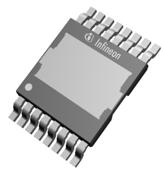
Infineon Automotive Quality

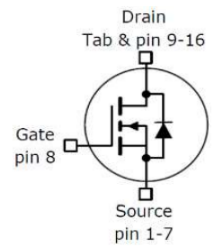
AEC Qualified

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- Extended qualification beyond AEC-Q101
- PPAP Capable
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

PG-HDSOP-16-1





Potential Applications

General automotive applications.

Product Validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	150	V
$R_{DS(on)}$	2.5	mΩ
I_D (chip limited)	245	A

Type	**Package**	**Marking**
IAUTN15S6N025T	PG-HDSOP-16-1	6N15N025

Table of Contents

Description . . . 1
Maximum ratings . . . 3
Thermal characteristics . . . 4
Electrical characteristics . . . 4
Electrical characteristics diagrams . . . 6
Package outline & footprint . . . 10
Revision history . . . 11
Disclaimer . . . 12

Maximum Ratings

at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS} = 10 V, Chip limitation[1,2]	245	A
		V_{GS} = 10 V, DC current	245	
		T_a = 100°C, V_{GS} = 10 V, R_{thJH} on 2s2p[2,4]	74	
Pulsed drain current[2]	$I_{D,pulse}$	T_C = 25°C, t_p = 100 µs	948	
Avalanche energy, single pulse[2]	E_{AS}	I_D = 123 A	490	mJ
Avalanche current, single pulse	I_{AS}	–	245	A
Gate source voltage	V_{GS}	–	±20	V
Power dissipation	P_{tot}	T_C = 25°C	357	W
Operating temperature	T_j	–	-55 ... +175	°C

Thermal Characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–		0.4	K/W
Thermal characterisation parameter, source pin[5)]	Ψ_{source}	–	–	0.9	–	
Thermal characterisation parameter, drain pin[6)]	Ψ_{drain}	–	–	0.9	–	
Thermal resistance, junction - heatsink[4)]	R_{thJH}	–	–	2.4	–	
Thermal resistance, junction - ambient[3)]	R_{thJA}	–	–	28.2	–	

Electrical Characteristics

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static Characteristics						
Drain-source breakdown voltage	$V_{(Br)DSS}$	V_{GS} = 0 V, I_D = 1 mA	150	–	–	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 270 µA	3	3.5	4	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V, T_j = 25°C	–	–	1	µA
		V_{DS} = 120 V, V_{GS} = 0 V, T_j = 100°C[2)]	–	–	100	
Gate-source leakage current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 8 V, I_D = 50 A	–	2.4	3.2	mΩ
		V_{GS} = 10 V, I_D = 100 A	–	2.1	2.5	
Gate resistance[2)]	R_G	–	–	1.1	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics[2)]						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 75 V, f = 1 MHz	–	7610	9900	pF
Output capacitance	C_{oss}		–	2370	3080	
Reverse transfer capacitance	C_{rss}		–	40	60	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 75 V, V_{GS} = 10 V, I_D = 123 A, R_G = 3.5 Ω	–	27	–	ns
Rise time	t_r		–	65	–	
Turn-off delay time	$t_{d(off)}$		–	43	–	
Fall time	t_f		–	60	–	

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD} = 75 V, I_D = 100 A, V_{GS} = 0 to 10 V	–	39	51	nC
Gate to drain charge	Q_{gd}		–	27	40	
Gate charge total	Q_g		–	107	139	
Gate plateau voltage	$V_{plateau}$		–	5.3	–	V

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Reverse Diode						
Diode continuous forward current[2)]	I_S	T_C = 25°C	–	–	245	A
Diode pulse current[2)]	$I_{S,pulse}$	T_C = 25°C, t_p = 100 µs	–	–	948	
Diode forward voltage	V_{SD}	V_{GS} = 0 V, I_F = 100 A, T_j = 25°C	–	0.9	1.0	V
Reverse recovery time[2)]	t_{rr}	V_R = 75 V, I_F = 50 A, di_F/dt = 100 A/µs	–	39	59	ns
Reverse recovery charge[2)]	Q_{rr}		–	23	46	nC

[1)] Practically the current is limited by the overall system design including the customer-specific PCB.

[2)] The parameter is not subject to production testing – specified by design.

[3)] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7) without thermal vias. PCB is vertical in still air.

[4)] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7) without thermal vias, heatsink of 71x110x2 mm is attached through TIM with 3.3 W/(m*K) and 400µm thickness to top side pad. Heatsink fixed to 85°C ambient temperature.

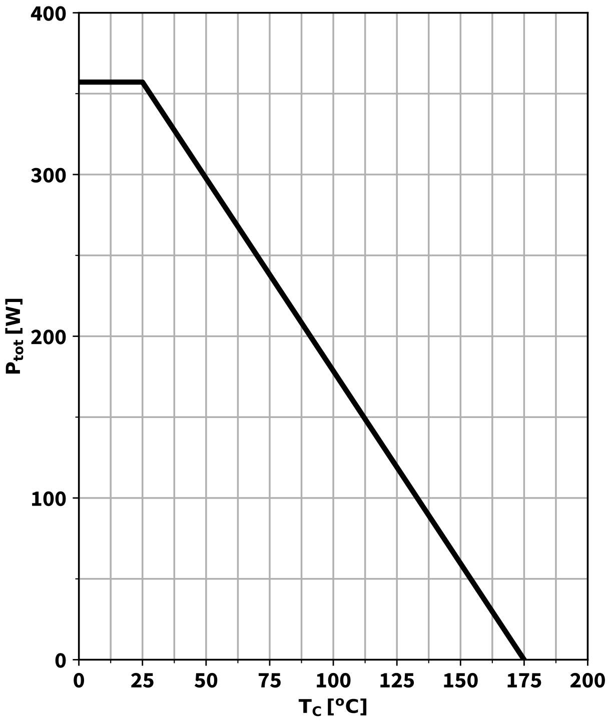
[5)] Thermal characterization parameter, calculated as $\psi_{source} = (T_{source} - T_{ambient})/P_{dis}$ in condition of 4). Used to determine PCB temperature at source pins for given power.

[6)] Thermal characterization parameter, calculated as $\psi_{drain} = (T_{drain} - T_{ambient})/P_{dis}$ in condition of 4). Used to determine PCB temperature at drain pins for given power.

Electrical characteristics diagrams

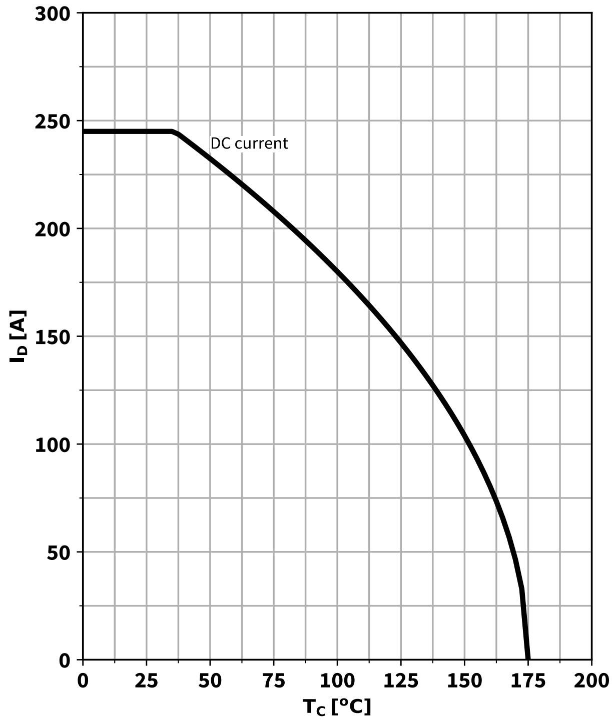
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



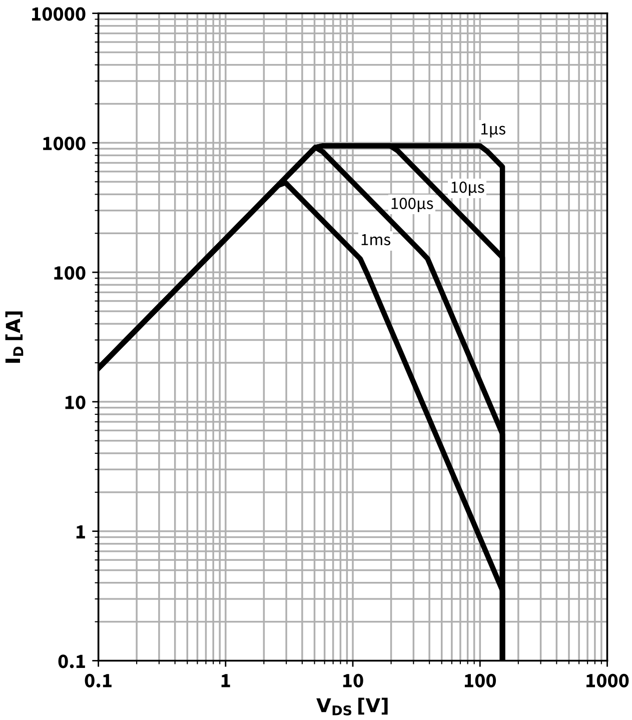
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6$ V



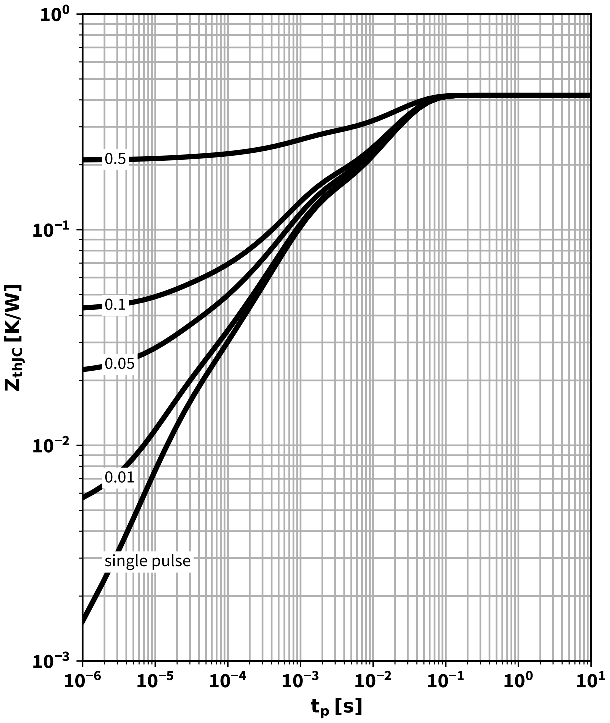
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



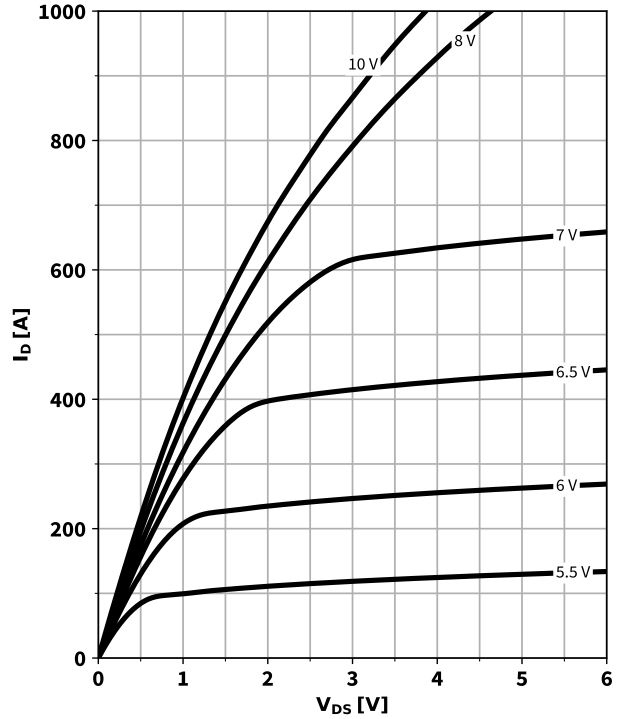
4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$



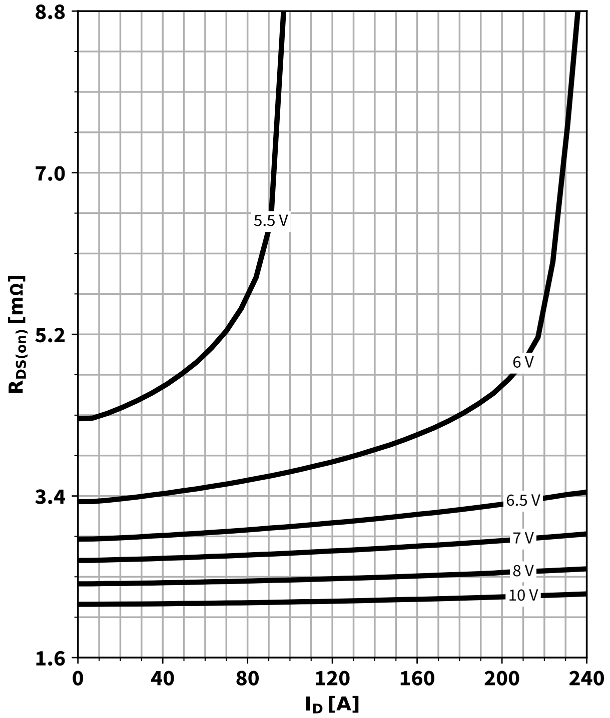
5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



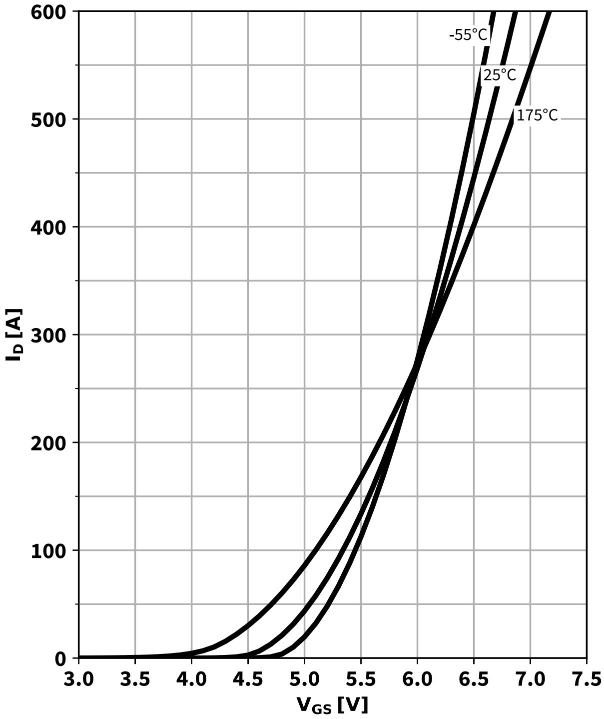
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



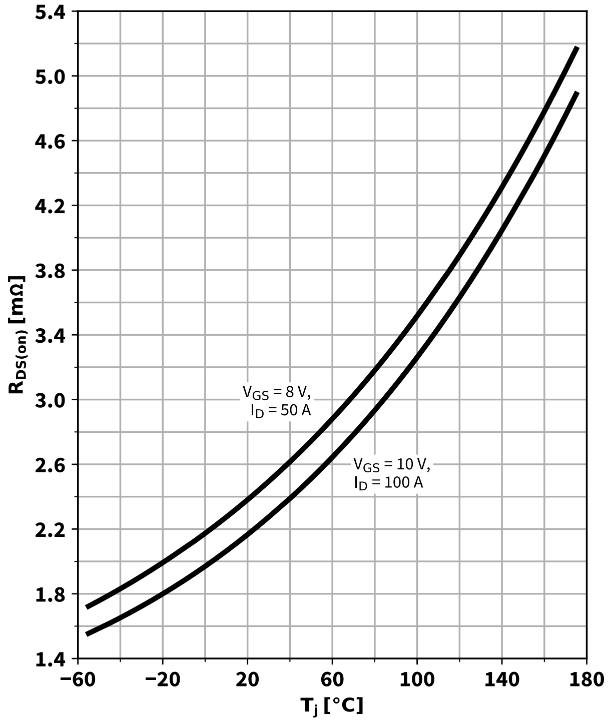
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$ V; parameter: T_j



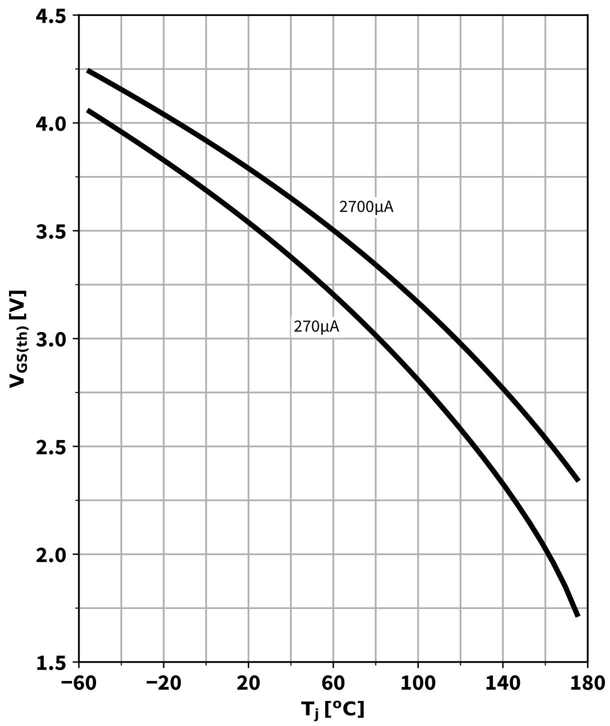
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



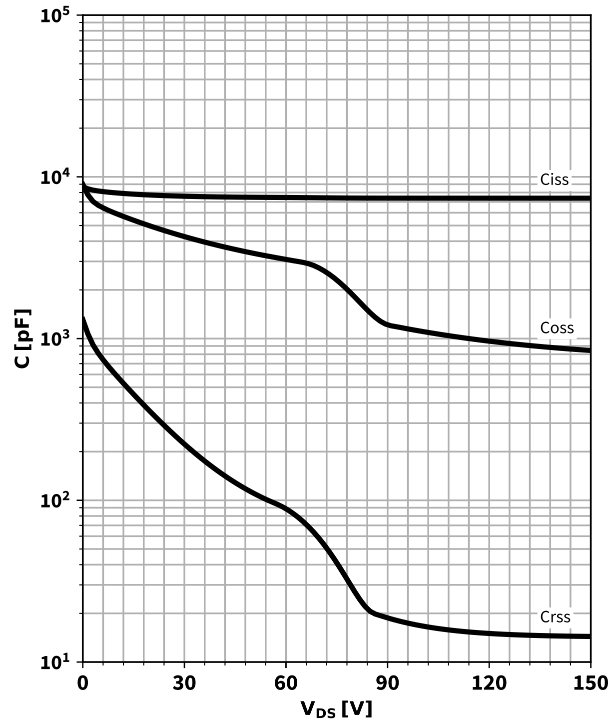
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



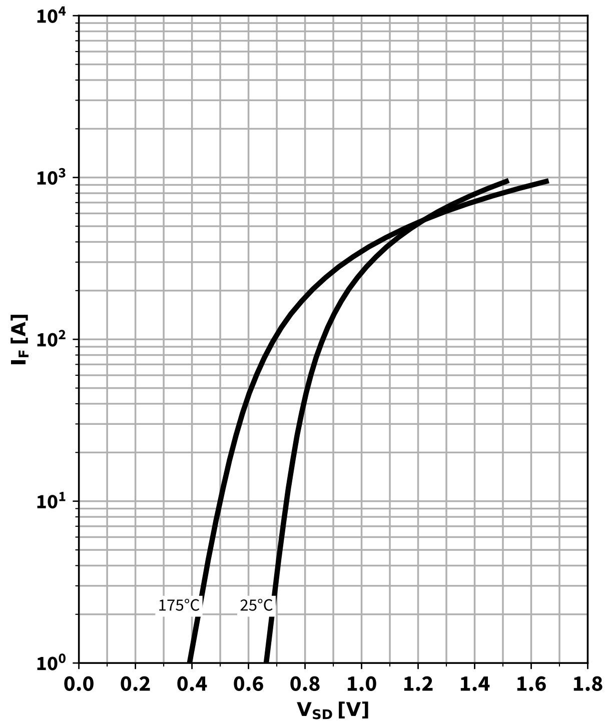
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



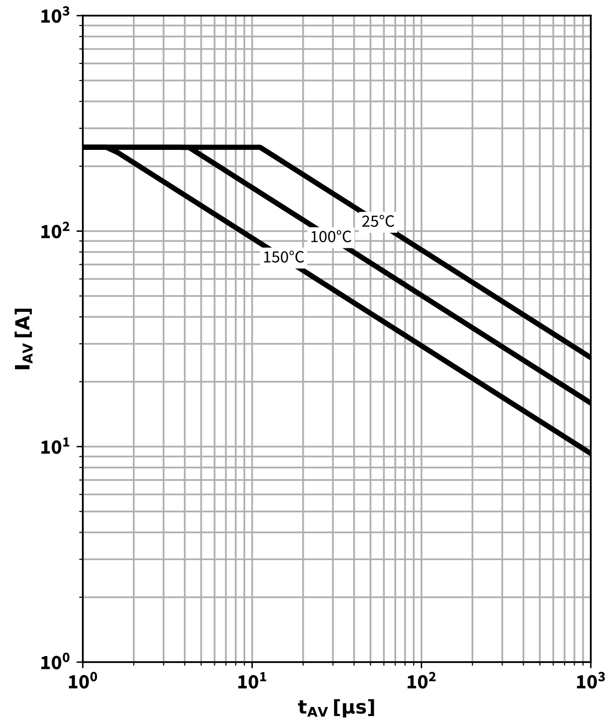
11 Typ. forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



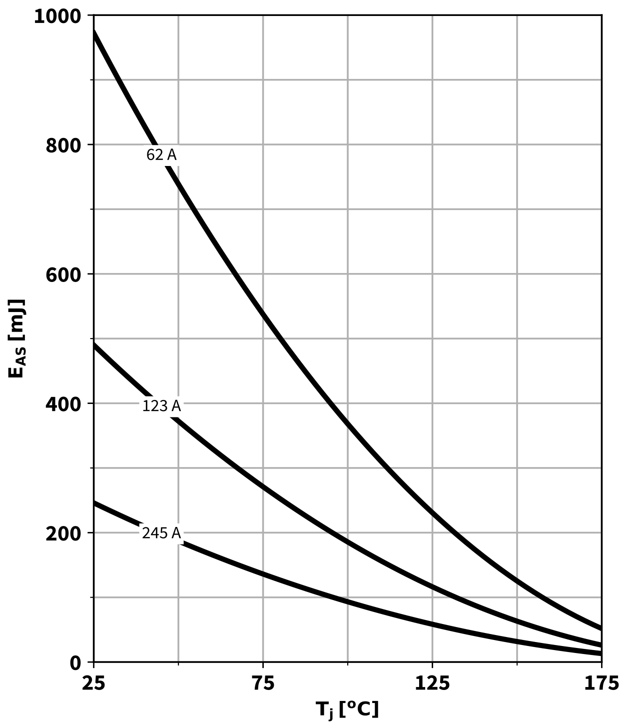
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



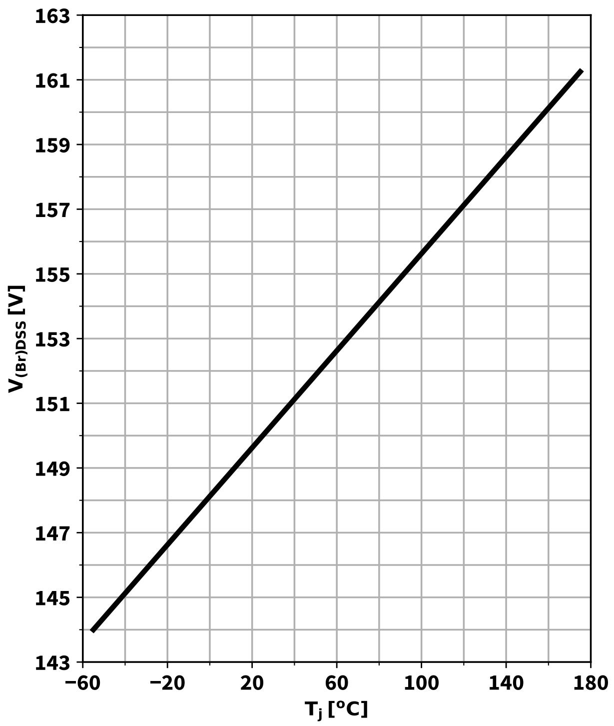
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



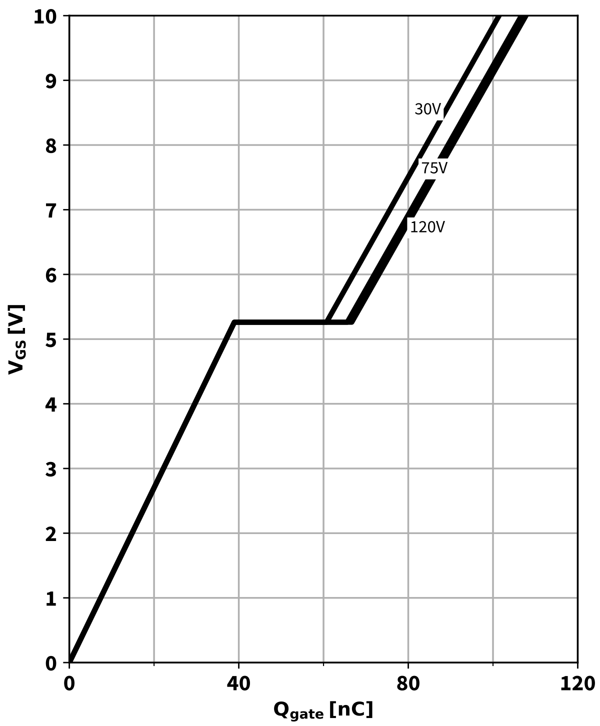
14 Drain-source breakdown voltage

$V_{(Br)DSS} = f(T_j)$; I_D = 10 mA

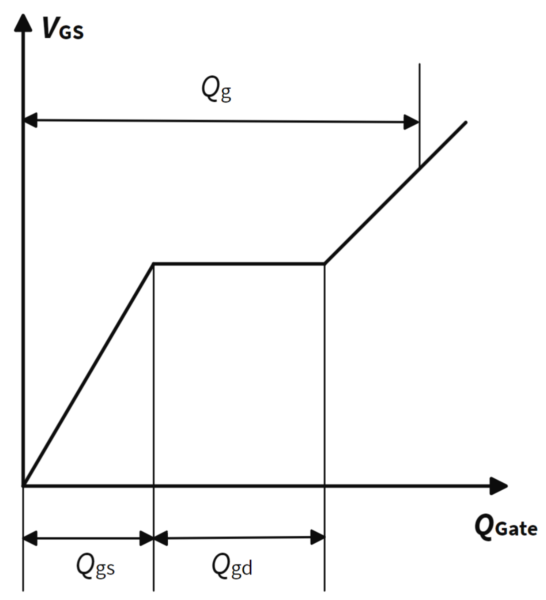


15 Typ. gate charge

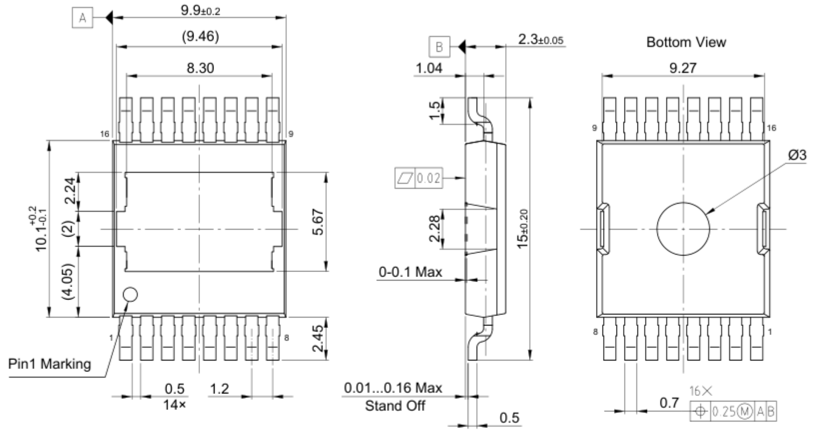
$V_{GS} = f(Q_{gate})$; I_D = 100 A pulsed; parameter: V_{DD}



16 Gate charge waveforms

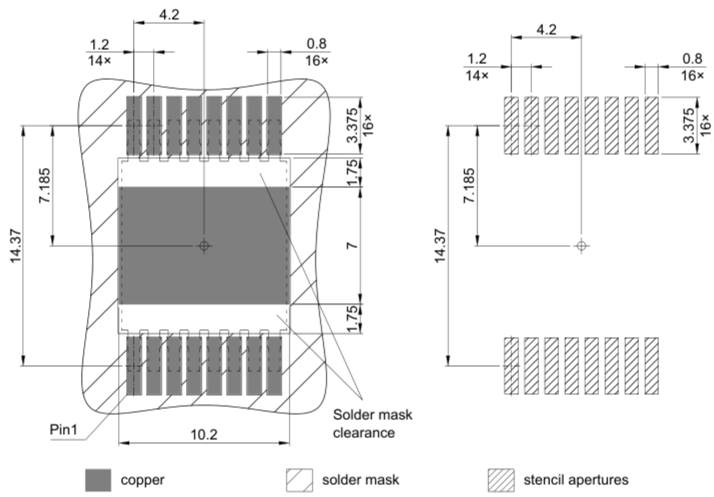


Package Outline



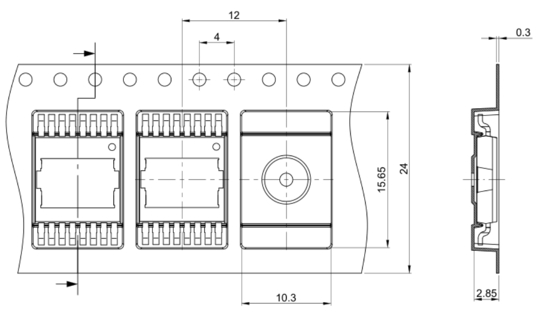
All metal surfaces tin plated except area of cut
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Footprint



All dimensions are in units mm
Based on stencil thickness 0.2 mm
All pads are non-solder mask defined

Packaging



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Revision History

Revision	Date	Changes
Revision 1.0	14.05.2025	Final data sheet

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