# iS20M028S1P

## SuperQ™ 200-V N-Channel Power MOSFET

### FEATURES

- Wide SOA and current capability
- Robustness under fault conditions
- 100% UIS tested in production
- Low switching losses, $Q_{SW}$ and $E_{OSS}$
- Easier parallelling with ± 0.5V gate threshold

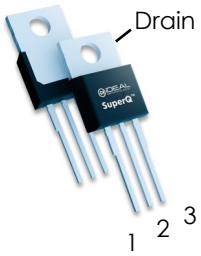
### APPLICATIONS

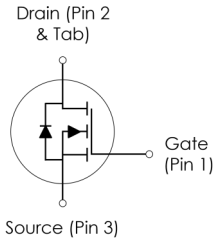
- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

### DESCRIPTION

Engineered for SMPS and high-efficiency motor drives, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust TO-220 package. Featuring best-in-class $R_{DS(on)}$,$Q_{SW}$ and $E_{OSS}$, it minimizes heat dissipation at both full and partial loads.

### PRODUCT SUMMARY




**TO-220**

| Parameter $T_A$ = 25°C | Value | Unit |
|---|---|---|
| $V_{DS}$ | 200 | V |
| $R_{DS(on),max}$ | 25 | mΩ |
| $I_D$ | 40 | A |
| $Q_G$ | 26.5 | nC |
| $Q_{SW}$ | 2.7 | nC |
| $E_{OSS}$ | 1 | µJ |

| ORDERING INFORMATION | | | |
|---|---|---|---|
| **Part Number** | **Package** | **Marking** | **Packaging** |
| iS20M028S1P | TO-220 | iS20M028S1 | 50pc Tube |

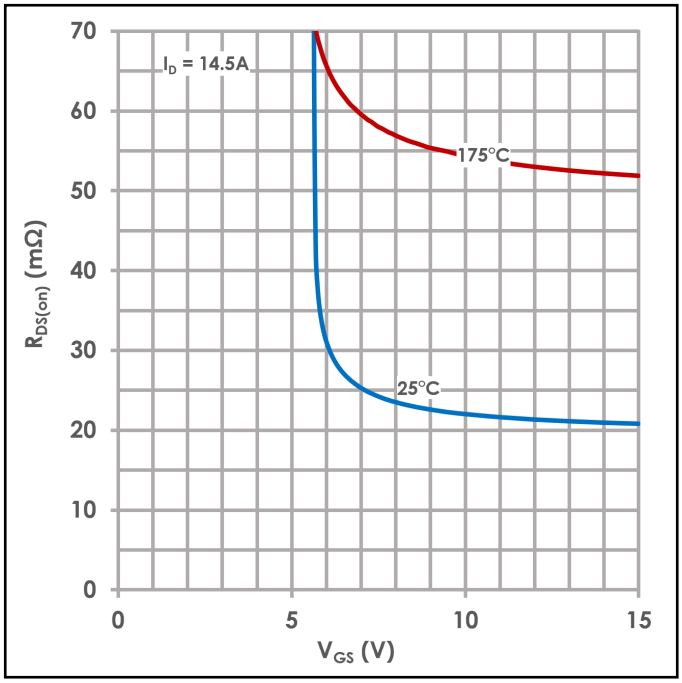



**Figure 1: Typical Drain-Source On Resistance**

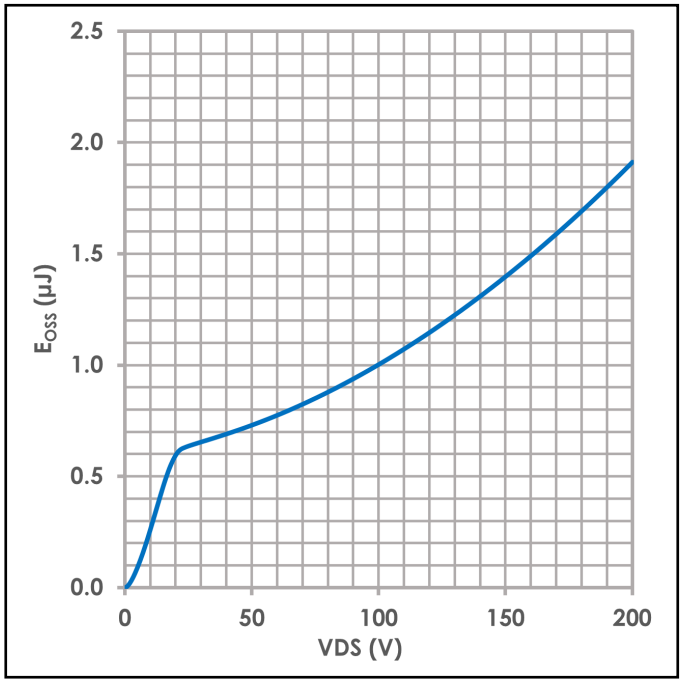



**Figure 2: Typical $C_{OSS}$ Stored Energy**

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|---|---|
| **SYMBOL** | **PARAMETER** ($T_A$ = 25°C unless otherwise specified) | **VALUE** | **UNIT** |
| $V_{GS}$ | Gate-to-source voltage | ± 20 | V |
| $I_D$ | Continuous drain current (silicon limited), $T_C$ = 25°C | 40 | A |
| | Continuous drain current (silicon limited), $T_C$ = 100°C | 28 | |
| $I_{DM}$ | Pulsed drain current | 154 | A |
| $P_D$ | Power dissipation, $T_C$ = 25°C | 100 | W |
| $T_J$, $T_{stg}$ | Operating junction, storage temperature | -55 to 175 | °C |
| $E_{AS}$ | Avalanche energy, single pulse $I_D$ = 17.8A, $R_{GS}$ = 25Ω | 159 | mJ |

| THERMAL CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|
| **SYMBOL** | **PARAMETER** ($T_A$ = 25°C unless otherwise specified) | **VALUE** | | | **UNIT** |
| | | **MIN** | **TYP** | **MAX** | |
| $R_{\theta JC}$ | Junction-to-case thermal resistance - TO-220 | - | - | 1.5 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (1) | - | - | 40 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance, minimal footprint | - | - | 62 | °C/W |

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 $cm^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

| ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified) | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOL | PARAMETER | TEST CONDITIONS | VALUE | | | UNIT |
| | | | MIN | TYP | MAX | |
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0V, $I_D$ = 1mA | 200 | - | - | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0V, $V_{DS}$ = 160V, $T_J$ = 25°C | - | 0.03 | 1 | µA |
| | | $V_{GS}$ = 0V, $V_{DS}$ = 160V, $T_J$ = 125°C (2) | - | 13 | 100 | |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0V, $V_{GS}$ = 20V | - | 0.4 | 100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 70µA | 3.1 | 3.6 | 4.1 | V |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS}$ = 10V, $I_D$ = 14.5A | - | 22 | 25 | mΩ |
| $g_{fs}$ | Transconductance (2) | $V_{DS}$ = 10V, $I_D$ = 14.5A | 16 | 31 | - | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input capacitance (2) | $V_{GS}$ = 0V, $V_{DS}$ = 100V, f = 100kHz | - | 1,865 | 2,425 | pF |
| $C_{rss}$ | Reverse transfer capacitance (2) | | - | 12 | 16 | |
| $C_{oss}$ | Output capacitance (2) | | - | 67 | 86 | |
| $C_{o(er)}$ | Effective output capacitance | $V_{DS}$ = 0 to 100V, $V_{GS}$ = 0V | - | 197 | - | |
| $R_G$ | Series gate resistance | f = 1MHz | - | 4.5 | 6.8 | Ω |
| $t_{d(on)}$ | Turn-on delay time | $V_{DS}$ = 100V, $V_{GS}$ = 10V, $I_{DS}$ = 14.5A, $R_{G,EXT}$ = 0 Ω | - | 8.5 | - | ns |
| $t_r$ | Rise time | | - | 1.9 | - | |
| $t_{d(off)}$ | Turn-off delay time | | - | 24.7 | - | |
| $t_f$ | Fall time | | - | 11.3 | - | |
| **GATE CHARGE CHARACTERISTICS** | | | | | | |
| $Q_g$ | Gate charge total (2) | $V_{DS}$ = 100V, $I_D$ = 14.5A, $V_{GS}$ = 0 to 10V | - | 26.5 | 34 | nC |
| $Q_{sw}$ | Switching charge (3) | | - | 2.7 | - | |
| $Q_{gd}$ | Gate to drain charge (2) | | - | 1.4 | 1.8 | |
| $V_{plateau}$ | Gate plateau voltage | | - | 5.7 | - | V |
| $Q_{oss}$ | Output charge (2) | $V_{DS}$ = 0 to 100V, $V_{GS}$ = 0V | - | 95 | 108 | nC |
| $E_{oss}$ | Capacitive stored energy | | - | 1 | - | µJ |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_{SD}$ = 14.5A, $V_{GS}$ = 0V | - | 1.0 | 1.2 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DS}$ = 100V, $I_F$ = 14.5A, di/dt = 100A/µs | - | 425 | - | nC |
| $t_{rr}$ | Reverse recovery time | | - | 107 | - | ns |

(2) Defined by design. Not subject to production test.
(3) $Q_{sw}$ should be used for switching loss calculations. See Figure 16 and $Q_{sw}$ application note on www.idealsemi.com

## Ratings and Characteristics Curves

($T_A$ = 25°C unless otherwise specified)

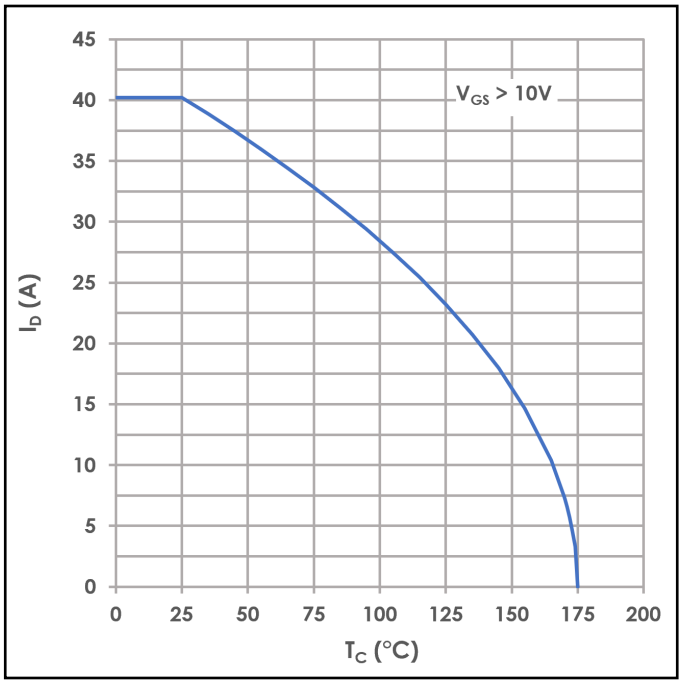



**Figure 3: Drain Current**

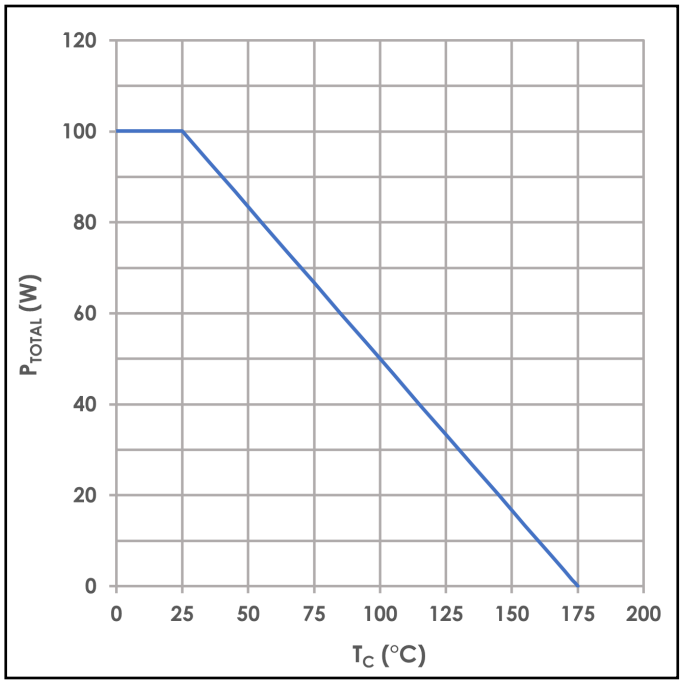



**Figure 4: Power Dissipation**

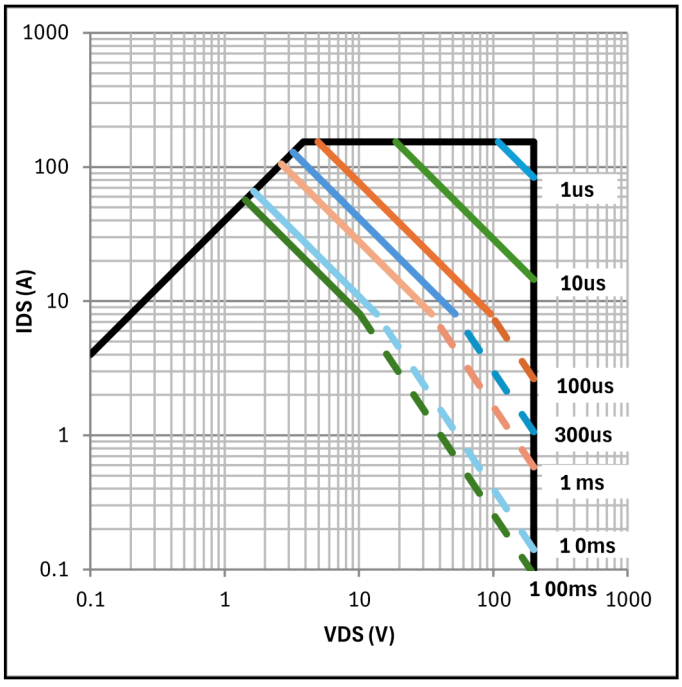



**Figure 5: Safe Operating Area**

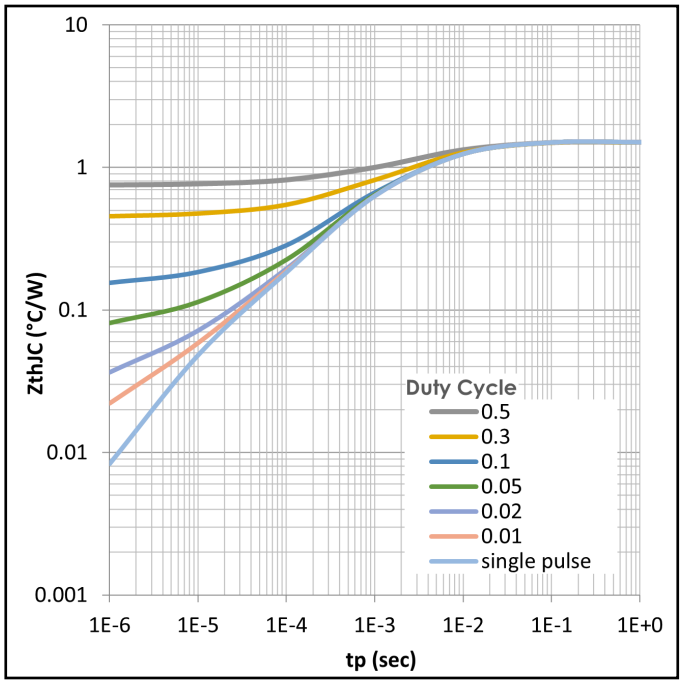



**Figure 6: Max Transient Thermal Impedance**

## Ratings and Characteristics Curves

($T_A$ = 25°C unless otherwise specified)

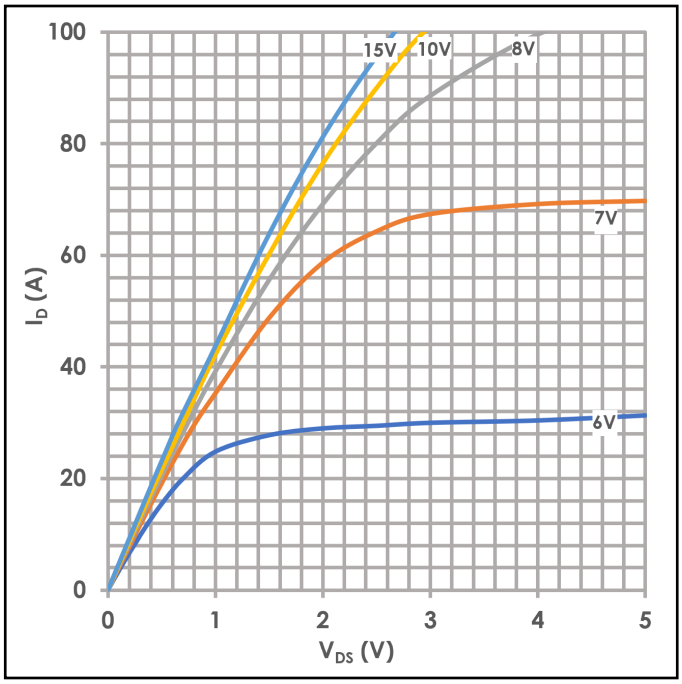



**Figure 7: Typical Output Characteristics**

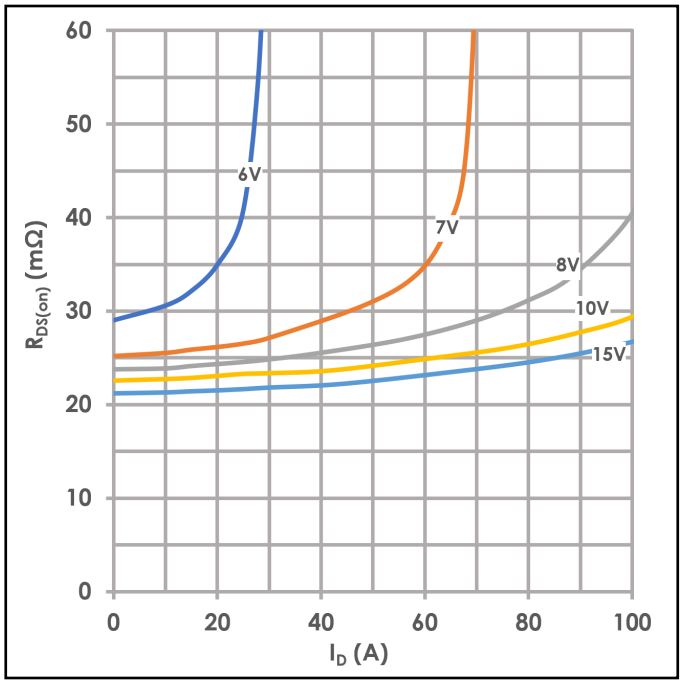



**Figure 8: Typical Drain-Source On-Resistance**

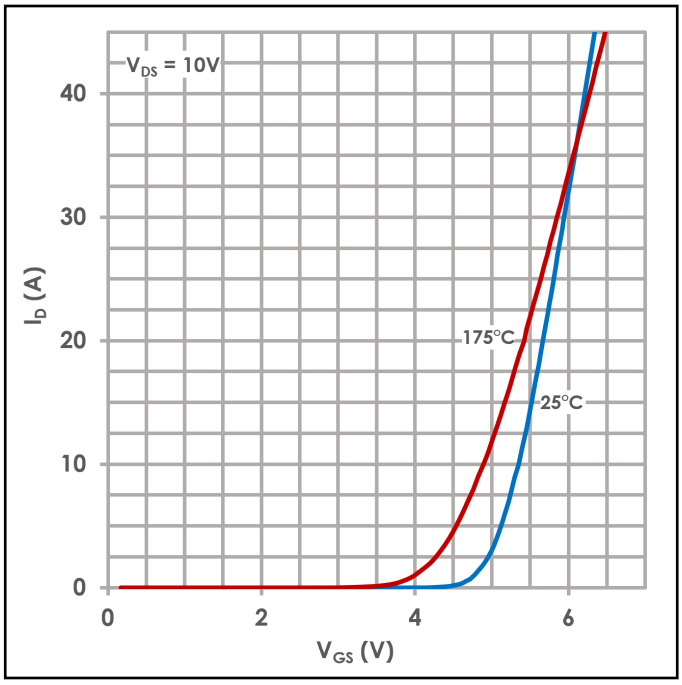



**Figure 9: Typical Transfer Characteristics**

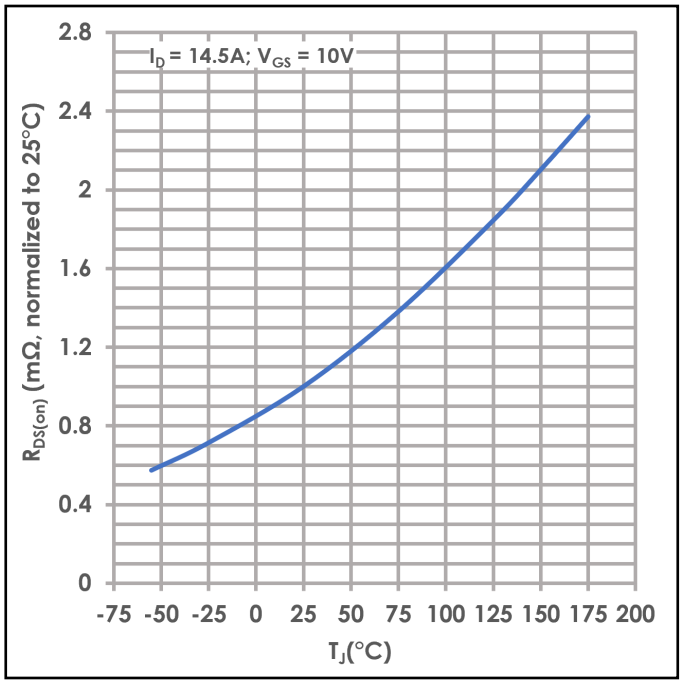



**Figure 10: Normalized On-State Resistance vs. Temperature**

## Ratings and Characteristics Curves

($T_A$ = 25°C unless otherwise specified)

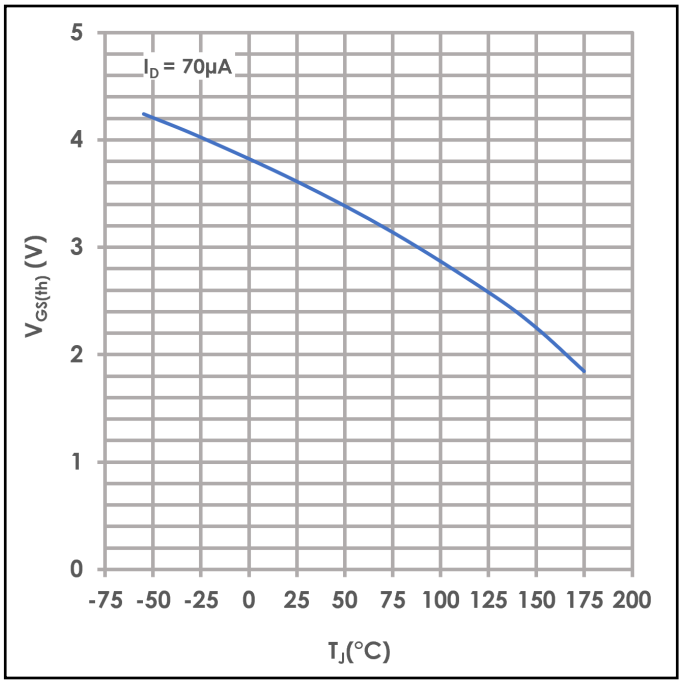



**Figure 11: Typical Threshold Voltage**

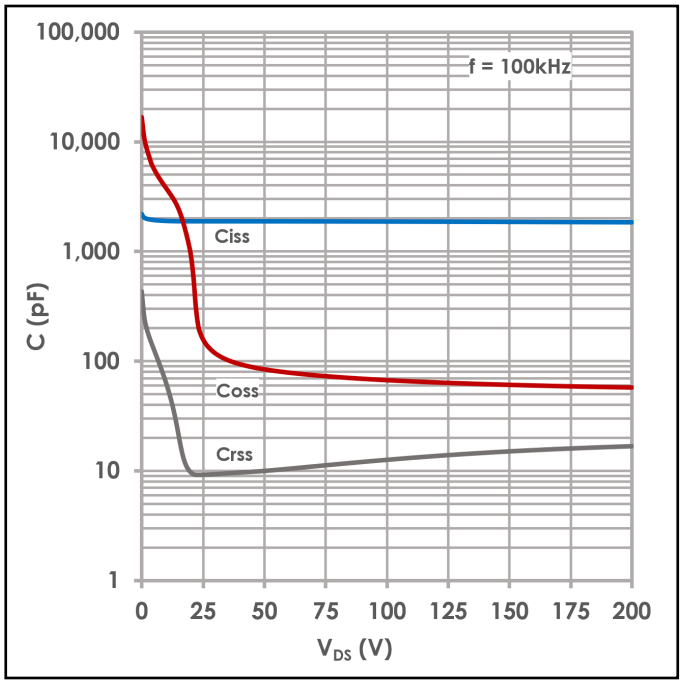



**Figure 12: Typical Capacitances**

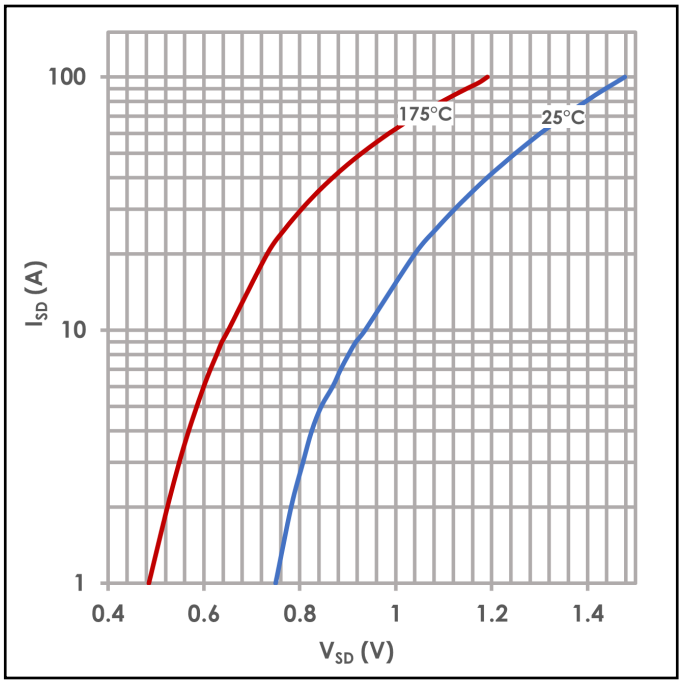



**Figure 13: Typical Diode Forward Voltage**

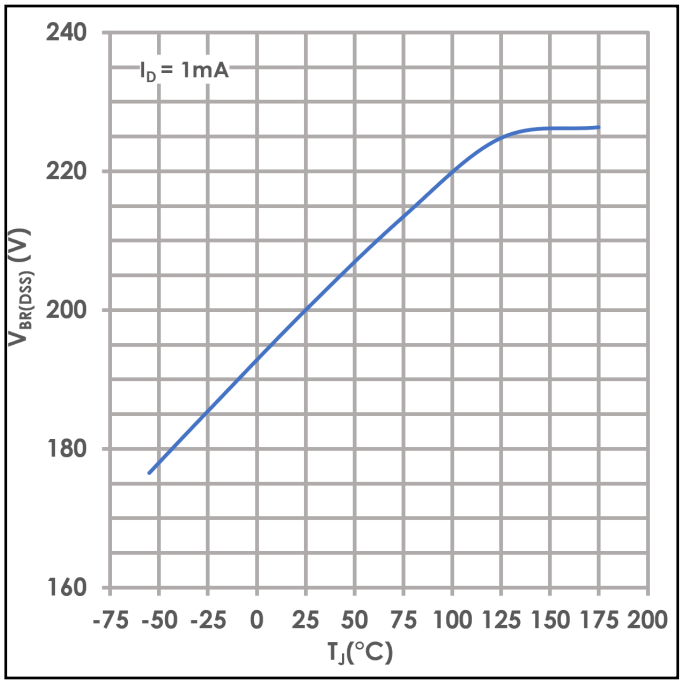



**Figure 14: Min Drain-Source Breakdown Voltage**

## Ratings and Characteristics Curves

($T_A$ = 25°C unless otherwise specified)

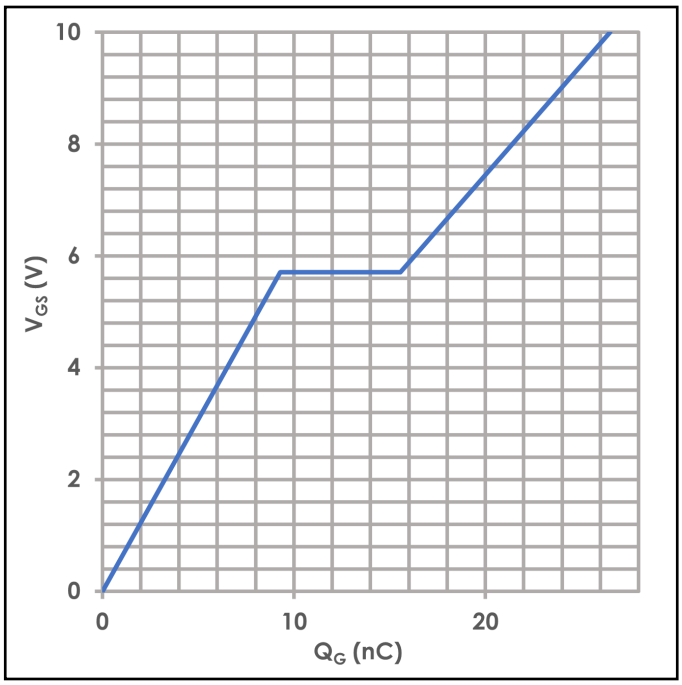



**Figure 15: Typical Gate Charge**

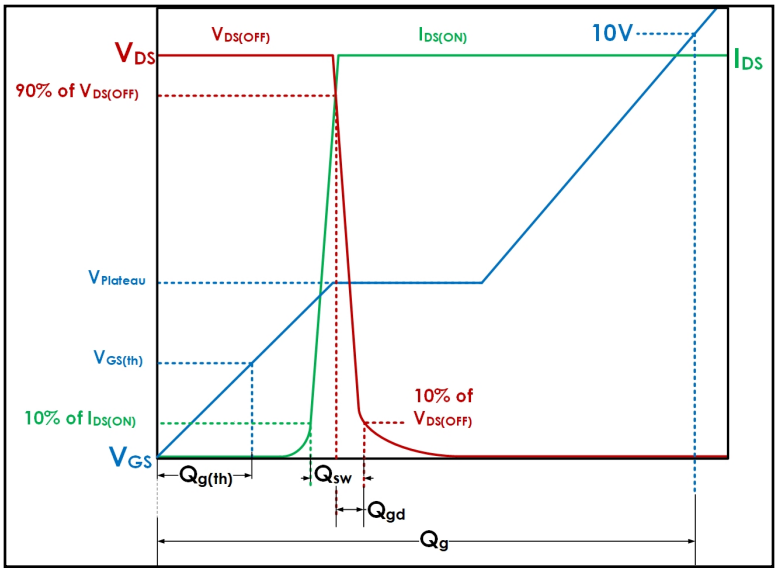
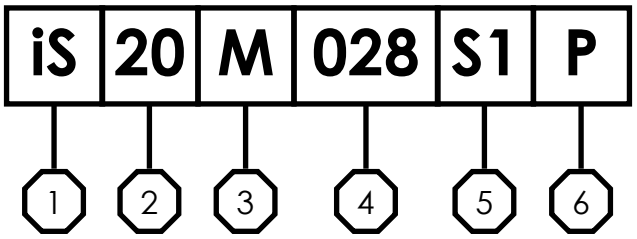



**Figure 16: Gate Charge Definitions**

# DEVICE DECODER RING

Device Code




1 – iDEAL Semiconductor product

2 – Voltage rating divided by 10 (200V)

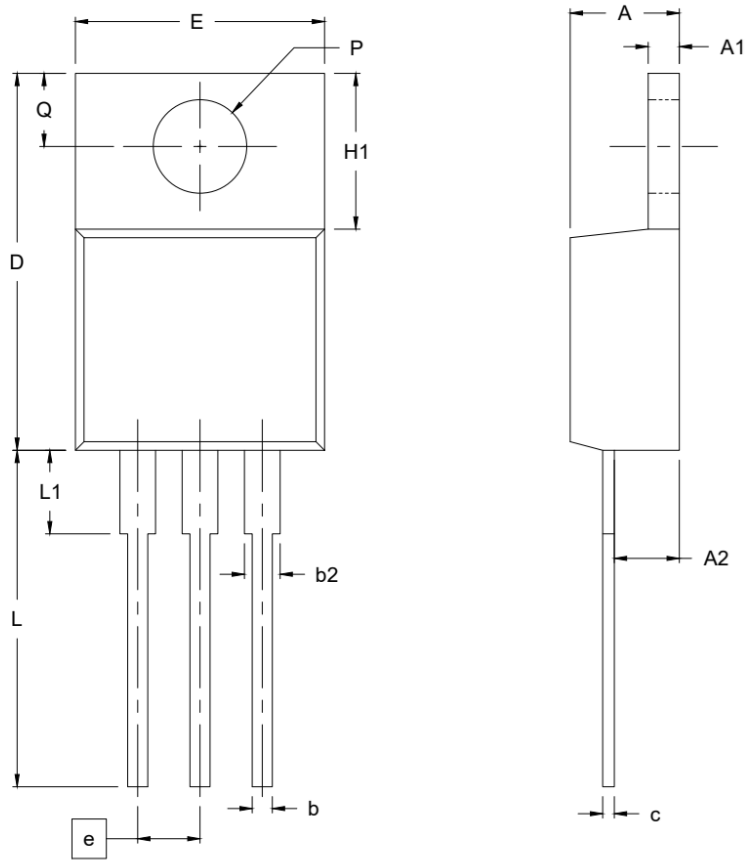
3 – M = N-Channel MOSFET, Standard Threshold

4 – Maximum drain-to-source resistance

5 – SuperQ™ Generation

6 – P = TO-220

# TO-220 Package Drawing




| SYMBOL | MIN | MAX |
|---|---|---|
| A | 4.19 | 4.82 |
| A1 | 1.14 | 1.40 |
| A2 | 2.38 | 2.92 |
| b | 0.63 | 1.01 |
| b2 | 1.13 | 1.78 |
| c | 0.31 | 0.64 |
| D | 14.22 | 16.51 |
| E | 9.66 | 10.66 |
| e | 2.54 BSC | |
| H1 | 5.85 | 6.85 |
| L | 12.70 | 14.73 |
| L1 | 2.39 | 4.42 |
| P | 3.54 | 4.08 |
| Q | 2.54 | 3.42 |

Notes:
1. All linear dimensions in millimeters
2. Dimensions D and E do not include mold flash or protrusions

| Revision History | | |
|---|---|---|
| **Version** | **Date** | **Comments** |
| 1.0 | July 2025 | Initial Release |
| 1.1 | September 2025 | Gate charge characteristics table updated. Figure 16 added |

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