



1200V 4.6 $m\Omega$ Half-Bridge SiC Module

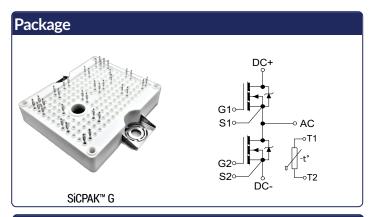
SiCPAK™ G Series

Trench-Assisted Planar Technology

 V_{DS} = 1200 V $R_{DS(ON)}$ = 4.6 mΩ $I_{D,DC (65°C)}$ = 216 A

Built for Performance and Endurance

- Epoxy-resin potting and trench-assisted planar SiC MOSFET technology for long-lasting reliability
- Engineered and qualified to withstand harsh stress, temperature variations, and power cycling
- ullet Low on-resistance $R_{DS(ON)}$ across temperature
- Optimized switching speed and balanced Q_{GD}/Q_{GS} for faster, cleaner, and efficient switching performance
- Stable and consistent V_{GS,th} for excellent current sharing and reliable switching
- Outstanding short-circuit & avalanche (UIS) performance
- THB (HV-H3TRB) qualification at module-level & dielevel
- Optional pre-applied Thermal Interface Material (TIM),
 "-T" orderable part number suffix



Applications

- EV Road Side Chargers
- Solar Inverters
- Energy Storage Systems (ESS)
- Uninterrupted Power Supplies (UPS)
- Motor Control and Drives
- Smard Grid and Distributed Generation
- Induction Heating and Welding

Absolute Maximum (per Switch Po	osition) (At T _C = 25°C Ui	nless Otherwise Stated)			
Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{ extsf{DS,max}}$	V_{GS} = 0 V, I_D = 100 μA	1200	V	
Gate-Source Voltage (Dynamic)	$V_{GS,max}$	Transient	-10/+22	V	
Gate-Source Voltage (Operation)	$V_{GS,op}$	Static	-5/+18	V	Note 1
Virtual Junction Temperature	Tj	Operation	-40 to 175	°C	
Power Dissipation	Pn	$T_H = 65^{\circ}C$, $T_{j,op} \le 175^{\circ}C$	444	W	Cia 17
	PD	$T_H = 120^{\circ}C, T_{j,op} \le 175^{\circ}C$	222	VV	Fig. 17
DC Continuous Drain Current	lana	$T_H = 65^{\circ}C$, $T_{j,op} \le 175^{\circ}C$, $V_{GS} = 18 \text{ V}$	216	^	Fig. 16
	I _{D,DC}	$T_H = 120$ °C, $T_{j,op} \le 175$ °C, $V_{GS} = 18 \text{ V}$	153	Α	гіу. 10

<u>NOTE</u>: This datasheet provides <u>preliminary specifications</u>. Parameters, conditions and values are subject to change.

Note 1: Recommended operating (static) on-state gate voltage is +15V to +18V and off-state gate voltage is -5V to -3V

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Rev 25/Mar (Preliminary) Page 1 of 12



Davamatav	Cumhal	O. I'v	Values				N .
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	Note
Drain-Source Breakdown Voltage	V_{DSS}	$V_{GS} = 0 \text{ V, } I_D = 100 \mu\text{A}$	1200			V	
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V		1		μA	
Gate Source Leakage Current	lgss	$V_{GS} = 22V, V_{DS} = 0V$ $V_{GS} = -10V, V_{DS} = 0V$			100 -100	nA	
Gate Threshold Voltage	V _{GS,th}	$V_{DS} = V_{GS}$, $I_D = 140 \text{ mA}$ $V_{DS} = V_{GS}$, $I_D = 140 \text{ mA}$, $T_j = 175^{\circ}\text{C}$	2.2	2.7 2.0	4.3	V	Note 2
Drain-Source On-State Resistance	R _{DS(ON)}	V_{GS} = 18V, I_D = 180 A V_{GS} = 18V, I_D = 180 A, T_j = 175°C		4.6 7.88	6.2	mΩ	Note 3,4 Fig. 6-9
Input Capacitance	Ciss			19700			Fig. 12
Output Capacitance	C_{oss}	$V_{DS} = 800V, V_{GS} = 0V$ - f = 100kHz, $V_{AC} = 25$ mV		728		pF	
Reverse Transfer Capacitance	C_{rss}	1 - 100KHZ, VAC - 25HIV		47			
Internal Gate Resistance	$R_{G,int}$	$V_{GS} = 18V$, $f = 500kHz$, $V_{AC} = 25mV$		0.33		Ω	
Gate-Source Charge	Q_{GS}	$V_{DS} = 800V$, $V_{GS} = +18/-5V$		224			
Gate-Drain Charge	\mathbf{Q}_{GD}	I _D = 180 A		156		nC	Fig. 11
Total Gate Charge	\mathbf{Q}_{G}	Per JEDEC JEP-192		784			
Turn-On Switching Energy (Body Diode)	E _{0n}	$T_{\rm j}$ = 25°C, $V_{\rm GS}$ = -5/+18V, $R_{\rm G(ext)}$ = 1 Ω , L =	3579		1	Fi 04 07	
Turn-Off Switching Energy (Body Diode)	E _{Off}	60 μH, I _D = 200 A, V _{DD} = 800 V		1089		μJ	Fig. 24-27
Rise Time	t _r	V _{DD} = 800 V, V _{GS} = -5/+18V		15			
Fall Time	t _f	$R_{G(ext)}$ = 1 Ω , L = 60 μ H, I_D = 200 A Timing relative to V_{DS} , Inductive load		30		ns	Fig. 26

Body Diode Characteristics (per Switch Position) (At T _j = 25°C unless otherwise specified)							
Daramatar	Cumbal	Conditions	Values			Lloit	Nete
Parameter	Symbol		Min.	Тур.	Max.	Unit	Note
Diode Forward Voltage	V	$V_{GS} = -5V$, $I_{SD} = 90 A$		4.5		V	Fig. 10.10
	V_{SD}	V_{GS} = -5V, I_{SD} = 90 A, T_j = 175°C	4.1		V	Fig. 18,19	
DC Continuous Diode Current	1.	$T_H = 65 ^{\circ}\text{C}, T_{j,op} \le 175 ^{\circ}\text{C}, V_{GS} = -5 \text{V}$	84 55			٨	
	ISD	T_H = 120 °C, $T_{j,op} \le 175$ °C, V_{GS} = -5 V			Α		

<u>NOTE</u>: This datasheet provides <u>preliminary specifications</u>. Parameters, conditions and values are subject to change.

Note 2: Tested after applying +25V for 80ms

Note 3: Device(Die) ON State resistance only: Package resistance reported separately in module characteristics

Note 4: Total effective resistance per switch position (HS or LS) = MOSFET R_{DS(ON)} + package resistance by switch position

Rev 25/Mar (Preliminary)
Page 2 of 12





Module Characteristics							
Parameter	Symbol	Conditions		Values			Note
Parameter	Зунион	Conditions		Тур.	Max.	Unit	Note
Thermal Resistance, Junction - Heatsink	R _{thJHS}	TIM = 100 per switch $\lambda = 4.4 \text{ W/(m.K)}$		0.22		°C/W	Fig. 14
Case Temperature	Tc		-40		150	°C	
Stray Inductance	Lstray	Between DC+ and DC- f = 10 MHz		4.34		nH	
Package Resistance, HS	R _{HS}	T _C = 125 °C		0.68		0	Note 4
Package Resistance, LS	R _{LS}	T _C = 125 °C				- mΩ	Note 4
Weight	W			48.3		g	
Case Isolation Voltage	V _{iso}	AC 50 Hz, 60s		4000		V	
Comparative Tracking Index	СТІ	Epoxy-resin EMC		200			
Crosmono Dietomos		Terminal to Terminal	6.4			mm	
Creepage Distance		Terminal to Heatsink		12.7		mm	

NTC-Thermistor Charac	cteristics						
Darameter	Cumbal	0	Values			1 to Sa	Maka
Parameter	rameter Symbol Condition	Conditions	Min.	Тур.	Max.	Unit	Note
Rated Resistance	R _{NTC,25}	T _{NTC} = 25 °C		5		kΩ	
Resistance Tolerance	ΔR/R	T _{NTC} = 25 °C	-5		+5	%	
Power Dissipation	P _{NTC,25}	T _{NTC} = 25 °C			20	mW	
	B ₂₅ /B ₅₀	T ₂ = 50 °C		3375			
Beta Value (B-value)	B ₂₅ /B ₈₀	$T_2 = 80 ^{\circ}C$		3410		K	
	B ₂₅ /B ₁₀₀	T ₂ = 100 °C		3435			

	<u>- </u>
Orderable Part number (OPN) Package	Packing Method
G3F05MT12GB2 SiCPAK™ G	Box (Qty - 12)
G3F05MT12GB2-T SiCPAK™ G w	vith TIM Box (Qty - 12)

Note 4: Total effective resistance per switch postition (HS or LS) = MOSFET R_{DS(ON)} + package resistance by switch position

Rev 25/Mar (Preliminary) Page 3 of 12



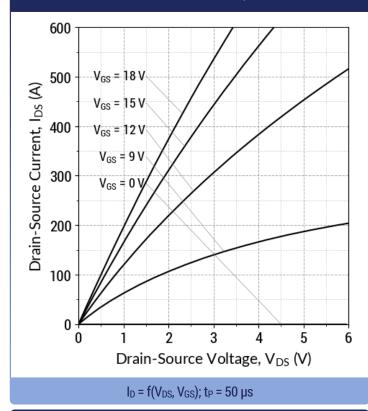
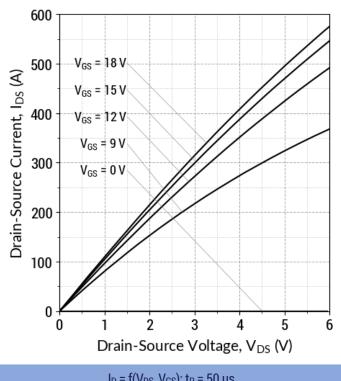


Fig 2: Typical Output Characteristics (T_j = 175°C)



 $I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu s$

Fig 3: Typical Output Characteristics (T_j = -55°C)

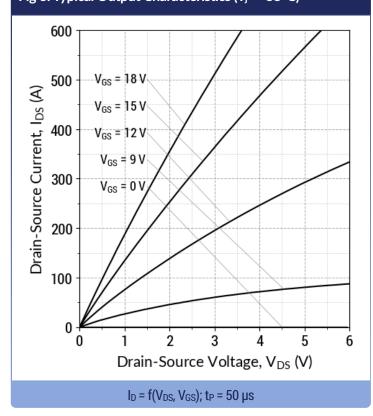
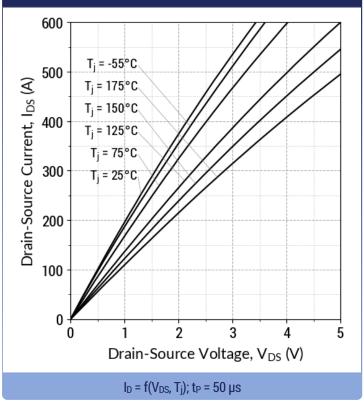
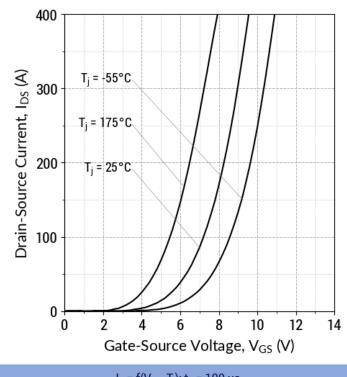


Fig 4: Typical Output Characteristics (V_{GS} = 18 V)



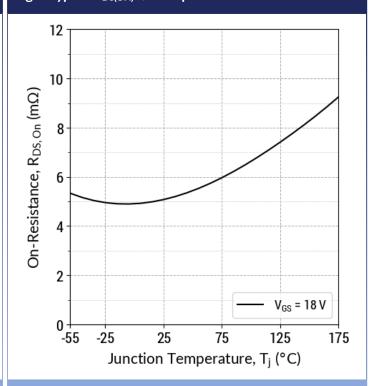
Rev 25/Mar (Preliminary) Page 4 of 12





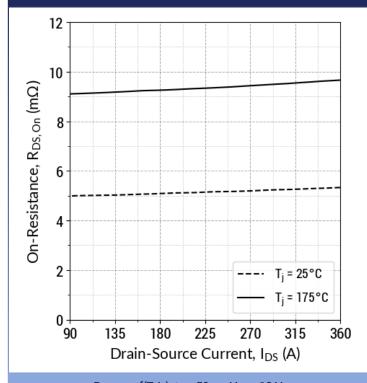
 $I_D = f(V_{GS}, T_i); t_P = 100 \mu s$

Fig 6: Typical R_{DS(ON)} v/s Temperature



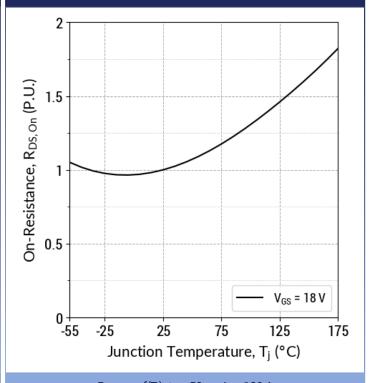
 $R_{DS(ON)} = f(T_i, V_{GS}); t_P = 50 \mu s; I_D = 180 A$

Fig 7: Typical RDS(ON) v/s Drain Current



 $R_{DS(ON)} = f(T_i, I_D); t_P = 50 \mu s; V_{GS} = 18 \text{ V}$

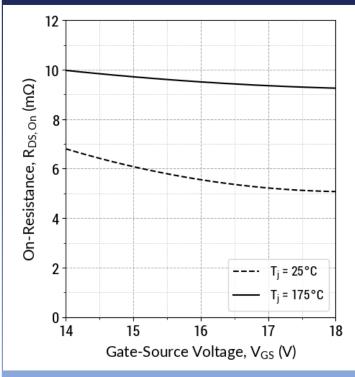
Fig 8: Typical Normalized RDS(ON) v/s Temperature



 $R_{DS(ON)} = f(T_i); t_P = 50 \mu s; I_D = 180 A$

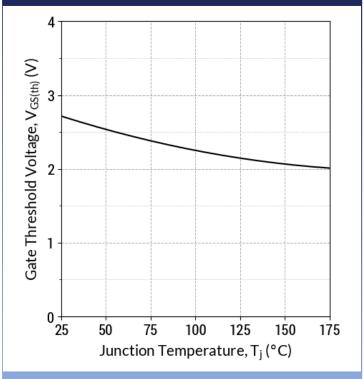
Rev 25/Mar (Preliminary) Page 5 of 12





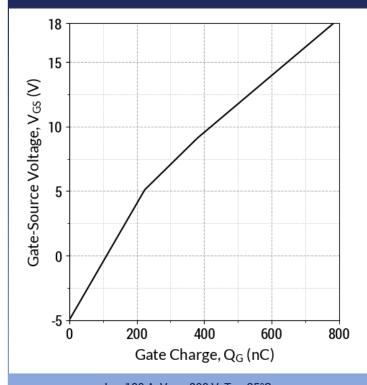
 $R_{DS(ON)} = f(T_i, V_{GS}); t_P = 50 \mu s; I_D = 180 A$

Fig 10: Typical Threshold Voltage Characteristics



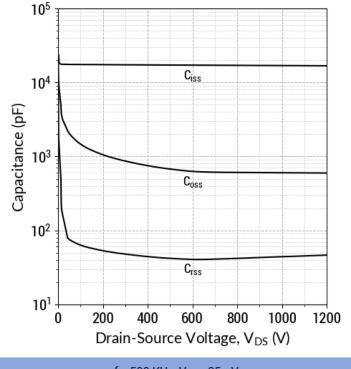
 $V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 140 \text{ mA}$

Fig 11: Typical Gate Charge Characteristics



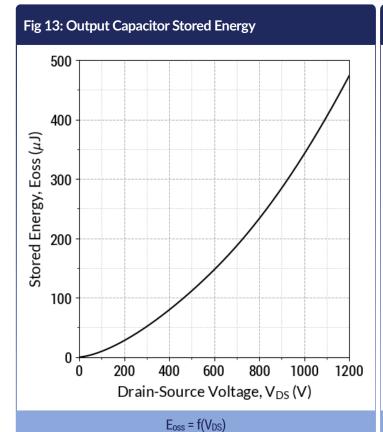
 $I_D = 180 \text{ A}$; $V_{DS} = 800 \text{ V}$; $T_c = 25^{\circ}\text{C}$

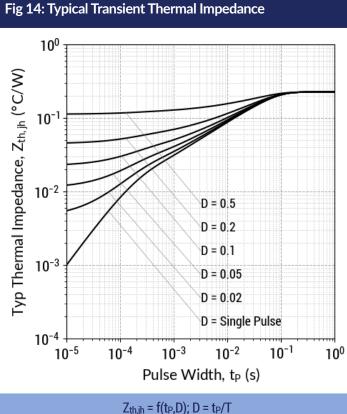
Fig 12: Typical Capacitance v/s Drain-Source Voltage

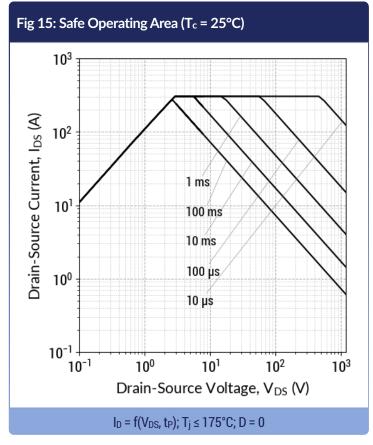


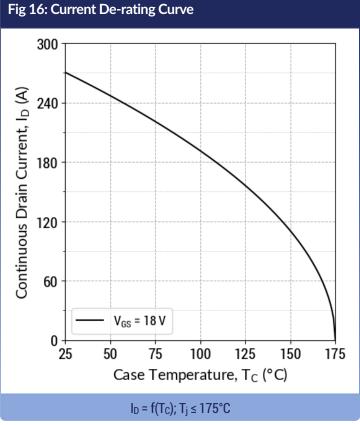
f = 500 KHz; V_{AC} = 25mV

Rev 25/Mar (Preliminary) Page 6 of 12









Rev 25/Mar (Preliminary) Page 7 of 12



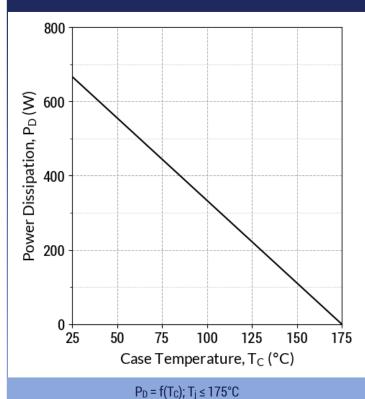
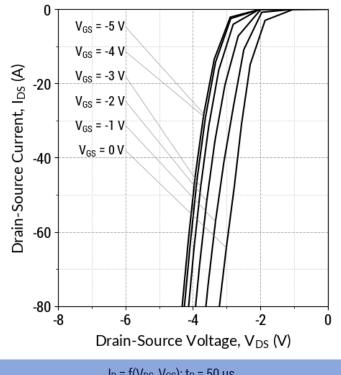


Fig 18: Typical Body Diode Characteristics ($T_j = 25$ °C)



 $I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu s$

Fig 19: Typical Body Diode Characteristics ($T_j = 175$ °C)

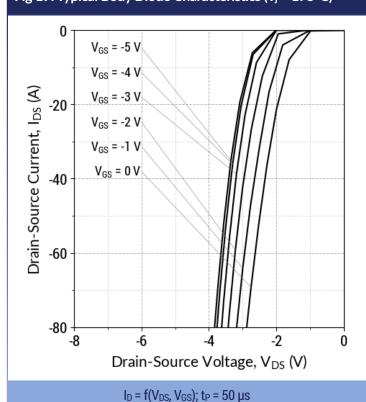
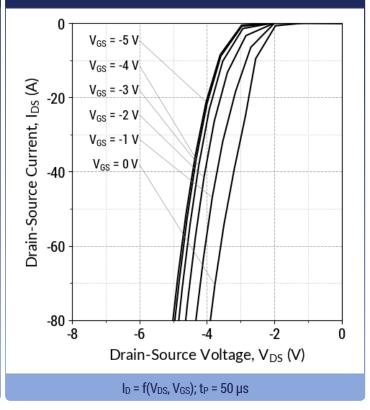


Fig 20: Typical Body Diode Characteristics ($T_j = -55$ °C)



Rev 25/Mar (Preliminary) Page 8 of 12

Fig 21: Typical Third Quadrant Characteristics ($T_j = 25$ °C)

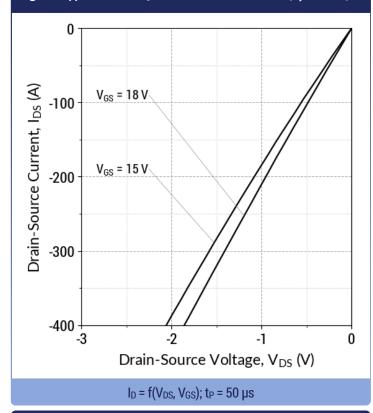
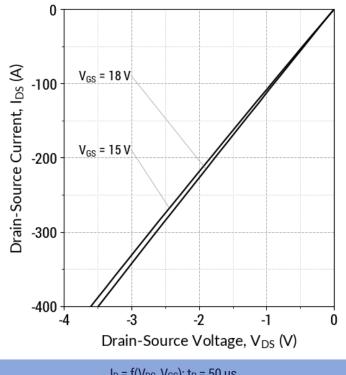


Fig 22: Typical Third Quadrant Characteristics ($T_j = 175^{\circ}$ C)



 $I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu s$

Fig 23: Typical Third Quadrant Characteristics (T_j = -55°C)

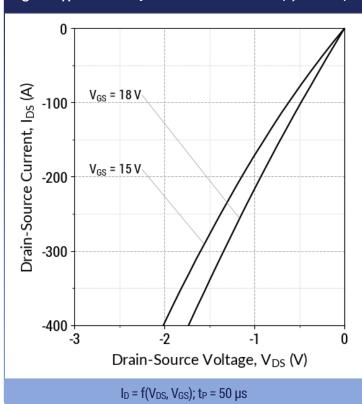
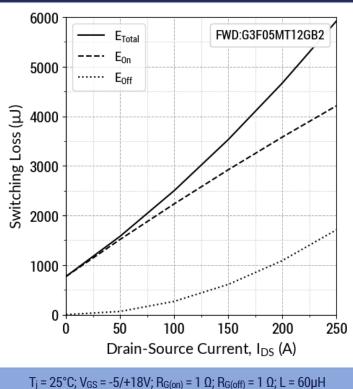
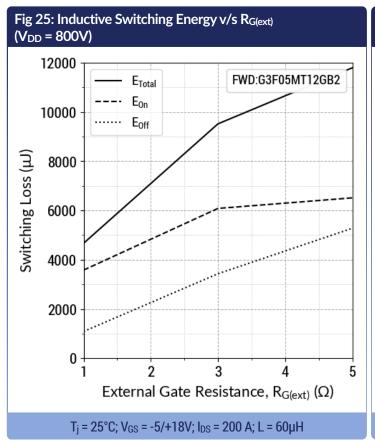
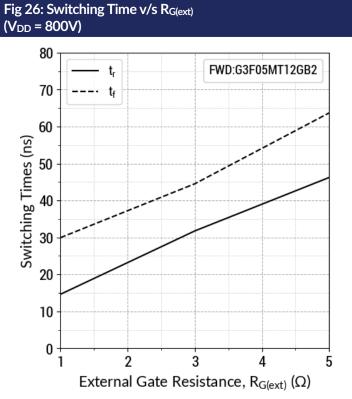


Fig 24: Inductive Switching Energy v/s Drain Current $(V_{DD} = 800V)$



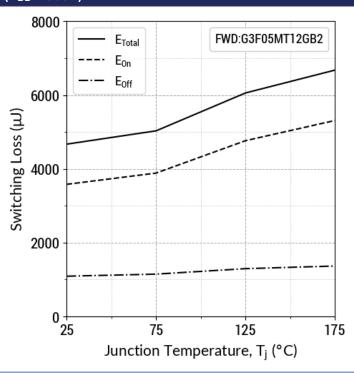
Rev 25/Mar (Preliminary) Page 9 of 12





 $T_i = 25$ °C; $V_{GS} = -5/+18V$; $I_{DS} = 200$ A; $L = 60\mu H$

Fig 27: Inductive Switching Energy v/s Temperature $(V_{DD} = 800V)$

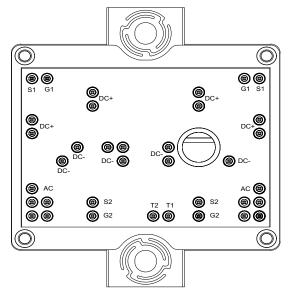


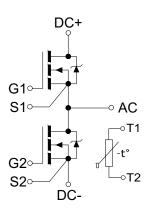
 V_{GS} = -5/+18V; $R_{G(on)}$ = 1 $\Omega;$ $R_{G(off)}$ = 1 $\Omega;$ I_{DS} = 200 A; L = $60\mu H$

Rev 25/Mar (Preliminary) Page 10 of 12

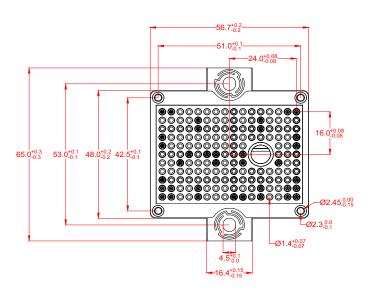


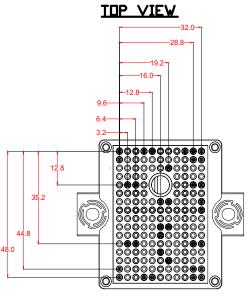
Pinout and Package Dimensions





TOP VIEW

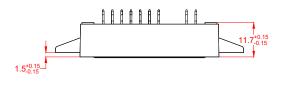




Pin Positions Tolerance $\phi 0.5$

SIDE VIEW 00 **0** 0 0 $12.0_{[-0.19]}^{+0.19} \ 16.4_{[-0.19]}^{+0.19}$ 0.3+0.12

SIDE VIEW



NOTES

- 1. Controlled dimension is millimeter (mm)
- 2. Dimensions do not include material protrusions

Rev 25/Mar (Preliminary) Page 11 of 12





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Rev 25/Mar (Preliminary) Page 12 of 12