

## R1810Z015A-EV

# 600 nA IQ Low Quiescent Current Boost DC/DC Converter for Energy Harvester Evaluation Board

No.EEV-423-Z015A-250110

R1810Z015A-EV is the evaluation board for R1810 which has the below features, benefits and specification.

#### OVERVIEW

R1810Z is a boost DC/DC converter for electrical power storage devices, especially dedicated for 1 cell photovoltaic energy harvester since the start-up voltage is Typ.0.35V.

This product can start up with only 9uW, and applicable for charging 1 cell photovoltaic element. A system which is working under low-illuminance environment can be composed with the R1810Z.

#### **KEY BENEFITS**

- Providing a low quiescent current (Iq\_vouт =Typ.600 nA), and high efficiency (66%@ Ιουτ=5 μΑ)
- Start up with low input energy, 9 μW (low illuminance) is possible.
- Maximum power point control function is built-in.

#### KEY SPECIFICATIONS

Start-up voltage: Typ. 0.35V

Max. 0.50V (0°C  $\leq$  Ta  $\leq$  65°C), Max. 0.55V (-40°C  $\leq$  Ta  $\leq$  85°C)

- Input Voltage Range: 0.2 V to 2.1 V (V<sub>SET</sub>=2.7V)
- Output Voltage: 2.7 V
- Output Voltage Accuracy: ±5.0%
- Low current consumption: Typ.600 nA (Ta = 25°C, at no load)
- Start-up power:  $9 \mu W (V_{MPSET} = 0.5 V / V_{SET} = 2.6 V)$
- Maximum Power Point Control Voltage: 0.3 V
- Input Power Good Function
- Output Power Good Function
- For more details on R1810 IC, please refer to

https://www.nisshinbo-microdevices.co.jp/en/products/dc-dc-switching-regulator/spec/?product=r1810

#### PART NUMBER INFORMATION

Product Name	Package
R1810Z015A-EV	WLCSP-15-P1

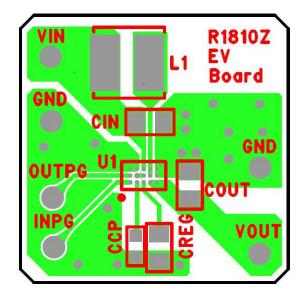
015: Output Voltage = 2.7 V

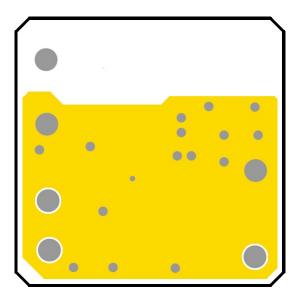
Maximum Power Point Control Voltage = 0.3 V OUTPG "High" Detection Voltage = 2.43 V

A: Set output power good low (PGL) = Vset x 80%

## **PCB LAYOUT**

### R1810Z ( WLCSP-15-P1 ) Board Layout Diagram





Top Layer Bottom Layer

No.EEV-423-Z015A-250110

#### **ABSOLUTE MAXIMUM RATINGS**

#### **Absolute Maximum Ratings**

(GND = 0 V)

Symbol	Parameter	Rating	Unit
VIN	Input Pin Voltage	-0.3 to 2.3	V
$V_{LX}$	LX Pin Voltage	-0.3 to 6.5	V
Vout	Output Pin Voltage	-0.3 to 6.5	V
$V_{REG}$	Output Voltage of Boost DC to DC Converter for Start-up	-0.3 to 6.5	V
V <sub>CP</sub>	Output Pin Voltage of Charge Pump Circuit	-0.3 to 6.5	V
V <sub>TEST1</sub> to 3	Pin Voltage for Testing	-0.3 to 6.5	V
VINPG	INPG Pin Voltage	-0.3 to 6.5	V
I <sub>INPG</sub>	INPG Pin Current	10	mA
Voutpg	OUTPG Pin Voltage	-0.3 to 6.5	V
l <sub>OUTPG</sub>	OUTPG Pin Current	10	mA
PD	Power Dissipation	Refer to the Power Diss in the supplementary	•
Tj	Junction Temperature Range	-40 to 85	°C
Tstg	Storage Temperature Range	−55 to 125	°C

#### **ABSOLUTE MAXIMUM RATINGS**

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field.

The functional operation at or over these absolute maximum ratings are not assured.

#### RECOMMENDED OPERATING CONDITIONS

**Recommended Operating Conditions** 

Symbol	Parameter	Rating	Unit
VIN	Input Voltage (Vset=2.7V)	0.20 to 2.1	V
Ta	Operating Temperature Range	-40 to 85	°C

#### **RECOMMENDED OPERATING CONDITIONS**

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. The semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

#### **ELECTRICAL CHARACTERISTICS**

VINPGL

INPG "Low" Output Voltage

The specifications surrounded by  $\square$  are guaranteed by design at  $-40^{\circ}$ C  $\leq$  Ta  $\leq$  85°C, not mass production tested.

#### **R1810Z Electrical Characteristics** $(Ta = 25^{\circ}C)$ **Symbol Parameter Conditions** Min. Max. Unit Typ. $V_{IN} = 0.5V$ **VOUT Pin Quiescent Current** 600 3000 nΑ I<sub>Q\_VOUT</sub> $V_{OUT} = 4.5 V$ , at no switching $V_{IN} = 0.5 V$ , VIN Pin Quiescent Current 400 $I_{Q_VIN}$ nΑ Vout = 4.5 V, at no switching $V_{SET}$ $V_{SET}$ ٧ Vout Output Pin Voltage $V_{\text{IN}} > V_{\text{MP}}$ ×0.95 ×1.05 -5 5 % Vout = Vset VMPSet ≥0.5V Accuracy of Maximum $V_{MP}$ Power Point Control Voltage 50 Vout = Vset, Vmpset < 0.5V -50 mV xxxA: 2.6V ≤ V<sub>SET</sub> $V_{SET}$ OUTPG "High" Threshold xxxB: 3.1V ≤ V<sub>SET</sub> $V_{\mathsf{SET}}$ VSET V Voutpgh Voltage xxxC: 3.6V ≤ V<sub>SET</sub> $\times 0.87$ $\times 0.93$ 0.90 xxxD: 4.3V ≤ V<sub>SET</sub> VSET $V_{\mathsf{SET}}$ VSET xxxA: $2.6V \le V_{SET} < 3.3V$ × (PGL × × (PGL V $xxxB: 3.1V \le V_{SET} < 3.3V$ **PGL** -0.05) +0.05) OUTPG "Low" Threshold Voutpgl xxxA: 3.3V ≤ V<sub>SFT</sub> Voltage $V_{\mathsf{SET}}$ $V_{\text{SET}}$ VSET xxxB: 3.3V ≤ V<sub>SET</sub> × (PGL × (PGL × xxxC: 3.6V ≤ V<sub>SET</sub> **PGL** -0.04)+0.04)xxxD: 4.3V ≤ V<sub>SET</sub> $V_{\mathsf{MPSET}}$ V $V_{\mathsf{INPGH}}$ INPG "High" Threshold Voltage × 1.05 $V_{\mathsf{MPSET}}$ ٧ VINPGL INPG "Low" Threshold Voltage × 0.95 2.11 ٧ Voutuvlor Voutuvlo Release Voltage 1.55 V Voutuvlof Voutuvlo Detection Voltage $V_{\mathsf{SET}}$ ٧ Voutpgh OUTPG "High" Output Voltage IOUTPG=-1µA ×0.9 $V_{\mathsf{SET}}$ VINPGH INPG "High" Output Voltage V I<sub>INPG</sub>=-1µA ×0.9 Voutpgl 0.1 V OUTPG "Low" Output Voltage IOUTPG=1µA

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj  $\approx$  Ta = 25°C). Test circuit is operated with "Open Loop Control" (GND = 0 V), unless otherwise specified.

 $I_{INPG}=1\mu A$ 

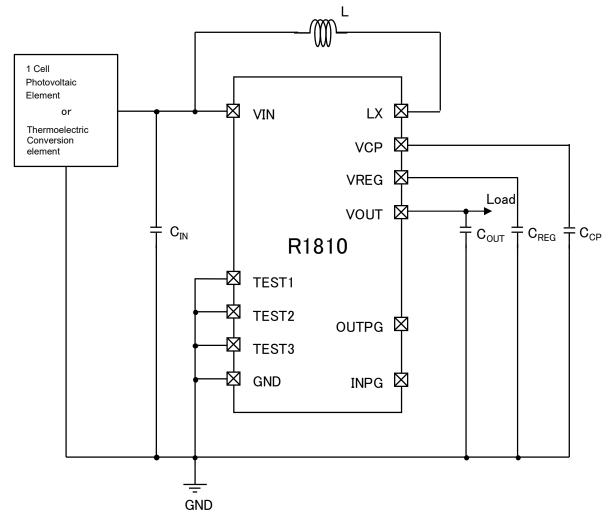
0.1

R1	810x
No.EEV-423-Z015A-25	50110
The specifications surrounded by are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C	
R1810ZxxxA Product-specific Electrical Characteristics	

Product	Output Voltage [V]			Maximum Power Point Control Voltage [V]			OUTPG"High" Detection Voltage [V]		
Name	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.
R1810Z015A	2.565	2.7	2.835	0.250	0.3	0.350	2.349	2.43	2.511

If VSET < 2.6V, the OUTPG function cannot be used.

## **APPLICATION INFORMATION**



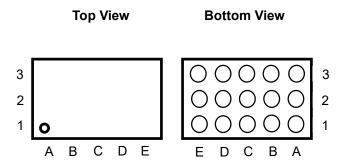
**R1810x Typical Application Circuit** 

#### **Recommended External Components**

Symbol	Descriptions Value
Cin	22 µF
Сср	0.022µF
C <sub>REG</sub>	4.7 µF
Соит	4.7 μF
L	22 µH

XThe bill of materials will be attached on the shipment of each purchased evaluation board.

## **PIN DESCRIPTIONS**



R1810Z (WLCSP-15-P1) Pin Configuration

R1810Z Pin Description

Symbol	Description		Pin No.
Symbol	Description	I/O	R1810Z
VIN	Power Supply Input Pin. Apply input voltage between VIN pin and GND. Connect the input capacitor between the VIN pin and GND.	I	С3
VOUT	Output voltage pin of step-up DC / DC converter. Connect the output load between VOUT pin and GND. Connect the output capacitor between VOUT pin and GND.	0	D1,E1
INPG	Power good output pin for power input voltage (V <sub>IN</sub> ).  "High" level of the output voltage for CMOS output is the output voltage (V <sub>OUT</sub> ) of the step-up DC / DC converter.  Outputs "High" when V <sub>IN</sub> exceeds V <sub>MPSET</sub> and V <sub>OUT</sub> exceeds V <sub>OUTUVLOR</sub> *1.  Please left open when not in use.	0	A1
VREG	Output pin of step-up DC / DC converter (internal power supply) for startup. Supply voltage to the main DC / DC converter circuit that produces VOUT at startup. Please connect a capacitor between VREG pin and GND for voltage stabilization.	0	C1
LX	The drain of the internal MOSFET. Connect an inductor between VIN pin and LX pin.	0	D2,D3
VCP	Output pin of the startup internal step-up charge pump (internal power source).  Supply voltage to the start-up DC / DC converter circuit that generates the VREG voltage at startup.  Please connect a capacitor between the VCP pin and GND for voltage stabilization.	0	B1

No.EEV-423-Z015A-250110

OUTPG	Power good output pin for Vout.  "High" level of the output voltage for CMOS output is Vout.  Outputs "High" when Vout is Voutpgh*1 or higher, and outputs "Low" when Vout is Voutpgl*1 or lower.  Please left open when not in use.	0	A2
TEST 1,2,3	Test pins for the IC. Be sure to connect to AGND.	_	C2,B2,A3
AGND	Analog ground of the internal circuit. Please connect to the PGND and GND.	_	В3
PGND	Power ground of the internal circuit. Please connect to the AGND and GND.	_	E2,E3
NC	No connection. It is recommended to make it open to prevent short circuit with adjacent pins during mounting.	_	_

#### %1 : Refer to electrical characteristics.

Product	OUTPG"Low" Detection Voltage [V]			INPG"High" Detection Voltage [V]	INPG"Low" Detection Voltage [V]	
Name	Min.	Тур.	Max.	Min.	Max.	
R1810x015A	2.025	2.160	2.295	0.315	0.285	

If VSET < 2.6V, the OUTPG function cannot be used.

No.EEV-423-Z015A-250110

#### **TECHNICAL NOTES**

The performance of the IC largely depends on the external components and circuitry layout. Especially, design the circuit carefully not to exceed each rating (voltage, current, power) for each component and the IC and consider the best layout pattern.

Use a ceramic capacitor with low ESR (equivalent series resistance). We recommend 22uF as CIN which is set between  $V_{IN}$  and GND.

We recommend 4.7uF ceramic capacitor or 10uF or more ceramic capacitor with large capacity of electrical storage device as Cout. The capacitors should cover the operating temperature range, and effective capacitance should be more than our recommendation capacity with 0 bias. Note that insulation resistance should not be too small. If insulation resistance is small, the leakage current may increase. Such a system cannot be recommended.

We recommend an inductor with equal or more current rating (400mA or more), ESR, DC superimposition characteristics as our recommendation part. If ESR is large, or bad DC superimposition characteristics may lead to the bad efficiency. If the current rating is too small, the inductor may be broken down.

If other than GND level is connected to the TEST1,2,3 pins, by the shoot current of logic circuits inside the IC, consumption current may increase. Make sure to connect these pins to the ground level.