# Radiation Hardened Quad 2-Input NAND Gate

with **cold sparing**

## 1 GENERAL DESCRIPTION

The **AP54RHC00** is a radiation-hardened by design **quad 2-Input NAND gate** that is ideally suited for space, medical imaging and other applications demanding radiation tolerance and high reliability. It is fabricated in a 180 nm CMOS process utilizing proprietary radiation-hardening techniques, delivering high resiliency to single-event effects (SEE) and to a total ionizing dose (TID) up to **30 krad (Si)**.

This device is a member of the Apogee Semiconductor AP54RHC logic family operating across a voltage supply range of **1.65 V to 5.5 V**.

Zero-power penalty™ cold-sparing is supported, along with Class 2 ESD protection on all inputs and outputs. A proprietary output stage and robust power-on reset (POR) circuit allow the AP54RHC00 to be cold-spared in any redundant configuration with no static power loss on any pad of the device. The redundant output stage also features a high drive capability with low static power loss.

The AP54RHC00 also features a triple-redundant design throughout its entire circuitry, which allows it to be immune to single-event transients (SET) without requiring additional redundant devices.

This device provides four instances of the Boolean logical function **NAND** ($Y = \overline{A \cdot B}$).

Ordering information may be found in Table 9 on Page 11.

### 1.1 FEATURES

- **1.65 VDC to 5.5 VDC** operation
- Inputs tolerant up to 5.5 VDC at any $V_{CC}$
- Provides logic-level down translation to $V_{CC}$
- Extended operating temperature range (-55 °C to +125 °C)
- Proprietary **cold-sparing capability** with **zero** static power penalty
- **Built-in triple redundancy** for enhanced reliability
- Internal power-on reset (POR) circuitry ensures reliable power up and power down responses during hot plug and cold sparing operations
- Class 2 ESD protection (4000 V HBM, 500 V CDM)
- TID resilience of **30 krad (Si)**.
- SEL resilient up to LET of **80 MeV-cm$^2$/mg**

### 1.2 LOGIC DIAGRAM

The AP54RHC00 logic function is shown below:

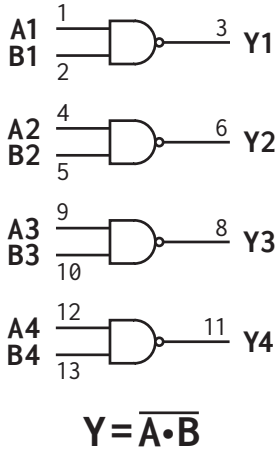



**Figure 1:** AP54RHC00 logic diagram

# CONTENTS



# LIST OF TABLES



# LIST OF FIGURES



# 2 ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| ESD | Electrostatic Discharge |
| POR | Power On Reset |
| RHA | Radiation Hardness Assurance |
| SEE | Single Event Effects |
| SEL | Single Event Latchup |
| SET | Single Event Transient |
| TID | Total Ionizing Dose |
| TMR | Triple Modular Redundancy |
| CDM | Charged-device Model |
| HBM | Human-body Model |

# 3 LOGIC DATA

## 3.1 TRUTH TABLE

The AP54RHC00 truth table is found in Table 1. **H** indicates HIGH logic level and **L** indicates LOW logic level. Subscript **n** reflects one of the four gates in the device (1 to 4).

**Table 1:** AP54RHC00 device truth table

| Input | | Output |
|---|---|---|
| $A_n$ | $B_n$ | $Y_n$ |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

# 4 PIN CONFIGURATION

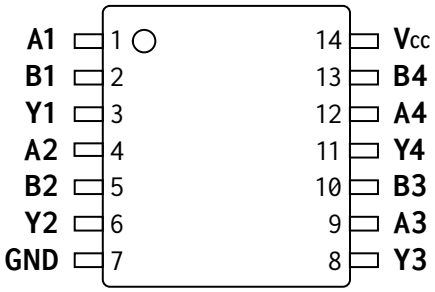



**Figure 2:** AP54RHC00 device pinout overview

**Table 2:** AP54RHC00 device pinout description

| PIN NAME(S) | PIN NUMBER(S) | DESCRIPTION |
|---|---|---|
| A1, B1<br>A2, B2<br>A3, B3<br>A4, B4 | 1, 2<br>4, 5<br>9, 10<br>12, 13 | Logic Inputs |
| Y1<br>Y2<br>Y3<br>Y4 | 3<br>6<br>8<br>11 | Logic Outputs |
| $V_{CC}$ | 14 | Positive Voltage Supply |
| GND | 7 | Ground |

# 5 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

## 5.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 3 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 4) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

**Table 3:** Absolute Maximum Ratings

| SYMBOL | PARAMETER | | VALUE | UNITS |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | -0.5 to +5.5 | V |
| $V_I$ | Input voltage range | | -0.5 to +5.5 | V |
| $V_O$ | Output voltage range | | -0.5 to $V_{CC}$ + 0.5 (1) | V |
| $I_{IK}$ ($V_I$ < 0) | Input clamp current | | 100 | mA |
| $I_O$ | Continuous output current (per pin) | | 100 | mA |
| $I_{CC}$ | Maximum supply current | | 100 | mA |
| $V_{ESD}$ | ESD Voltage | HBM | 4000 | V |
| | | CDM | 500 | V |
| $T_J$ | Operating junction temperature range | | -55 to +150 | °C |
| $T_{STG}$ | Storage temperature range | | -65 to +150 | °C |

(1) $V_O$ must remain below absolute maximum rating of $V_{CC}$

## 5.2 RECOMMENDED OPERATING CONDITIONS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified.

**Table 4:** Recommended Operating Conditions

| SYMBOL | PARAMETER | | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 5.5 | V |
| $V_I$ | Input voltage range | | 0 | 5.5 | V |
| $V_O$ | Output voltage range | | 0 | $V_{CC}$ | V |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.65 to 1.95 V | 1.4 | - | V |
| | | $V_{CC}$ = 2.3 to 2.7 V | 1.9 | - | |
| | | $V_{CC}$ = 3.0 to 3.6 V | 2.5 | - | |
| | | $V_{CC}$ = 4.5 to 5.5 V | 3.8 | - | |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.65 to 1.95 V | - | 0.4 | V |
| | | $V_{CC}$ = 2.3 to 2.7 V | - | 0.6 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | - | 0.9 | |
| | | $V_{CC}$ = 4.5 to 5.5 V | - | 1.35 | |
| $I_{OH}$ | HIGH-level output current | $V_{CC}$ = 1.65 to 1.95 V | - | -4 | mA |
| | | $V_{CC}$ = 2.3 to 2.7 V | - | -8 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | - | -16 | |
| | | $V_{CC}$ = 4.5 to 5.5 V | - | -24 | |
| $I_{OL}$ | LOW-level output current | $V_{CC}$ = 1.65 to 1.95 V | - | 4 | mA |
| | | $V_{CC}$ = 2.3 to 2.7 V | - | 8 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | - | 16 | |
| | | $V_{CC}$ = 4.5 to 5.5 V | - | 24 | |
| $t_r$, $t_f$ | Input rise or fall time (10% - 90%) | $V_{CC}$ = 1.65 to 1.95 V | - | 1000 | ns |
| | | $V_{CC}$ = 2.3 to 2.7 V | - | 600 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | - | 500 | |
| | | $V_{CC}$ = 4.5 to 5.5 V | - | 400 | |

**Table 5:** Thermal Information

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $T_J$ | Operating junction temperature | -55 | - | +125 | °C |
| $R_{\theta JA}$ | Junction to ambient thermal resistance | - | 100 | - | °C/W |

## 5.3 STATIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

**Table 6:** DC Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW-level output voltage | $I_O$ = 100 µA | 1.65 to 5.5 V | - | 0.02 | 0.05 | V |
| | | $I_O$ = 1 mA | 1.65 to 5.5 V | - | 0.05 | 0.1 | V |
| | | $I_O$ = 4 mA | 2.3 V | - | 0.3 | 0.6 | V |
| | | | 3.0 V | - | 0.2 | 0.4 | V |
| | | | 4.5 V | - | 0.2 | 0.4 | V |
| | | $I_O$ = 8 mA | 2.3 V | - | 0.6 | 1.0 | V |
| | | | 3.0 V | - | 0.4 | 0.8 | V |
| | | | 4.5 V | - | 0.3 | 0.6 | V |
| | | $I_O$ = 16 mA | 3.0 V | - | 1.0 | 1.4 | V |
| | | | 4.5 V | - | 1.1 | 1.5 | V |
| | | $I_O$ = 24 mA | 4.5 V | - | 1.1 | 1.5 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_O$ = -100 µA | 1.65 to 5.5 V | $V_{CC}$ - 0.1 | $V_{CC}$ - 0.02 | - | V |
| | | $I_O$ = -1 mA | 1.65 to 5.5 V | $V_{CC}$ - 0.15 | $V_{CC}$ - 0.08 | - | V |
| | | $I_O$ = -4 mA | 2.3 V | 1.8 | 2.0 | - | V |
| | | | 3.0 V | 2.6 | 2.8 | - | V |
| | | | 4.5 V | 4.2 | 4.4 | - | V |
| | | $I_O$ = -8 mA | 2.3 V | 1.4 | 1.7 | - | V |
| | | | 3.0 V | 2.2 | 2.5 | - | V |
| | | | 4.5 V | 3.9 | 4.1 | - | V |
| | | $I_O$ = -16 mA | 3.0 V | 1.5 | 2.0 | - | V |
| | | | 4.5 V | 3.3 | 3.8 | - | V |
| | | $I_O$ = -24 mA | 4.5 V | 3.0 | 3.5 | - | V |
| $I_{CC}$ | Quiescent supply current | $V_I$ = $V_{CC}$ or GND<br>$I_O$ = 0 mA | 5.5 V | - | 105 | 168 | µA |
| $I_I$ | Input current | $V_I$ = $V_{CC}$ or GND | 1.65 to 5.5 V | - | - | ±1 | µA |
| $I_{OFF}$ | Powerdown leakage current(1) | $V_I$ = $V_{CC}$ or GND | OFF(2) | - | - | 5 | µA |

(1) into any input or output port
(2) $V_{CC}$ is disconnected or at GND potential

## 5.4 DYNAMIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified.

**Table 7:** AC Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{pd}$[1] | Propagation Delay (Input $\mathbf{A_n}$ or $\mathbf{B_n}$ to Output **Y**) | $C_L$ = 50 pF | 4.5 to 5.5 V | - | 7.6 | 11 | ns |
| | | | 3.0 to 3.6 V | - | 9 | 13 | ns |
| | | | 2.3 to 2.7 V | - | 11 | 15 | ns |
| | | | 1.65 to 1.95 V | - | 17 | 25 | ns |
| $C_{IN}$ | Input Capacitance[2] | $V_I$ = $V_{CC}$ or GND | 1.65 to 5.5 V | - | 2 | 4 | pF |
| $C_{PD}$ | Power dissipation capacitance[2] | $I_O$ = 0 mA<br>f = 1 MHz | 5.5 V | - | 40 | - | pF |

[1] equivalent to $t_{PLH}$, $t_{PHL}$

[2] guaranteed by design

## 5.5 RADIATION RESILIENCE

For detailed radiation testing reports, please contact Apogee Semiconductor at sales@apogeesemi.com.

**Table 8:** Radiation Resilience Characteristics

| PARAMETER | CONDITIONS | VALUE | UNITS |
|---|---|---|---|
| Total Ionizing Dose (TID) | Please contact Apogee Semiconductor for test report. | 30 | krad (Si) |
| SEE LET Threshold | Please contact Apogee Semiconductor for test report. | <80 | MeV-cm$^2$/mg |

## 5.6 CHARACTERISTICS MEASUREMENT INFORMATION

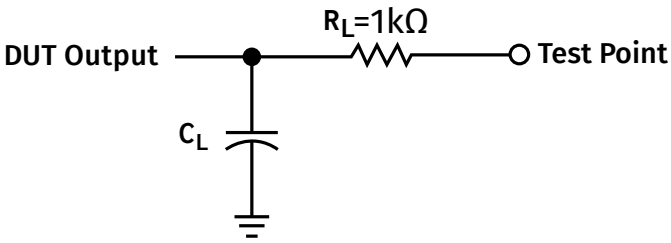



**Figure 3:** Load circuit for outputs

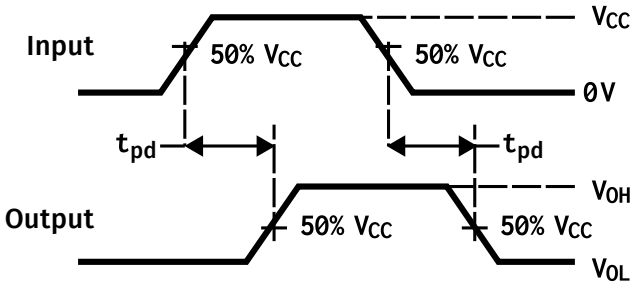



**Figure 4:** Propagation delay measurement

# 6 DETAILED DESCRIPTION

The AP54RHC00 is a quad 2-Input NAND gate intended to perform the Boolean function **NAND** ($Y = \overline{A \cdot B}$) in positive logic. Designed to operate from a wide supply voltage of 1.65 to 5.5 V, it has fully redundant input and output stages providing for superior resiliency to single event effects.

The output and input stages are constructed with transient activated clamps (Figure 5, 6) that prevent inadvertent biasing of the $V_{CC}$ power rail through parasitic diodes inherent to conventional input, output, and ESD circuits. The IC also incorporates an internal power-on reset (POR) circuit that prevents the output from driving erroneous results during power-on, and guarantees correct operation at power supply voltages as low as 1.65 V. While the supply is ramping, the POR holds the output buffer in tri-state, a feature that prevents unwanted DC current during cold sparing on input and output pins.

The AP54RHC family's I/O protection circuitry allows for cold sparing configurations as it avoids a leakage current penalty on inputs and outputs while in a power-down state. This can result in considerable power savings in systems where multiple-path redundancy is employed. The ESD clamp circuits for this logic family are designed to support Class 2 ESD levels of 4 kV HBM and 500 V CDM.

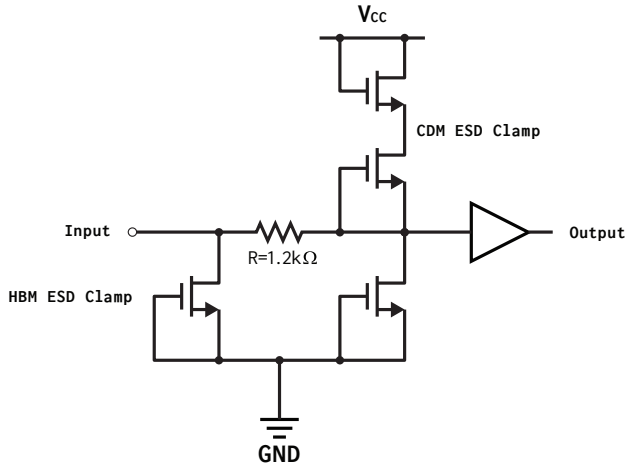



**Figure 5:** Details of input pin structure

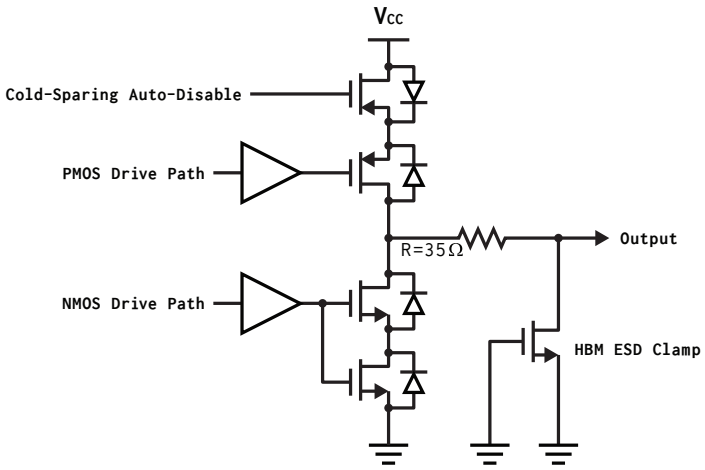



**Figure 6:** Details of output pin structure

# 7 APPLICATIONS INFORMATION

## 7.1 USE IN COLD-SPARING CONFIGURATION

As the AP54RHCfamily is radiation-hardened by design and includes internal TMR, it can be utilized in high-reliablity applications without additional supporting circuitry or devices. Nonetheless, some application requirements call for fully-redundant designs, where an “A” and a “B” device are required, often on separate power rails.

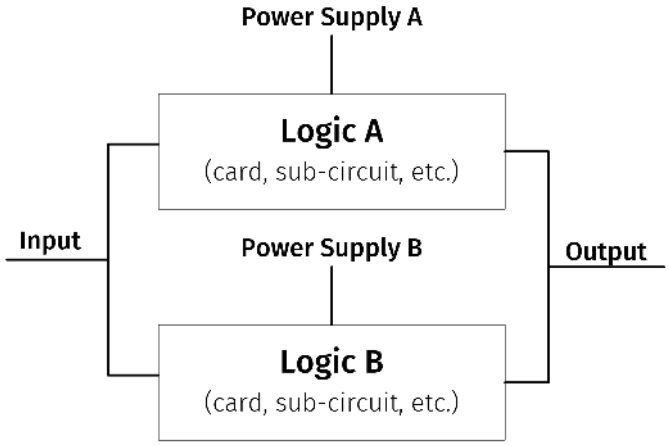



**Figure 7:** Two-path cold-sparing configuration.

With the cold-sparing capability of the AP54RHCfamily, fully redundant “A” and “B” functions may be placed in parallel (as seen in Figure 7) running off redundant power supplies. The inputs and outputs on each one of these functions are assumed to be based on the AP54RHCfamily, allowing for direct parallel connection without unwanted leakage current paths during cold sparing. In the event of a failure in power supply A or within function A, the system can simply shut power supply A off and switch on power supply B, without requiring additional input or output switching or configuration changes.

## 7.2 POWER SUPPLY RECOMMENDATIONS

This device can operate at any voltage within the range specified in Table 4 Recommended Operating Conditions.

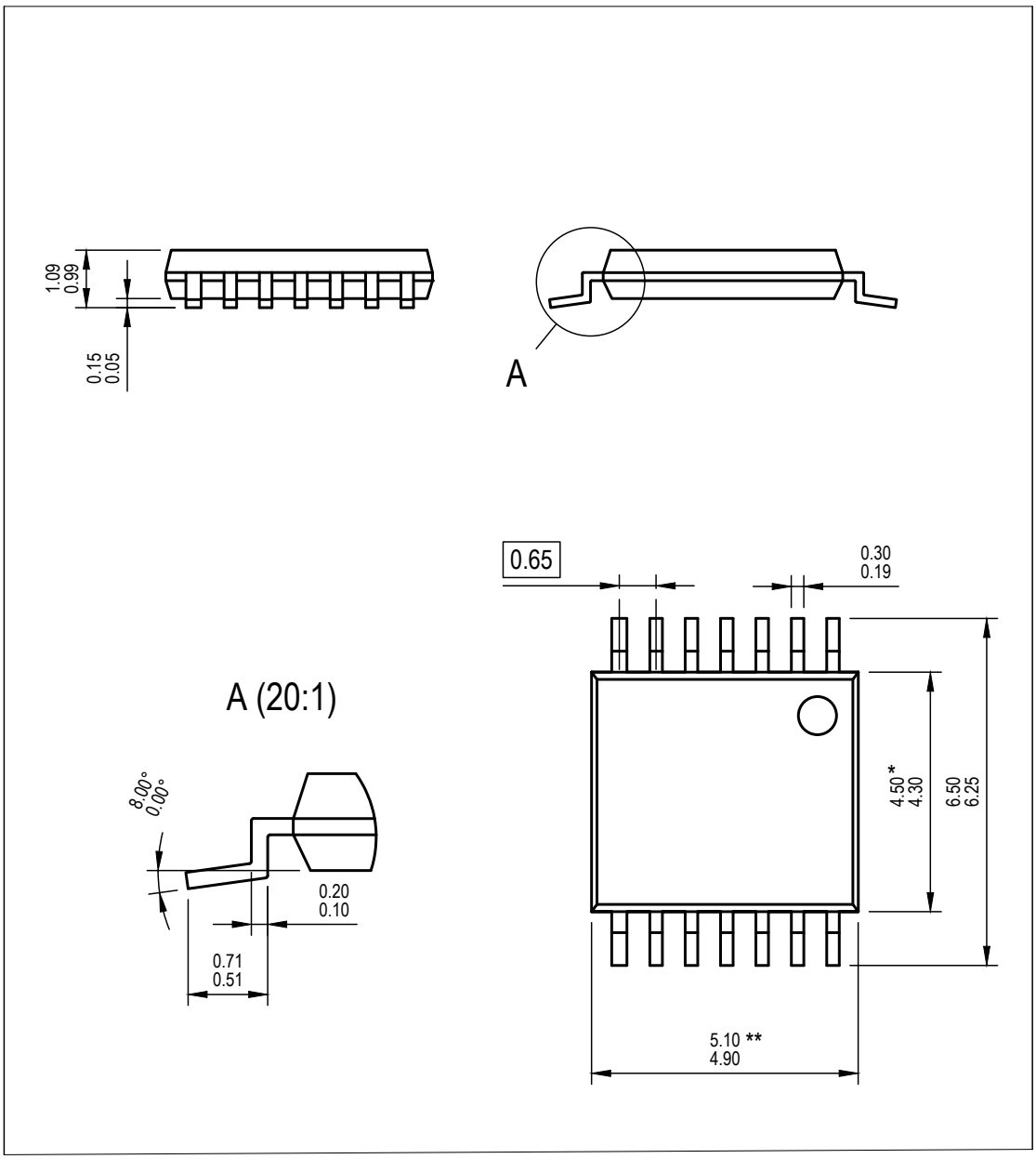
At a minimum, a 16 VDC (or higher), X7R-rated 0.1 µF ceramic decoupling capacitor should be placed near (within 1 cm) the $V_{CC}$ pin of the device.

## 7.3 APPLICATION TIPS

Unused **inputs** must **not** be left floating. They may be connected to either a low (GND) or high ($V_{CC}$) bias to provide a known state at the input of the device. Resistors may be used to tie off unused inputs. In the event of a design change, such resistors can be removed, thereby allowing use of the inputs without having to cut traces on the PCB.

An unused **output** may be left floating. It is suggested that it be routed to a test point or similar accessible structure in case the gate needs to be utilized as part of a design revision.

# 8 PACKAGING INFORMATION




Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

**Figure 8:** Package Mechanical Detail

# 9 ORDERING INFORMATION

Example part numbers for the AP54RHC00 are listed in Table 9. The full list of options for this part can be found in Figure 9. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

**Table 9:** AP54RHC00 Ordering Information

| DEVICE | DESCRIPTION | PACKAGE |
|---|---|---|
| AP54RHC00ELT-W | Radiation Hardened Quad 2-Input NAND Gate (for evaluation only) | Plastic TSSOP-14 |
| AP54RHC00ALT-R | Radiation Hardened Quad 2-Input NAND Gate (30 krad (Si)) | Plastic TSSOP-14 |

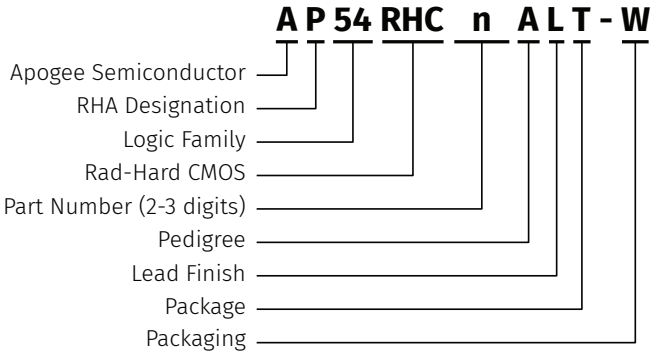



**Figure 9:** Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
   - **F** 300 krad (Si)
2. Part Number
   - **_** 00 (Quad 2-Input NAND Gate)
3. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
4. Lead Finish
   - **L** Tin-Lead (SnPb)
5. Package
   - **T** 14-pin Thin Shrink Small Outline Package (TSSOP)
6. Packaging
   - **W** Waffle Pack or Pillow Stat Box
   - **R** Tape and Reel[1]

[1] Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

# 10 REVISION HISTORY

| REVISION | DESCRIPTION | DATE |
|---|---|---|
| A05 | Fix test load diagram | 2024-03-21 |
| A04 | Correct output pin structure diagram. | 2021-12-06 |
| A03 | Revamped static and dynamic characteristics with new test data. | 2021-03-01 |
| A02 | Update Static and Dynamic characteristics. | 2020-08-07 |
| A01 | Initial public release. | 2020-02-29 |
| A00 | Initial internal release. | 2019-07-05 |

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# 11 LEGAL

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