DATA SHEET

Si8921 and Si8922 Isolated Amplifiers for Current Shunt Measurement

The Si8921 and Si8922 galvanically isolated analog amplifiers feature low-voltage differential input, ideal for measuring voltage across a current shunt resistor or any place where a sensor must be isolated from the control system. The output is a differential analog signal amplified by either 8.2x or 32.8x.

The very low signal delay of the Si8921/22 allows control systems to respond quickly to fault conditions or changes in load. Low offset and gain drift ensure that accuracy is maintained over the entire operating temperature range. Exceptionally high common-mode transient immunity means the Si8921/22 delivers accurate measurements even in the presence of high-power switching as found in motor drive systems and inverters.

The Si8921/22 isolated voltage sensing amplifier utilizes Skyworks proprietary isolation technology, and withstands up to 5.0 kV_{RMS} per UL1577. This technology enables high performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.

Automotive Grade is available for certain part numbers. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Applications

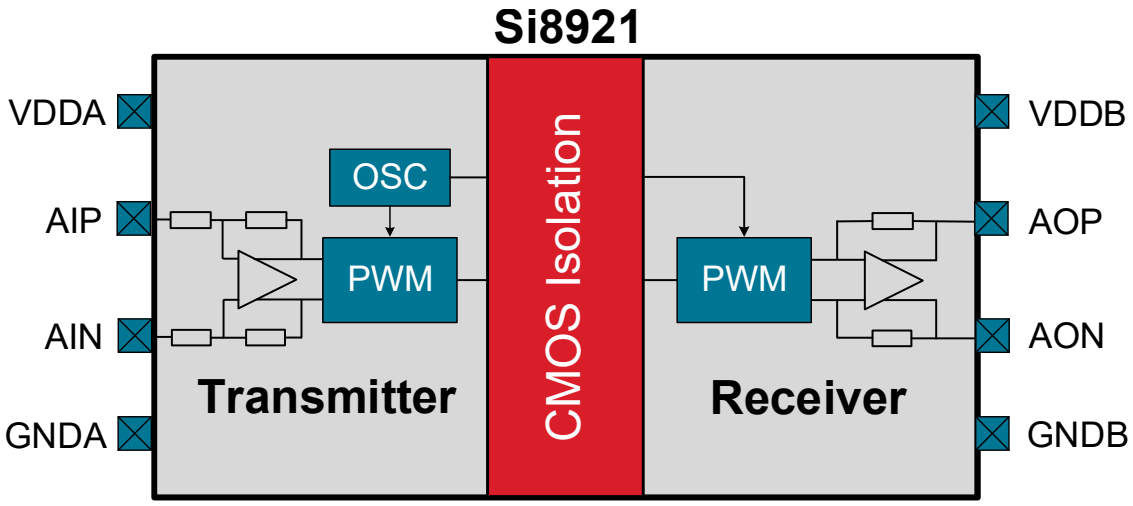
- Industrial, HEV, and renewable energy inverters
- AC, brushless, and dc motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies
- Automotive on-board chargers, battery management systems, and charging stations

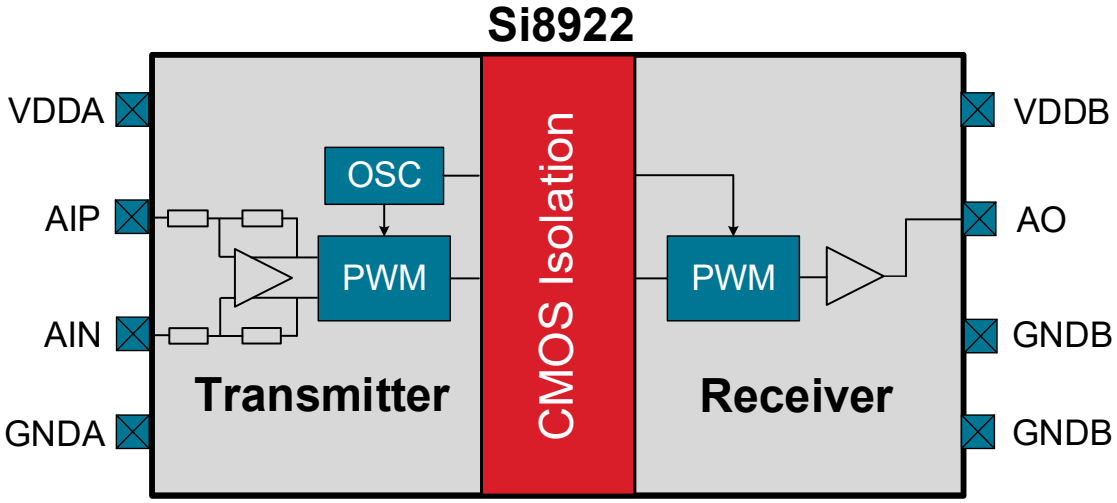
Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 5000 kV_{RMS} for one minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
- VDE certification conformity (pending)
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1

Key Features

- Low-voltage differential input: ±62.5 mV and ±250 mV options
- Low signal delay: 0.8 µs
- Typical input offset: ±0.40 µV
- Typical gain error: ±0.06%
- Excellent drift specifications
  - 0.5 µV/°C offset drift
  - –9 ppm/°C typical gain drift
- Typical nonlinearity: 0.003% full-scale
- Typical SNR: 82 dB over 100 kHz bandwidth
- Typical THD: –88 dB
- High common-mode transient immunity: 75 kV/µs
- Automotive-grade OPNs available
  - AEC-Q100 qualification
  - AIAG-compliant PPAP documentation support
  - IMDS and CAMDS listing support
- Compact packages
  - 8-pin wide body stretched SOIC
  - 8-pin narrow body SOIC
- –40 to 125 °C
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.


Si8921
VDDA
AIP
AIN
GNDA
OSC
PWM
Transmitter
CMOS Isolation
PWM
Receiver
VDDB
AOP
AON
GNDB


Si8922
VDDA
AIP
AIN
GNDA
OSC
PWM
Transmitter
CMOS Isolation
PWM
Receiver
VDDB
AO
GNDB
GNDB

1. Pin Descriptions

1.1. Si8921

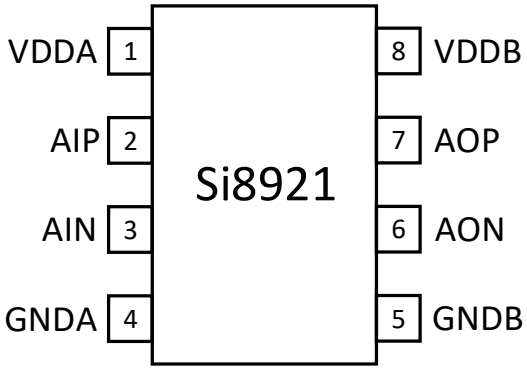


Figure 1. Si8921 Pinout (Top View)

Table 1. Si8921 Pin Descriptions

Name	Pin Number	Description
VDDA	1	Input side power supply
AIP	2	Analog input high
AIN	3	Analog input low
GNDA	4	Input side ground
GNDB	5	Output side ground
AON	6	Analog output low
AOP	7	Analog output high
VDDB	8	Output side power supply

1.2. Si8922

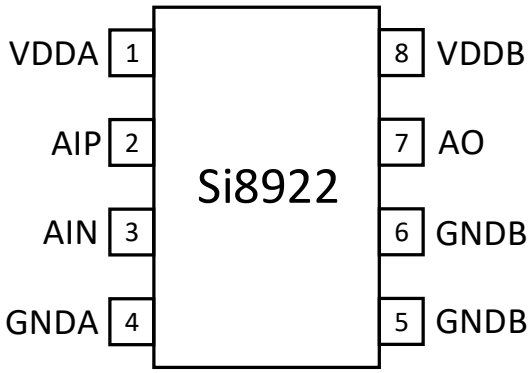


Figure 2. Si8922 Pinout (Top View)

Table 2. Si8922 Pin Descriptions

Name	Pin Number	Description
VDDA	1	Input side power supply
AIP	2	Analog input high
AIN	3	Analog input low
GNDA	4	Input side ground
GNDB[1]	5	Output side ground
GNDB[1]	6	Output side ground
AO	7	Analog output
VDDB	8	Output side power supply

1. Both Pin 5 and Pin 6 must be connected to ground.

2. Device Operation

The input to the Si8921/22 is designed for low-voltage, differential signals. This is ideal for connection to low resistance current shunt measurement resistors.

The Si8921A has a specified full scale input range of ±62.5 mV, and the Si8921B has a specified full scale input range of ±250 mV. In both cases, the internal gain is set so the full scale output is 2.05 V. The Si8921 provides a differential output voltage while the Si8922 provides a single-ended output voltage.

The Si8921/22 modulates the analog signal in a unique way for transmission across the semiconductor based isolation barrier. The input signal is first converted to a pulse-width modulated digital signal.

On the other side of the isolation barrier, the signal is demodulated. The resulting PWM signal is then used to faithfully reproduce the analog signal. This solution provides exceptional signal bandwidth and accuracy.

2.1. Fail-Safe and Low-Power Modes

The Si8921/22 implements a fail-safe output when the high voltage side supply voltage (VDDA) goes away. This is important for safe operation in systems with high safety requirements. The fail-safe output is nominally 2.8 V (Si8922) or –2.8 V (Si8921) which can be differentiated from the maximum clipping output voltage of 2.6 V to simplify diagnostics on the system level.

Table 3. Si8921 and Si8922 Output Voltages

Device	Output Voltage (VDDA Normal)	Output Voltage (VDDA Removed)
Si8921	~ ±2.6 V	~ –2.8 V
Si8922	0 to ~2.6 V	~ +2.8 V

In addition to the fail-safe output, when a loss of VDDA supply occurs, the part will automatically move into a lower power mode that reduces IDDB current to approximately 1 mA. Similarly, a loss of VDDB supply will reduce IDDA current to approximately 1 mA. When the supply voltage is returned, normal operation begins in approximately 250 µs.

2.2. Current Sense Application

In the driver circuit presented below, the Si8921 is used to amplify the voltage across the sense resistor, RSENSE, and transmit the analog signal to the low-voltage domain across an isolation barrier. Isolation is needed because the voltage of RSENSE with respect to ground will swing between 0 V and the high voltage rail connected to the drain of Q1.

The load in this application can be a motor winding or a similar inductive winding. In a three-phase motor drive application, this circuit would be repeated three times, one for each phase. RSENSE should be a small resistor value to reduce power loss. However, an excessively low resistance will reduce the signal-to-noise ratio of the measurement. Si8921/22 offers two specified full-scale input options, ±62.5 mV (Si8921A/22A) and ±250 mV (Si8921B/22B), for optimizing the value of RSENSE.

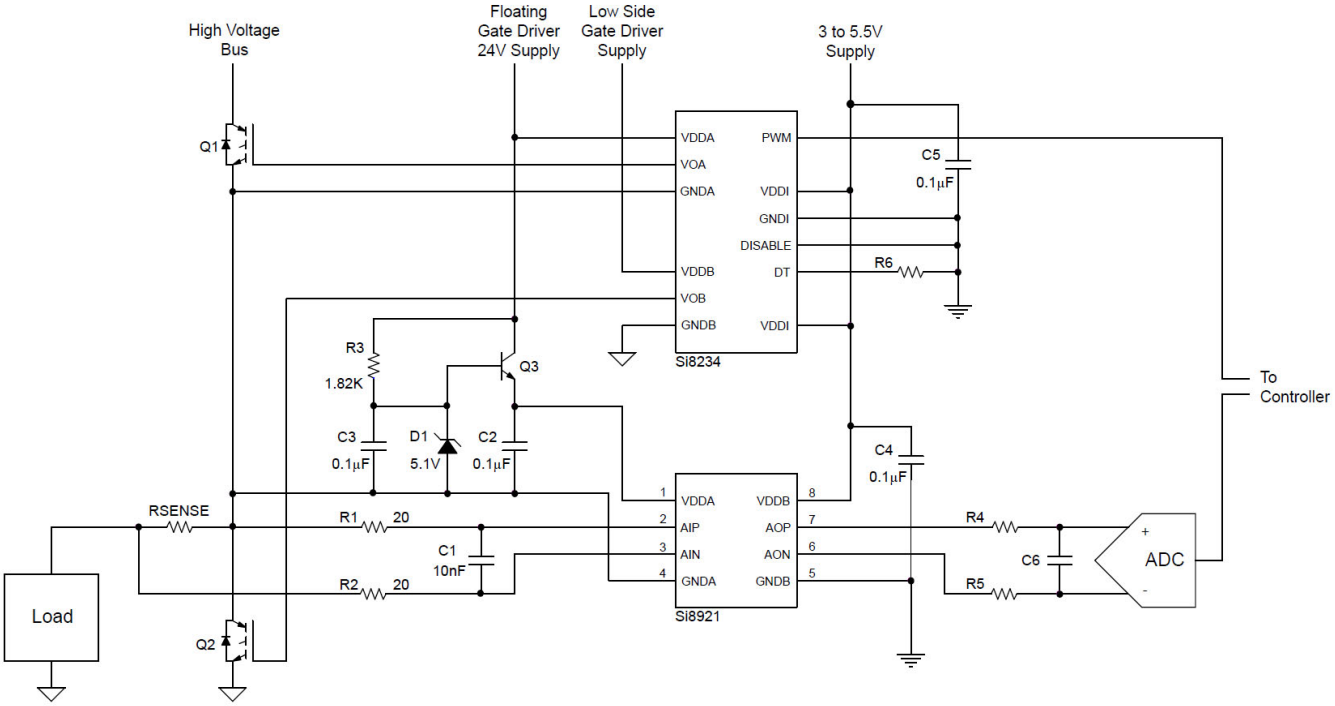


Figure 3. Current Sense Application

AIP and AIN connections to the RSENSE resistor should be made as close as possible to each end of the RSENSE resistor as trace resistance will add error to the measurement. The input to the Si8921/22 is differential, and the PCB traces back to the input pins should run in parallel. This ensures that any large noise transients that occur on the high-voltage side are coupled equally to the AIP and AIN pins and will be rejected by the Si8921/22 as a common-mode signal.

The amplifier bandwidth of the Si8921/22 is approximately 600 kHz. If further input filtering is required, a passive differential RC low-pass filter can be placed between RSENSE and the input pins.

As shown in Figure 5, values of R1 = R2 = 20 Ω and C1 = 10 nF provide a cutoff at approximately 400 kHz. For the lowest gain error, R1 and R2 should always be less than 33 Ω to keep the source impedance sufficiently low compared to the Si8921/22 input impedance.

The common-mode voltage of AIN and AIP must be greater than –0.2 V but less than 1 V with respect to GNDA. To meet this requirement, connect GNDA of the Si8921/22 to one side of the RSENSE resistor. In this example, GNDA, RSENSE, the source of Q1, and the drain of Q2 are connected. The ground of the gate driver (Skyworks Si8234 in this circuit) is also commonly connected to the same node.

The Q1 gate driver has a floating supply, 24 V in this example. Since the input and output of the Si8921/22 are galvanically isolated from each other, separate power supplies are necessary on each side. Q3, R3, C3, and D1 make a regulator circuit for powering the input side of the Si8921/22 from this floating supply. D1 establishes a voltage of 5.6 V at the base of Q3. R3 is selected to provide a Zener current of 10 mA for D1. C3 provides filtering at the base of Q3, and the emitter output of Q3 provides approximately 5 V to VDDA. C2 is a bypass capacitor for the supply and should be placed at the VDDA pin with its return trace connecting to the GNDA connection at RSENSE.

C4, the local bypass capacitor for the B-side of Si8921/22, should be placed close to the VDDB supply pin with its return close to GNDB. The output signal at AOP and AON is differential with a nominal gain of 8.2 (Si8921B) or 34.8 (Si8921A) and common mode of 1.4 V.

The outputs are sampled by a differential input ADC. Depending on the sample rate of the ADC, an anti-aliasing filter may be required. A simple anti-aliasing filter can be made from the passive components, R4, C6, and R5. (For the Si8922, Pin 6 and C6 are both grounded, and R5 is removed.)

The characteristics of this filter are dictated by the input topology and sampling frequency of the ADC. However, to ensure the Si8921 outputs are not overloaded, R4 = R5 > 5 kΩ and C6 can be calculated by the equation:

$$C6 = \frac{1}{2 \times \pi \times (R5 + R6) \times f_{3dB}}$$

2.3. Typical Performance Characteristics

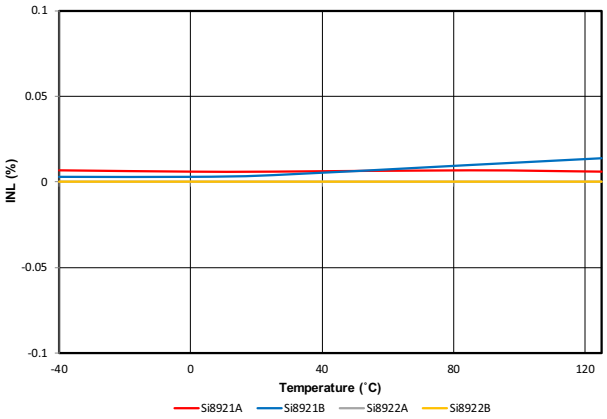


Figure 4. Nonlinearity (%) vs. Temperature (°C)

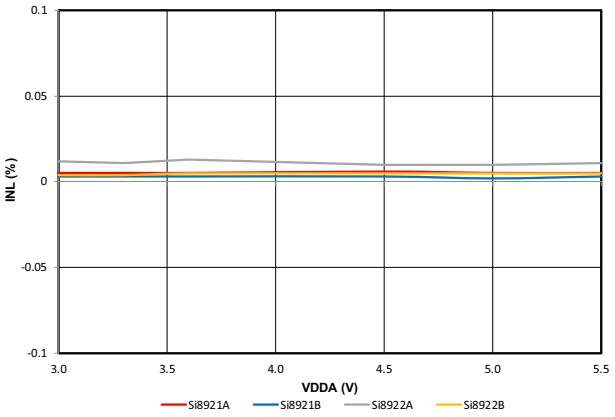


Figure 5. Nonlinearity (%) vs. VDDA Supply (V)

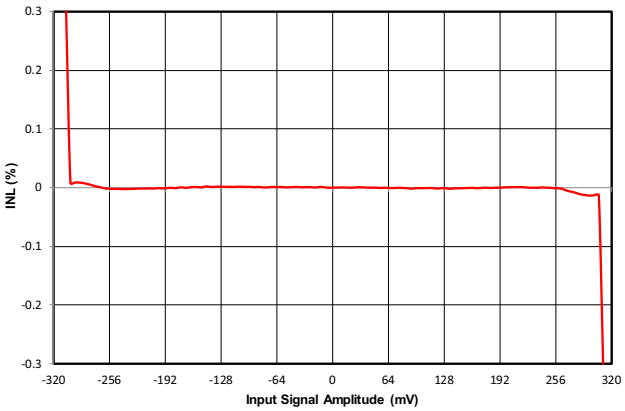


Figure 6. Si8921B Nonlinearity (%) vs. Input Signal Amplitude (mV)

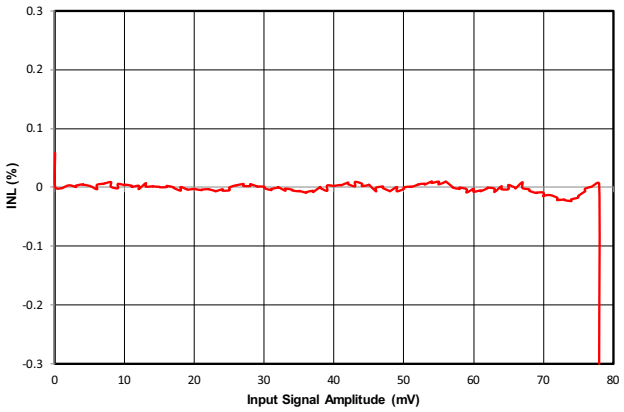


Figure 7. Si8921A Nonlinearity (%) vs. Input Signal Amplitude (mV)

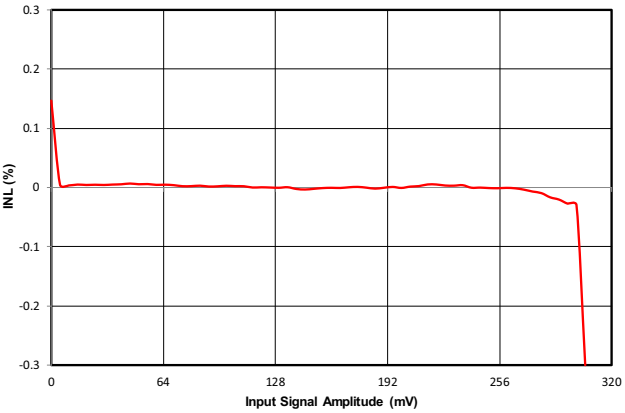


Figure 8. Si8922B Nonlinearity (%) vs. Input Signal Amplitude (mV)

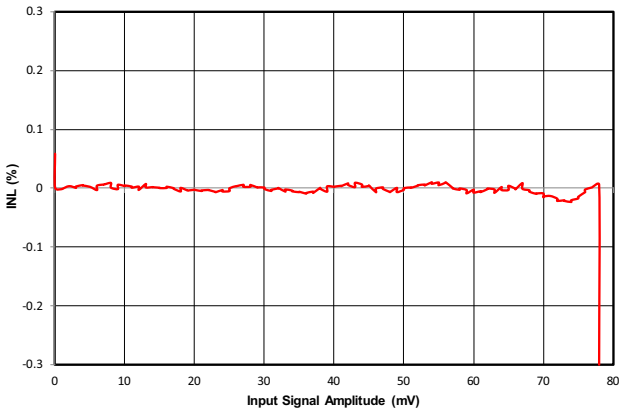


Figure 9. Si8922A Nonlinearity (%) vs. Input Signal Amplitude (mV)

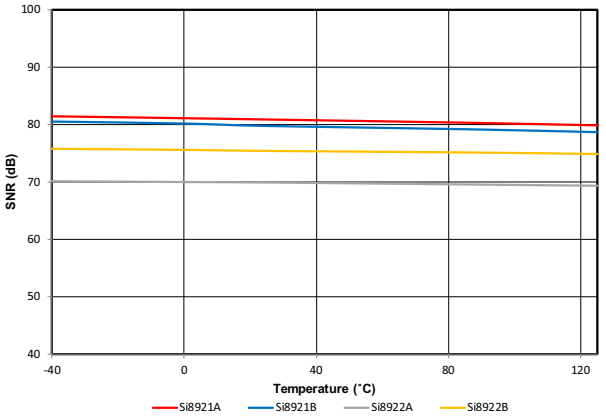


Figure 10. Signal-to-Noise Ratio (dB) vs. Temperature (°C)

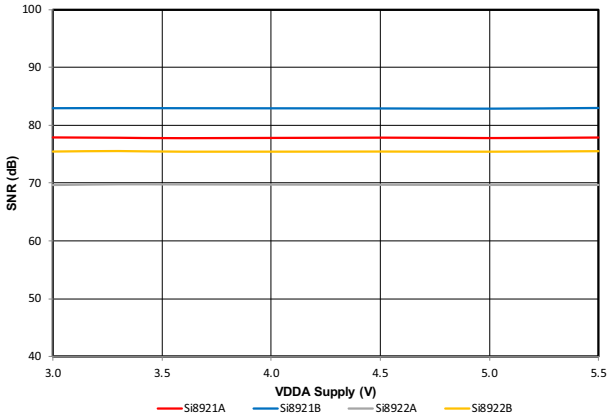


Figure 11. Signal-to-Noise Ratio (dB) vs. VDDA Supply (V)

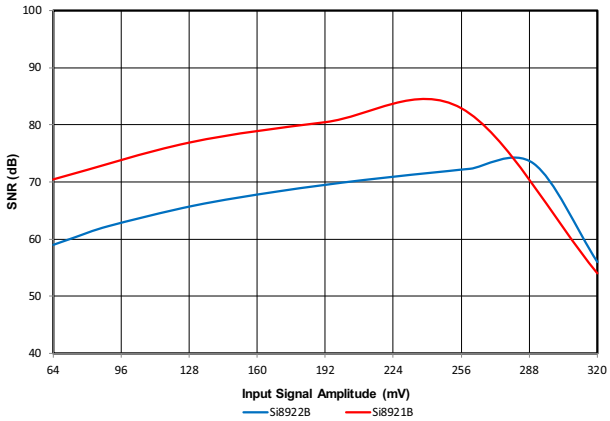


Figure 12. Si892xB Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)

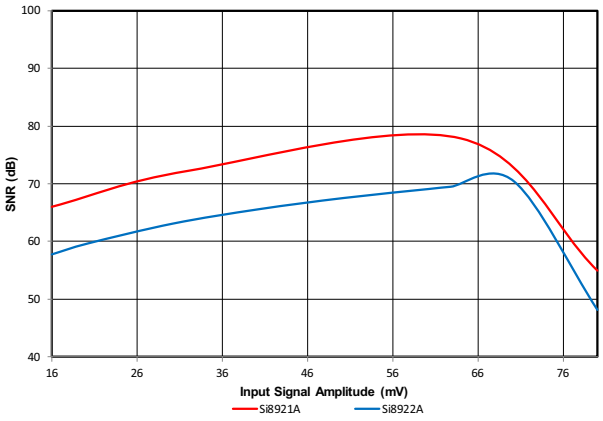


Figure 13. Si892xA Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)

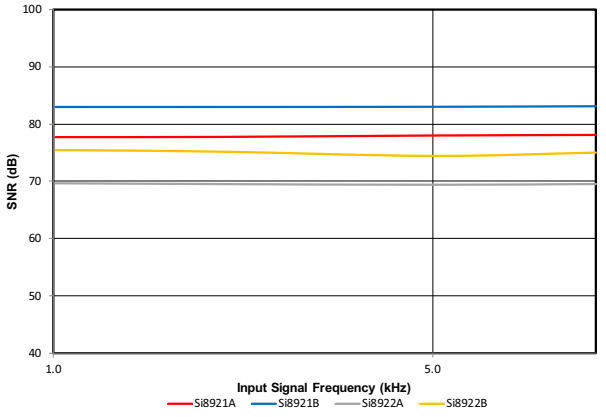


Figure 14. Signal-to-Noise Ratio (dB) vs. Input Signal Frequency (kHz)

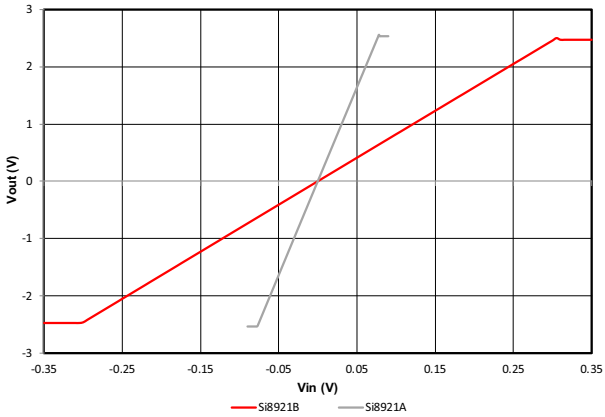


Figure 15. Si8921 Output Voltage (V) vs. Input Voltage (V)

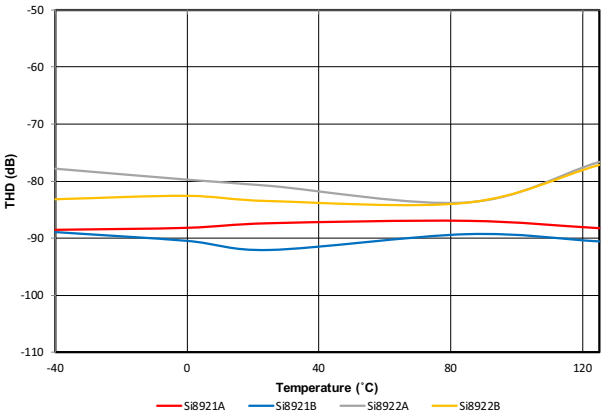


Figure 16. Total Harmonic Distortion (dB) vs. Temperature (°C)

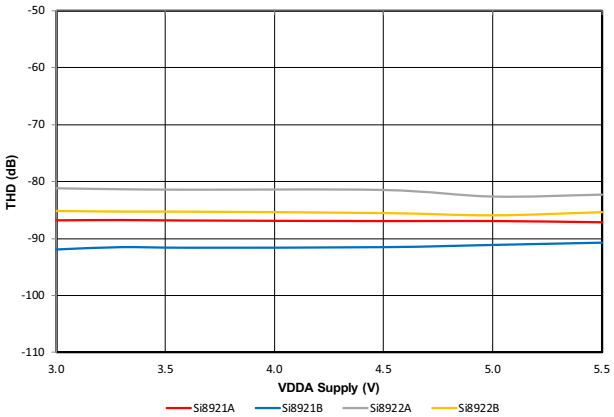


Figure 17. Total Harmonic Distortion (dB) vs. VDDA Supply (V)

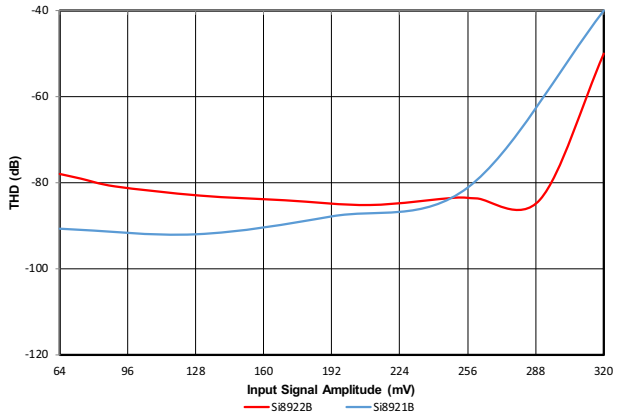


Figure 18. Si892xB Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)

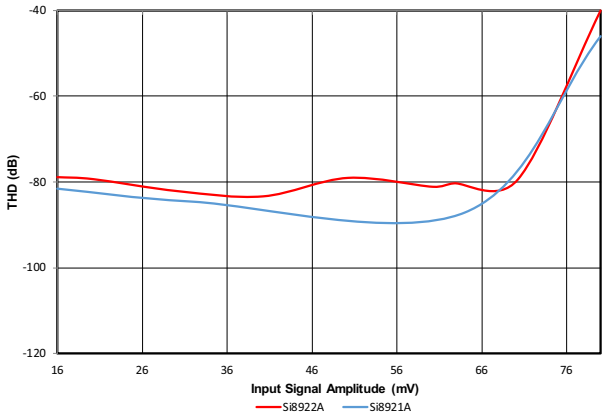


Figure 19. Si892xA Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)

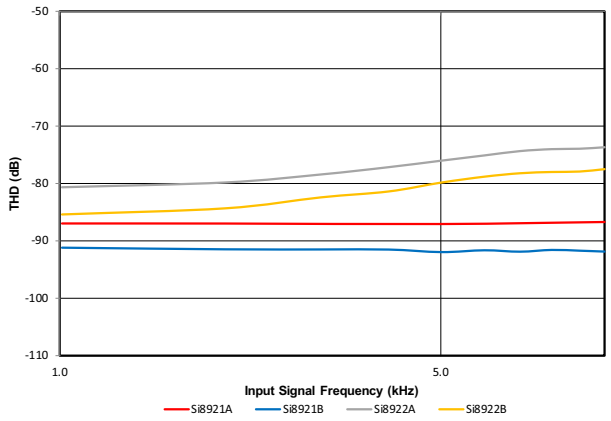


Figure 20. Total Harmonic Distortion (dB) vs. Input Signal Frequency (kHz)

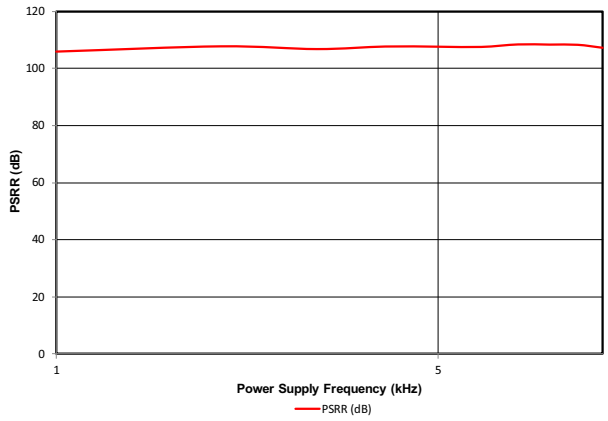


Figure 21. Power Supply Rejection Ratio vs. Power Supply Frequency (kHz)

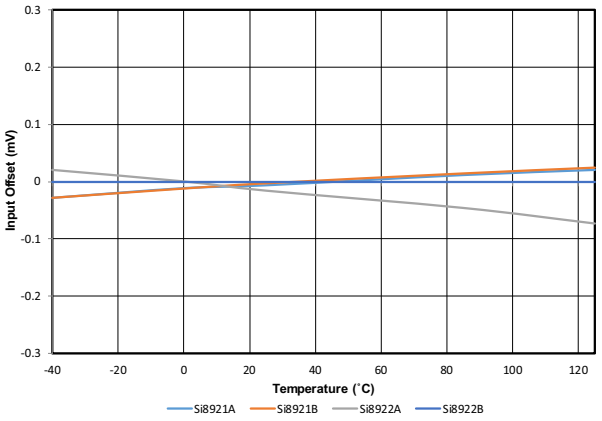


Figure 22. Input Offset (mV) vs. Temperature (°C)

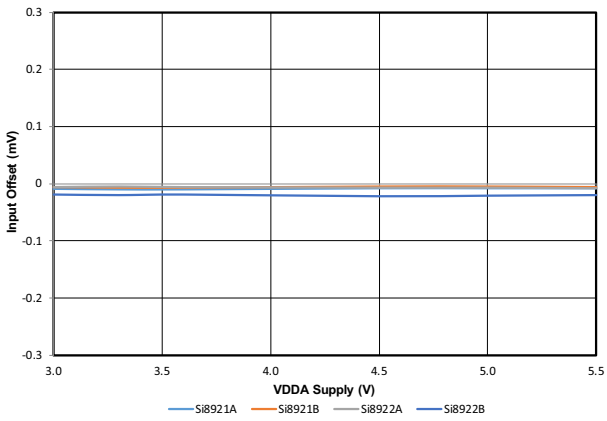


Figure 23. Input Offset (mV) vs. VDDA Supply (V)

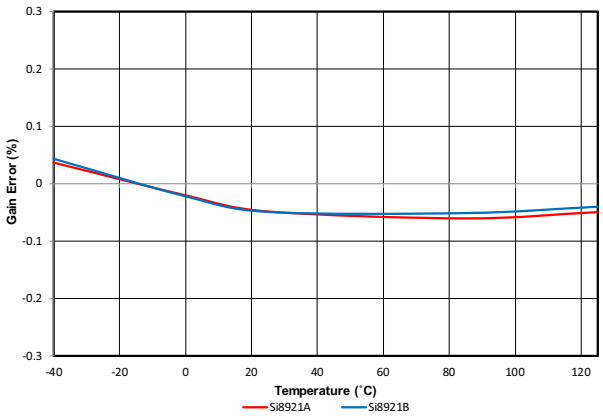


Figure 24. Gain Error (%) vs. Temperature (°C)

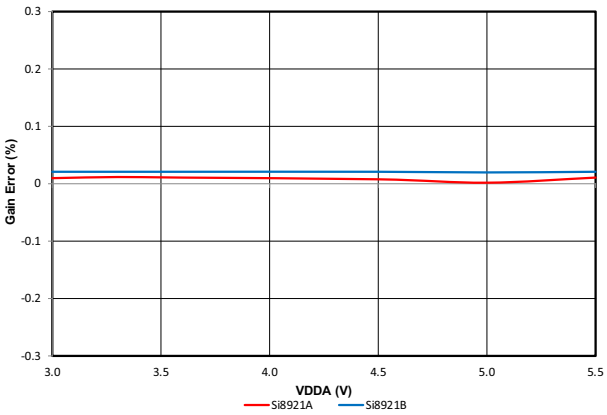


Figure 25. Gain Error (%) vs. VDDA Supply (V)

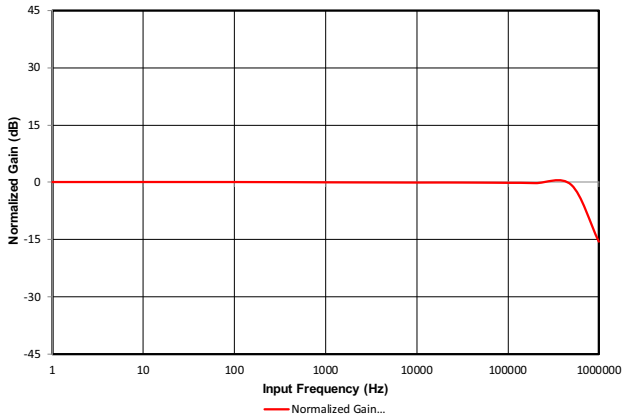


Figure 26. Amplifier Bandwidth

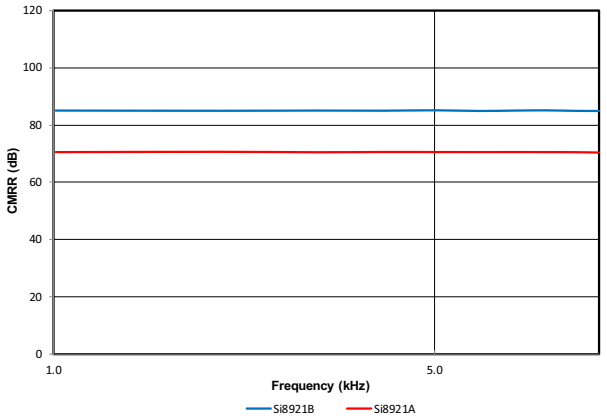


Figure 27. Common-Mode Rejection Ratio (dB) vs. Input Frequency (kHz)

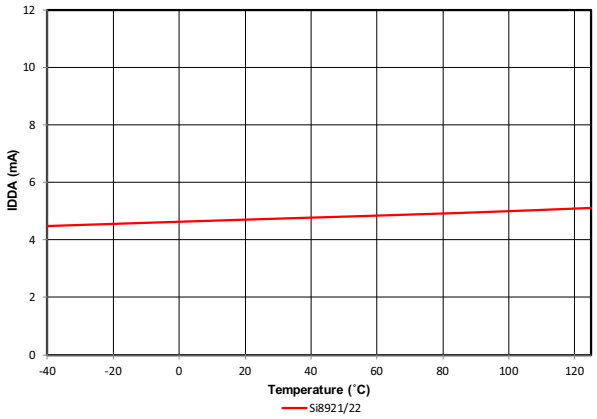


Figure 28. IDDA (mA) vs. Temperature (°C)

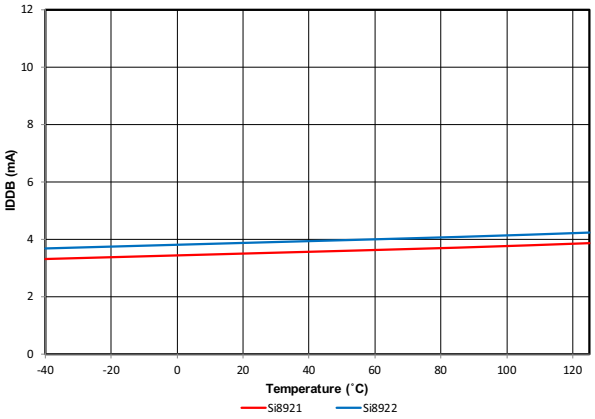


Figure 29. IDDB (mA) vs. Temperature (°C)

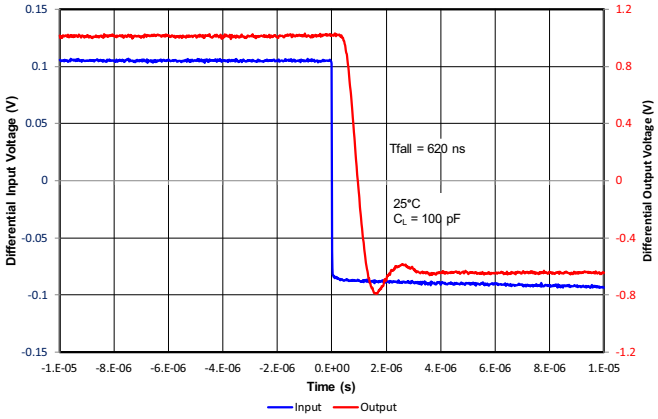


Figure 30. Si8921B High-to-Low Step Response

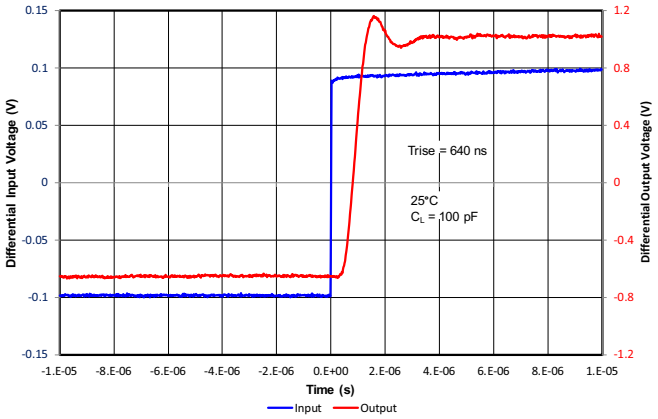


Figure 31. Si8921B Low-to-High Step Response

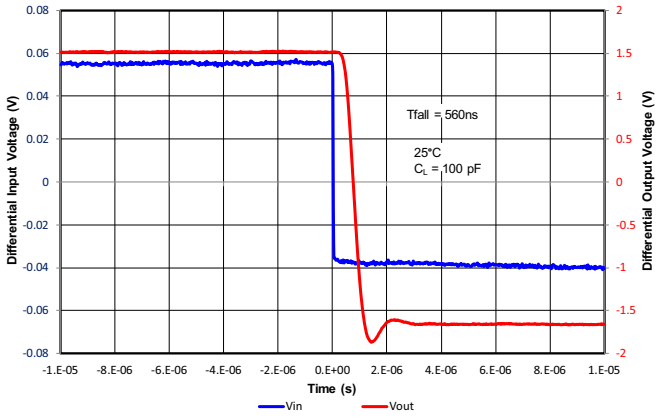


Figure 32. Si8921A High-to-Low Step Response

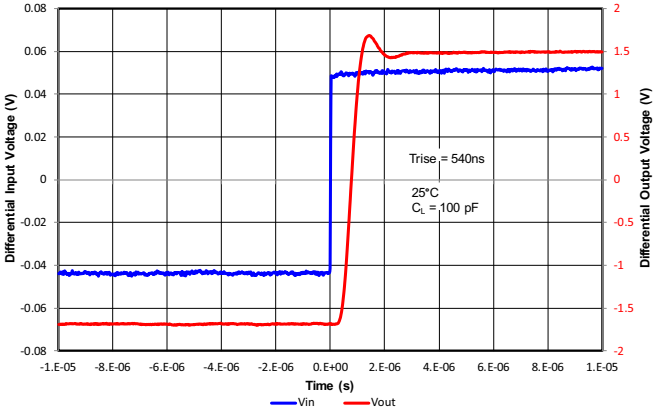


Figure 33. Si8921A Low-to-High Step Response

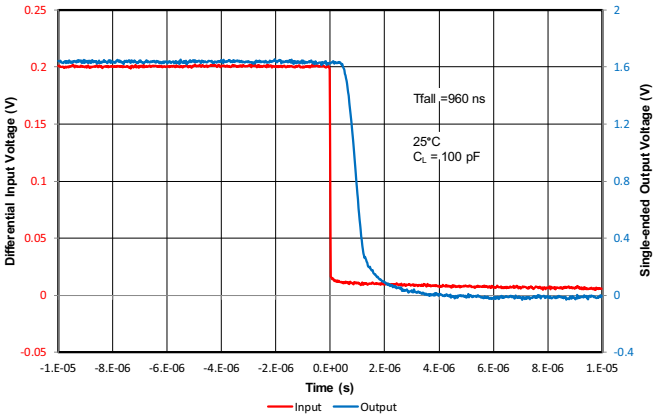


Figure 34. Si8922B High-to-Low Step Response

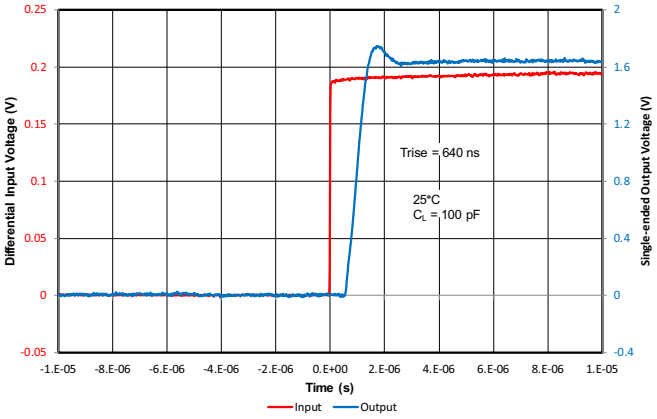


Figure 35. Si8922B Low-to-High Step Response

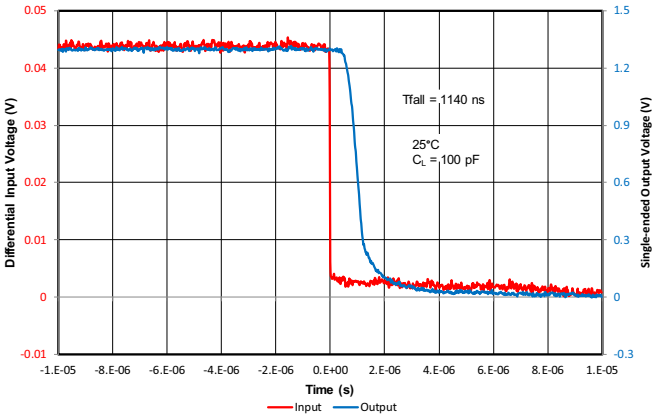


Figure 36. Si8922A High-to-Low Step Response

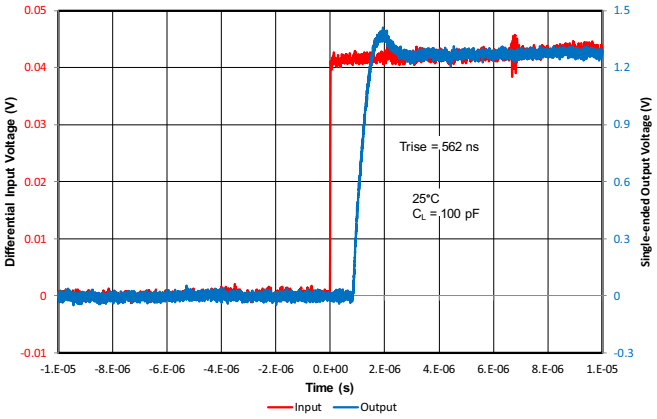


Figure 37. Si8922A Low-to-High Step Response

3. Specifications

3.1. Absolute Maximum Ratings

The absolute maximum ratings of the Si8921 and Si8922 are provided below and followed by electrical specifications, performance graphs, and mechanical specifications.

Table 4. Si8921 and Si8922 Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	–65	150	°C
Ambient temperature under bias	T_A	–40	125	°C
Junction temperature	T_J	—	150	°C
Supply voltage	VDDA, VDDB	–0.5	6.0	V
Input voltage respect to GNDA	VAIP, VAIN	–0.5	VDDA + 0.5	V
Output sink or source current	$\lvert I_O \rvert$	—	5	mA
Total power dissipation	P_T	—	212	mW
Lead solder temperature (10 s)		—	260	°C
Human Body Model ESD rating	HBM	—	6000	V
Charged Device Model ESD rating	CDM	—	2000	V

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

3.2. Electrical Characteristics

Table 5. Si8921 and Si8922 Electrical Specifications[1]

T_A = –40 to +125 °C, typical specs at 25 °C with VDDA = VDDB = 5 V unless specified differently under Test Condition

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
Input Side Supply Voltage		VDDA		3.0		5.5	V
Input Supply Current	Si8921A/21B	IDDA	VDDA = 3.3 V		4.6	6	mA
	Si8922A/22B	IDDA	VDDA = 3.3 V		4.5	6.1	mA
Output Side Supply Voltage		VDDB		3.0		5.5	V
Output Supply Current	Si8921A/21B	IDDB	VDDB = 3.3 V		3.5	4.5	mA
	Si8922A/22B	IDDB	VDDB = 3.3 V		4.3	5.6	mA
Amplifier Bandwidth					600		kHz
Amplifier Input							
Specified Linear Input Range	Si8921A	VAIP – VAIN		–62.5		62.5	mV
	Si8921B			–250		250	mV
	Si8922A	VAIP – VAIN		8		68.5	mV
	Si8922B			30		274	mV
Maximum Input Voltage Before Clipping	Si8921A	VAIP – VAIN			±77		mV
	Si8921B				±310		mV
	Si8922A			0	77		mV
	Si8922B			0	310		mV
Common-Mode Operating Range		VCM	AIN ≠ GNDA	–0.2		1	V
Input Referred Offset	Si8921A/21B	VOS	T_A = 25 °C, AIP = AIN = 0	–0.15	±0.04	0.15	mV
	Si8922A/22B	VOS	T_A = 25 °C, AO = 0.25 V	–0.35	±0.07	0.35	mV
Input Offset Drift		VOS_T		–0.3	0.5	3	µV/°C
Differential Input impedance	Si8921A/22A	RIN			6.3		kΩ
	Si8921B/22B				21.4		kΩ
Differential Input Impedance Drift		RIN_T			850		ppm/°C
Amplifier Output							
Full-Scale Output		VAOP – VAON			2.5		Vpk
Gain	Si8921A/22A				32.8		
	Si8921B/22B				8.2		
Gain Error			T_A = 25 °C	–0.2	±0.06	0.2	%
Gain Error Drift				–24	–9	0	ppm/°C
Output Common Mode Voltage (Si8921)		(VAOP + VAON)/2		1.34	1.39	1.49	V

Table 5. Si8921 and Si8922 Electrical Specifications[1] (Continued)

T_A = –40 to +125 °C, typical specs at 25 °C with VDDA = VDDB = 5 V unless specified differently under Test Condition

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
Nonlinearity	Si8921A		T_A = 25 °C	–0.04	0.01	0.04	%
	Si8921B		T_A = 25 °C	–0.02	0.003	0.02	%
	Si8922A		T_A = 25 °C	–0.08	0.02	0.08	%
	Si8922B		T_A = 25 °C	–0.04	0.01	0.04	%
Nonlinearity Drift				–16		16	ppm/°C
Signal-to-Noise Ratio	Si8921A	SNR	FIN = 10 kHz, BW = 100 kHz	70	77		dB
	Si8921B			75	82		dB
	Si8922A			64	71		dB
	Si8922B			69	76		dB
Signal-to-Noise Ratio	Si8921A	SNR	FIN = 1 kHz, BW = 10 kHz		86		dB
	Si8921B				91		dB
	Si8922A				79		dB
	Si8922B				83		dB
Total Harmonic Distortion	Si8921A	THD	F_{IN} = 1 kHz		–85	–74	dB
	Si8921B	THD	F_{IN} = 1 kHz		–88	–71	dB
	Si8922A	THD	F_{IN} = 1 kHz		–82	–60	dB
	Si8922B	THD	F_{IN} = 1 kHz		–85	–63	dB
Power-Supply Rejection Ratio		PSRR	VDDA at DC		–100		dB
			VDDA at 100 mV and 10 kHz ripple		–100		dB
			VDDB at DC		–100		dB
			VDDB at 100 mV and 10 kHz ripple		–100		dB
Output Resistive Load	Si8921	RLOAD	Between AON and AOP	5			kΩ
	Si8922		Between AO and GND	5			kΩ
Output Capacitive Load		CLOAD	Each pin to ground			100	pF
Timing							
Signal Delay (Si8921)		t_{PD}	50% to 50%		0.8		µs
Signal Delay (Si8922)		t_{PD}	50% to 50%		1		µs
Rise Time		t_R	10% to 90%		0.8		µs
Startup Time		$t_{STARTUP}$			250		µs
Common-Mode Transient Immunity[2]		CMTI	AIP = AIN = AGND, VCM = 1500 V	50	75		kV/µs

1. Performance is guaranteed only under the conditions listed in this Table and is not guaranteed over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.
2. An analog CMTI failure is defined as an output error of more than 100 mV persisting for at least 1 µs.

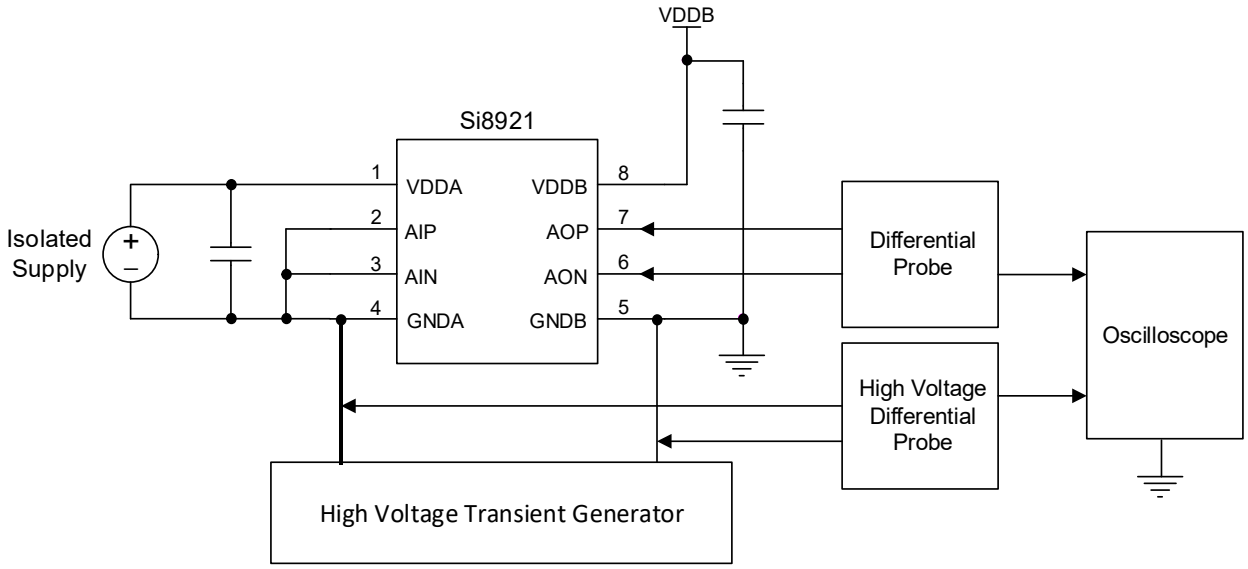


Figure 38. Common-Mode Transient Immunity Characterization Circuit

3.3. Thermal Characteristics

Table 6. Thermal Characteristics

Parameter	Symbol	WB Stretched SOIC-8	NB SOIC-8	Unit
IC Junction-to-air thermal resistance	θ_{JA}	90	112	°C/W

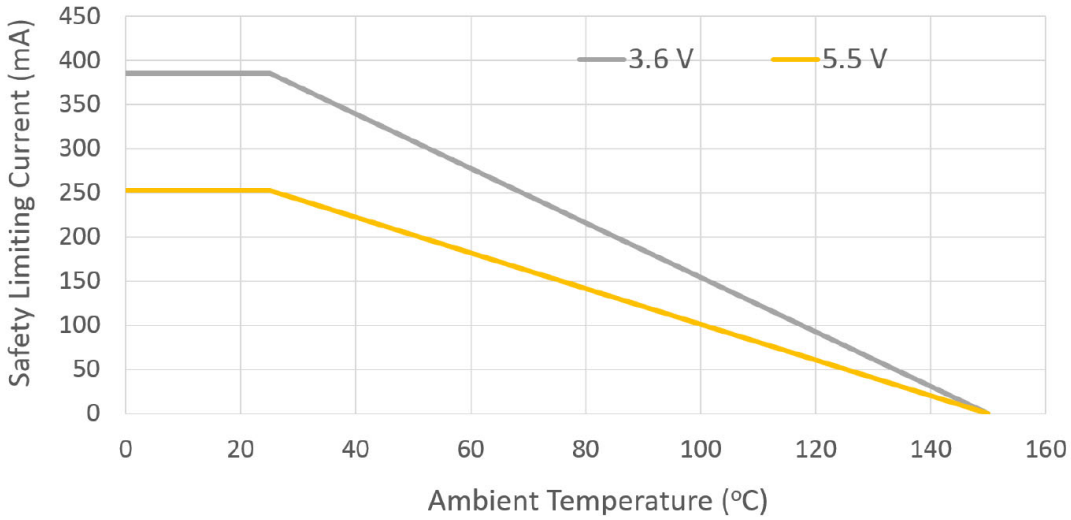


Figure 39. WB Stretched SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)

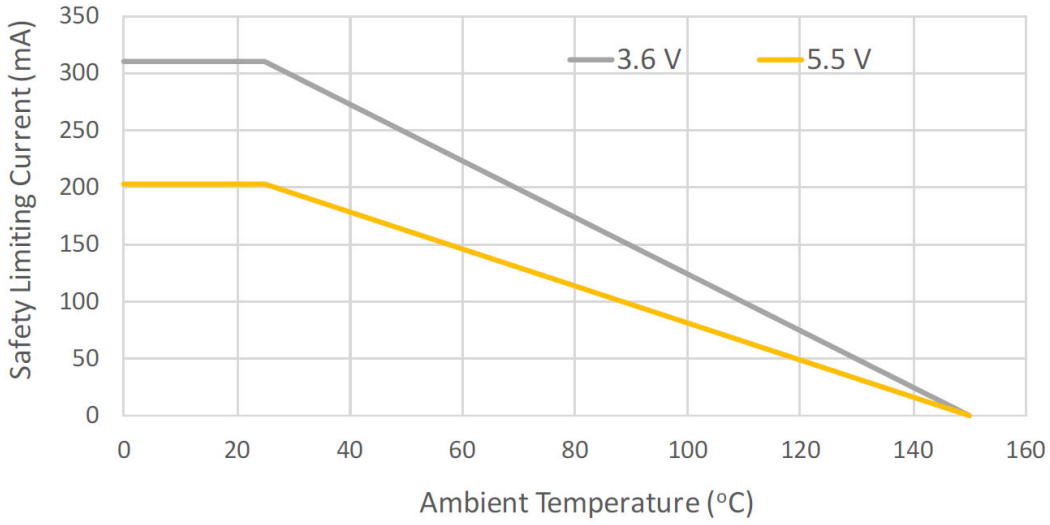


Figure 40. NB SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)

3.4. Safety Certifications and Specifications

Table 7. Regulatory Information[1]

CSA
The Si8921/Si8922 is certified under CSA. For more details, see Master Contract File 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si8921/Si8922 is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 V_{peak} for reinforced insulation working voltage.
UL
The Si8921/Si8922 is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si8921/Si8922 is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see Section 8. "Ordering Guide,"

Table 8. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Nominal external air gap (clearance)	CLR		8.0	4.0	mm
Nominal external tracking (creepage)	CRP		8.0	4.0	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	mm
Tracking resistance	PTI or CTI	IEC60112	600	600	V_{RMS}
Erosion depth	ED		0.04	0.04	mm
Resistance (input-output)[1]	R_{IO}	Test voltage = 500 V, 25 °C	10^{12}	10^{12}	Ω
Capacitance (input-output)[1]	C_{IO}	f = 1 MHz	1	1	pF

1. To determine resistance and capacitance, the Si8921/Si8922 is converted into a two-terminal device. Pins 1 to 4 are shorted together to form the first terminal, and pins 5 to 8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 9. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification	
		WB Stretched SOIC-8	NB SOIC-8
Material group		I	I
Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-IV	I-III
	Rated mains voltage ≤600 V_{RMS}	I-IV	I-II
	Rated mains voltage ≤1000 V_{RMS}	I-III	I

Table 10. IEC 60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	1500	445	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	2121	630	V_{peak}
Apparent charge	q_{pd}	Method b: At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	7070	3535	V_{peak}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile	10400	10400	V_{peak}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile	8000	5000	V_{peak}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 11. UL 1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Maximum withstanding isolation voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	2500	V_{RMS}

Table 12. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
Safety temperature	T_S		150	°C
Safety input, output or supply current (WB stretched SOIC-8)	I_S	θ_{JA} = 90 °C/W V_{DD} = 5.5 V T_J = 150 °C T_A = 25 °C	253	mA
		θ_{JA} = 90 °C/W V_{DD} = 3.6 V T_J = 150 °C T_A = 25 °C	386	mA
Safety input, output or supply current (NB SOIC-8)	I_S	θ_{JA} = 112 °C/W V_{DD} = 5.5 V T_J = 150 °C T_A = 25 °C	203	mA
		θ_{JA} = 112 °C/W V_{DD} = 3.6 V T_J = 150 °C T_A = 25 °C	310	mA
Safety input, output or total power (WB stretched SOIC-8)	P_S	θ_{JA} = 90 °C/W T_J = 150 °C T_A = 25 °C	1389	mW
Safety input, output or total power (NB SOIC-8)	P_S	θ_{JA} = 112 °C/W T_J = 150 °C T_A = 25 °C	1116	mW

1. Maximum value allowed in the event of a failure. Refer to the derating curves Figure 39, "WB Stretched SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)," on page 18 and Figure 40, "NB SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)," on page 18.

4. Package Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si8921 and Si8922 devices with an -IS and -AS suffix are rated to Moisture Sensitivity Level 2 (MSL2) at 260 °C. Devices with an -IS4 and -AS4 suffix are rated to Moisture Sensitivity Level 2A (MSL2A) at 260 °C.

All devices can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, “PCB Design and SMT Assembly/Rework Guidelines,” Document Number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

5. Package Outlines

5.1. 8-Pin, Wide-Body Stretched SOIC

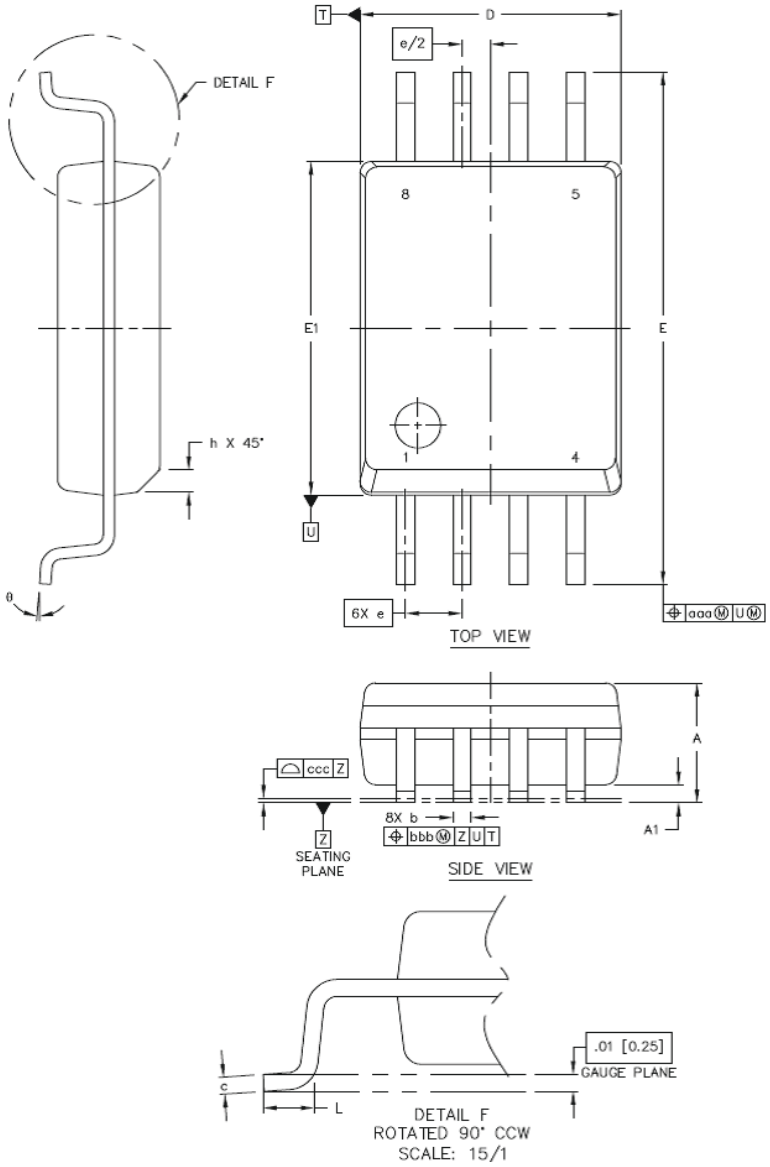


Figure 41. 8-Pin Wide Body Stretched SOIC Package

Table 13. 8-Pin Wide Body Stretched SOIC Package Dimensions[1,2]

Dimension	Millimeters	
	Min	Max
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.20	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
h	0.25	0.76
θ	0°	8°
aaa		0.25
bbb		0.25
ccc		0.10

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

5.2. 8-Pin, Narrow-Body SOIC

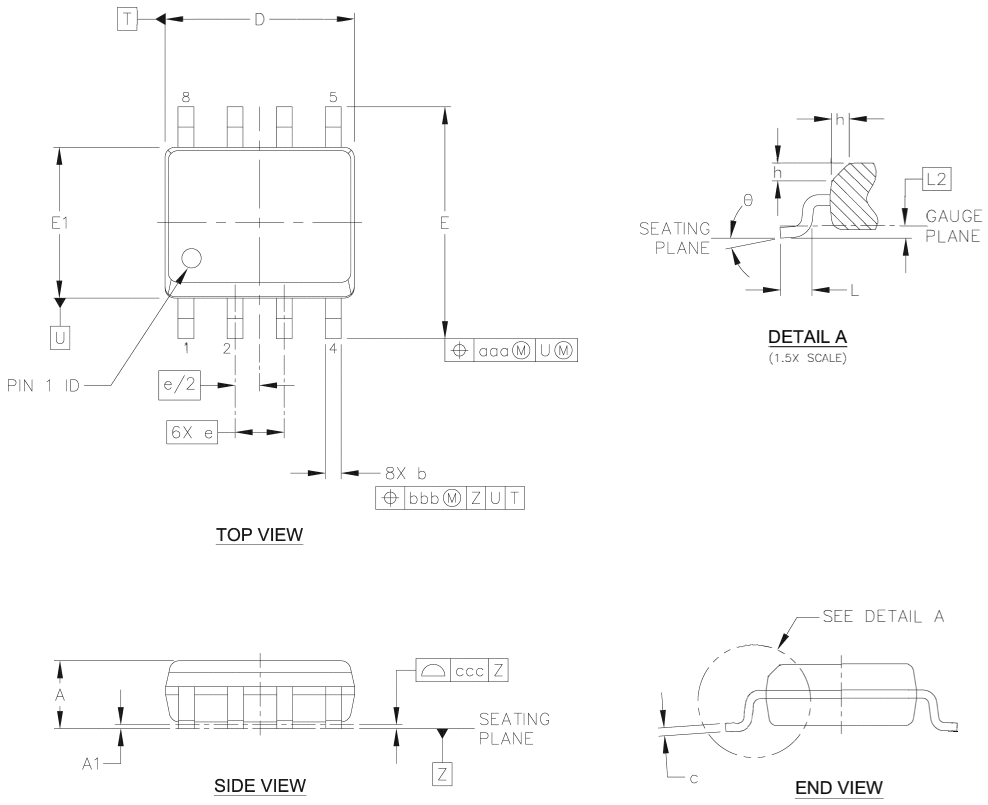


Figure 42. 8-Pin Narrow Body SOIC Package

Table 14. 8-Pin Narrow Body SOIC Package Dimensions[1,2,3,4,5]

Dimension	Symbol	Min	Max
Overall height	A	—	1.75
Stand off	A1	0.10	0.25
Lead width	b	0.33	0.51
L/F thickness	c	0.19	0.25
Body size	D	4.80	5.00
	E	5.80	6.20
	E1	3.80	4.00
Lead pitch	e	1.27 BSC	
Lead length	L	0.40	1.27
Gauge plane	L2	0.25 BSC	
Corner chamfer	h	0.25	0.50
Foot angle	θ	0°	8°

Table 14. 8-Pin Narrow Body SOIC Package Dimensions[1,2,3,4,5]

Dimension	Symbol	Min	Max
Lead edge tolerance	aaa		0.10
Lead offset	bbb		0.20
Coplanarity	ccc		0.10

1. All linear dimensions are in millimeters.
2. Dimensioning and tolerancing per ANSI Y14.5M.
   BSC: Basic dimension. Theoretically exact shown without tolerance.
   REF: Reference dimension. Usually without tolerance; for information purposes only.
3. Dimension D does not include mold flash, protrusions, or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. This drawing conforms to the JEDEC Solid State Outline MS-137, Variation AB.
5. Recommended reflow profile per JEDEC J_STD_020 specification for small body, lead-free components.

6. Land Patterns

6.1. 8-Pin, Wide-Body Stretched SOIC

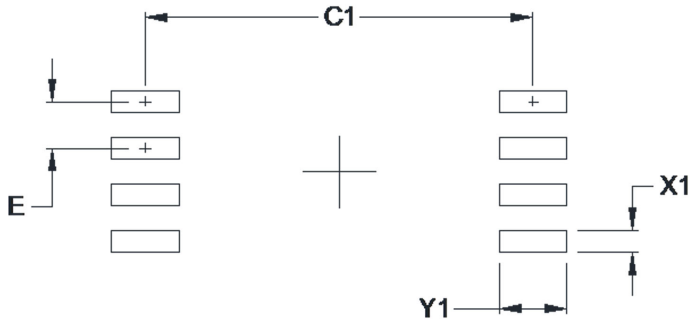


Figure 43. 8-Pin Wide Body Stretched SOIC Land Pattern

Table 15. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions

Dimension	mm	Notes
C1	10.60	**General** 1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. 2. This land pattern design is based on the IPC-7351 guidelines. **Solder Mask Design** 1. All metal pads are to be non-solder-mask-defined (NSMD). 2. Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
E	1.27	
X1	0.60	
Y1	1.85	

6.2. 8-Pin, Narrow-Body SOIC

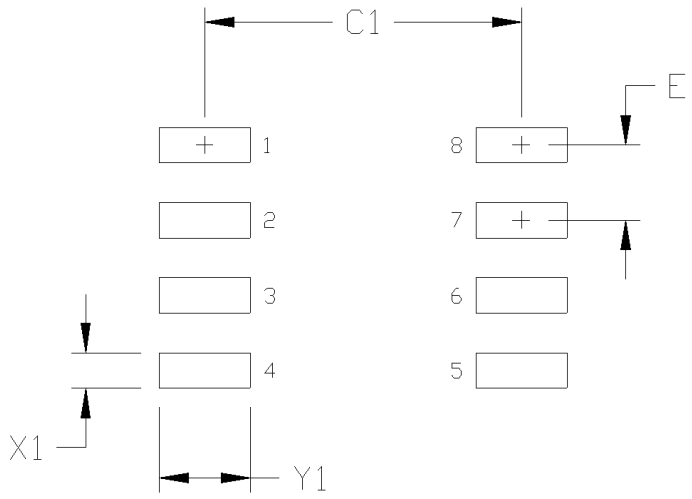


Figure 44. 8-Pin Narrow Body SOIC Land Pattern

Table 16. 8-Pin Narrow Body SOIC Land Pattern Dimensions[1,2]

Dimension	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
2. This land pattern design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).

7. Top Markings

7.1. 8-Pin, Wide-Body Stretched SOIC

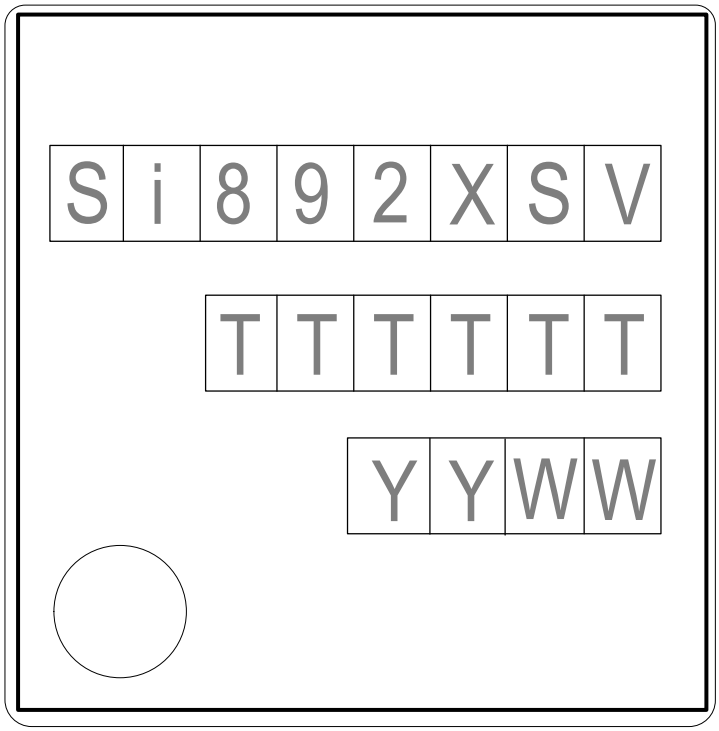


Figure 45. Si8921 Typical Package Marking, 8-Pin Wide Body Stretched SOIC

Table 17. 8-Pin Wide Body Stretched SOIC Top Marking Explanation

Line 1	Part Number	Si892x Isolator Amplifier Series X = Base part number 1 = Differential output 2 = Single-ended output S = Specified linear input range A = ±62.5 mV for Si8921, 8 to 68.5 mV for Si8922 B = ±250 mV for Si8921, 30 to 274 mV for Si8922 V = Insulation rating D = 5.0 kV_{RMS}
Line 2	TTTTTT	Manufacturing code The first character is a letter in the range N through Z to indicate Automotive Grade
Line 3	YY = Year WW = Work Week Circle = 43 mils diameter left justified	Year and work week

7.2. 8-Pin, Narrow-Body SOIC

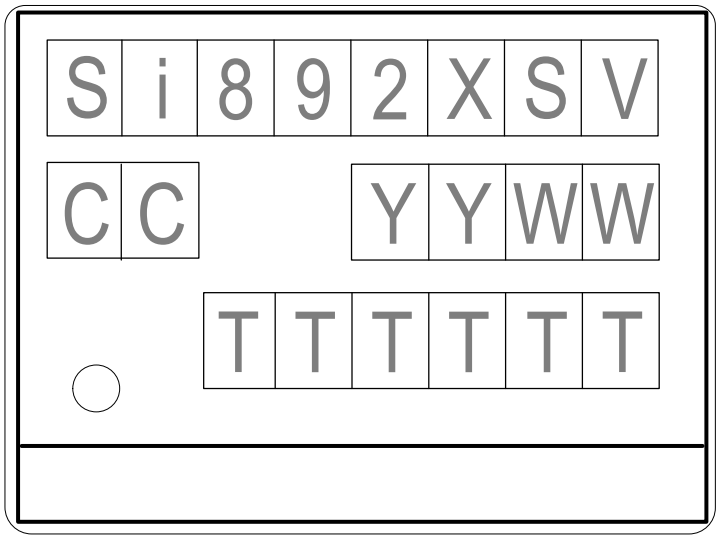


Figure 46. Si8921/22 Typical Package Marking, 8-Pin Narrow Body SOIC

Table 18. 8-Pin Narrow Body SOIC Top Marking Explanation

Line 1	Part Number	Si892x Isolator Amplifier Series X = Base part number 1 = Differential output 2 = Single-ended output S = Specified linear input range A = ±62.5 mV for Si8921, 8 to 68.5 mV for Si8922 B = ±250 mV for Si8921, 30 to 274 mV for Si8922 V = Insulation rating B = 2.5 kV_{RMS}
Line 2	CC = Country of origin ISO code abbreviation	
	YY = Year WW = Work Week	Year and work week
Line 3	TTTTTT - Manufacturing code Circle = 19.7 mils diameter left justified	Manufacturing code The first character is a letter in the range N through Z to indicate Automotive Grade

8. Ordering Guide

Industrial and Automotive Grade Ordering Part Numbers (OPNs)

Industrial-grade devices (part numbers with an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers with an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listings. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass-production steps.

Table 19. Ordering Guide

Ordering Part Number[1, 2, 3]	Automotive Ordering Part Number[1, 2, 3, 4, 5]	Ordering Options			
		Specified Input Range	Isolation Rating	Output	Package Type
Si8921AD-IS4	Si8921AD-AS4	±62.5 mV	5.0 kV_{RMS}	Differential	WB stretched SOIC-8
Si8921BD-IS4	Si8921BD-AS4	±250 mV	5.0 kV_{RMS}	Differential	WB stretched SOIC-8
Si8921AB-IS	Si8921AB-AS	±62.5 mV	2.5 kV_{RMS}	Differential	NB SOIC-8
Si8921BB-IS	Si8921BB-AS	±250 mV	2.5 kV_{RMS}	Differential	NB SOIC-8
Si8922AD-IS4	Si8922AD-AS4	8 to 68.5 mV	5.0 kV_{RMS}	Single-ended	WB stretched SOIC-8
Si8922BD-IS4	Si8922BD-AS4	30 to 274 mV	5.0 kV_{RMS}	Single-ended	WB stretched SOIC-8
Si8922AB-IS	Si8922AB-AS	8 to 68.5 mV	2.5 kV_{RMS}	Single-ended	NB SOIC-8
Si8922BB-IS	Si8922BB-AS	30 to 274 mV	2.5 kV_{RMS}	Single-ended	NB SOIC-8

1. All packages are RoHS-compliant.
2. “Si” and “SI” are used interchangeably.
3. An “R” at the end of the part number denotes tape and reel packaging option.
4. Automotive-grade devices (“-A” suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial Grade (“-I suffix”) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
5. In the top markings of each device, the Manufacturing Code represented by “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive Grade.

9. Revision History

Revision	Date	Description
D	September, 2025	• Updated 8-Pin, Narrow-Body SOIC package. • Removed Tape and Reel information.
C	September, 2023	• Updated regulatory information. • Updated Absolute Maximum Note 1. • Removed unneeded minimum IDD specifications.
B	May, 2023	• Reformatted to new standards. • Added new text for Automotive Grade products, AEC-Q100 qualification. • Added MSL ratings and tape and reel information. • Updated THD specifications. • Updated specified linear input range. • Updated block diagrams on page 1. • Updated Si8922 pin description.
A	December, 2022	• Updated decimal-based revision number to alphanumeric code.
0.9	September, 2022	• Updated Safety Approvals. • Updated minimum supply currents in Electrical Specifications. • Updated Regulatory Information.
0.8	June, 2021	• Added Automotive OPNs and updated specified input range in Ordering Guide. • Updated Current Sense Application figure. • Added linearity minimum specification to Table 4.1 Electrical Specifications.
0.7	April, 2020	• Numerous clarifications throughout. • Updated Electrical Specifications after full characterization. • Changed Si8922 Pin 6 from NC to GND.
0.51	June, 2019	• Added section for Automotive Grade OPNs. • Corrected error in Specified Linear Input Range. • Changed DTI Specification. • Corrected Si8922 Pin Diagram. • Updated supply currents.
0.5	March, 2019	• Updated specifications. Added narrow body SOIC-8 package.
0.1	February, 2018	Initial release.