DATA SHEET

Si5386: 12-Channel, Any-Frequency, Any-Output Wireless Jitter Attenuator/Clock Multiplier with Ultra-Low Noise

The Si5386 is an ultra-high performance wireless jitter attenuator with any frequency outputs for Ethernet-based Common Public Radio Interface (eCPRI) applications, which demand the highest level of integration and phase noise performance. Based on Skyworks Solutions fourth generation DSPLL® technology, the Si5386 combines frequency synthesis and jitter attenuation in a highly integrated digital solution with a cost-effective oscillator, and without the need of any external loop filter components. The fixed frequency oscillator provides frequency stability for free-run and holdover modes.

This all-digital solution provides superior performance that is highly immune to external board disturbances such as power supply noise.

eCPRI-based remote radio heads and fixed wireless systems require a diverse set of clocks such as ADC/DAC, RF LOs, and Ethernet clocks. The Si5386 architecture is designed to deliver high-performance JESD204B DCLK and SYSREF clock pairs and flexible any-rate clocks for non-CPRI clocks such as Ethernet and system reference clocks all from a single IC.

Applications

- Wireless infrastructure
  - eCPRI Remote Radio Head (RRH)
  - Baseband Unit (BBU)
  - Small cell and µBTS
- DOCSIS
- Test and measurement

Key Features

- Flexible timing in a single IC
  - Generates any combination of output frequencies from any input frequency
- Input frequency range:
  - Differential: 80 kHz to 750 MHz
  - LVCMOS: 80 kHz to 250 MHz
  - Output frequency range (integer):
  - Differential: up to 2.94912 GHz
- Output frequency range (fractional):
  - Differential: up to 735 MHz
  - LVCMOS: up to 250 MHz
- Ultra-low RMS jitter:
  - 72 fs typ (12 kHz to 20 MHz)
- Phase noise of 122.88 MHz carrier frequency:
  - 118 dBc/Hz @ 100 Hz offset
- ITU-T G.8262 compliant
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

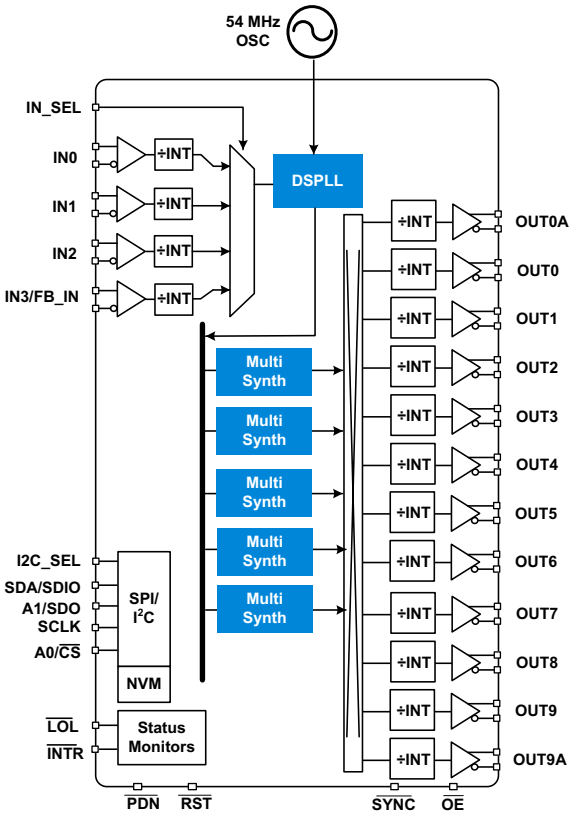


Figure 1. Functional Block Diagram

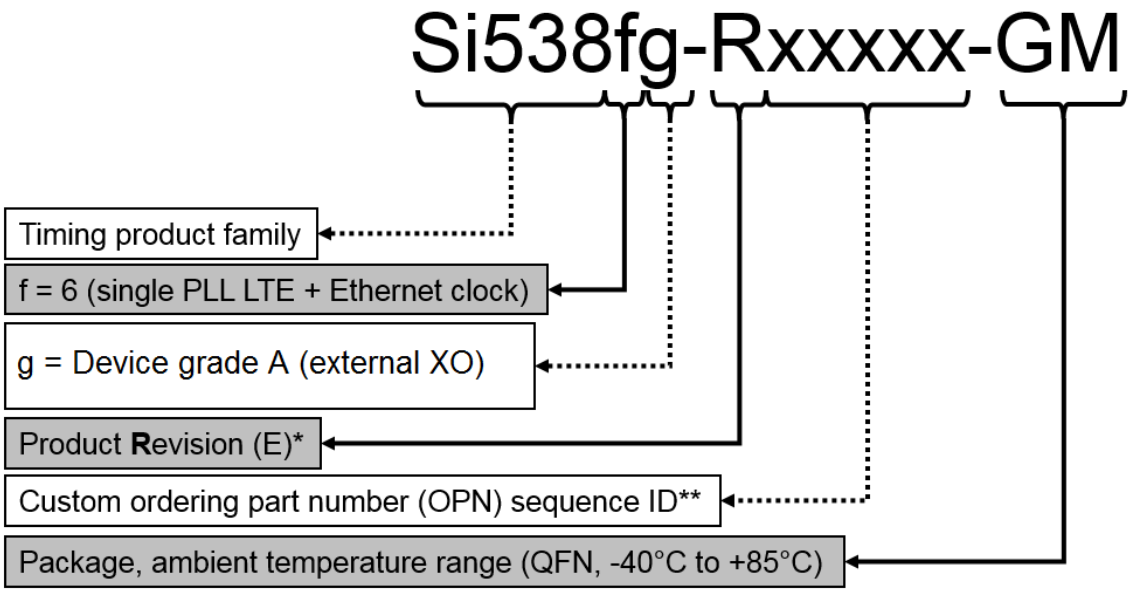
1. Features List

- ITU-T G.8262 compliant
- Flexible timing in a single IC
  - Generates any combination of output frequencies from any input frequency
- Input frequency range:
  - Differential: 80 kHz to 750 MHz
  - LVCMOS: 80 kHz to 250 MHz
- Output frequency range (integer):
  - Differential: up to 2.94912 GHz with JESD204B support
- Output frequency range (fractional):
  - Differential: up to 735 MHz
  - LVCMOS: up to 250 MHz
- Ultra-low RMS jitter (12 kHz to 20 MHz):
  - 72 fs typ. at 122.88 MHz
  - 88 fs typ. at 156.25 MHz
  - 79 fs typ. at 322.265625 MHz
- Programmable jitter attenuation bandwidth from 1 Hz to 4 kHz
- Phase noise of 122.88 MHz carrier frequency:
  - –118 dBc/Hz @ 100 Hz offset
  - –133 dBc/Hz @ 1 kHz offset
  - –142 dBc/Hz @ 10 kHz offset
  - –149 dBc/Hz @ 100 kHz offset
  - –154 dBc/Hz @ 1 MHz offset
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL. CML outputs can be programmed to have 100 to 1600 mVpp single-ended swing.
- Status monitoring: Loss of Signal (LOS), Out of Frequency (OOF), Loss of Lock (LOL)
- Pin controlled input switching
- DSPLL with special wireless calibration
- Optional zero delay mode
- Hitless input clock switching: automatic or manual
- Automatic free-run and holdover modes
- Fastlock feature
- Glitchless on the fly output frequency changes
- Core voltage:
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- Independent output clock supply pins: 3.3 V, 2.5 V, or 1.8 V
- Output-output skew: 20 ps typ.
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder® Pro software simplifies device configuration
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

2. Ordering Information

Ordering Part Number (OPN)	Reference	Number of Input/Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes	Package	Temperature Range (°C)
Si5386						
Si5386A-E-GM[1,2]	External XO	4/12	0.0001 to 2949.12	Integer and fractional	64-QFN 9 x 9 mm	–40 to 85

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. Ordering part numbers are assigned by Skyworks and the ClockBuilder Pro software utility. Custom part number format is “Si5386A-Exxxxx-GM” where “xxxxx” is a unique numerical sequence representing the preprogrammed configuration.



*See Ordering Guide table for current product revision.
** (Optional) 5 digits; assigned by ClockBuilder Pro for Custom, factory-preprogrammed OPN devices only;
(The “xxxxx” field is not included for “Base” OPNs).

Figure 2. Ordering Guide Key

3. Functional Description

The Si5386 internal DSPLL provides jitter attenuation and any-frequency multiplication of the selected input frequency without the need for (external) VCXOs and loop filters. Input switching is controlled manually or automatically using an internal state machine. The external oscillator provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode.

The high-performance MultiSynth™ dividers (N) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the MultiSynth generated frequencies to any of the outputs. Additional integer division (R) determines the final output frequency. Further, the DSPLL is specially calibrated for ultra-low phase noise when configured for CPRI frequencies with JESD204B outputs. This integration provides a clock-tree-on-a-chip solution for applications that need a mix of 4G/CPRI, Ethernet, and general-purpose frequencies.

3.1. Frequency Configuration

The DSPLL frequency configuration is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (P_n/P_d), fractional frequency multiplication (M_n/M_d), fractional output MultiSynth division (N_n/ N_d), and integer output division (R_n) allows the generation of virtually any output frequency on any of the outputs with very low-phase noise suitable for wireless applications when synthesizing CPRI frequencies. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

3.2. DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 20 Hz to 4 kHz are available for selection. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

3.3. Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g., 20 Hz) will generally lengthen the lock acquisition time. The Fastlock feature allows setting a temporary Fastlock loop bandwidth that is used during the lock acquisition process. Higher Fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock loop bandwidth settings in the range of 20 Hz to 4 kHz are selectable. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

3.4. Modes of Operation

Once initialization is complete the DSPLL operates in one of five modes: Free-run Mode, VCO Freeze Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown below. The following sections describe each of these modes in greater detail.

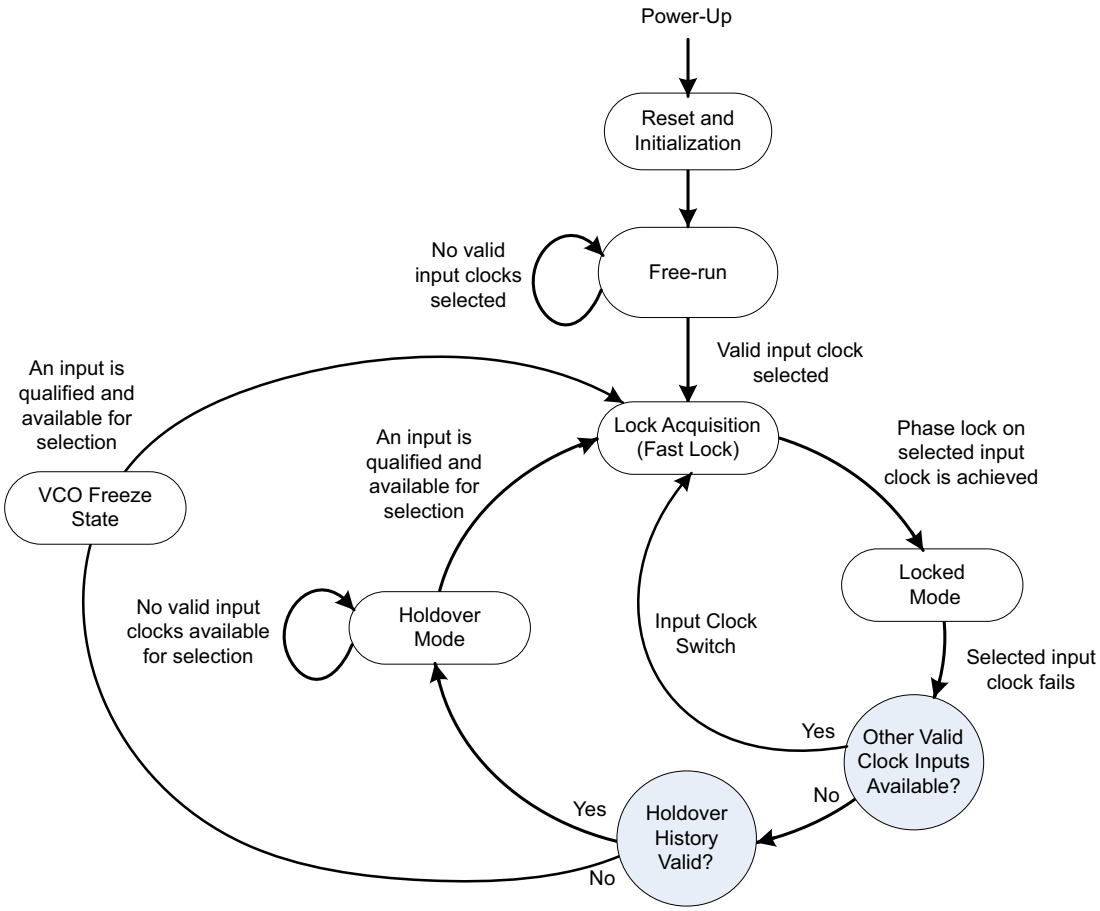


Figure 3. Modes of Operation

3.4.1. Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks are generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers are restored to the values stored in NVM, and all circuits including the serial interface is restored to their initial state. A hard reset is initiated using the RSTb pin or by asserting the hard reset register bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

3.4.2. Freerun Mode

The DSPLL will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the reference clock on the XA/XB pins. For example, if the oscillator stability is ±50 ppm, then all the output clocks will be generated at their configured frequency with ±50 ppm stability in freerun mode. Any drift of the oscillator frequency is tracked at the output clock frequencies. Freerun mode is maintained as long as no input clocks are valid.

3.4.3. Lock Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL automatically starts the lock acquisition process. If the fast lock feature is enabled, the DSPLL acquires lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition, the output generates a clock that follows the VCO frequency change as it pulls in to the input clock frequency.

3.4.4. Locked Mode

Once locked, the DSPLL generates output clocks that are both frequency and phase locked to their selected input clocks. At this point, any oscillator frequency drift does not affect the output frequency. A loss of lock (LOL) pin and status bit indicate when lock is achieved. See “3.7.4. LOL Detection” on page 12 for more details on the operation of the loss-of-lock circuit.

3.4.5. Holdover Mode

If holdover history is valid, the DSPLL automatically enters holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

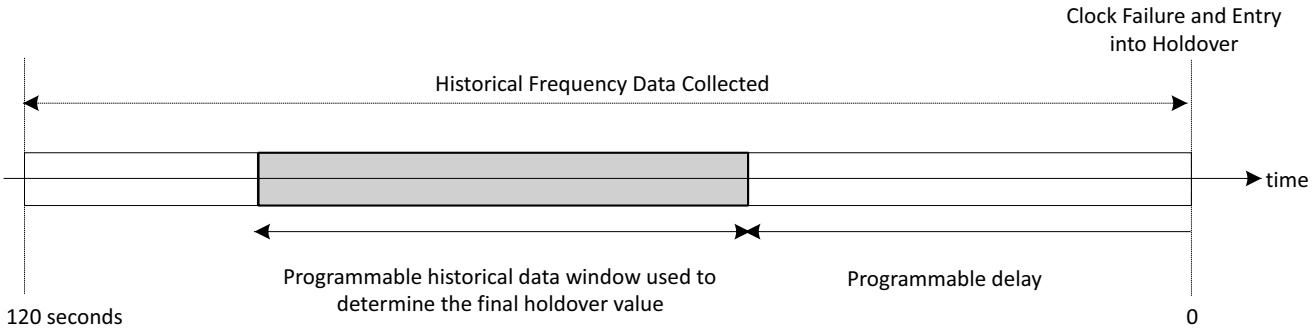


Figure 4. Programmable Holdover Window

When entering holdover, the DSPLL pulls its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL automatically exits the holdover mode and re-acquires lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the Fastlock bandwidth.

The DSPLL output frequency when exiting holdover can be ramped (recommended). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in-between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching, see “3.6.4. Ramped Input Switching” on page 10.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

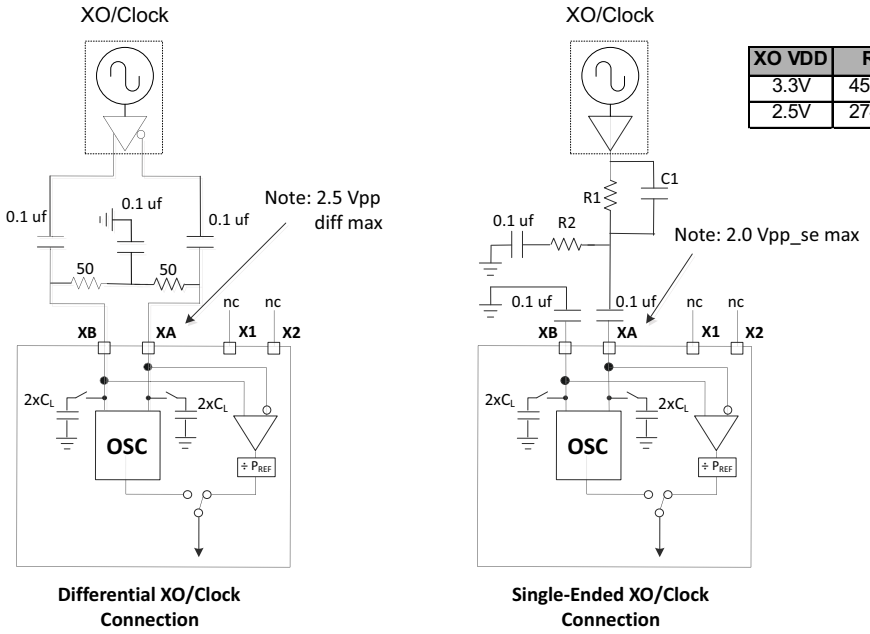
3.4.6. VCO Freeze Mode

If holdover history is not valid, the DSPLL automatically enters VCO Freeze mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses the last measured input frequency to set the output frequencies in the VCO Freeze mode. If an input clock becomes valid, the DSPLL automatically exits the VCO Freeze mode and re-acquires lock to the new input clock.

3.5. External Reference (XA/XB)

An external crystal oscillator (XO) is required to set the reference for the Si5386. Only a 54 MHz XO is used as the reference to the wireless jitter attenuator. For the jitter and phase noise performance that is specified in this data sheet, the only XOs that can be used are the 54 MHz XOs recommended for the Si5381/82/86 in the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual.

Place the XO as close to the XaXb pins as possible. See the figure below for guidelines on how to connect the XO to the XaXb input. C1 increases the slew rate to the Xa input, which is needed to get the jitter and phase noise performance that is specified in this data sheet.



Differential XO/Clock Connection

Single-Ended XO/Clock Connection

XO VDD	R1	R2	C1	Appro. Vpp @ XA Input
3.3V	453 Ω	549 Ω	12 pf	1.8V
2.5V	274 Ω	732 Ω	30 pf	1.8V

Figure 5. XA/XB Input

3.6. Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize the DSPLL. The inputs accept both differential and single-ended clocks. Input selection can be manual (pin or register controlled) or automatic with user definable priorities. See the Si5386 Rev. E Family Reference Manual for details and input termination requirements.

3.6.1. Manual Input Switching (IN0, IN1, IN2, IN3)

Input clock selection can be made manually using the IN_SEL[1:0] pins or through a register. A register bit determines input selection as pin selectable or register selectable. The IN_SEL pins are selected by default. If there is no clock signal on the selected input, the device automatically enters free-run or holdover mode. When the zero delay mode is enabled, IN3 becomes the feedback input (FB_IN) and is not available for selection as a clock input.

Table 1. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input	
		Zero Delay Mode Disabled	Zero Delay Mode Enabled
0	0	IN0	IN0
0	1	IN1	IN1
1	0	IN2	IN2
1	1	IN3	Reserved

3.6.2. Automatic Input Selection (IN0, IN1, IN2, IN3)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on input clock qualification, input priority, and the revertive option. Only input clocks that are valid can be selected by the automatic clock selection state machine. If there are no valid input clocks available, the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input is initiated. With non-revertive switching, the active input always remains selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority is initiated.

3.6.3. Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or at a fractional frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during an input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 7.68 MHz.

3.6.4. Ramped Input Switching

When switching between two plesiochronous input clocks (i.e., the frequencies are almost the same, but not quite), ramped input switching should be enabled to ensure a smooth transition between the two inputs. Ramped input switching avoids frequency transients and overshoot when switching between frequencies and so is the default switching mode in CBPro. The feature should be turned off when switching between input clocks that are always frequency locked (i.e., are always the same exact frequency). The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover see "3.4.5. Holdover Mode" on page 6.

3.6.5. Glitchless Input Switching

The DSPLL has the ability of switching between two input clock frequencies that are up to 40 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no abrupt phase change at the output during the transition.

3.7. Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3/FB_IN) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLL. There is also a loss of lock (LOL) indicator which is asserted when the DSPLL loses synchronization.

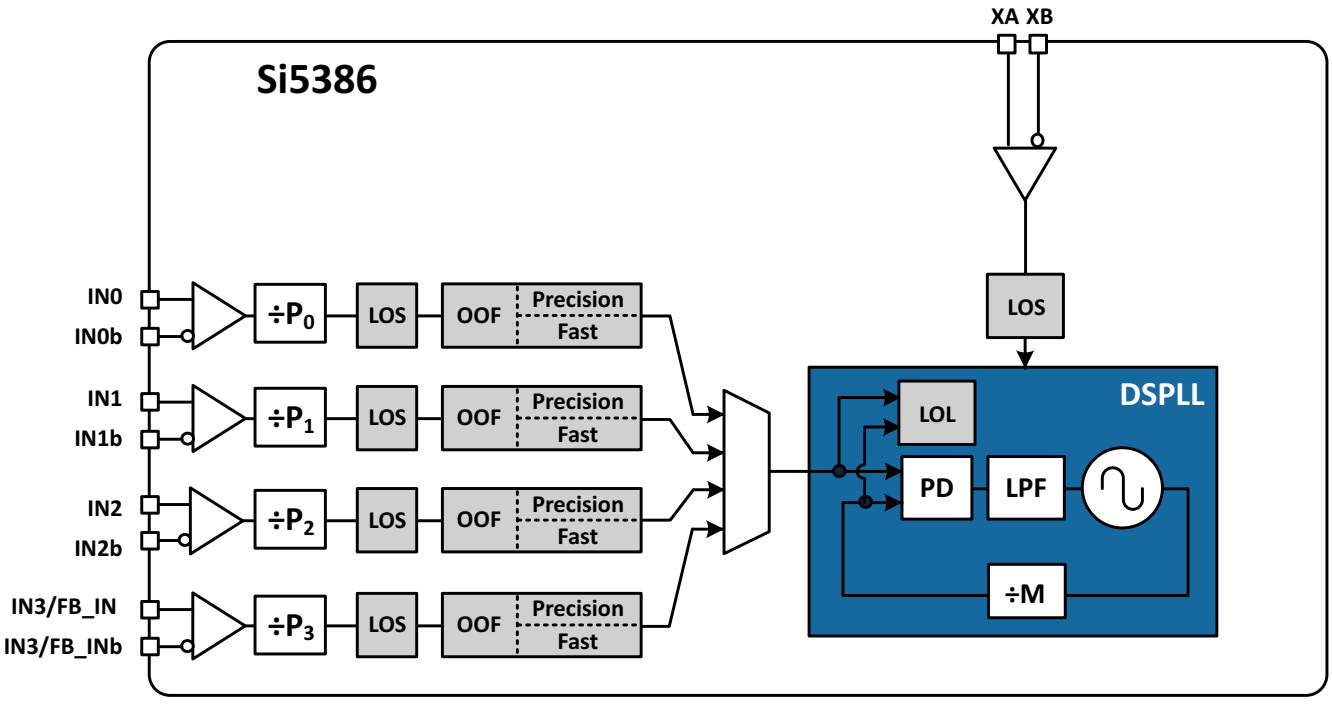


Figure 6. Si5386 Fault Monitors (Grade A)

3.7.1. Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility.

The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

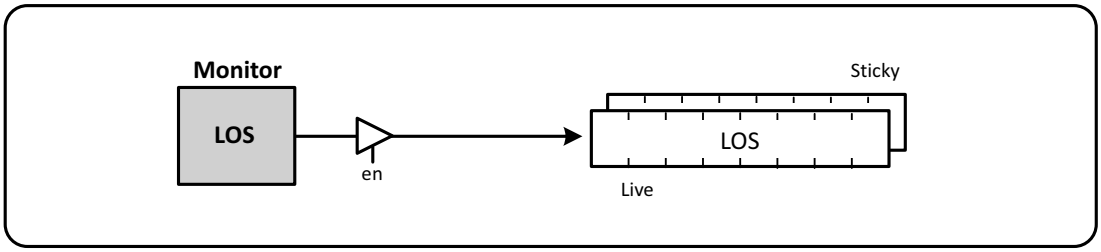


Figure 7. LOS Status Indicators

3.7.2. Reference Clock LOS Detection

An LOS monitor is available to ensure that the external reference oscillator is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

3.7.3. OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0_ppm” reference. This OOF reference can be selected as either:

- The XA/XB reference
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

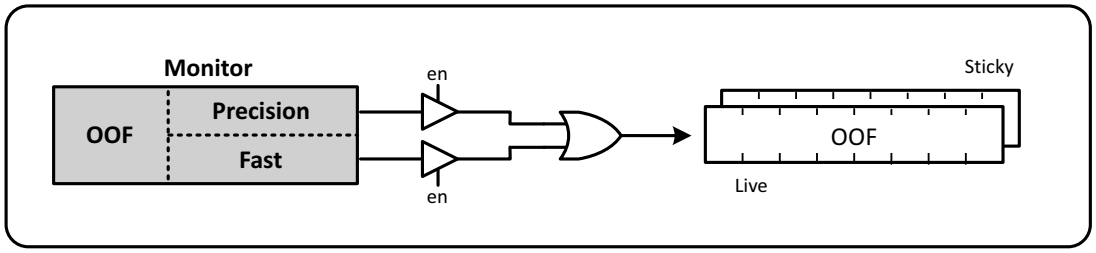


Figure 8. OOF Status Indicator

3.7.3.1. Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable up to 511 ppm in steps of 1/16 ppm. If the Xa input is chosen as the frequency reference, then the minimum OOF assert threshold should be 60 ppm or greater to account for the ±50 ppm error from the recommended XO at the Xa input. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±60 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 to IN3) as the 0 ppm OOF reference instead of the external XO reference is available. This option is register configurable.

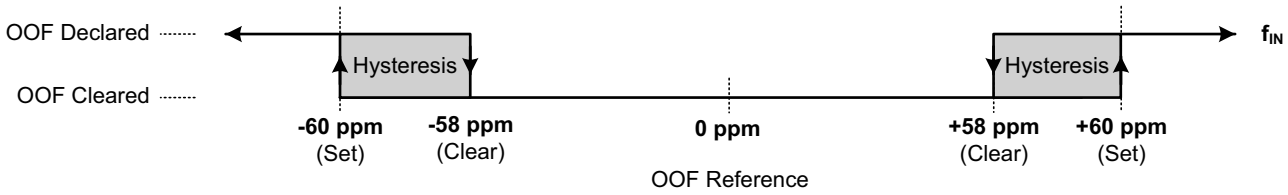


Figure 9. Example of Precise OOF Monitor Assertion and Deassertion Triggers

3.7.3.2. Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±1,000 ppm to ±16,000 ppm. This threshold can be configured in CBPro.

3.7.4. LOL Detection

The Loss Of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock.

There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

The LOL frequency monitors have an adjustable sensitivity which is register configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status.

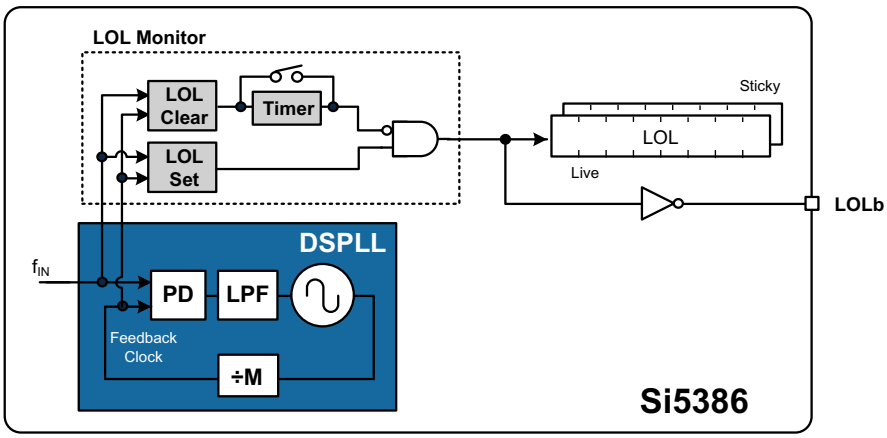


Figure 10. LOL Status Indicators

An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there is more than 1 ppm frequency difference is shown in the following figure.

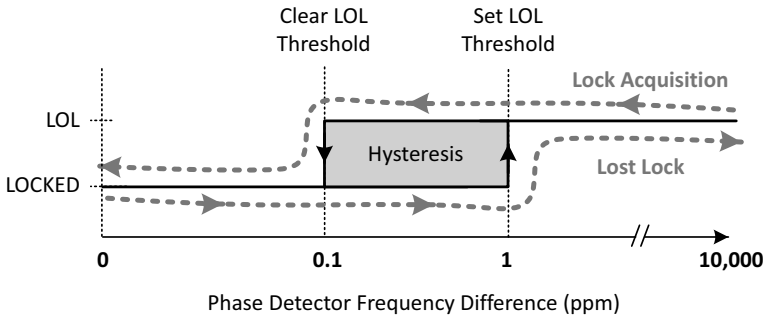


Figure 11. LOL Set and Clear Thresholds

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

3.7.5. Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state of the status indicators (LOS, OOF, LOL, HOLD). Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the status register that caused the interrupt.

3.8. Outputs

The Si5386 supports up to twelve differential output drivers. Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

3.8.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the MultiSynths as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

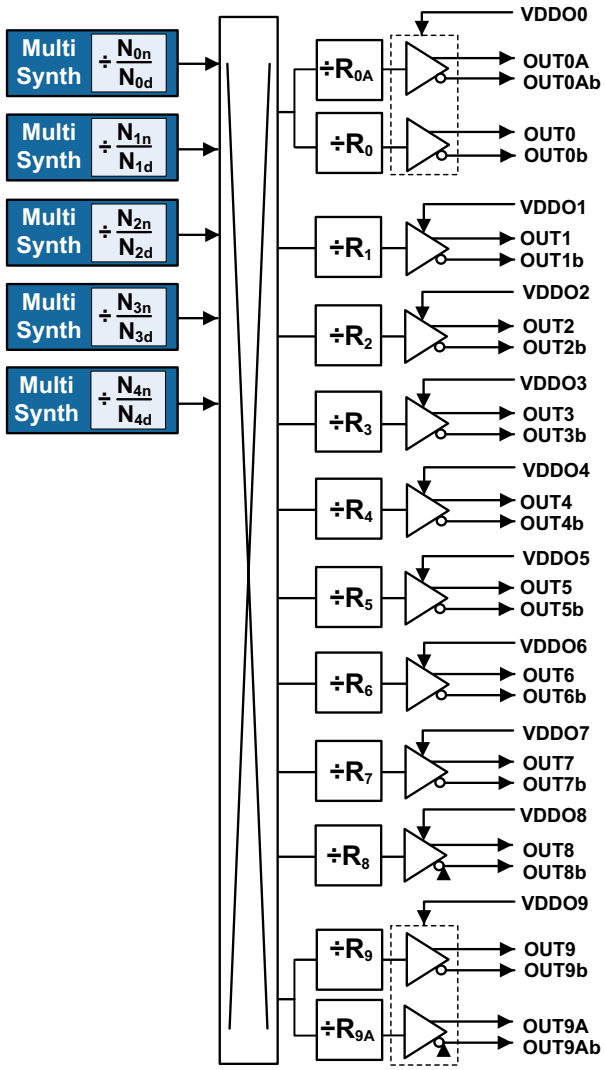


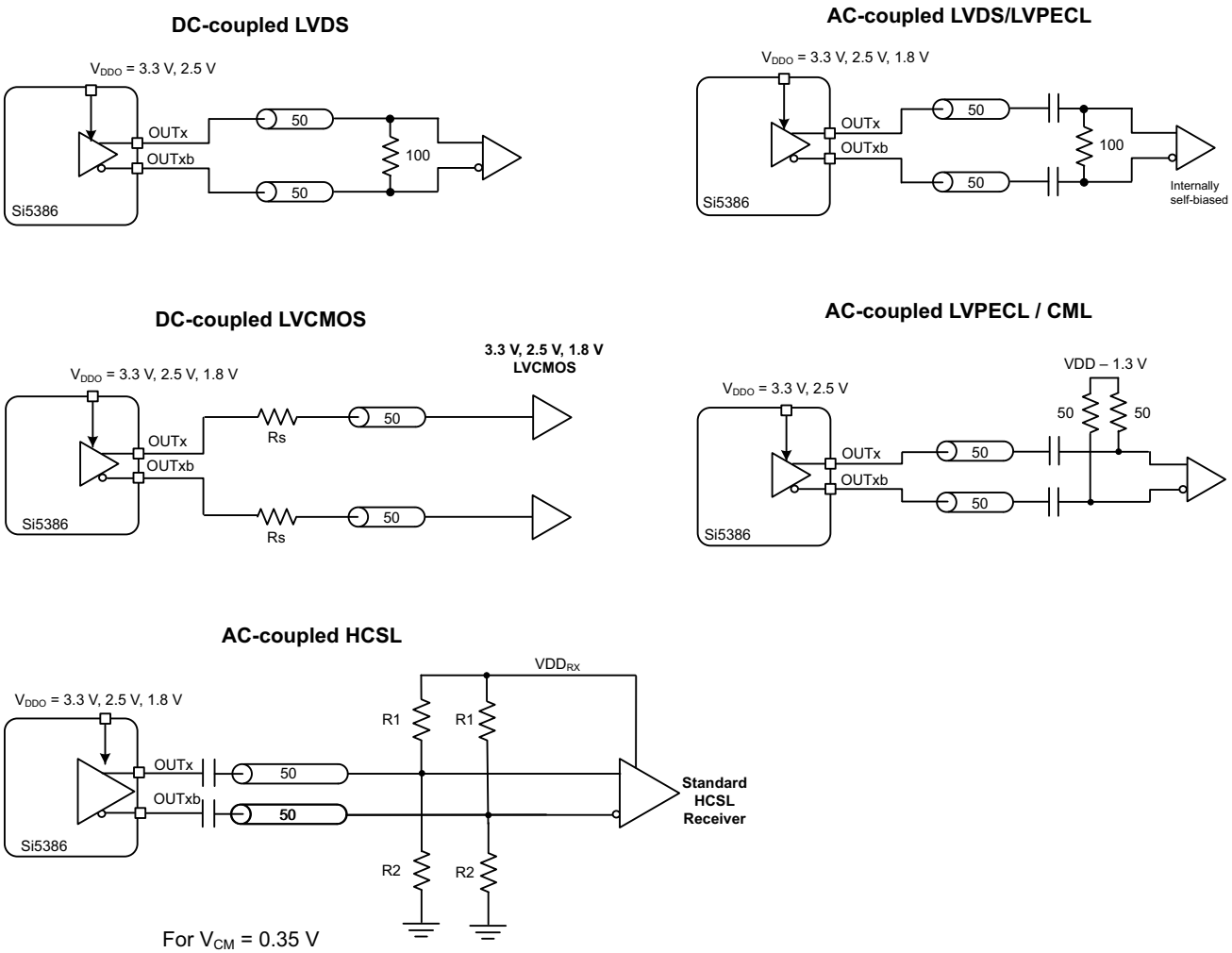
Figure 12. MultiSynth to Output Driver Crosspoint

3.8.2. Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

3.8.3. Output Terminations

The output drivers support both ac-coupled and dc-coupled terminations as shown in the following figure.



For V_{CM} = 0.35 V

VDD_{RX}	R1	R2
3.3 V	442 Ω	56.2 Ω
2.5 V	332 Ω	59 Ω
1.8 V	243 Ω	63.4 Ω

Figure 13. Supported Output Terminations

3.8.4. Programmable Amplitude For Differential Outputs

See the Si5386 Rev. E Reference Manual Appendix for programming the outputs to variable amplitudes when ac-coupled.

3.8.5. LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO options as shown in the table below.

Table 2. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03*	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03*	24 Ω	11 mA
1.8 V	0x03*	31 Ω	5 mA
Note: Use of the lowest impedance setting is recommended for all supply voltages for best edge rates.			

3.8.6. LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

3.8.7. LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTx pin is generated with the same polarity (in phase) as the clock on the OUTxb pin. The polarity of these clocks is configurable, enabling complementary clock generation or inverted polarity with respect to other output drivers.

3.8.8. Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling all of the output drivers at the same time. When the OEb pin is held high all outputs will be disabled. When held low, the outputs will all be enabled. Outputs in the enabled state can still be individually disabled through register control.

3.8.9. Output Disable During LOL

By default, a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL intoholdover.

3.8.10. Output Disable During Reference LOS

The external XA/XB reference provides a critical function for the operation of the DSPLLs. In the event of the XO failure, the device will assert an XAXB_LOS alarm. By default, all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability is indeterminate during this fault condition.

3.8.11. Output Driver State When Disabled

The disabled state of an output driver is configurable as disable low or disable high.

3.8.12. Synchronous Output Disable Feature

The output drivers provide a selectable synchronous disable feature. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

3.8.13. Static Output Skew Control

The static phase adjust will allow a programmable phase offset between outputs on different N dividers. The resolution of the static phase adjustment is 68 ps with up to ±1 ms of total range. This feature is intended for use in JESD204B subclass 1 applications to adjust the phase of SYSREF signals with respect to DCLK. See the family Reference Manual and Application Note AN1165: Configuring Si538x Devices for JESD204B/C Wireless Applications for more details.

3.8.14. Dynamic Output Skew Control

The dynamic phase adjust will allow the device to dynamically and glitchlessly change the outputs phase using register writes while the device remains locked. The resolution of the dynamic phase adjustment is 68 ps step size with up to ±1 ms of total range. See the family Reference Manual for more details.

3.8.15. Zero Delay Mode

Zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally around as shown in the figure below. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any output can be fed back to the IN3/FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9A and IN3/FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. The order of the OUT9A and FB_IN polarities is such that they may be routed on the device side of the PCB without requiring vias or needing to cross each other.

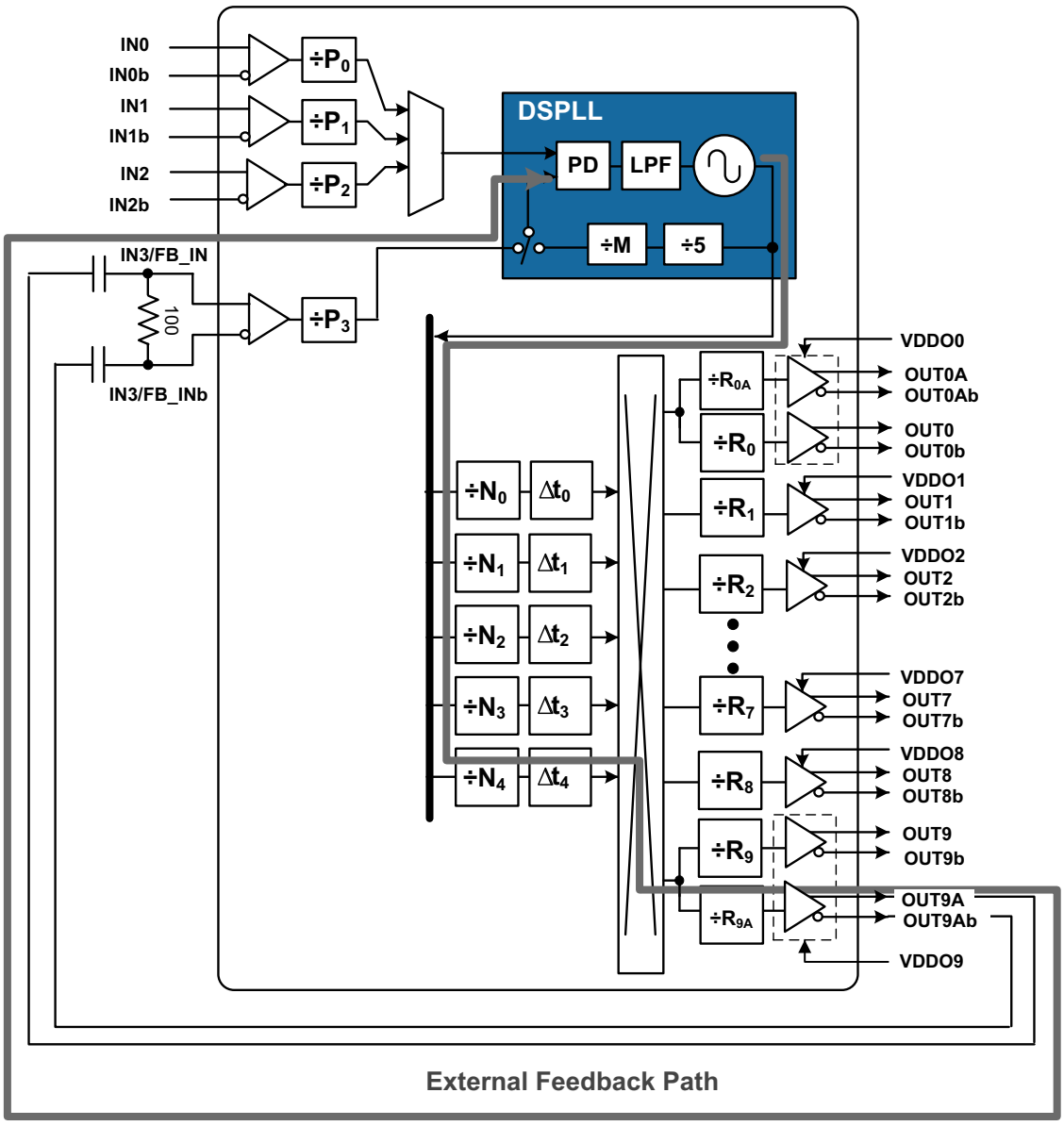


Figure 14. Si5386 Zero Delay Mode Setup

3.8.16. Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result.

3.9. Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Reference Manual and ClockBuilder Pro configuration utility for details.

3.10. In-Circuit Programming

The Si5386 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD and VDDA pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Reference Manual for a detailed procedure for writing registers to NVM.

3.11. Serial Interface

Configuration and operation of the Si5386 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either four-wire or three-wire. The SCLK in SPI mode does not need to be present when CSb is high. See the timing diagram for SPI and the Reference Manual for details.

3.12. Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory preprogrammed part will generate clocks at power-up. Custom, factory-programmed devices are available. The ClockBuilder Pro custom part number wizard can be used to quickly and easily generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Skyworks sales representative. Samples of your preprogrammed device will typically ship in about two weeks.

3.13. Enabling Features or Configuration Settings Unavailable in ClockBuilder Pro for Factory Preprogrammed Devices

As with essentially all modern software utilities, ClockBuilder Pro is continually updated and enhanced. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Reference Manual.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact a Skyworks applications engineer for assistance. One example of this type of feature or custom setting is the

customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and requirements, the Skyworks applications engineer will email back your CBPro project file with your specific features and register settings enabled using what is referred to as the manual settings override feature of CBPro. Override settings to match your request(s) will be listed in your design report file. Examples of setting overrides in a CBPro design report are shown in the following table.

Table 3. Setting Overrides

Location	Name	Type	Target	Dec Value	Hex Value
0x0435[0]	FORCE_HOLD_PLLA	No NVM	N/A	1	0x1
0x0B48[0:4]	OOF_DIV_CLK_DIS	User	OPN and EVB	0	0x00

Once you receive the updated design file, open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown below.

Note: Contact Skyworks Technical Support at https://www.skyworksinc.com/support-ia.

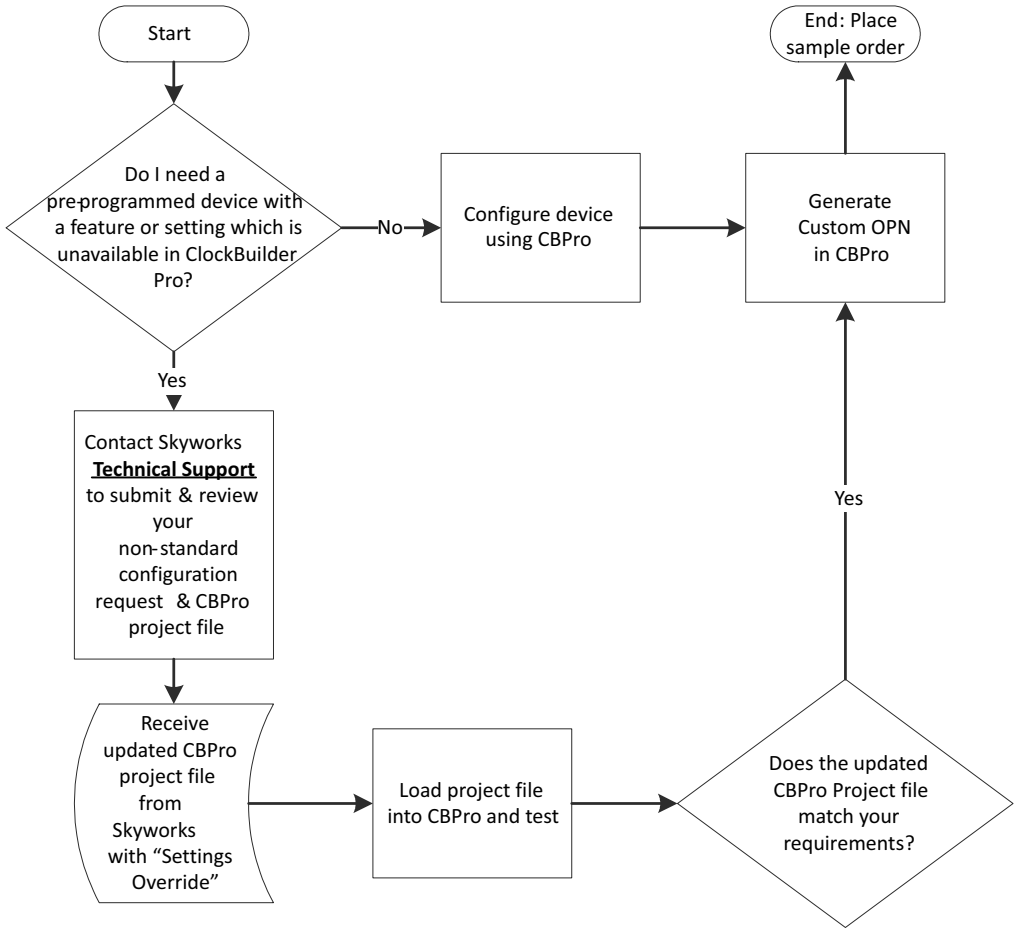


Figure 15. Process for Requesting Non-Standard CBPro Features

4. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in the High-Level Register Map. Refer to the Reference Manual for a complete list of register descriptions and settings. Skyworks strongly recommends using ClockBuilder Pro to create and manage register settings.

4.1. Addressing Scheme

The device registers are accessible using a 16-bit address that consists of an 8-bit page address plus an 8-bit register address. By default, the page address is set to 0x00. Changing to another page is accomplished by writing to the Set Page Address byte located at address 0x01 of each page.

4.2. High-Level Register Map

Table 4. High-Level Register Map

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
00	00	Revision IDs
	01	Set page address
	02 to 0A	Device IDs
	0B to 15	Alarm status
	17 to 1B	INTR masks
	1C	Reset controls
	1D	FINC, FDEC control bits
	2B	SPI (3-wire vs 4-wire)
	2C to E1	Alarm configuration
	E2 to E4	NVM controls
	FE	Device ready status
01	01	Set page address
	08 to 3A	Output driver controls
	41 to 42	Output driver disable masks
	FE	Device ready status
02	01	Set page address
	02 to 05	Reference clock frequency adjust
	08 to 2F	Input divider (P) settings
	30	Input divider (P) update bits
	47 to 6A	Output divider (R) settings
	6B to 72	User scratch pad memory
	FE	Device ready status

Table 4. High-Level Register Map (Continued)

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
03	01	Set page address
	02 to 37	MultiSynth divider (N0-N4) settings
	0C	MultiSynth divider (N0) update bit
	17	MultiSynth divider (N1) update bit
	22	MultiSynth divider (N2) update bit
	2D	MultiSynth divider (N3) update bit
	38	MultiSynth divider (N4) update bit
	39 to 58	FINC/FDEC settings N0-N4
	59 to 62	Output delay (Δt) settings
	FE	Device ready status
04	87	Zero delay mode set up
05	0E to 14	Fast lock loop bandwidth
	15 to 1F	Feedback divider (M) settings
	2A	Input select control
	2B	Fastlock control
	2C to 35	Holdover settings
	36	Input clock switching mode select
	38 to 39	Input priority settings
	3F	Holdover history valid data
06 to 08	00 to FF	Reserved
09	01	Set page address
	1C	Zero delay mode settings
	43	Control I/O voltage select
	49	Input settings
00-FF	00 to FF	Reserved

5. Electrical Specifications

Table 5. Recommended Operating Conditions[1]

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
Ambient temperature	T_A	–40	25	85	°C
Maximum junction temperature	TJ_{MAX}	—	—	125	°C
Core supply voltage	V_{DD}	1.71	1.80	1.89	V
	VDDA	3.14	3.30	3.47	
Output driver supply voltage	VDDO	3.14	3.30	3.47	V
		2.38	2.50	2.62	
		1.71	1.80	1.89	

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

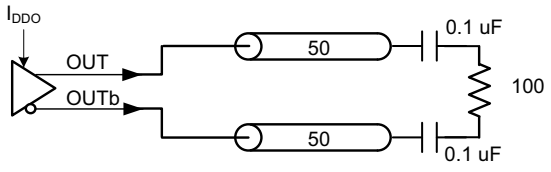
Table 6. DC Characteristics

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core supply current	I_{DD}	Notes[1,2]	—	210	375	mA
	I_{DDA}		—	125	140	mA
Output buffer supply current	I_{DDO}	LVPECL output[3] @ 156.25 MHz	—	22	26	mA
		LVDS output[3] @ 156.25 MHz	—	15	18	mA
		3.3 V LVCMOS[4] output @ 156.25 MHz	—	22	30	mA
		2.5 V LVCMOS[4] output @ 156.25 MHz	—	18	23	mA
		1.8 V LVCMOS[4] output @ 156.25 MHz	—	12	16	mA
Total power dissipation	P_d	Note [1,5]	—	1150	1520	mW

1. Si5386 test configuration: 10 clock outputs enabled (10 MHz and 30.72 MHz 3.3V CMOS complementary, 125 MHz LVDS 3.3 V, all other outputs are 1.8 V sub-LVDS, 3 x 122.88 MHz, 2 x 960 kHz, 1 x 49.152 MHz, 1 x 307.2 MHz). Excludes power in termination resistors.
2. VDDO0 supplies power to both OUT0 and OUT0A buffers. Similarly, VDDO9 supplies power to both OUT9 and OUT9A buffers.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 5-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs are set to OUTx_CMOS_DRV = 3, the strongest driver setting.
5. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration



LVCMOS Output Test Configuration

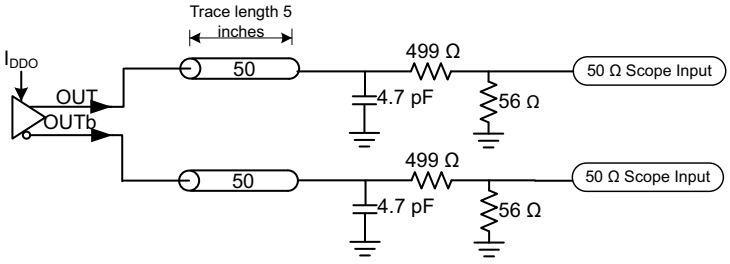


Table 7. Input Clock Specifications[1]

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Differential or Single-Ended: AC-coupled (IN0, IN1, IN2, IN3)						
Input frequency range	fIN_DIFF	Differential	0.08	—	750	MHz
	fIN_SE	Single-ended	0.08	—	250	
Input voltage amplitude	VIN_DIFF	fIN_DIFF < 250 MHz	100	—	1800	mVpp_se
		250 MHz < fIN_DIFF<750 MHz	225	—	1800	mVpp_se
Single-ended input amplitude	VIN_SE	fIN_SE< 250 MHz	100	—	3600	mVpp_se
Slew rate[2,3]	SR		400	—	—	V/µs
Duty cycle	DC		40	—	60	%
Capacitance	CIN		—	2.4	—	pF
LVCMOS/Pulsed CMOS DC-coupled Input Buffer (IN0, IN1, IN2, IN3/FB_IN)[4, 5]						
Input frequency	fIN_CMOS	Standard CMOS and non-standard CMOS	0.008	—	250	MHz
		Pulsed CMOS	0.008	—	1	MHz
Input voltage	VIL	Standard CMOS	—	—	0.5	V
		Non-standard CMOS and pulsed CMOS	—	—	0.4	V
	VIH	Standard CMOS	1.3	—	—	V
		Non-standard CMOS and pulsed CMOS	0.8	—	—	V
Slew rate[1,2]	SR		400	—	—	V/µs
Duty cycle	DC	Standard CMOS and non-standard CMOS	40	—	60	%
		Pulsed CMOS	5		95	
Minimum pulse width	PW	Standard CMOS and non-standard CMOS (250 MHz @ 40% Duty Cycle)	1.6	—	—	ns
		Pulsed CMOS (1 MHz @ 5% duty cycle)	50	—	—	

Table 7. Input Clock Specifications[1] (Continued)

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input resistance	RIN		—	8	—	kΩ
XO (Applied to XA/XB)[4]						
Frequency	fIN_REF		—	54	—	MHz
Total frequency tolerance[6]	fRANGE		–50	—	+50	ppm
Input voltage amplitude	VIN_SE	Single-ended input	365	—	2000	mVpp_se
	VIN_DIFF	Differential input	365	—	2500	mVpp_diff
Slew rate[2, 3]	SR		400	—	—	V/µs
Input duty cycle	DC		40	—	60	%
Activity dip[7]					2	ppm/°C

1. Voltage swing is specified as single-ended mVpp
2. Recommended for specified jitter performance. Slew rate can go lower, but jitter performance could degrade if the minimum slew rate specification is not met (see the Si5386 Reference Manual).
3. Slew rate can be estimated using the following simplified equation: SR = ((0.9 – 0.1) x $V_{IN\_VPP\_se}$)/$tr_{10\text{-}90}$.
4. Standard, non-standard and pulsed CMOS refer to different formats of CMOS each with a voltage swing of 1.8 V, 2.5 V or 3.3 V +/-5%.
   - Standard CMOS refers to the industry standard LVCMOS signal.
   - Non-standard CMOS refers to a signal that has been attenuated/level-shifted in order to comply with the specified non-standard VIL and VIH specifications.
   - Pulsed CMOS refers to a signal that has been attenuated/level-shifted and has a low/high duty cycle and must be dc coupled. A typical application example is a low-frequency video frame sync pulse. Refer to the Si5386 Reference Manual for the recommended connections/termination for the different modes.
5. CMOS signals that exceed 3.3 V + 5% can be used as inputs as long as a resistive attenuation network is used to guarantee that the input voltage at the pin does not violate the device input ratings. Refer to the Si5386 Reference Manual for the recommended connections/termination for this mode.
6. Includes aging and temperature affects.
7. Activity dip is also called frequency perturbation.

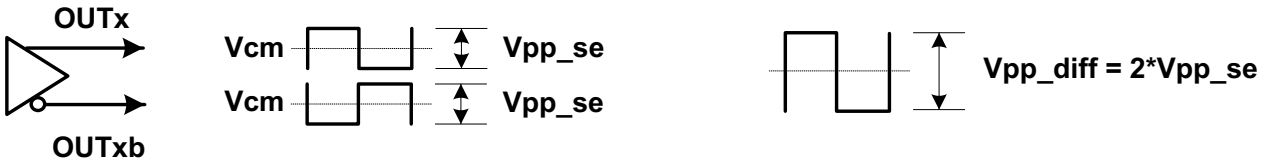


Table 8. Serial and Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial and Control Input Pins (IN_SEL[1:0], RSTb, OEb, PDNb, A1/SDO, SCLK, A0/CSb, SDA/SDIO)						
Input voltage thresholds	VIL		—	—	0.3 x VDDIO[1]	V
	VIH		0.7 x VDDIO[1]	—	—	V
Input capacitance	CIN		—	2	—	pF
Input resistance	IL		—	20	—	kΩ
Minimum pulse width	PW	RSTb, PDNb	100	—	—	ns

1. VDDIO is determined by the IO_VDD_SEL bit. It is selectable as VDDA or VDD. See the Si5386 Reference Manual for more details on the register settings.

Table 9. Differential Clock Output Specifications

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, TA = –40 to 85 °C)

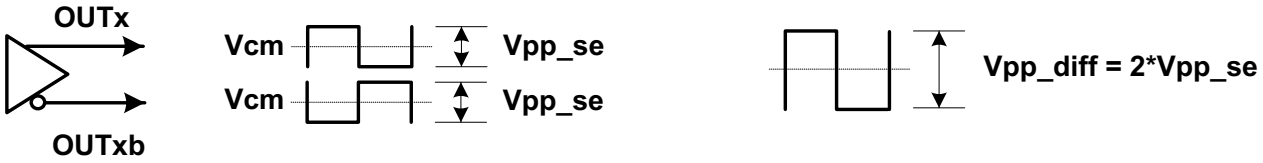
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output frequency[1]	f_{OUT}	N >= 10, R >= 2		0.0001	—	737.28	MHz
		N = 9, R = 2		—	819.2	—	
		N = 8, R = 2		—	921.6	—	
		N = 7.5, R = 2		—	983.04	—	
		N = 7, R = 2		—	14745.6/14	—	
		N = 6, R = 2		—	1228.8	—	
		N = 5, R = 2		—	1474.56	—	
		N = 9, R = 1		—	1638.4	—	
		N = 8, R = 1		—	1843.2	—	
		N = 7, R = 1		—	2106.53	—	
		N = 6, R = 1		—	2457.6	—	
		N = 5, R = 1		—	2949.12	—	
Duty cycle	DC	fOUT < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 800 MHz		45	—	55	
		800 MHz < fOUT < 1474.56 MHz		40	—	60	
		f > 1474.56 MHz		25	—	75	
Output-output skew[2]	T_{SK}	Differential output specified for outputs using the same MultiSynth		—	0	75	ps
		Differential output specified for outputs using different MultiSynths		-150	0	150	ps
Output dynamic/static delay adjustment	T_{delay_step}			—	68	—	ps
	T_{delay_range}			—	±1	—	ms
OUT-OUTb skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	50	ps
Output voltage amplitude[3]	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	450	530	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	610	780	950	
Common mode voltage[3,4]	VCM	V_{DDO} = 3.3 V	LVDS	1.1	1.2	1.3	V
			LVPECL	1.9	2.0	2.1	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.1	1.2	1.3	
		V_{DDO} = 1.8 V	sub-LVDS	0.8	0.9	1.0	
Rise and fall times (20% to 80%)	t_F	LVPECL and LVDS outputs		—	100	200	ps
Differential output impedance[4]	Z_0	LVPECL and LVDS outputs		—	100	—	Ω

Table 9. Differential Clock Output Specifications (Continued)

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power supply noise rejection[5]	PSRR	10 kHz sinusoidal noise	—	–101	—	dBc
		100 kHz sinusoidal noise	—	–96	—	
		500 kHz sinusoidal noise	—	–99	—	
		1 MHz sinusoidal noise	—	–97	—	
Output-output crosstalk[6]	XTALK	Differential	—	–72	—	dB

1. VDDO = 2.5 V or 3.3 V required for fOUT > 1474.56 MHz
2. For any R divider settings that differ by a power of 2.
3. Output amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical normal mode (or low power mode) LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. Refer to the Si5386 Reference Manual for recommended output settings.
4. Not all combinations of voltage amplitude and common-mode voltage settings are possible.
5. Measured for 156.25 MHz carrier frequency. Sine wave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.
6. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 122.88 MHz and the aggressor at 156.25 MHz. Refer to application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems", guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.



Differential Output Test Configuration

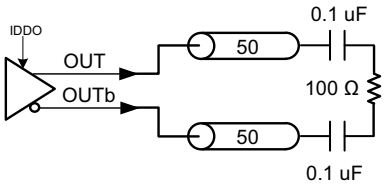


Table 10. LVCMOS Clock Output Specifications

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output frequency	f_{OUT}			0.0001	—	250	MHz
Duty cycle	DC	fOUT <100 MHz		48	—	52	%
		100 MHz < fOUT < 250 MHz		44	—	56	
Output voltage high[1, 2, 3]	V_{OH}	**VDDO = 3.3 V**					
		OUTx_CMOS_DRV=1	IOH = –10 mA	VDDO x 0.85	—	—	V
		OUTx_CMOS_DRV=2	IOH = –12 mA		—	—	
		OUTx_CMOS_DRV=3	IOH = –17 mA		—	—	
		VDDO = 2.5 V					
		OUTx_CMOS_DRV=1	IOH = –6 mA	VDDO x 0.85	—	—	V
		OUTx_CMOS_DRV=2	IOH = –8 mA		—	—	
		OUTx_CMOS_DRV=3	IOH = –11 mA		—	—	
		VDDO = 1.8 V					
		OUTx_CMOS_DRV=2	IOH = –4 mA	VDDO x 0.85	—	—	V
		OUTx_CMOS_DRV=3	IOH = –5 mA		—	—	
Output voltage low[1, 2, 3]	V_{OL}	**VDDO = 3.3 V**					
		OUTx_CMOS_DRV=1	IOL = 10 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=2	IOL = 12 mA	—	—		
		OUTx_CMOS_DRV=3	IOL = 17 mA	—	—		
		VDDO = 2.5 V					
		OUTx_CMOS_DRV=1	IOL = 6 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=2	IOL = 8 mA	—	—		
		OUTx_CMOS_DRV=3	IOL = 11 mA	—	—		
		VDDO = 1.8 V					
		OUTx_CMOS_DRV=2	IOL = 4 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=3	IOL = 5 mA	—	—		

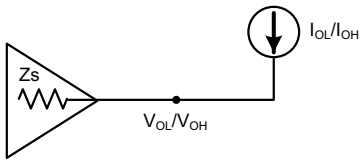
Table 10. LVCMOS Clock Output Specifications (Continued)

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVCMOS rise and fall times[3] (20% to 80%)	tr/tf	VDDO = 3.3 V	—	400	600	ps
		VDDO = 2.5 V	—	450	600	
		VDDO = 1.8 V	—	550	750	

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5386 Reference Manual for more details on register settings.
2. IOL/IOH is measured at VOL/VOH as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 4.7 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, at 156.25 MHz.

DC Test Configuration



AC Output Test Configuration

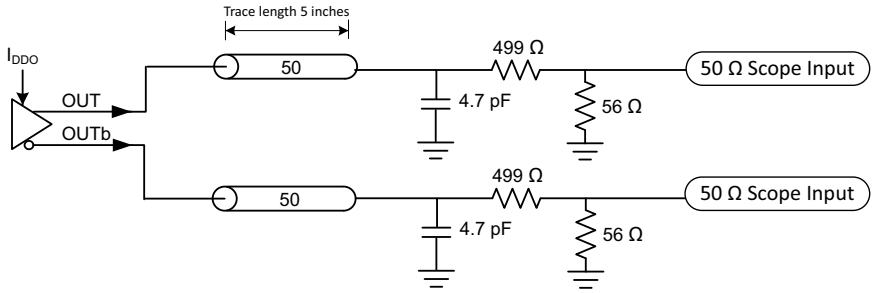


Table 11. Output Serial and Status Pin Specifications

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, VDDS = 3.3 V ±5%, 1.8 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial and Status Output Pins (INTRb, LOLb, SDA/SDIO[1], A1/SDO)						
Output Voltage	VOH	IOH = –2 mA	VDDIO[2] x 0.85	—	—	V
	VOL	IOL = 2 mA	—	—	VDDIO[2] x 0.15	V

1. The VOH specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I2C mode or is unused with I2C_SEL pulled high internally. VOL remains valid in all cases.
2. VDDIO is determined by the IO_VDD_SEL bit. It is selectable as VDDA or VDD. Users normally select this option in the ClockBuilder Pro GUI. Alternatively, refer to the Si5386 Reference Manual for more details on register settings.

Table 12. Performance Characteristics

(VDD = 1.8 V ±5%, or 3.3 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL loop bandwidth programming range	f_{BW}		20	—	4000	Hz
Initial start-up time	t_{START}	Time from power-up or deassertion of PDNb to when the device generates free-running clocks	—	370	625	ms
PLL lock time	t_{ACQ}	Fastlock enabled, fIN = 19.44 MHz[1]	—	280	300	ms
POR to serial interface ready[2]	t_{RDY}		—	15	—	ms
Jitter peaking	J_{PK}	25 MHz input, 25 MHz output, loop bandwidth of 4 Hz	—	—	0.1	dB
Jitter tolerance	J_{TOL}	Compliant with G.8262 options 1 and 2 for 1G, 10G or 25G synchronous Ethernet jitter modulation frequency = 10 Hz	—	3180	—	UI pk-pk
Input-to-output delay variation[3]	$t_{IODELAY}$	Non ZDM mode, device only	—	—	0.7	ns pp
		Non ZDM mode, device and XO[5,6]	—	—	1.2	
Input to output delay[3]	$t_{IODELAYZ}$	ZDM mode, device only[4]	–275	0	275	ps
		ZDM mode, device and XO[4,5]	–500	0	500	
XO frequency rate of change	dFdT_XO	See Note[6]	–6		6	ppm/min
Maximum phase transient	t_{SWITCH}	Single manual or automatic switch between two 2 MHz inputs, DSPLL BW = 400 Hz	—	—	0.3	ns
Pull-in range	ωP		—	20	—	ppm
RMS jitter generation3	J_{GEN}	12 kHz to 20 MHz	—	72	—	fs RMS
Phase noise performance[3] (122.88 MHz carrier frequency)	PN	100 Hz	—	–118	—	dBc/Hz
		1 kHz	—	–133	—	
		10 kHz	—	–142	—	
		100 kHz	—	–149	—	
		1 MHz	—	–154	—	
		10 MHz	—	–165	—	
MultiSynth spur performance	SPUR	From 1 MHz to 30 MHz offset	—	–95	—	dBc

1. Lock time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal bandwidth set to 100 Hz, Fastlock bandwidth set to 1 kHz, LOL set/clear thresholds of 6/0.6 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator deassertion.
2. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
3. Jitter generation test conditions: fIN = fOUT = 122.88 MHz, DSPLL LBW = 20 Hz. Jitter integrated from 12 kHz to 20 MHz offset. Does not include jitter from PLL input reference.
4. OLPD gain = 32x, Fzero = 32x, Fpfd >= 80 kHz, Fin >= 80 kHz, PLL bandwidth >= 15 Hz, integer P dividers.
5. Measured between the INx pin (clock input) and IN3 (feedback input) pin.
6. XO limits for meeting the IO delay specs. Includes XO stability over temperature and activity dips and any other effects. The XO maximum rate of change of frequency per °C is computed by dividing 6 ppm/minute by the temperature sweep rate in °C/minute. For example, if the temperature sweep rate is 1 °C/minute then the XO maximum frequency rate of change per °C is 6 ppm/°C. Temperature may be sweeping up or down.

Table 13. I²C Timing Specifications (SCL, SDA)

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		—	100	—	400	kHz
SMBus timeout	—	When timeout is enabled	25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data set-up time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of Both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

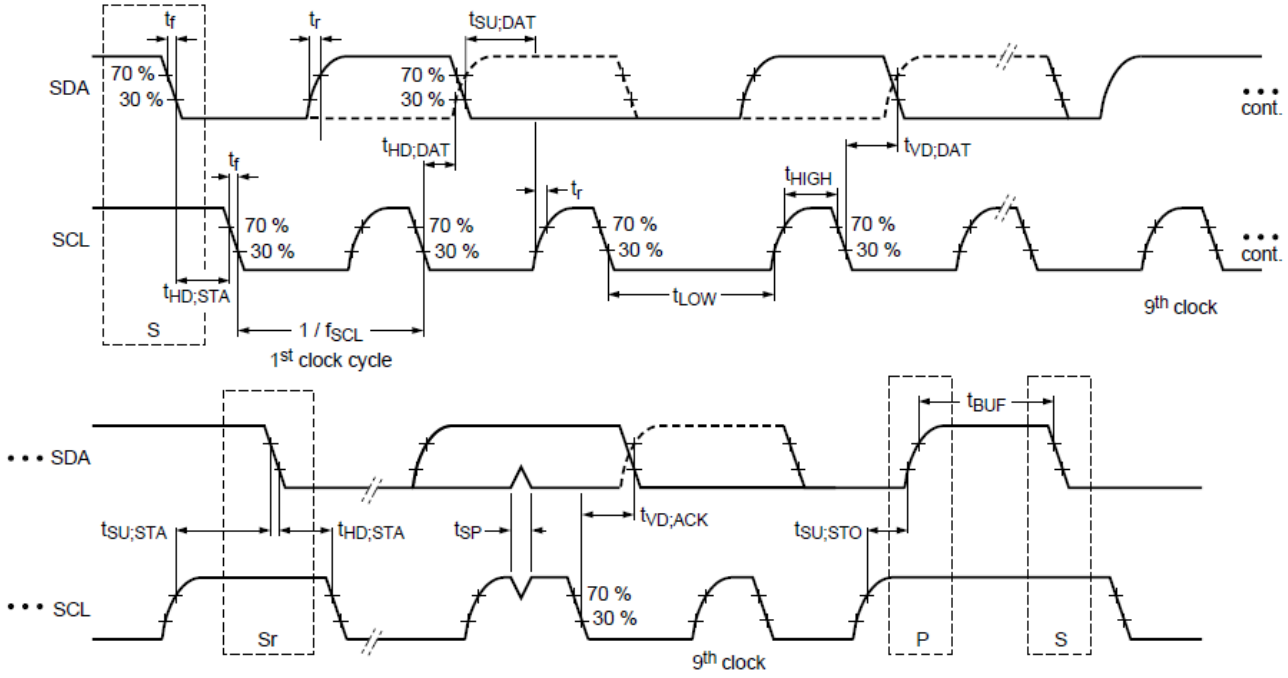


Figure 16. I²C Serial Port Timing Standard and Fast Modes

Table 14. SPI Timing Specifications (4-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	20	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	50	—	—	ns
Delay time, SCLK fall to SDO active	T_{D1}	—	12.5	18	ns
Delay time, SCLK fall to SDO	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDO Tri- state	T_{D3}	—	10	15	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	95	—	—	ns

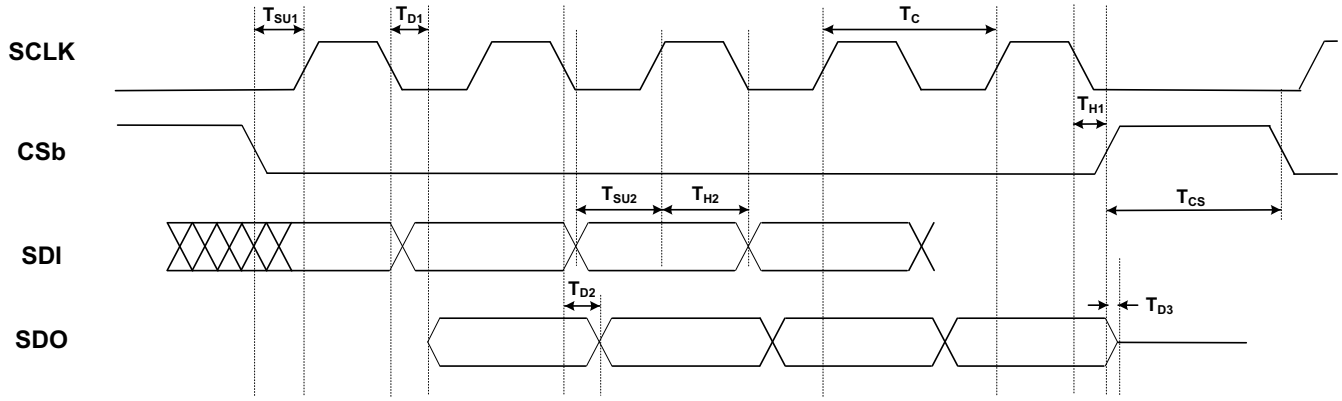


Figure 17. 4-Wire SPI Serial Interface Timing

Table 15. SPI Timing Specifications (3-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	20	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	50	—	—	ns
Delay time, SCLK fall to SDIO turn-on	T_{D1}	—	12.5	18	ns
Delay time, SCLK fall to SDIO next-bit	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDIO tri-State	T_{D3}	—	10	15	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	95	—	—	ns

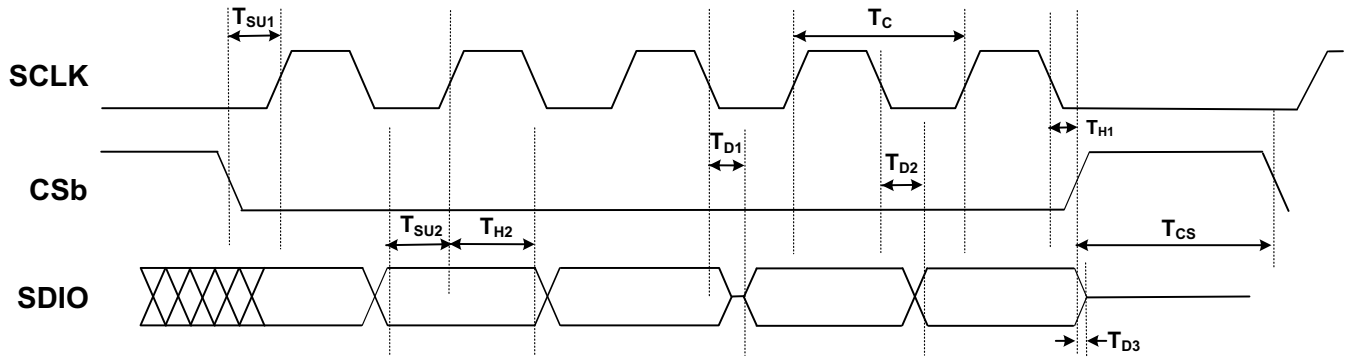


Figure 18. 3-Wire SPI Serial Interface Timing

Table 16. Thermal Characteristics (QFN-64)

Parameter	Symbol	Test Condition[1]	Value	Unit
Thermal resistance junction to ambient	Θ_{JA}	Still air	22	°C/W
		Air flow 1 m/s	19.4	
		Air flow 2 m/s	18.3	
Thermal resistance junction to case	Θ_{JC}		9.5	
Thermal resistance junction to board	Θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal resistance junction to top center	Ψ_{JT}		0.2	

1. Based on PCB dimension: 3” x 4.5”, PCB thickness: 1.6 mm, PCB land/via under GNP pad: 36, number of Cu layers: 4

Table 17. Absolute Maximum[1, 2, 3]

Parameter	Symbol	Test Condition	Value	Unit
DC supply voltage	VDD		–0.5 to 3.8	V
	VDDA		–0.5 to 3.8	V
	VDDO		–0.5 to 3.8	V
Input voltage range	VI1	IN0 – IN3	–1.0 to 3.8	V
	VI2	IN_SEL[1:0], RSTb, PDNb, OEb, I2C_SEL, SYNC SDA/SDIO, A1/SDO, SCLK, A0/ CSb	–0.5 to 3.8	V
	VI3	XA/XB	–0.5 to 2.7	V
Latch-up tolerance	LU		JESD78 compliant	
ESD tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Maximum junction temperature in opera- tion	T_{JCT}		125	°C
Storage temperature range	T_{STG}		–55 to +150	°C
Soldering temperature (Pb-free profile)	T_{PEAK}		260	°C
Soldering temperature time at TPEAK(Pb- free profile)	T_P		20 to 40	sec

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For detailed MSL and packaging information, go to https://www.skyworksinc.com/support-ia
3. The device is compliant with JEDEC J-STD-020.

ESD Handling: *Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

6. Detailed Block Diagrams

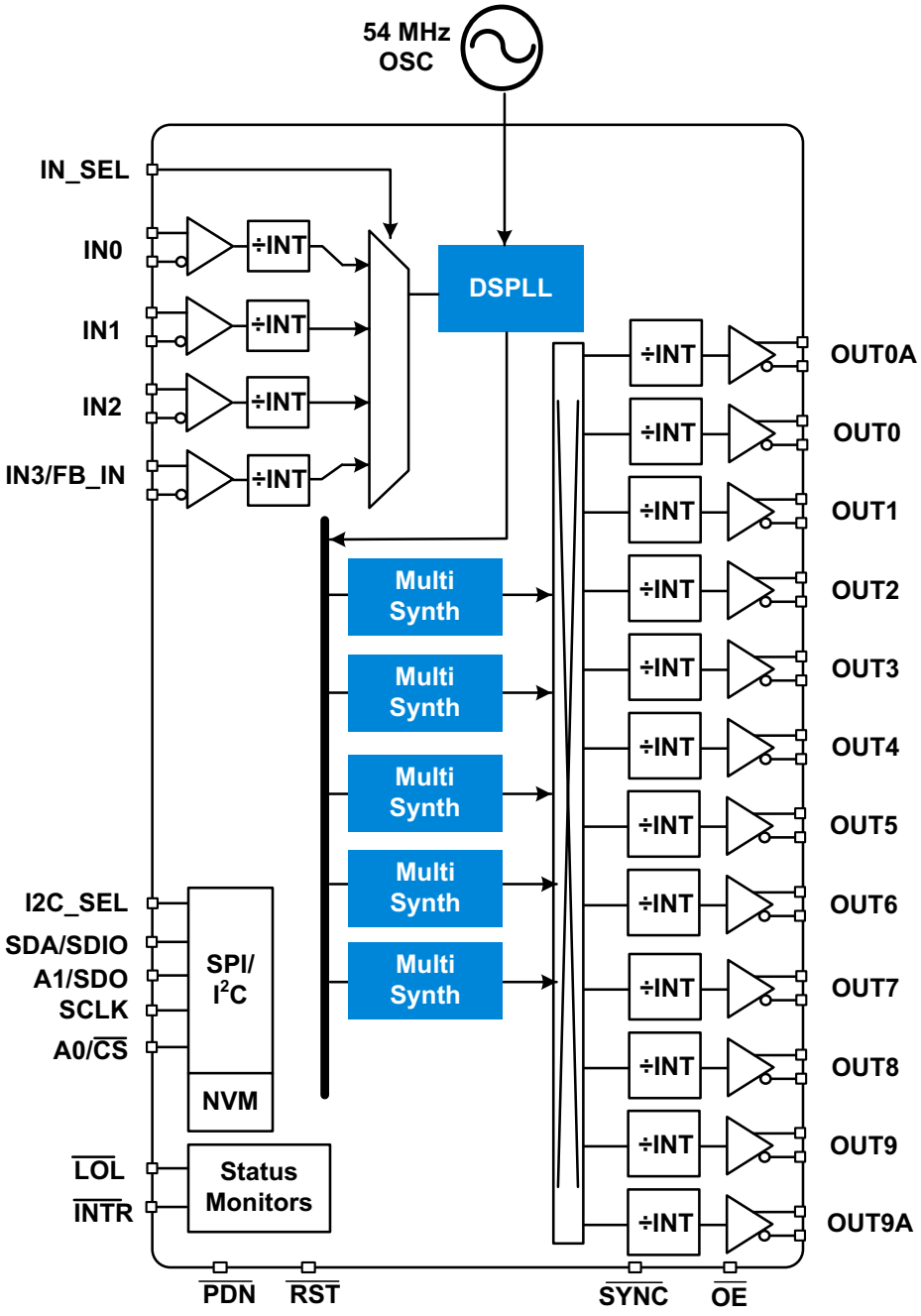


Figure 19. Block Diagram

7. Typical Operating Characteristics

The phase noise plots below were taken under the following conditions: V_{DD} = 1.8 V; V_{DDA} = 3.3 V; V_{DDS} = 3.3 V, 1.8 V; OLBW = 40Hz; T_a = 25 °C.

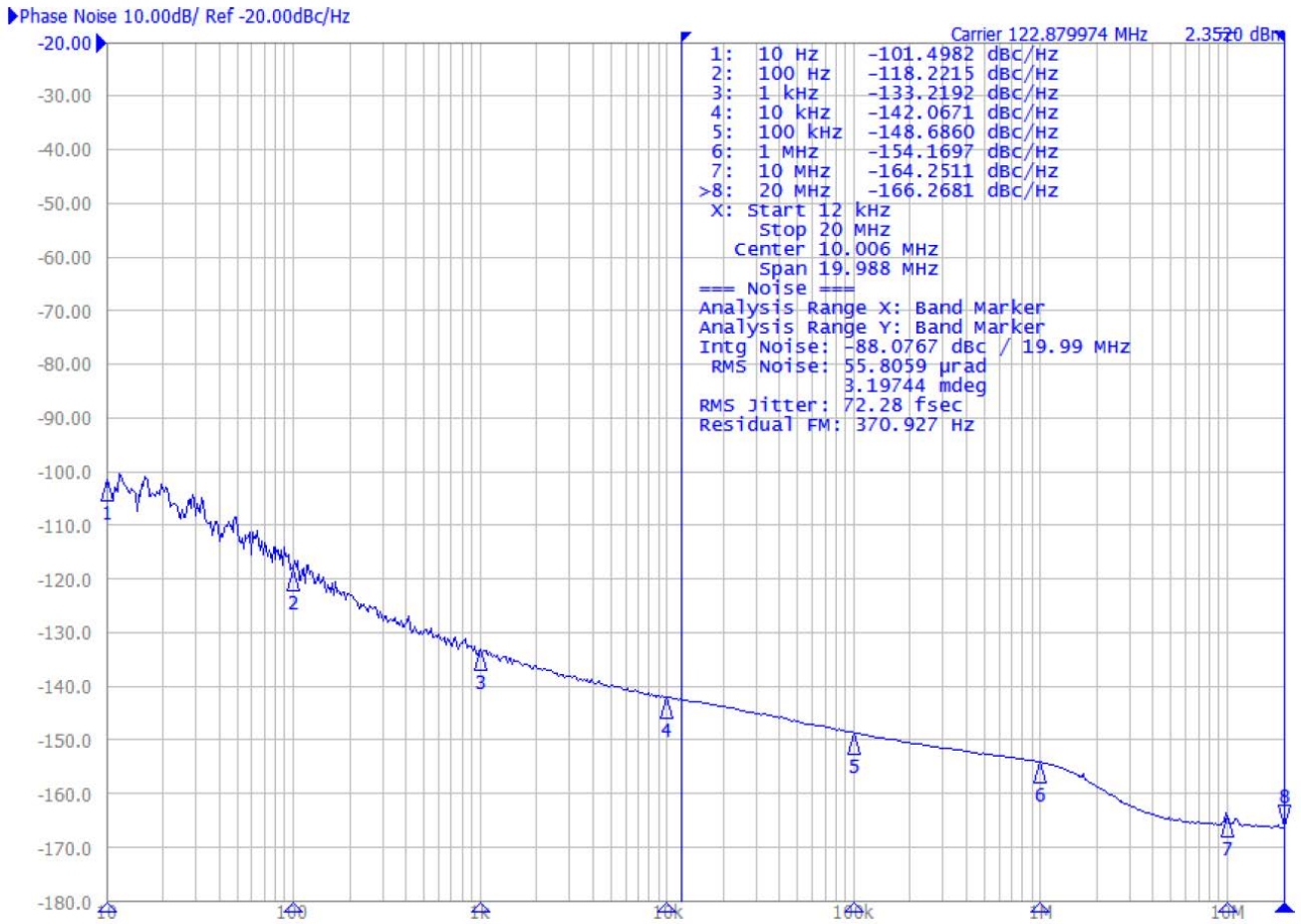


Figure 20. f_{IN} = 156.25 MHz, f_{OUT} = 122.88 MHz

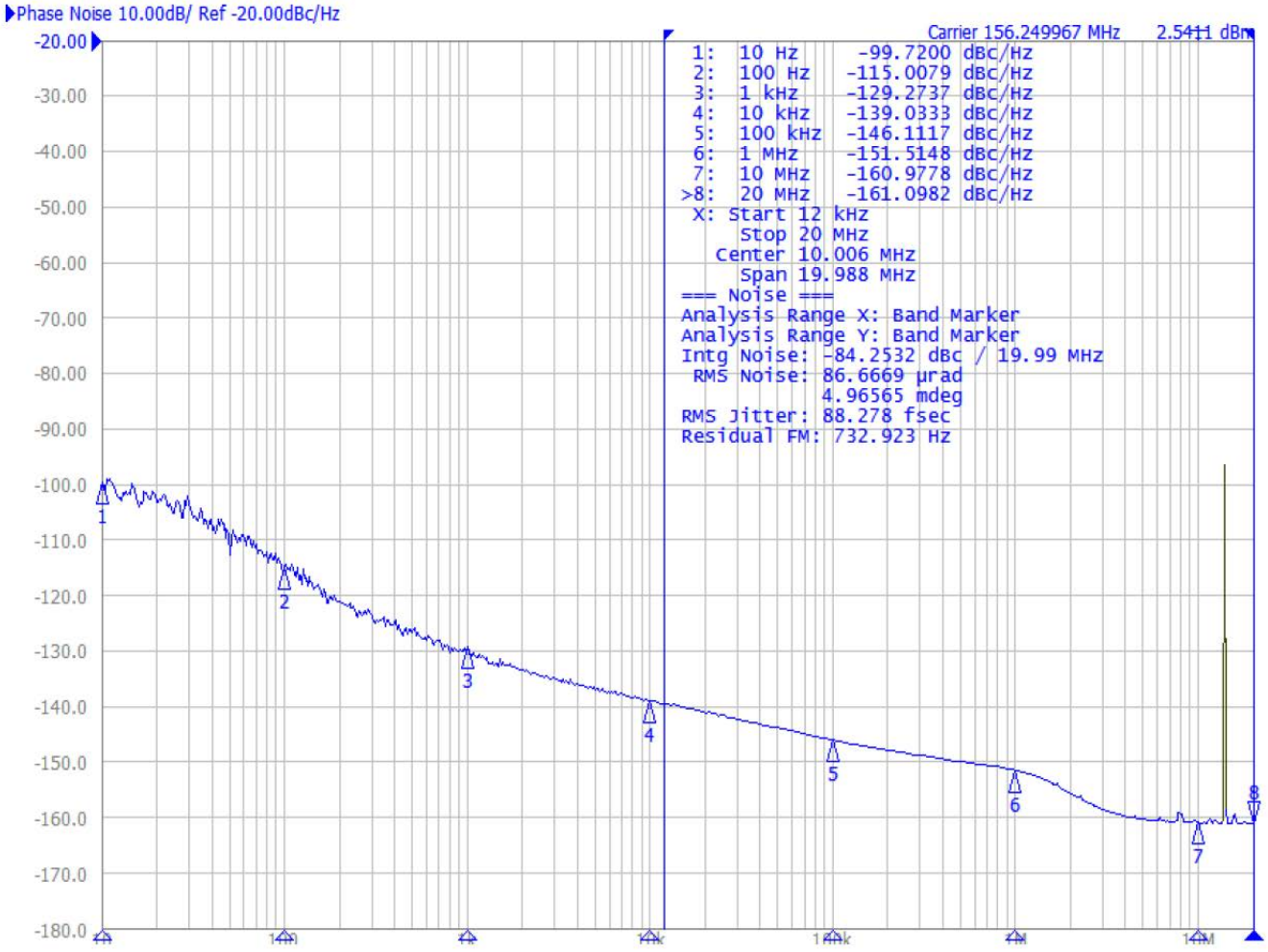


Figure 21. f_{IN} = 156.25 MHz, f_{OUT} = 156.25 MHz

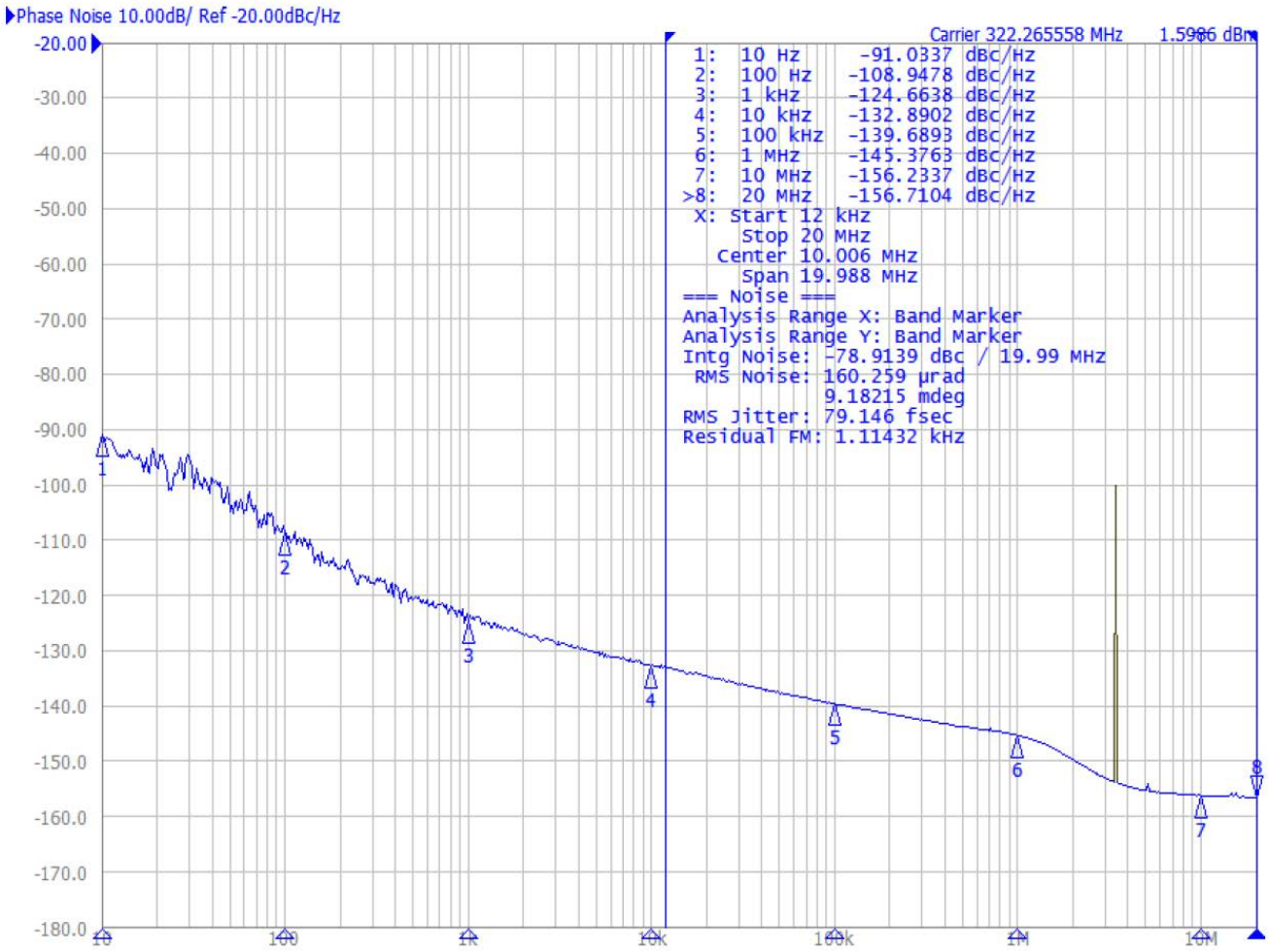


Figure 22. f_{IN} = 322.265625 MHz, f_{OUT} = 322.265625 MHz

8. Pin Descriptions

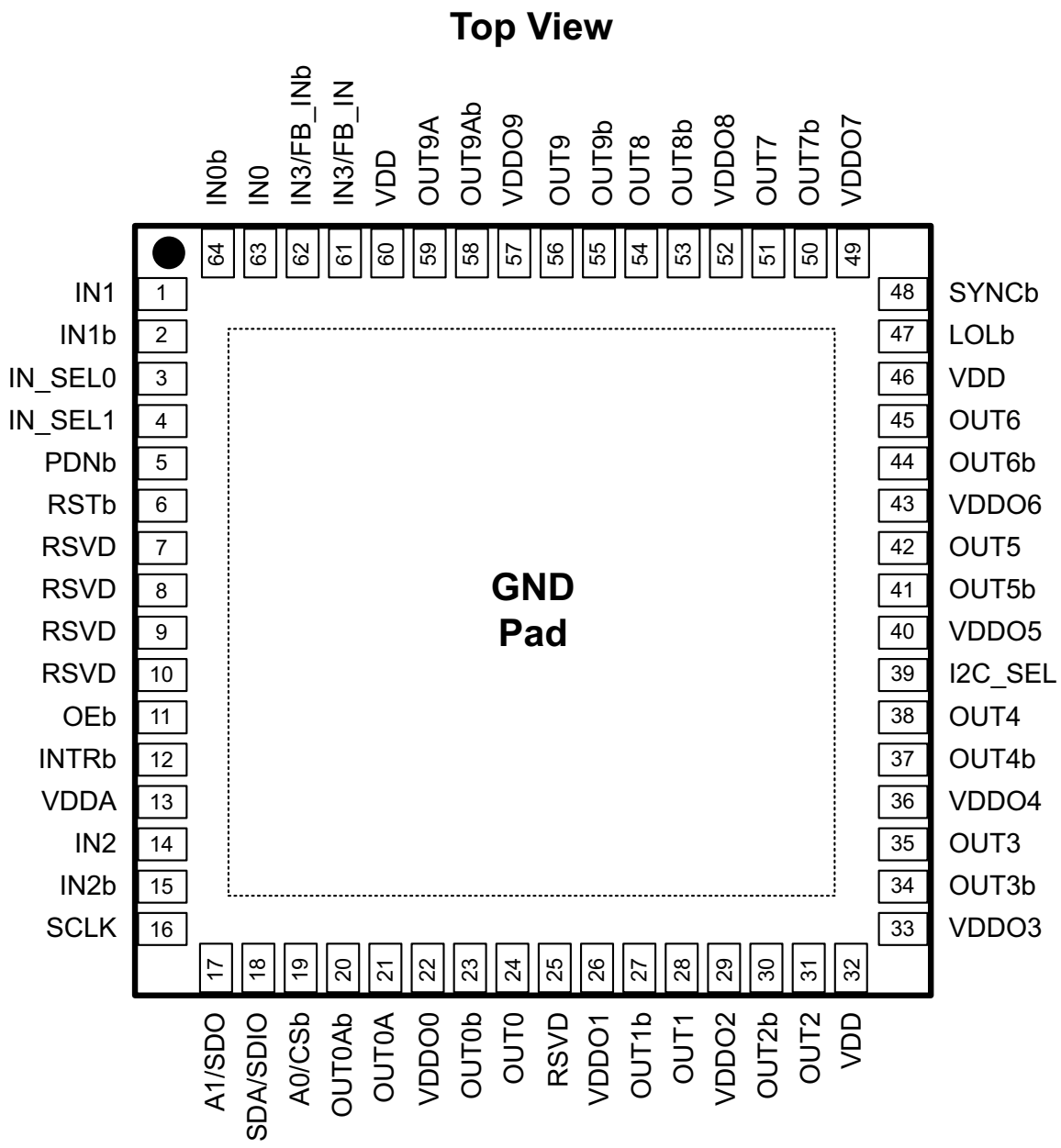


Figure 23. Pinout Top View

Table 18. Si5386 Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
Inputs			
IN0	63	I	**Clock inputs.** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. See "3.6. Inputs (IN0, IN1, IN2, IN3)" on page 9 for input termination options. These pins are high-impedance and must be terminated externally when being used. The negative side of the differential input must be ac-grounded when accepting a single-ended clock. Unused inputs may be left unconnected.
IN0b	64	I	
IN1	1	I	
IN1b	2	I	
IN2	14	I	
IN2b	15	I	
IN3/FB_IN	61	I	**Clock input 3/external feedback input.** By default, these pins are used as the 4th clock input (IN3/ IN3). They can also be used as the external feedback input (FB_IN/FB_IN) for the optional zero delay mode. See "3.6.1. Manual Input Switching (IN0, IN1, IN2, IN3)" on page 9 for details on the optional zero delay mode.
IN3/FB_INb	62	I	
Outputs			
OUT0A	21	O	**Output clocks.** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in "3.8.3. Output Terminations" on page 15 and "3.8.5. LVCMOS Output Impedance and Drive Strength Selection" on page 16. Unused outputs should be left unconnected.
OUT0Ab	20	O	
OUT0	24	O	
OUT0b	23	O	
OUT1	28	O	
OUT1b	27	O	
OUT2	31	O	
OUT2b	30	O	
OUT3	35	O	
OUT3b	34	O	
OUT4	38	O	
OUT4b	37	O	
OUT5	42	O	
OUT5b	41	O	
OUT6	45	O	
OUT6b	44	O	
OUT7	51	O	
OUT7b	50	O	
OUT8	54	O	
OUT8b	53	O	

Table 18. Si5386 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
OUT9	56	O	**Output clocks.** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in section "3.8.3. Output Terminations" on page 15 and "3.8.5. LVCMOS Output Impedance and Drive Strength Selection" on page 16. Unused outputs should be left unconnected.
OUT9b	55	O	
OUT9A	59	O	
OUT9Ab	58	O	
Serial Interface			
I2C_SEL	39	I	**I²C select.** This pin selects the serial interface mode as I²C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high.
SDA/SDIO	18	I/O	**Serial data interface.** This is the bidirectional data pin (SDA) for the I²C mode, the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I²C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.
A1/SDO	17	I/O	**Address select 1/serial data output.** In I²C mode this pin functions as the A1 address input pin. In 4-wire SPI mode, this is the serial data output (SDO) pin. This pin is 3.3 V tolerant.
SCLK	16	I	**Serial clock input.** This pin functions as the serial clock input for both I²C and SPI modes. When in I²C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.
A0/CSb	19	I	**Address select 0/chip select.** This pin functions as the hardware controlled address A0 in I²C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up. This pin is 3.3 V tolerant.
Control/Status			
INTRb	12	O	**Interrupt[2]** This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use. This pin has a push-pull driver and does not need a pull- up resistor.
PDNb	5	I	**Power down[2]** The device en- ters into a low power mode when this pin is pulled low. This pin is internally pulled-up. This pin is 3.3 V tolerant. It can be left unconnected when not in use.
RSTb	6	I	**Device Reset[2]** Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during re- set. This pin is internally pulled- up. This pin is 3.3 V tolerant.
OEb	11	I	**Output enable[2]** This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. This pin is 3.3 V tolerant.
LOLb	47	O	**Loss of lock[2]** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use.
SYNC	48	I	**Output clock synchronization[2]** An active low signal on this pin resets the output dividers for the purpose of re-aligning the output clocks. This pin is internally pulled-up and can be left unconnected when not in use.
IN_SEL0	3	I	**Input Reference Select[2].** The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in Table 1 on page 9.
IN_SEL1	4	I	
XA	8	I	**Oscillator input.** Single-ended input must be connected to the XA pin, with the XB pin appropriately terminated.
XB	9	I	
RSVD	7	NC	**Reserved.** Leave disconnected.
	10	NC	
	25	NC	

Table 18. Si5386 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
Power			
VDD	32	P	**Core supply voltage.** The device operates from a 1.8 V supply. A 1 uF bypass capacitor should be placed very close to each pin.
VDD	46	P	
VDD	60	P	
VDDA	13	P	**Core supply voltage, 3.3 V.** This core supply pin requires a 3.3 V power source. A 1 uF bypass capacitor should be placed very close to this pin.
VDDO0	22	P	**Output clock supply voltage.** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTn outputs. Note that VDDO0 supplies power to OUT0 and OUT0A; VDDO9 supplies power to OUT9 and OUT9A. Leave VDDO pins of unused output drivers unconnected. An alternative is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	26	P	
VDDO2	29	P	
VDDO3	33	P	
VDDO4	36	P	
VDDO5	40	P	
VDDO6	43	P	
VDDO7	49	P	
VDDO8	52	P	
VDDO9	57	P	
GND PAD		P	**Ground pad.** This pad provides connection to ground and must be connected for proper opera- tion.

1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.

9. Package Outlines

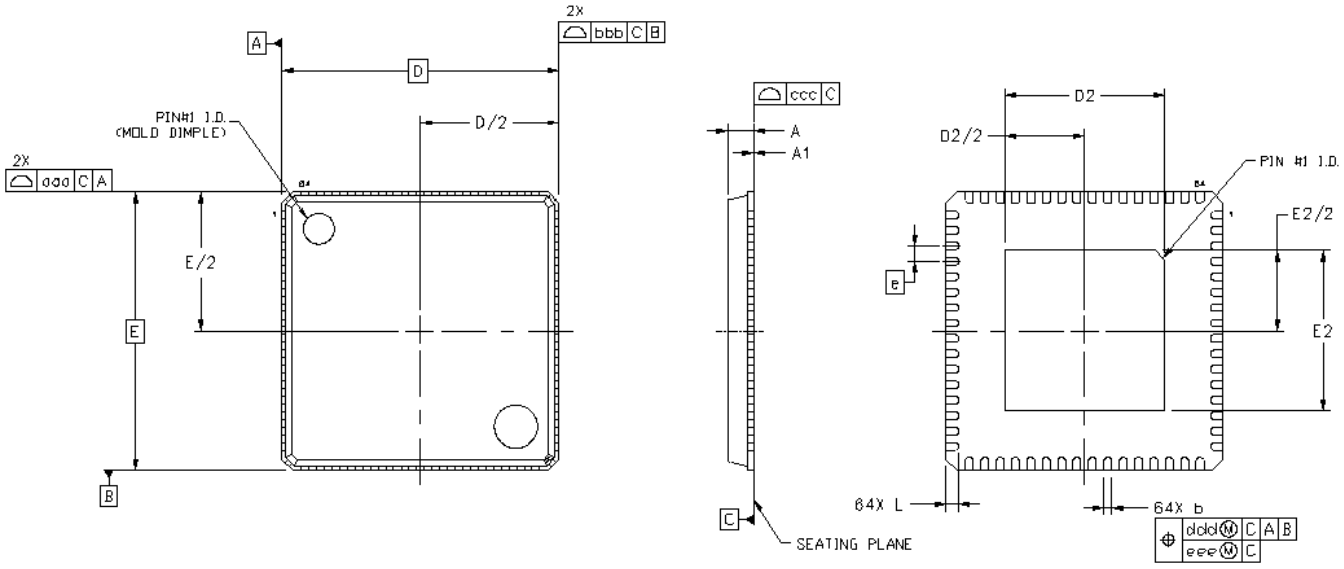


Figure 24. 9 x 9 mm 64-QFN Package Diagram

Table 19. Package Diagram Dimensions[1, 2, 3, 4]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerance per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

10. PCB Land Pattern

The following figure illustrates the PCB land pattern details for the devices. The table lists the values for the dimensions shown in the illustration.

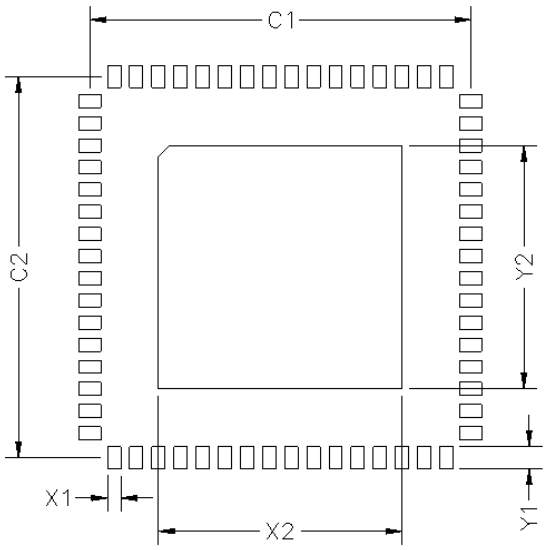


Figure 25. PCB Land Pattern

Table 20. PCB Land Pattern Dimensions

Dimension	Si5386 (Max)
C1	8.6
C2	8.6
E	0.50
X1	0.30
Y1	0.50
X2	5.5
Y2	5.5

Notes
General
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.65mm square openings on a 0.90mm pitch should be used for the center ground pad.

Card Assembly
1. A no-clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

11. Top Marking

Figure 26. Top Marking

Line	Characters	Description
1	Si538fg-	Base part number and Device Grade for Any-frequency, Any-output, Jitter Cleaning Clock (single PLL): f = 6, 12-Output LTE + Ethernet Clock g = Grade (internal versus external crystal oscillator option)
2	Rxxxxx-GM	R = Product revision. (Refer to 2. Ordering Guide for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code as- signed for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See Section 2. Ordering Guide for more information. -GM = Package (LGA) and temperature range (–40 to +85 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/1.6 mm (64-QFN) diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; center-justified TW = Taiwan; country of origin (ISO abbreviation)

12. Device Errata

See https://www.skyworksinc.com/support-ia to access the device errata document.

13. Revision History

Revision	Date	Description
A	June 2025	Revised to comply with Skyworks standards. Added specifications for input-output delay and minimum input frequency. Updated minimum slew rate recommendation for XO (applied to XA/XB).
1.02	August 2020	Updated tables, block diagrams, and figures throughout the document. Added and removed various sections.
1.01	April 2019	Tightened output-out skew (different MultiSynths) specifications. Added input-output delay variation specifications.
1.0	July 2018	Final release. Updated tables, block diagrams, and figures throughout the document. Added and removed sections.
0.9	September 2017	Initial release.