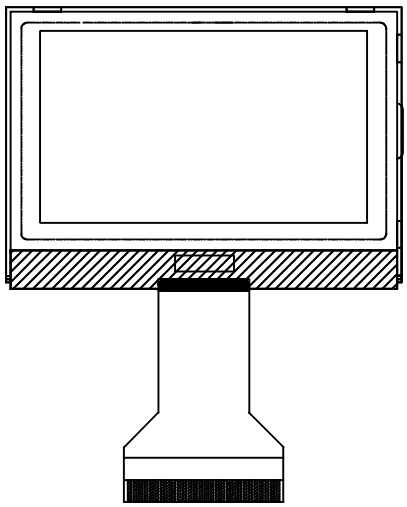
HANTRONIX

PRODUCT SPECIFICATION

HDG12864L-6

128x64 GRAPHICS
Chip-On-Glass
LCD DISPLAY MODULE
with LED Backlight



HANTRONIX, INC. 10080 BUBB RD. CUPERTINO, CA 95014	**Q.A.:** JK	**REV.:** 1.0	HDG12864L-6	SHEET 1 OF 21 **DATE:** 7/23/03

1. MECHANICAL DATA

(1) Product No.	**HDG12864L-6**
(2) Module Size	72.0 (W)mm x 50.4 (H)mm x 6.2 (D)mm (LED B.L.)
(3) Dot Size	0.45 (W)mm x 0.53 (H)mm
(4) Dot Pitch	0.465(W)mm x 0.545 (H)mm
(5) Number of Characters	128 (W) x 64 (H)
(6) Duty	1/64
(9) LCD Display Mode	STN: Gray Mode
	Rear Polarizer: Transflective
(10) Viewing Direction	6 O'clock
(11) Backlight	LED B/L
(12) Weight	25.7g(approx)
(13) Controller (COG)	SED1565D0B OR Compatible

2. ABSOLUTE MAXIMUM RATINGS

(1) ELECTRICAL ABSOLUTE RATINGS

VSS=0V

	SYMBOL	MIN	MAX	UNIT	COMMENT
Power Supply for Logic	VDD−VSS	−0.3	5.5	V	SED1565D0B
Input Voltage	VDD	−0.3	VDD	V	
Static Electricity	−	−	−	−	Note 1

(2) ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE	
	MIN.	MAX.	MIN.	MAX.
Ambient Temperature	−20	70	−30	80
	Note 3,4		Note 4,6	
Humidity (Without Condensation)	Note 2		Note 5	

Note 1 LCM should be grounded during handling LCM.

Note 2 Ta ≦ 50°C : 85%RH max
Ta > 50°C : Absolute humidity must lower than the humidity of 85%RH at 50°C

Note 3 Ta at −20°C will be < 48 hrs, at 70°C will be < 120 hrs

Note 4 Background color will change slightly depending on ambient temperature. That phenomenon is reversible.

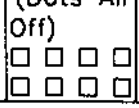
Note 5 Ta ≦ 70°C : 75%RH max
Ta > 70°C : Absolute humidity must lower than the humidity of 75%RH at 70°C

Note 6 Ta at −30°C will be < 48 hrs, at 70°C will be < 120 hrs

3. ELECTRICAL CHARACTERISTICS

3-1. ELECTRICAL CHARACTERISTICS OF LCM

(VDD= 3.3V ± 10%)

ITEM		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage		VIH	H level		0.8VDD	–	VDD	V
		VIL	L level		0	–	0.2VDD	V
Recommended LCD Driving Voltage (WIDE TEMP. LCM)		Vop (VDD-V5)	DUTY= 1/64 Bias= 1/9	-20°C	9.2	9.5	9.8	V
				0°C	8.9	9.2	9.5	
				25°C	8.3	8.6	8.9	
				50°C	8.1	8.4	8.7	
				70°C	7.8	8.1	8.4	
Power Supply Current		IDD	VDD = 3.3V 		–	0.4	0.6	mA
LCM	Surface Luminance	L	VAK=3.2V (RBL=10Ω)	PATTERN: (Dots All On) 	–	0.59	–	cd/m²
				PATTERN: (Dots All Off) 	–	1.26	–	

3–2.ELECTRICAL CHARACTERISTICS OF BACKLIGHT

Used LED Rating

Temp.=25°C

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
Peak forward current	I_P	–	–	150	mA	–
Maximum reverse voltage	V_R	–	–	4	V	–
Applied forward current	I_F	–	90	120	mA	at V_F = 3.2V
Applied forward voltage	V_F	–	3.2	3.5	V	at I_F = 90 mA
LED power consumption	P_F	–	0.288	0.525	W	–
LED life time	L_L	–	40000	–	hrs	at I_F = 90 mA (*1)

(*1) LED life time is defined as follows : The final brightness is at 50% of original brightness .

4. OPTICAL CHARACTERISTICS

(For Wide Temperature Mode LCM)

AT Vop

ITEM / MODE		Cr(Contrast Ratio)										θ(Viewing Angle)		φ(Viewing Angle)	
		-20℃		0℃		25℃		50℃		70℃		25℃		25℃	
		MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	MIN.	TYP.
H	A	3.5	4.0	4.0	4.5	4.5	5.0	4.0	4.5	3.0	3.5	–	60	–	(L)25 (R)30
NOTE		NOTE 6										NOTE 5			

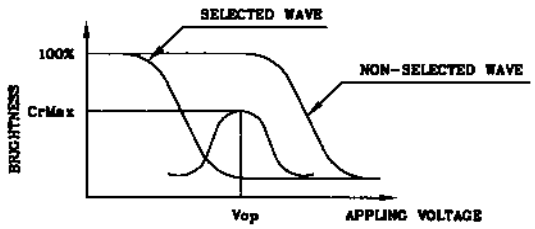
NOTE :
H : Transflective (High Transflective)
A : Gray , 6 O'CLOCK

AT $\phi=0^\circ$ $\theta=0^\circ$

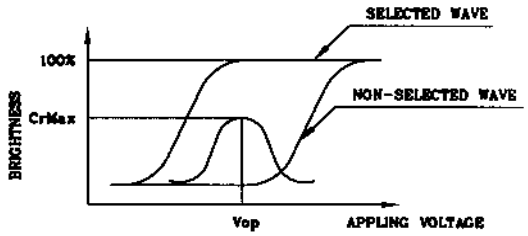
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Response Time (rise)	Tr	-20℃	3600	4500	6700	ms	NOTE 2
		0℃	680	850	1200		
		25℃	200	250	370		
		50℃	70	95	140		
		70℃	45	60	90		
Response Time (fall)	Tf	-20℃	1900	2400	3600	ms	NOTE 2
		0℃	370	470	700		
		25℃	120	150	225		
		50℃	45	60	90		
		70℃	30	45	65		

(NOTE 1)

Definition of Operation Voltage(Vop)



(positive type)



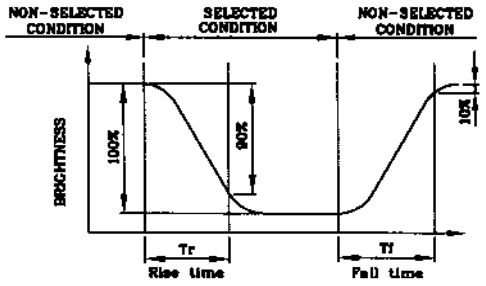
(negative type)

*Conditions

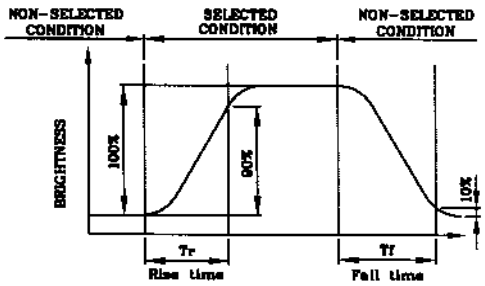
Viewing Angle : 0
Frame Frequency : 70Hz
Appling Waveform : 1/N duty 1/a bias

(NOTE 2)

Definition of Response Time(Tr,Tf)



(positive type)



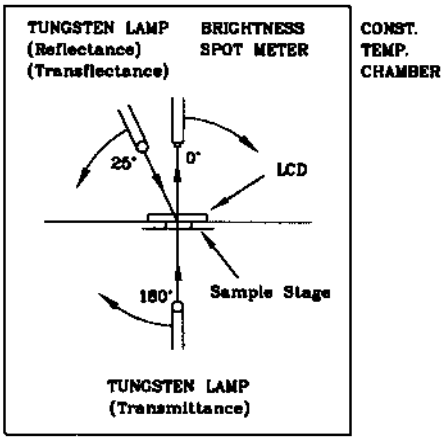
(negative type)

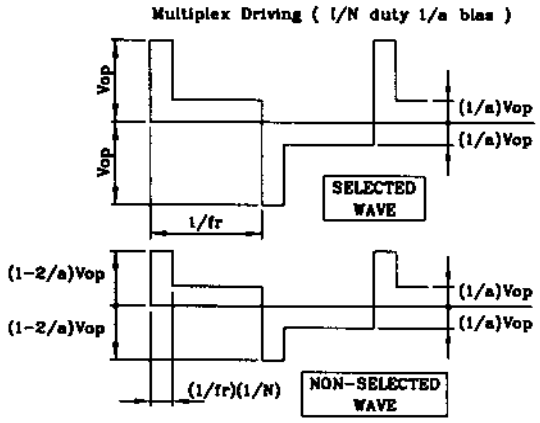
*Conditions

Operating Voltage : Vop
Viewing Angle (ϕ,θ) : (0,0)
Frame Frequency : 70Hz
Appling Waveform : 1/N duty 1/a bias

(NOTE 3)

Description of Measuring Equipment and Driving Waveforms





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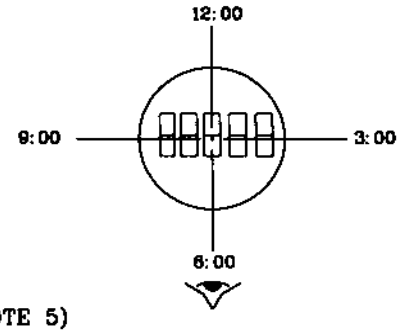
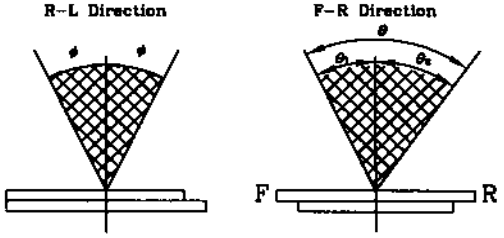
(NOTE 4)

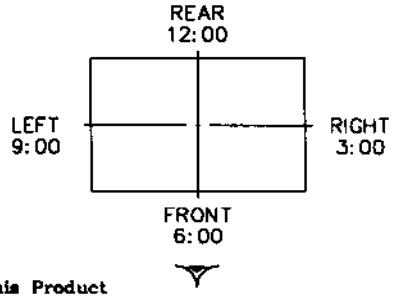
Definition of Viewing Direction



(NOTE 5)

Definition of Viewing Angle





*For This Product

The Viewing Direction Is 6 O'clock

So $\theta 1 > \theta 2$

$\theta = \theta_1 + \theta_2$

*Conditions

Operating Voltage : Vop

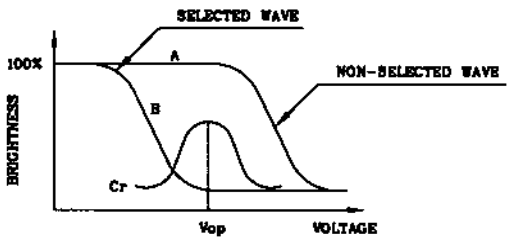
Frame Frequency : 70Hz

Appling Waveform : 1/N duty 1/a bias

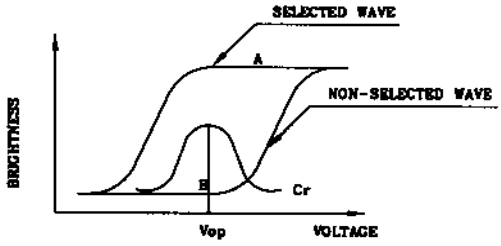
Contrast Ratio : larger than 2

(NOTE 6)

Definition of Contrast Ratio (Cr)



(positive type)



(negative type)

Contrast Ratio : Cr=A/B

*Conditions

Viewing Angle : 0

Frame Frequency : 70Hz

Appling Waveform : 1/N duty 1/a bias

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5. INTERNAL PIN CONNECTION

CN1: FPC CONNECTOR (PITCH 1.0)

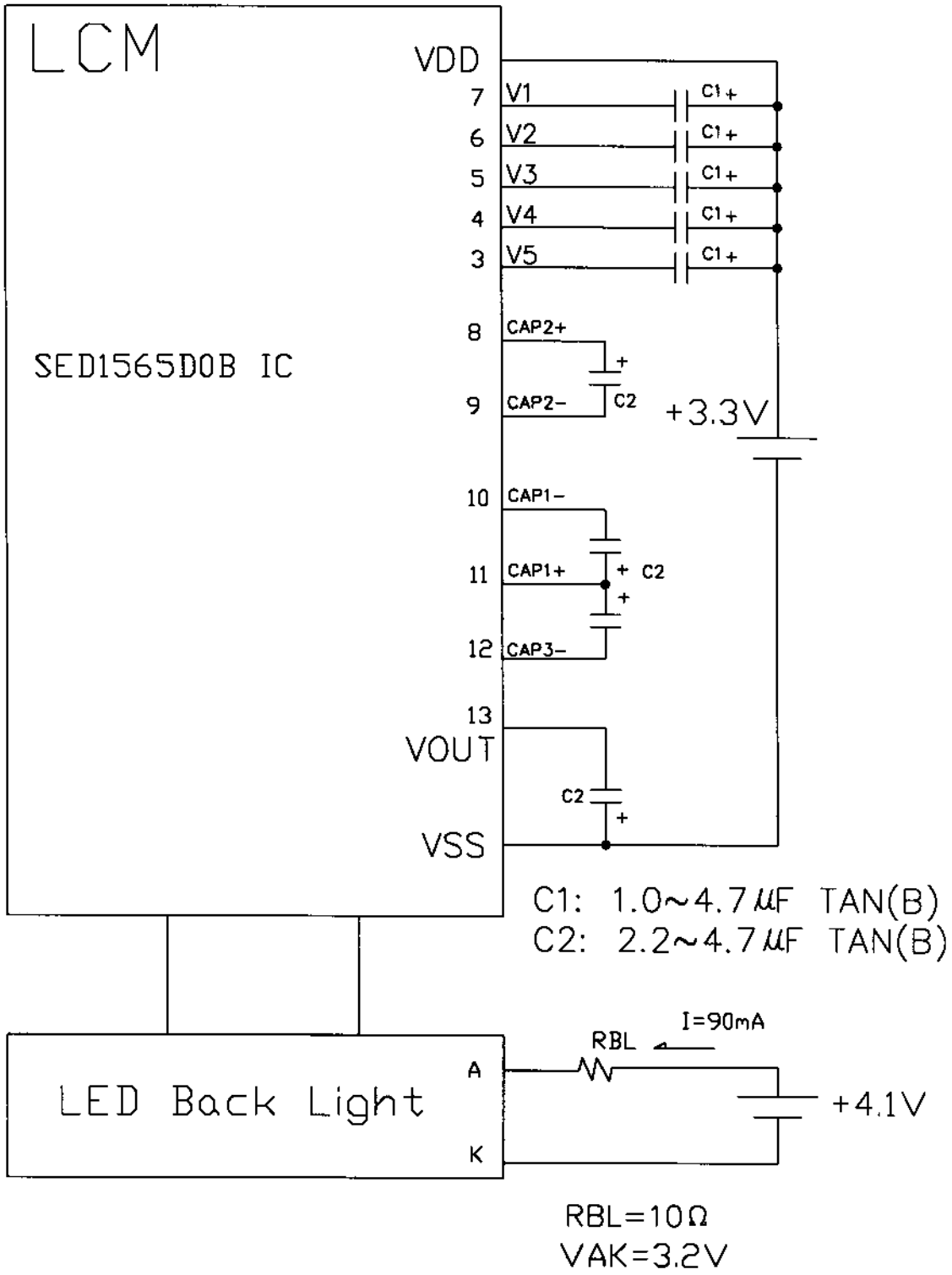
PIN NO	SED1565D0B	FUNCTION
1	P/S	Select Parallel / Serial mode
2	C86	"H" : 6800 Series MPU ; "L": 8080 MPU
3	V5	This is a multi-level power supply for the liquid crystal drive
4	V4	
5	V3	
6	V2	
7	V1	
8	CAP2+	DC/DC Voltage converter
9	CAP2-	
10	CAP1-	
11	CAP1+	
12	CAP3-	
13	Vout	
14	Vss	This is a 0V terminal connected to the system GND
15	VDD	Shared with the MPU power supply terminal VCC
16	D7(SI)	Serial data input
17	D6(SCL)	Serial clock input
18	D5	Parallel data input
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	$\overline{RD}$(E)	Fixed to either "H" or to "L"
25	$\overline{WR}$($\overline{R}$/W)	Fixed to either "H" or to "L"
26	A0	"H" = Display data , "L" = Control data
27	/RES	Reset signal
28	/CS1	Chip select signal

Mating Connector Molex 52271-2890

CN2:

PIN NO	SYMBOL	FUNCTION
1	A	Power Supply Voltage LED Backlight (2.1V)
2	K	GND

6. POWER SUPPLY/BOOSTER CAPACITANCE



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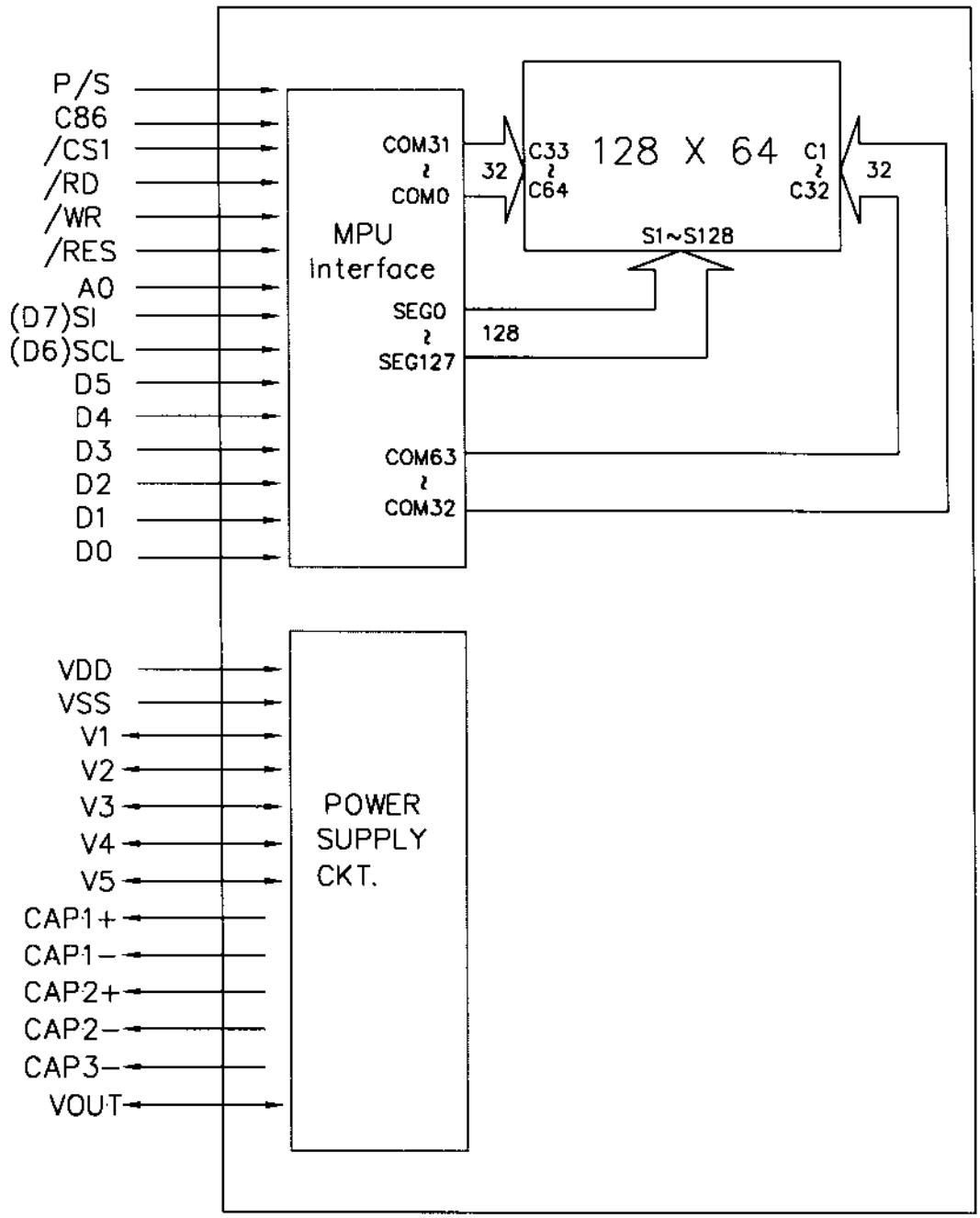
7. MPU INTERFACE/BLOCK DIAGRAM



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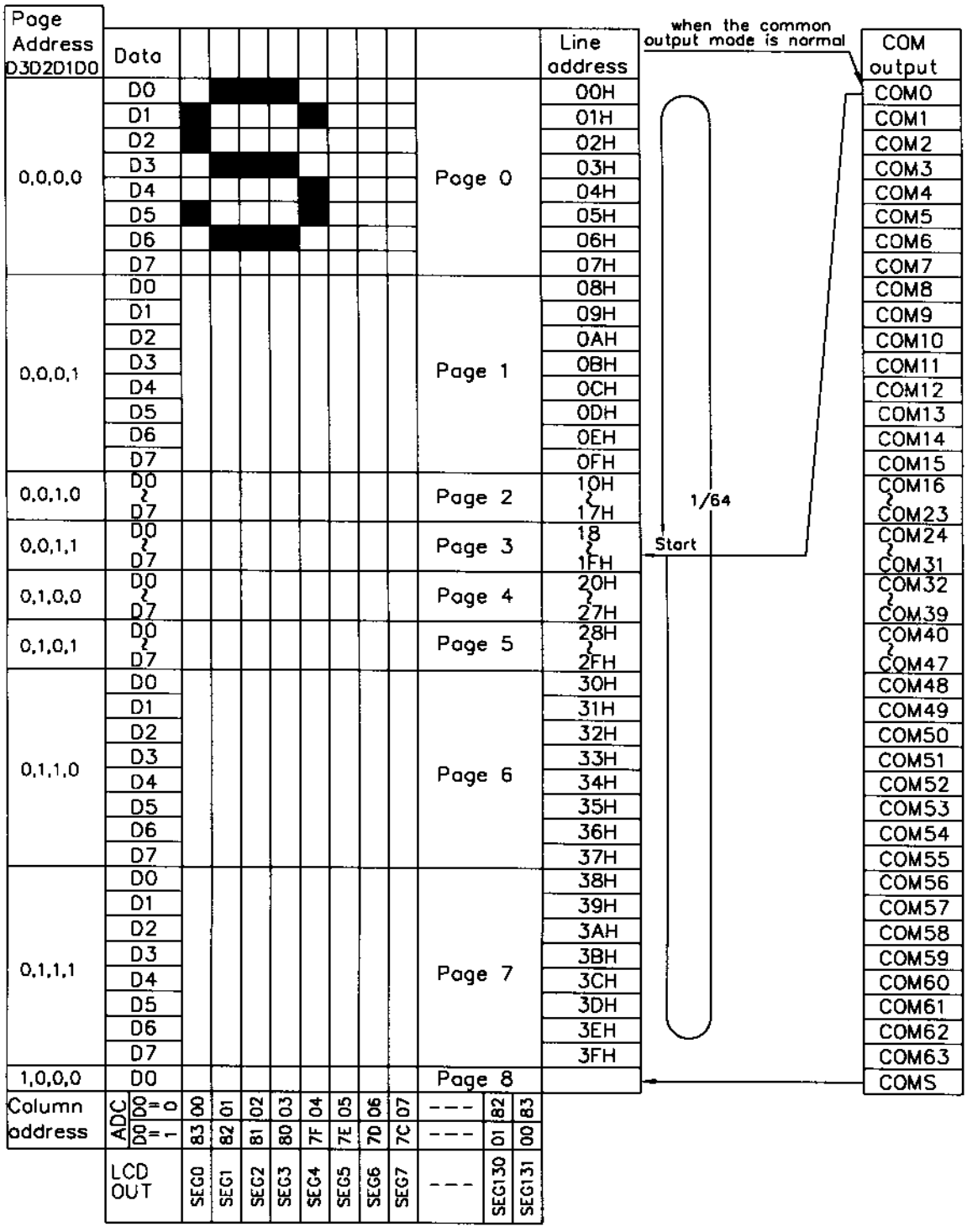
8-1. SED1565 Series Commands

Command	Command Code												Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0		
(1)Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1		LCD display ON/OFF 0: OFF, 1: ON
(2)Display start line set	0	1	0	0	1	Display start address							Sets the display RAM display start line address
(3)Page address set	0	1	0	1	0	1	1	Page address					Sets the display RAM page address
(4)Column address set upper bit	0	1	0	0	0	0	1	Most significant column address					Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address					Sets the least significant 4 bits of the display RAM column address.
(5)Status read	0	0	1	Status				0	0	0	0		Reads the status data
(6)Display data write	1	1	0	Write data									Writes to the display RAM
(7)Display data read	1	0	1	Read data									Reads from the display RAM
(8)ADC select	0	1	0	1	0	1	0	0	0	0	0 1		Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1		Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1		Display all points 0: normal display 1: all point ON
(11)LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1		Sets the LCD drive voltage bias ratio SED1565***....0: 1/9, 1: 1/7 SED1566***....0: 1/8, 1: 1/6 SED1567***....0: 1/6, 1: 1/5
(12)Read/modify/write	0	1	0	1	1	1	0	0	0	0	0		Column address increment At write: +1 At read: 0
(13)End	0	1	0	1	1	1	0	1	1	1	0		Clearv read/modify/write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0		Internal reset
(15)Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*		Select COM output scan direction 0: normal direction, 1: reverse direction
(16)Power control set	0	1	0	0	0	1	0	1	Operating mode				Select internal power supply operating mode
(17)V5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio				Select internal resistor ratio (Rb/Ra) mode
(18)Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1		
Electronic volume register set	0	1	0	*	*	Electronic volume value							Set the V5 output voltage electronic volume register
(19)Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1		0: OFF, 1: ON
Static indicator register set	0	1	0	*	*	*	*	*	*	mode			Set the flashing mode
(20)Power saver													Display OFF and display all points ON compound command
(21)NOP	0	1	0	1	1	1	0	0	0	1	1		Command for non-operation
(22)Test	0	1	0	1	1	1	1	*	*	*	*		Command for IC test. Do not use this command
(23)Test mode reset	0	1	0	1	1	1	1	0	0	0	0		Enter during the refresh sequence.

(Note)*: disabled data

8-2. DISPLAY DATA RAM and ADDRESSES

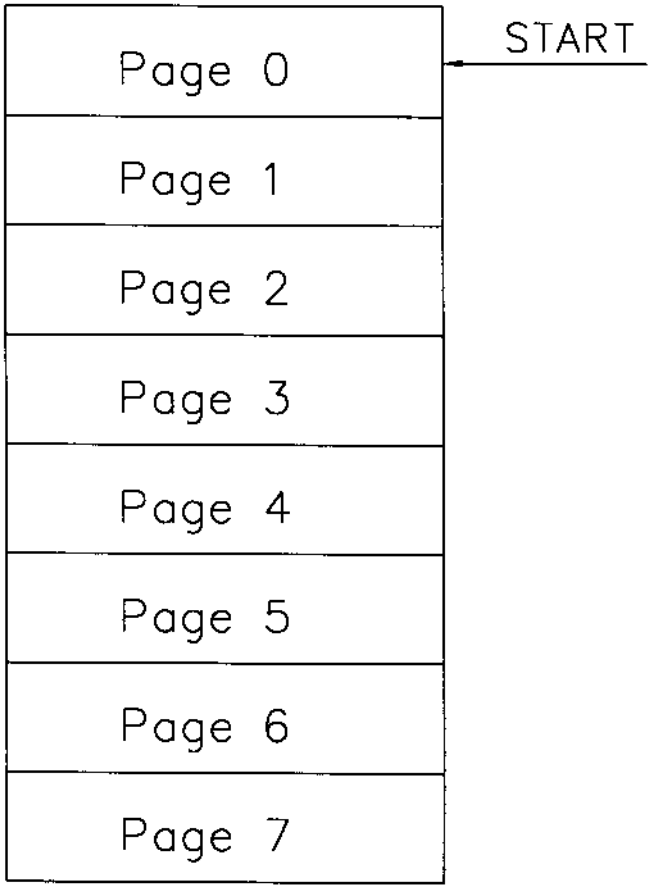


Page Address D3D2D1D0	Data	Line address	Page
0,0,0,0	D0	00H	Page 0
	D1	01H	
	D2	02H	
	D3	03H	
	D4	04H	
	D5	05H	
	D6	06H	
	D7	07H	
0,0,0,1	D0	08H	Page 1
	D1	09H	
	D2	0AH	
	D3	0BH	
	D4	0CH	
	D5	0DH	
	D6	0EH	
	D7	0FH	
0,0,1,0	D0 ~ D7	10H ~ 17H	Page 2
0,0,1,1	D0 ~ D7	18 ~ 1FH	Page 3
0,1,0,0	D0 ~ D7	20H ~ 27H	Page 4
0,1,0,1	D0 ~ D7	28H ~ 2FH	Page 5
0,1,1,0	D0	30H	Page 6
	D1	31H	
	D2	32H	
	D3	33H	
	D4	34H	
	D5	35H	
	D6	36H	
	D7	37H	
0,1,1,1	D0	38H	Page 7
	D1	39H	
	D2	3AH	
	D3	3BH	
	D4	3CH	
	D5	3DH	
	D6	3EH	
	D7	3FH	
1,0,0,0	D0		Page 8

Column address														
	ADC	D0 = 0	00	01	02	03	04	05	06	07	---	82	83
		D0 = 1	83	82	81	80	7F	7E	7D	7C	---	01	00
	LCD OUT		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	---	SEG130	SEG131

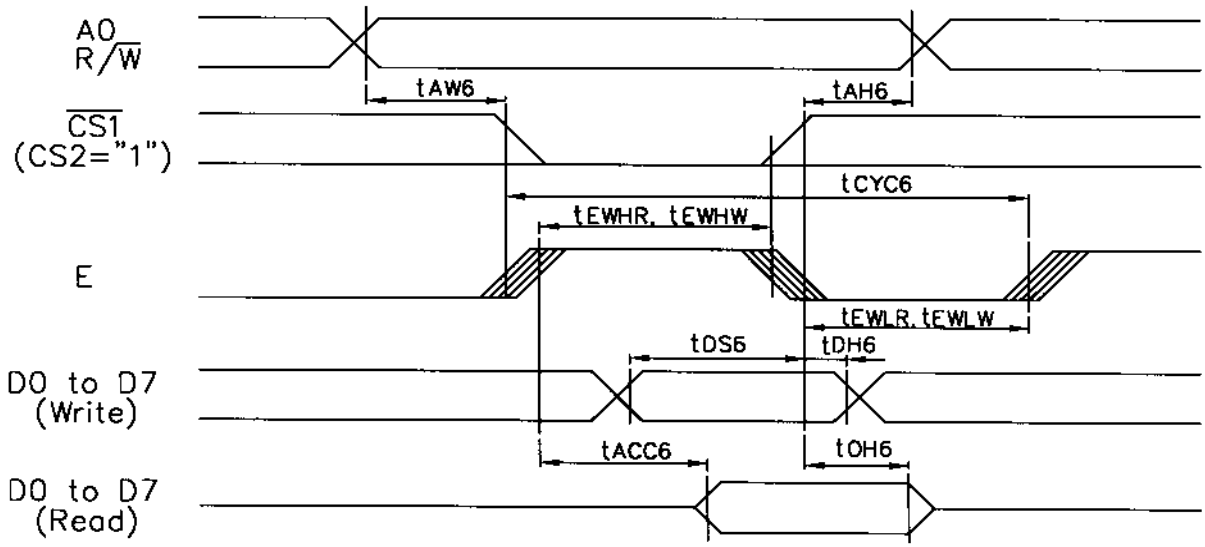
COM output
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16 ~ COM23
COM24 ~ COM31
COM32 ~ COM39
COM40 ~ COM47
COM48
COM49
COM50
COM51
COM52
COM53
COM54
COM55
COM56
COM57
COM58
COM59
COM60
COM61
COM62
COM63
COMS

8-3. DISPLAY PATTRN



9-1. TIMING CHARACTERISTICS

(For 6800 Series MPU)



VDD=4.5~5.5V, Ta=-40~85°C

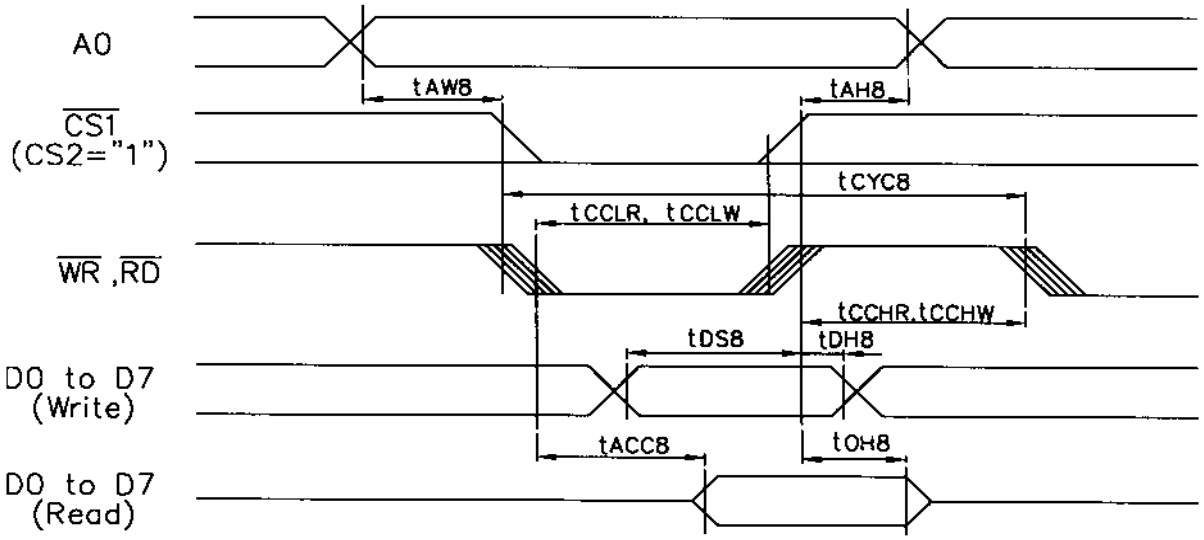
Item		Signal	Symbol	Condition	Rating		Unites
					Min	Max	
Address hold time Address setup time		A0	tAH6 tAW6		0 0	– –	ns ns
System cycle time		A0	tCYC6		166	–	ns
Data setup time Data hold time		D0 to D7	tDS6 tDH6		30 10	– –	ns ns
Access time Output disable time			tACC6 tOH6	CL=100pF	– 10	70 50	ns ns
Enable H pulse time	Read Write	E	tEWHR tEWHW		70 30	– –	ns ns
Enable L pulse time	Read Write	E	tEWLR tEWLW		30 30	– –	ns ns

VDD=2.7~4.5V, Ta=-40~85°C

Item		Signal	Symbol	Condition	Rating		Unites
					Min	Max	
Address hold time Address setup time		A0	tAH6 tAW6		0 0	– –	ns ns
System cycle time		A0	tCYC6		300	–	ns
Data setup time Data hold time		D0 to D7	tDS6 tDH6		40 15	– –	ns ns
Access time Output disable time			tACC6 tOH6	CL=100pF	– 10	140 100	ns ns
Enable H pulse time	Read Write	E	tEWHR tEWHW		120 60	– –	ns ns
Enable L pulse time	Read Write	E	tEWLR tEWLW		60 60	– –	ns ns

9-2. TIMING CHARACTERISTICS

(For 8080 Series MPU)



VDD=4.5~5.5V, Ta=-40~85°C

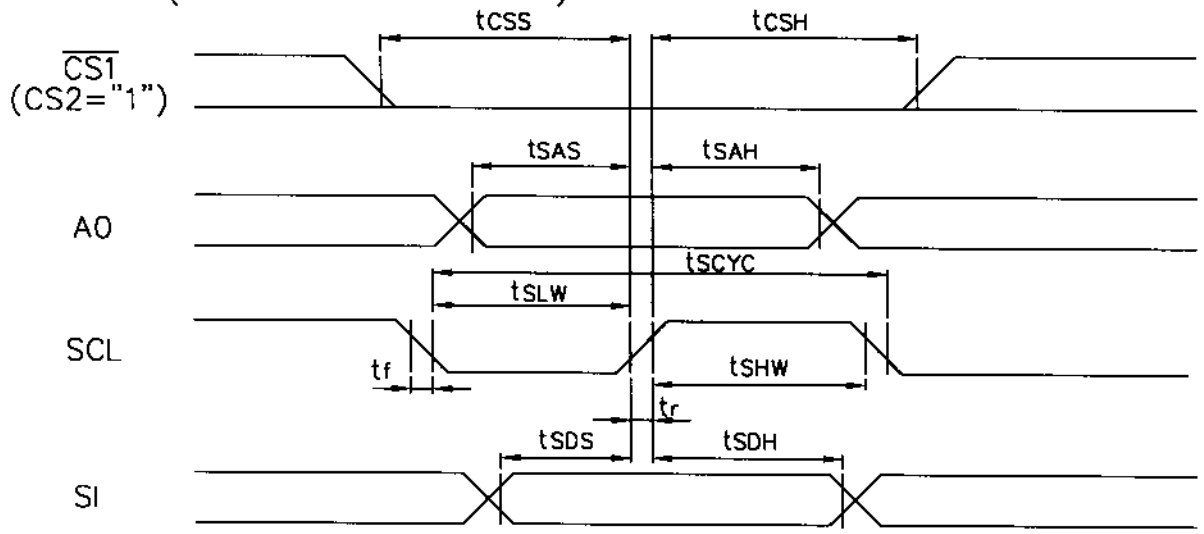
Item	Signal	Symbol	Condition	Rating		Unites
				Min	Max	
Address hold time	A0	tAH8		0	-	ns
Address setup time		tAW8		0	-	ns
System cycle time	A0	tCYC8		166	-	ns
Control L pulse width	$\overline{WR}$	tCCLW		30	-	ns
Control L pulse width	$\overline{RD}$	tCCLR		70	-	ns
Control H pulse width	$\overline{WR}$	tCCHW		30	-	ns
Control H pulse width	$\overline{RD}$	tCCHR		30	-	ns
Data setup time	D0 to D7	tDS8		30	-	ns
Data hold time		tDH8		10	-	ns
$\overline{RD}$ access time		tACC8	CL=100pF	-	70	ns
Output disable time		tOH8		5	50	ns

VDD=2.7~4.5V, Ta=-40~85°C

Item	Signal	Symbol	Condition	Rating		Unites
				Min	Max	
Address hold time	A0	tAH8		0	-	ns
Address setup time		tAW8		0	-	ns
System cycle time	A0	tCYC8		300	-	ns
Control L pulse width	$\overline{WR}$	tCCLW		60	-	ns
Control L pulse width	$\overline{RD}$	tCCLR		120	-	ns
Control H pulse width	$\overline{WR}$	tCCHW		60	-	ns
Control H pulse width	$\overline{RD}$	tCCHR		60	-	ns
Data setup time	D0 to D7	tDS8		40	-	ns
Data hold time		tDH8		15	-	ns
$\overline{RD}$ access time		tACC8	CL=100pF	-	140	ns
Output disable time		tOH8		10	100	ns

9-3. TIMING CHARACTERISTICS

(For Series Interface)



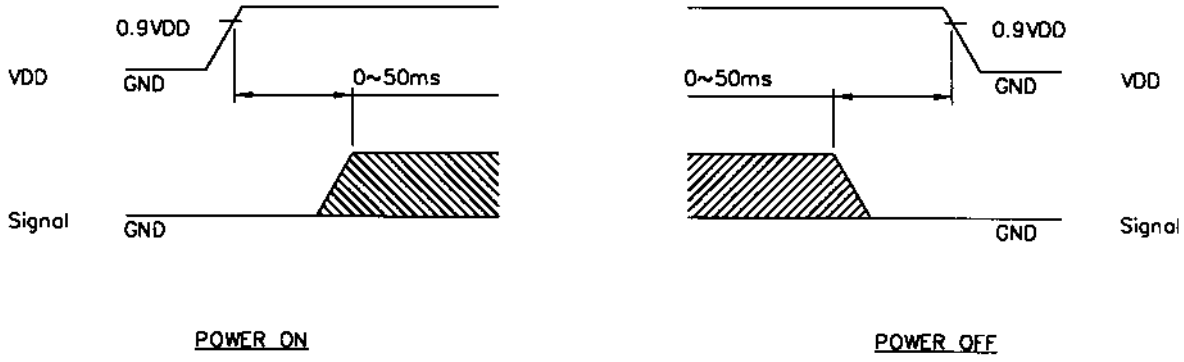
VDD=4.5~5.5V, Ta=-40~85°C

Item	Signal	Symbol	Condition	Rating		Unites
				Min	Max	
Serial Clock Period	SCL	tSCYC		200	-	ns
SCL "H" pulse width		tSHW		75	-	ns
SCL "L" pulse width		tSLW		75	-	ns
Address setup time	A0	tSAS		50	-	ns
Address hold time		tSAH		100	-	ns
Data setup time	SI	tSDS		50	-	ns
Data hold time		tSDH		50	-	ns
CS-SCL time	CS	tCSS		100	-	ns
		tCSH		100	-	ns

VDD=2.7~4.5V, Ta=-40~85°C

Item	Signal	Symbol	Condition	Rating		Unites
				Min	Max	
Serial Clock Period	SCL	tSCYC		250	-	ns
SCL "H" pulse width		tSHW		100	-	ns
SCL "L" pulse width		tSLW		100	-	ns
Address setup time	A0	tSAS		150	-	ns
Address hold time		tSAH		150	-	ns
Data setup time	SI	tSDS		100	-	ns
Data hold time		tSDH		100	-	ns
CS-SCL time	CS	tCSS		150	-	ns
		tCSH		150	-	ns

9-4. POWER ON/OFF TIMING



POWER ON

POWER OFF

The missing pixels may occur when the LCM is driven beyond above power interface timing sequence.

10. RELIABILITY TEST

NO	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	70°C	120HR		Appearance without defect	
2	Low Temp. Storage	−20°C	120HR		Appearance without defect	
3	High Temp. & High Humi. Storage	40°C 90%RH	120HR		Appearance without defect	
4	Thermal Shock	−20°C, 30min → 25°C, 5min → 70°C, 30min → 25°C, 5min (1cycle)			Appearance without defect	5 cycles

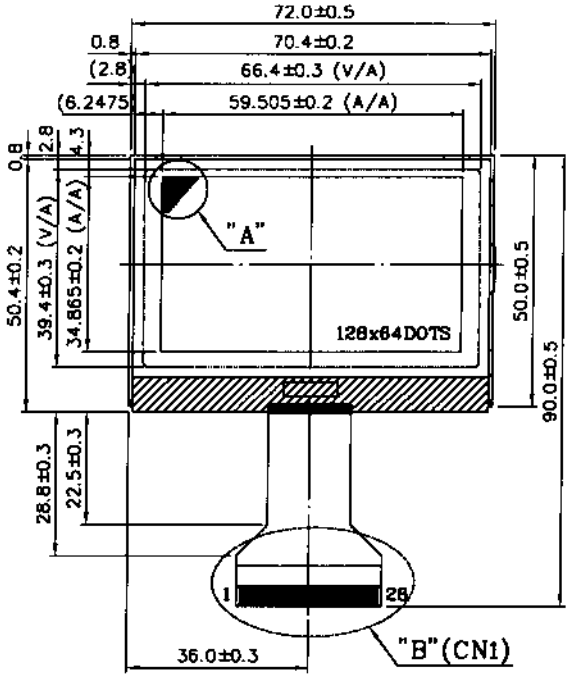
NOTICE:

- SAFETY
  1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
  2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

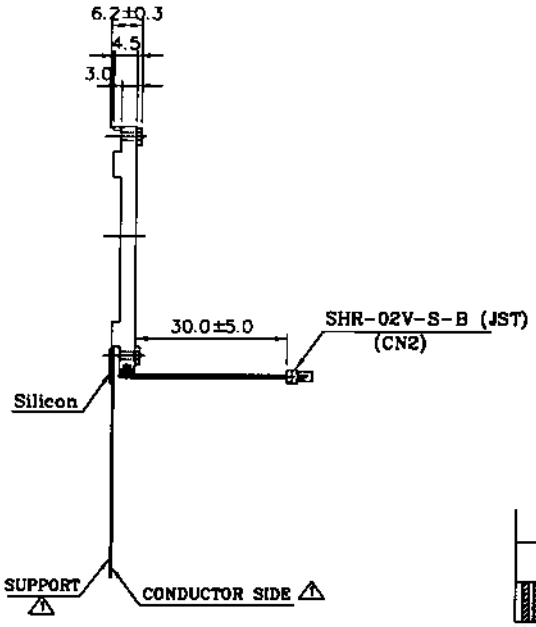
- HANDLING
  1. Avoid static electricity which can damage the CMOS LSI.
  2. Do not remove the panel or frame from the module.
  3. The polarizing plate of the display is very fragile. So, please handle it very carefully.
  4. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
  5. Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.

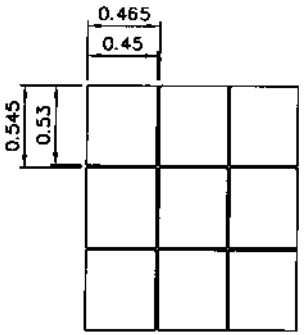
- STORAGE
  1. Store the panel or module in a dark place where the temperature is 25°C±5°C and the humidity is below 65% RH.
  2. Do not place the module near organics solvents or corrosive gases.
  3. Do not crush, shake, or jolt the module.

- TERMS OF WARRANT
  1. Acceptance inspection period
     The period is within one month after the arrival of contracted commodity at the buyer's factory site.
  2. Applicable warrant period
     The period is within twelve months since the date of shipping out under normal using and storage conditions.

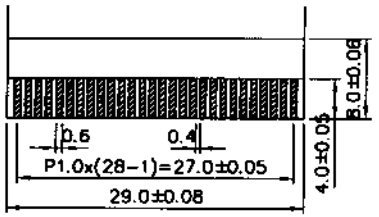


⇧
VIEW DIRECTION

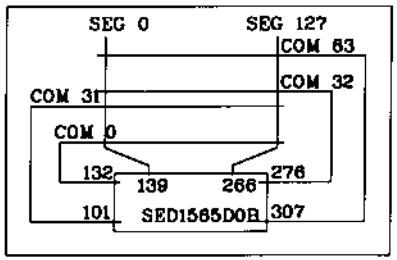




"A" DETAIL
S=30:1



"B" DETAIL
S=2:1



Layout Diagram

NOTES :
1. RESOLUTION : 128 x 64 DOTS
2. COG IC : SED1565D0B or COMPATIBLE
3. GLASS THICKNESS : 0.7 mm
4. BACKLIGHT : LED (BLUE)

SHEET 21 OF 21	DATE: 7/23/03
HDG12864L-6	
REV.: 1.0	
Q.A.: JK	

HANTRONIX, INC.
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CUPERTINO, CA 95014