# User's Guide

SDA64 EVK Evaluation Kit is used with the following ADC boards: SDE11xx-C, SD11xx-L and SDE9609-C.

This user's guide describes the characteristics, operation, and use of the Silanna Semiconductor SDA64 Evaluation Kit (EVK). This user's guide discusses how to set up and configure the hardware and software, and reviews various aspects of the programming operation.
In the following sections of this document, the SDA64 daughter card is referred to as the "*ADC board*" and the device under test is referred to as the "*data converter*", while the Digilent's ZedBoard Zynq-7000 ARM/FPGA SoC Development Board is referred to as the "*ZedBoard*" or "*FPGA board*".

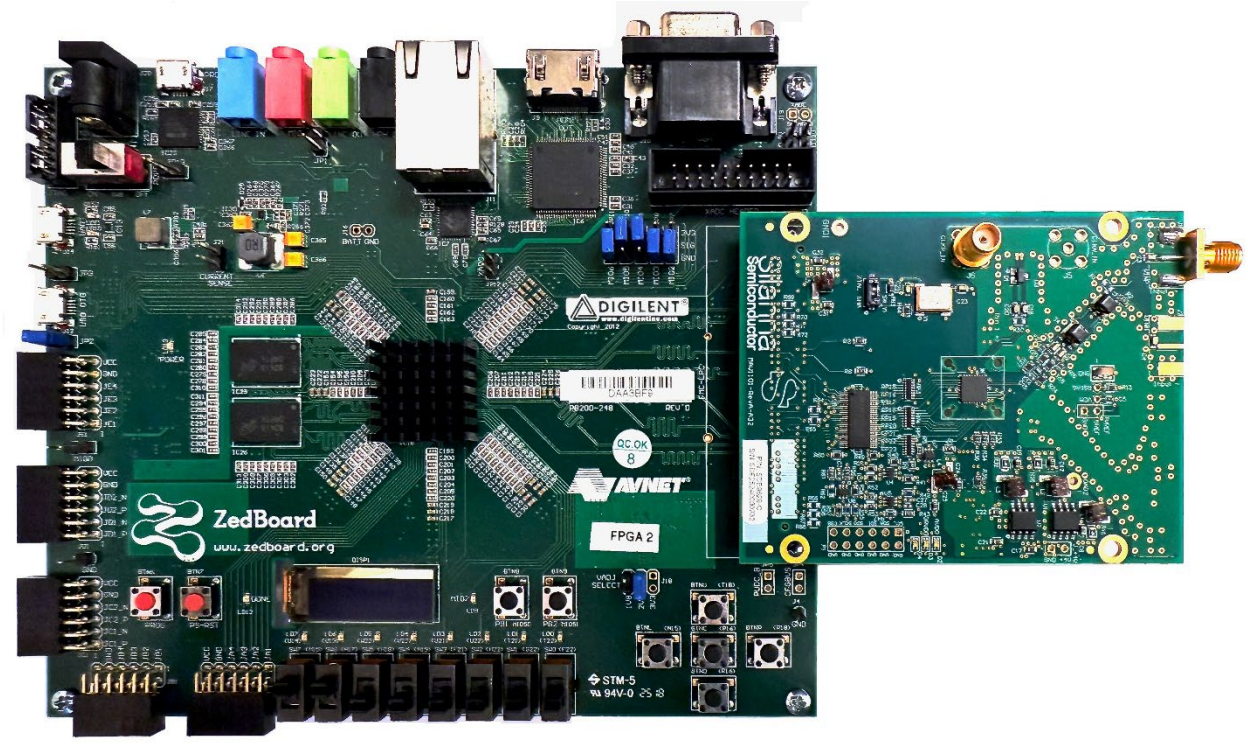


*Figure 1: The SDA64 Evaluation Kit.*

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# 1. Introduction

The SDA64 EVK is used to evaluate analog-to-digital converters (ADC) from Silanna Semiconductors. The Silanna data converters support either a CMOS or LVDS interface to output digital data. The CMOS interface can support output rates up to 160MSps while the LVDS interface can support output rates up to 500MSps in double data-rate mode. The ADC board is equipped with the following features:

- Option to use single-ended or differential signal(s) and clock.
- Option to use an onboard crystal oscillator (XO) or an off-board clock generator, via SMA connector(s).
- Monitors for evaluating power consumption.
- FMC connector to connect the ADC board to the ZedBoard FPGA.

The SDA64 EVK is configured to receive single-ended analog inputs. An on-board bias network performs the single-ended to differential conversion and provides the differential, AC-coupled, input to the ADC(s). The clock is provided by an on-board crystal oscillator or, optionally, by a single-ended external input.

# 2. Equipment

The SDA64 EVK box contains the following:

1. The Silanna ADC board.
2. One SD memory card.
3. One USB-C to ethernet dongle.
4. The Quick Start Guide.

**NOTE:** The SDA64 EVK requires a ZedBoard Zynq-7000 ARM/FPGA SoC Development Board (not provided). See the Quick Start Guide to quickly get started.

Figure 2 shows the ZedBoard with the Silanna ADC board plugged into the mezzanine connector. It also identifies parts of the boards that might require user interaction.

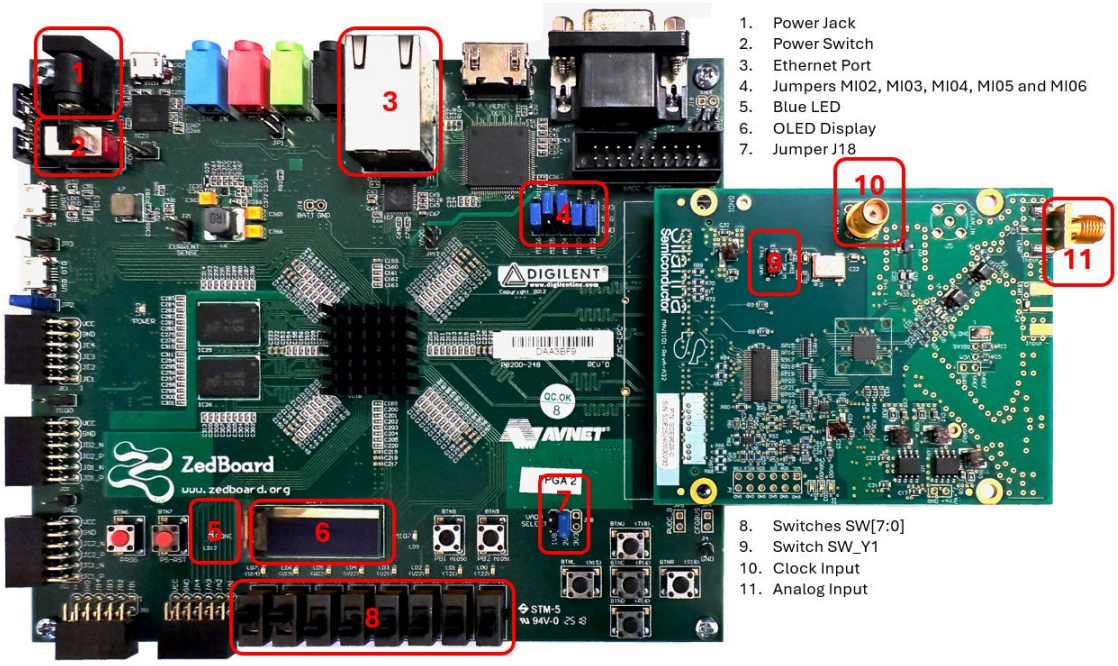
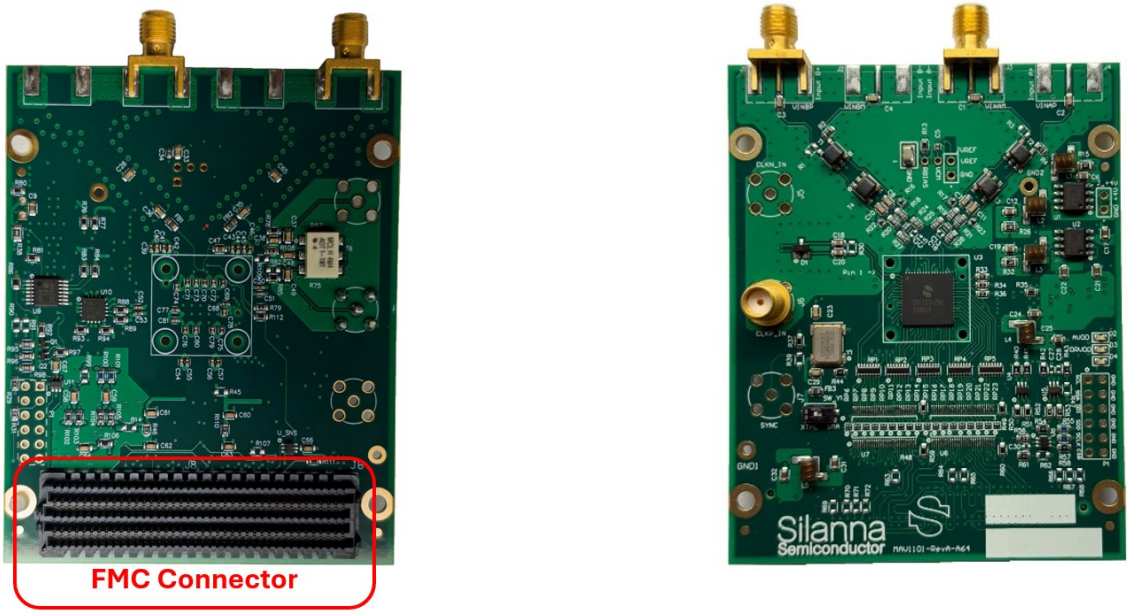



*Figure 2: Top view of Silanna's Plural SDEVK system.*

Figure 3 displays the Silanna ADC board. This card is to be plugged into the front of the ZedBoard into the corresponding mezzanine connector.




a. Bottom side.

b. Top side.

*Figure 3: The Silanna ADC Board.*

Before powering up, the user will be required to load the provided SD card correctly into the ZedBoard (see Figure 4). The SD card holds the firmware that runs on the ZedBoard on-board processor to perform data capture from the ADC board, display the Graphical User Interface (GUI), as well as communicate with the chip during testing.

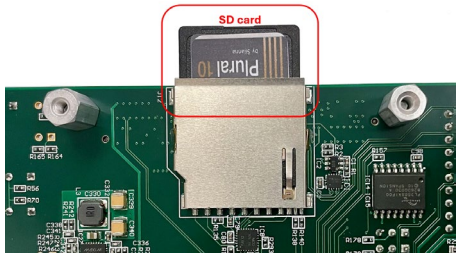



*Figure 4: The SD-card location on the ZedBoard.*

## 2.1. Other Equipment

For clock and analog input connections, utilize low phase noise signal generators (e.g., Rhode & Schwarz SMA, Keysight N5182B) to ensure signal integrity. Interface with the evaluation board using a high-quality, shielded coaxial cable to minimize signal degradation and EMI susceptibility. Additionally, proper filtering of the analog input signal might be required to suppress the signal generator harmonics and broadband noise.

# 3. Set Up Procedure

## 3.1. Board Connections

1. Insert the SD Card
   - Remove the SD card from the Silanna Data Converter EVK box and insert it into the SD card slot on the back of the ZedBoard, as shown in Figure 2.
2. Power Off the ZedBoard
   - Ensure the ZedBoard's power switch is in the OFF position before proceeding (see Figure 4).
3. Configure Jumpers
   Verify the following jumper settings on the ZedBoard:
   - J18: Set to 2.5V
   - MI02: Set to GND
   - MI03: Set to 3.3V
   - MI04: Set to 3.3V
   - MI05: Set to GND
   - MI06: Set to GND
4. Connect Ethernet
   - Connect an Ethernet cable (not provided) from the ZedBoard to the computer that will be used to display and analyze the data or a network switch.
5. Attach the Mezzanine Connector
   - Plug the mezzanine connector from the Silanna ADC board into the corresponding mezzanine connector on the ZedBoard.
6. Set Clock Source
   - If using the onboard crystal oscillator, set SW_Y1 to XTAL.
   - If using an external clock source connected to the SMA clock input, set SW_Y1 to SMA.
7. Connect Power
   - Plug the power cable into the ZedBoard and then into an AC power outlet.

## 3.2. IP Address

Ensure that the PC has been configured to be part of the same sub-network as the SDA64 EVK.
The FPGA will test for the availability of a DHCP server and try to get an IP address. If this fails, the FPGA will assume a local network identity and the IP address will be 192.168.0.XX, where XX = 10+SW[5:3].
In case multiple SDA64 EVKs are used at the same time on the same network, the lower 3 bits of the MAC address can be selected using SW[2:0]. The new MAC address will be XX:XX:XX:XX:50+SW[2:0].
Changing the switches will require a reboot of the FPGA board.

## 3.3. Power-Up Process

Follow these steps to power on the ZedBoard and verify proper initialization of both the ZedBoard and the Silanna ADC board:

1. Turn on the ZedBoard
   - Flip the Power Switch on the ZedBoard to the ON position.
2. Verify Initial Power Indicators
   - The green LED labeled "Power" on the ZedBoard will illuminate.
   - The Ethernet port LED will begin blinking, indicating network activity.
   - The D4 LED on the Silanna EVK will turn red, confirming power is being supplied to the EVK.
3. Boot Sequence
   - The blue LD12 LED near the OLED screen on the ZedBoard will turn on.
   - The ZedBoard FPGA will begin booting and loading its firmware.

- During this process, a progress bar will appear on the OLED screen, indicating the firmware loading status (up to 80 seconds).
- Once the boot process is complete, an IP address will be displayed at the bottom of the OLED screen (see Figure 5).

4. EVK Initialization
   - After the ZedBoard has successfully loaded its firmware, the D3 and D2 LEDs on the Silanna ADC board (located near D4) will also turn red, indicating that the system is fully initialized and ready for operation.

# 4. Graphical User Interface

The SDA64 EVK can be controlled via a web-based graphical user interface. Once the SDA64 EVK is initialized an IP address is displayed on the OLED display on the ZedBoard (Figure 5).


*Figure 5: GUI EVK IP address.*

Bring up your web browser on your computer and type the IP address shown on the display in the address bar. Once the connection is established, the following on your screen will load on your web browser:

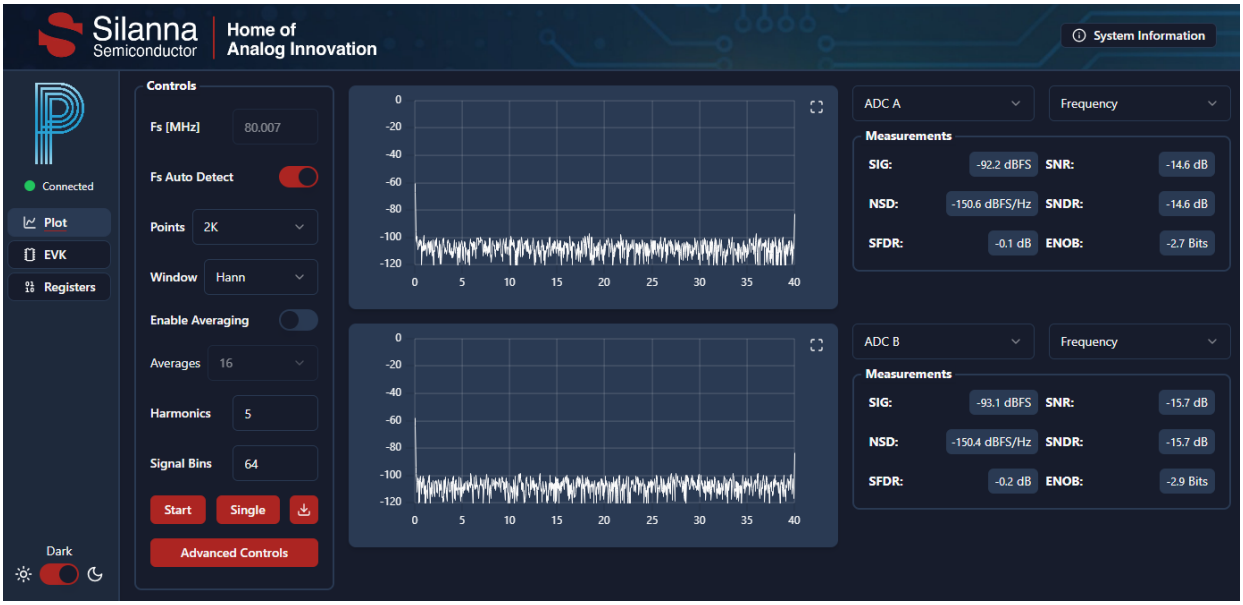



*Figure 6: GUI Start-Up page (dark mode).*

## 4.1. General Control Features

The GUI offers the general features described below. Moreover, the location of some of the controls might change to comfortably fit the display size.

- Dark/Light control for the appearance of the GUI.
- Connection status indicator indicates whether the EVK is connected to the GUI.
- System Information: A pop-up window provides detailed information about the SDA64 system components, including the data converter chip, evaluation board, firmware, and helpful documentation links.

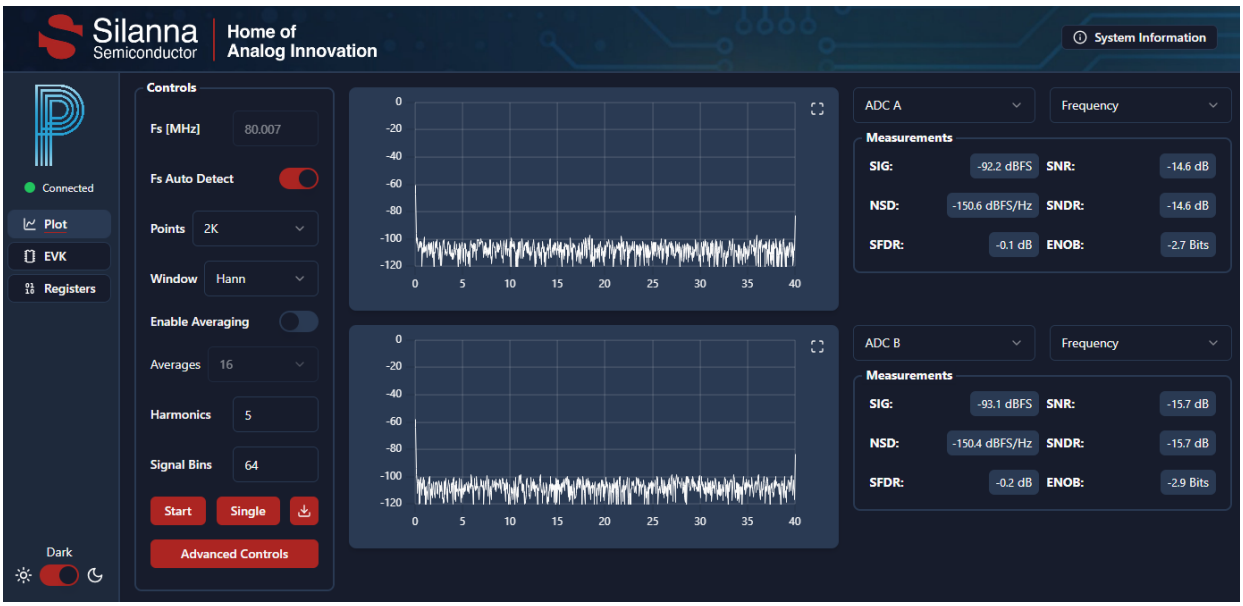
- **Part** (displays information about the Silanna ADC chip)
  *Type*: Indicates the resolution (number of bits) the device can decode.
  *Revision*: Specifies the silicon revision of the chip installed on the evaluation board.
- **ADC Board** (provides identification details for the ADC board)
  *ID*: The first letter indicates the board type. The number denotes the pin count of the supported chip.
  *Revision*: Indicates the hardware revision of the ADC board.
  *Serial Number*: A unique serial number assigned to each ADC board.
  *Build*: Specifies the interface type used to connect to the ZedBoard (e.g., LVDS or CMOS).
- **Firmware** (displays firmware-related information)
  *ID*: Identifies the firmware type (1120 for CMOS interface or 1121 for LVDS interface).
  *FPGA Revision*: The first letter (C or D) indicates whether the FPGA is running CMOS or LVDS build. The following 3 numbers represent the version of the build.
  *Application*: Shows the version of the application software running on the ZedBoard.
- **Links**
  *User Guide*: The official User Guide for the EVK.
  *Firmware Update*: The latest Firmware Update available on the Silanna website.

## 4.2. Plot Tab

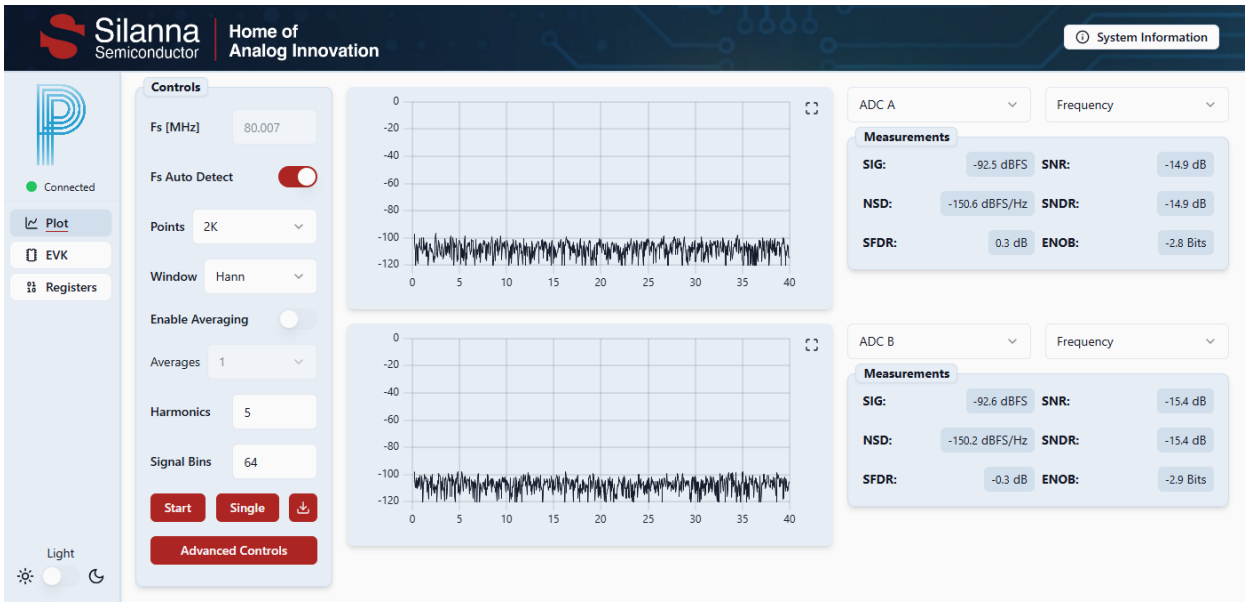
The Plot tab is shown in Figure 7 and is used to display the display controls, the captured data from the ADC board and some basic metrics. It includes 3 main panels:

- Controls Panel
  - Used to set parameters for basic calculation and display:
    **Fs** – indicates the sampling rate of the ADC board.
    **Fs Auto Detect** – When selected, it automatically calculates the sampling rate of the ADC board.
    **Points** – Select the number of points to capture from a drop-down menu.
    **Window** – Set the window function used to reduce leakage in the Discrete Fourier Transform (DFT) calculations.
    **Enable Averaging** – Enables frequency-domain averaging during DFT calculations. The number of averages is determined by the value selected in the **Averages** drop-down menu. Each average corresponds to one block of captured data, and the final spectrum is computed by averaging the power spectra of multiple blocks. This reduces noise and improves measurement stability.
    **Harmonics** – Specifies the number of harmonics included in the Total-Harmonic Distortion calculation and excluded from the Signal-to-Noise Ratio (SNR) calculation.
    **Signal Bins** – Defines the number of frequency bins used to identify the fundamental input signal in the DFT spectrum.
    **Start** – Initiates continuous data acquisition. While active, the system continuously samples incoming signals and updates the graphs in real time, providing a live view of the signal behavior.
    **Stop** – Halts the ongoing data capture and retains the most recently acquired data displayed on the graphs.
    **Single** – Captures and displays a one-time snapshot of the sampled signal on the graphs.
    **Download** – Allows the user to export the captured data to a .CSV file. Users can select one or both displayed graphs for export. The downloaded data can be used for offline analysis or custom plotting.

- Display(s)
  - Used to display the time-domain or frequency-domain waveform of the captured data, according to the mode selected in the Measurement Panel.
  - The top-right corner of the display includes a button to create a full-screen display of the captured data.
- Measurement Panel(s)
  - Allows the selection of data source (ADC_A or ADC_B, for a dual channel ADC board) and the graph mode (time-domain or frequency domain).
  - Displays some basic metrics of the captured data:
    **SIG** – Power of the waveform (in dBFS)
    **SNR** (Signal-to-Noise Ratio) – The ratio of the RMS amplitude of the fundamental input signal to the RMS amplitude of all other spectral components excluding harmonic distortion and DC. It quantifies the ADC's ability to distinguish the desired signal from background noise, in dB.
    **NSD** (Noise Spectral Density) – It quantifies the amount of noise power generated by the ADC per unit bandwidth, in dBFS/Hz. It represents the noise floor of the ADC in the frequency domain.
    **SNDR** (Signal-to-Noise and Distortion Ratio) – The ratio of the RMS amplitude of the fundamental input signal to the RMS sum of all other spectral components, including noise and harmonic distortion (but excluding DC), in dB.
    **SFDR** (Spurious-Free Dynamic Range) – The ratio of the RMS amplitude of the fundamental input signal to the RMS amplitude of the largest spurious spectral component (excluding DC), measured over the ADC's Nyquist bandwidth, in dB.
    **ENOB** (Effective Number of Bits) – The measure of an ADC's actual resolution based on its dynamic performance (SNDR), accounting for all noise and distortion sources.




a. Dark mode.




b. Light mode.

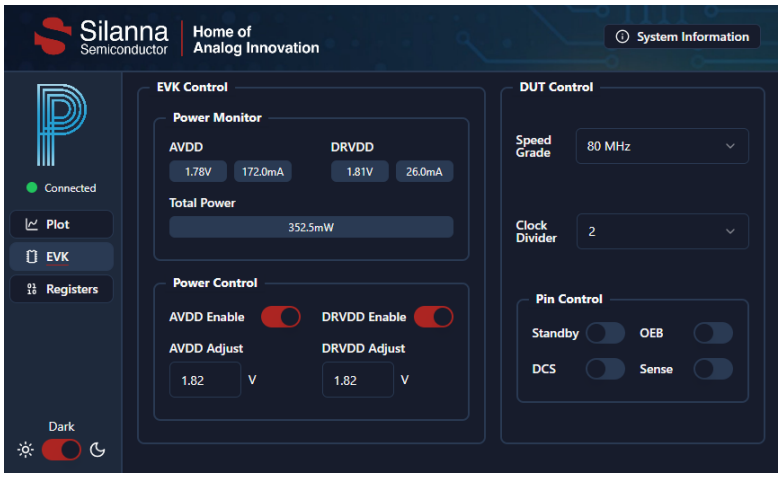
*Figure 7: The Plot Tab.*

## 4.3. EVK Tab

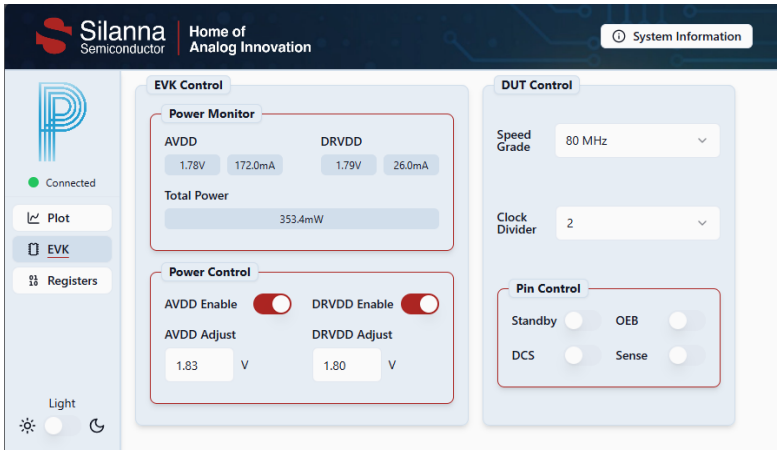
The EVK tab, see Figure 8, includes two panels, one for EVK control and monitoring and one for device-under-test (DUT) control. The functionality of each element is as follows:

- **Power Monitor** – The Silanna EVK uses a sense resistor in line with the AVDD and DRVDD power supplies to measure the power dissipated by the data converter chip.
  - $V_{AVDD}/I_{AVDD}$ – measure of analog supply voltage and current being utilized by the Silanna data converter.
  - $V_{DRVDD}/I_{DRVDD}$ – measure of digital I/O supply voltage and current being utilized by the Silanna data converter.
  - Total Power – power dissipated in the Silanna data converter.
- **Power Control**
  - AVDD Enable – control button to enable/disable the $V_{AVDD}$ supply.
  - DRVDD Enable – control button to enable/disable the $V_{DRVDD}$ supply.
  - AVDD Adjust – control to set the desired $V_{AVDD}$. This is the target voltage at the on-board regulator to achieve the voltage shown by the Power Monitor, $V_{AVDD}$.
  - DRVDD Adjust – control to set the desired $V_{DRVDD}$. This is the target voltage at the on-board regulator to achieve the voltage shown by the Power Monitor, $V_{DRVDD}$.
- **DUT Control**
  - Speed Grade – select the maximum sample rate for the Silanna data converter under test. Depending on the EVK purchased, the supported Speed Grades are listed in the pull-down menu. The Speed Grade can be changed to overwrite the data converter's default settings.
  - Clock Divider – select the clock divider to set the sampling rate for the Silanna data converter.
- **Pin Control**
  - The content of this panel is dependent on the specific DUT. The GUI identifies the device under test and then displays the control pins that the specific data converter offers to the user. The user can then manipulate those control pins manually for their testing purposes. Examples of these are:

- Standby – Enable the standby mode (in External Pin Mode).
- DCS – Duty Cycle Stabilizer control (in External Pin Mode).
- OEB – Output Enable (active low).
- Sense – Voltage reference programming pin.




a. Dark mode




b. Light mode

*Figure 8: The EVK Tab.*

*NOTE*: Data converters on Silanna's EVK board are not sample rate limited as they are in Silanna's data converter portfolio.

## 4.4. Registers Control Tab

The Register Control Tab, shown in Figure 9, allows the user to read and write registers in the data converter's memory map.

- **Address** – The address in the data converter's memory map to read from or write to.
- **Value** – The value that sits in the register that you would like to query, or the value that you would like to write to a specific register.
- **Mask** – A value used to modify only selected bits in a register (read-modify-write operation).
    - *Example*: Consider a register located at address 0x463 with a current value of 0x19. In binary, this is represented as 0b00011001. Bits [7:5] control the clock divider setting, and a value of 0b000 indicates that the divider is bypassed.

- To update the clock divider to a value of 0b001 (divide by 2), the following steps are performed:
  - Create a mask to isolate the target bits: 0b11100000 (or 0xE0), this selects bits [7:5].
  - Prepare the new value to be written to the selected bits: 0b00100000 (or 0x20).
- Apply the read-modify-write operation:

- **Read/Write Buttons** – Enact the Read or Write operation.

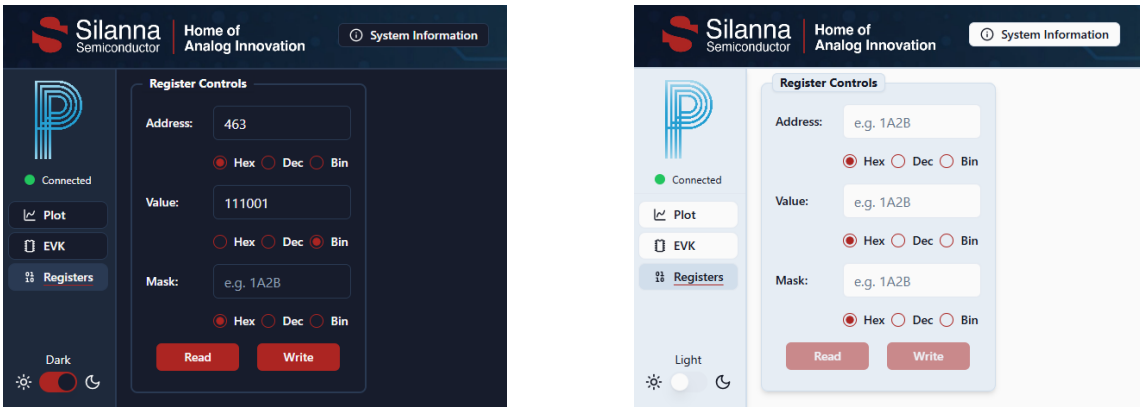



*Figure 9: The Register Control Tab (dark mode and light mode).*

## 4.5. Check for Firmware Release (Optional)

To check for the latest firmware release, follow these steps:

- Click the System Information button located in the upper-right corner of the GUI. The System Information pop-up window will appear (see Figure 10).
- Click the Firmware link and compare the displayed firmware application version with the latest version available on the Silanna Support Website.

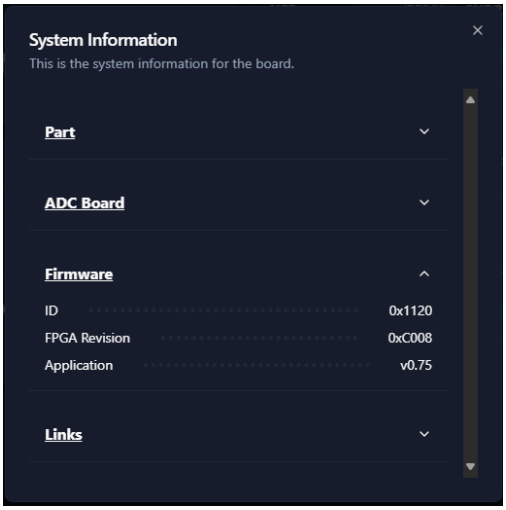



*Figure 10: System Information - Firmware.*

If a newer version of the firmware is available, follow the steps below to install it on an SD card.

- Download and Prepare the Firmware
  - Download the latest firmware update package to your computer.

- Unzip the package to extract all files.

- Install on a New SD Card
  If you're using a new SD card:
  - Format the SD card using the FAT32 file system.
  - Copy all extracted files to the root directory of the SD card.
- Reuse an Existing SD Card
  If you're reusing an existing SD card:
  - Back up any important data from the card.
  - Copy all extracted files to the root directory of the SD card (overwrite the old firmware files).

Once the files are copied, the SD card is ready for use with the device.

# 5. ADC Board Configuration

## 5.1. Analog Input

The analog input circuit on the ADC board is designed to accommodate several input configurations. By default, it is configured as an AC-coupled, single-ended input.

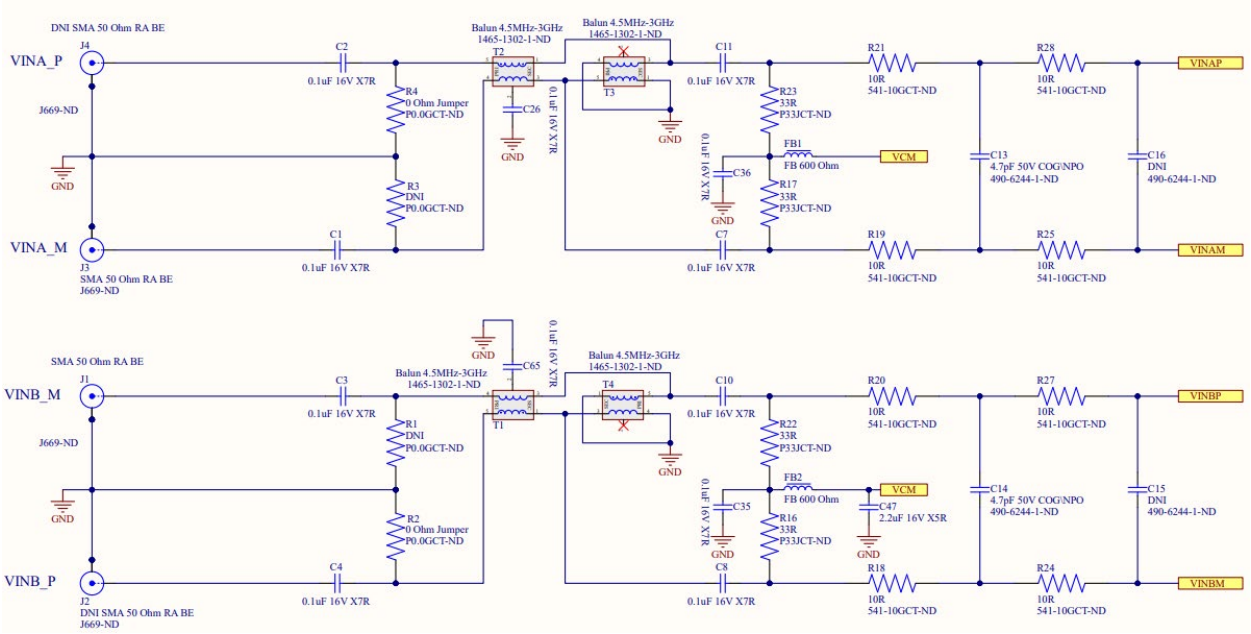



*Figure 11: Analog Input Circuit.*

The single-ended input can be converted into a differential input by adding a new SMA (J2/J4) and removing resistors R1/R4 (R2/R3 are DNI in the default configuration). If the input balance from the signal source is good, the ADC performance might be improved by removing the baluns, T3 and T4.
*NOTE*: The input signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

The RC network formed by R18/R19, R20/R21, R24/R25, R27/R28, C13/C14 and C15/C16 is a simple low-pass filter with an approximate bandwidth of 600MHz. The user might need to change these resistor and capacitor values to better fit the target application.

*NOTE*: Many ADC input drivers benefit from adding a low value series resistor in series with the inputs of the ADC as well as a shunt capacitor.

## 5.2. Clock Input

The clock input circuit of the ADC board is shown in Figure 12. Switch SW_Y1 is used to select between the on-board crystal oscillator (Y1) or an external source. By default, the external clock input is configured for AC-coupled, single-ended operation, via the J6 SMA connector (*CLKP_IN*).
The on-board crystal oscillator can be further configured to provide a differential clock signal to the data converter using either a balun or a transformer (default). Refer to Table 1 for the required hardware modifications and component placements.

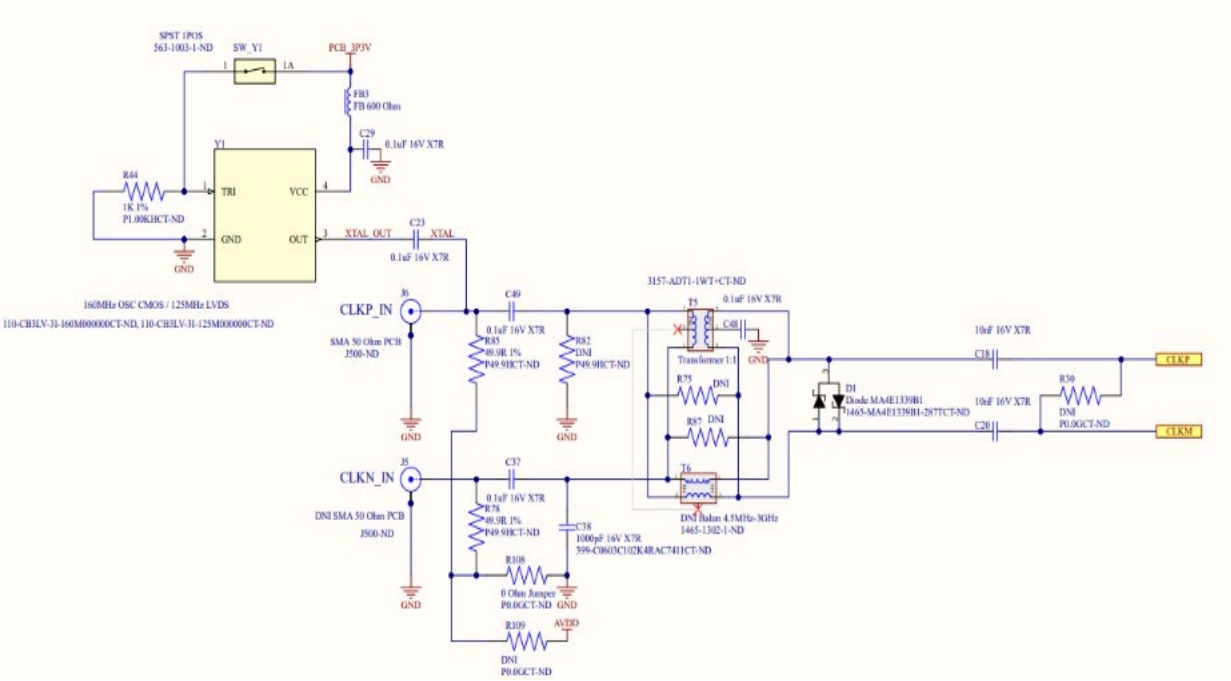



*Figure 12: Clock Input Circuit.*

Similarly, the external single-ended clock input (via the J6 SMA connector) can be converted to differential by installing the J5 SMA connector and following the configuration steps outlined in Table 1.

| Clock Option | T5 | T6 | C38 | R75/R87 |
|---|---|---|---|---|
| T – Transformer | Install | DNI | 0Ω (resistor) | DNI |
| B – Balun | DNI | Install | 1000pF | DNI |
| Differential | DNI | DNI | DNI | 0Ω |

*Table 1: Clock Option Table.*

# 6. Troubleshooting

**Q:** Why is the ZedBoard not booting?

**A:** If the ZedBoard fails to boot, begin by checking the blue LED indicator shown in Figure 2. If the LED is not illuminated, the issue is likely related to the SD card or board configuration. Follow the steps below to diagnose and resolve the problem:

1. **SD card is not properly inserted**. Ensure the SD card is fully and securely inserted into its slot. Gently press the card until it clicks into place.
2. **Corrupted SD card**. A corrupted SD card can prevent the board from booting. Visit the Silanna Support website and follow the recovery instructions provided in Section 4.5 to reimage or replace the SD card contents.
3. **Incorrect File System Format**. The SD card must be formatted using the FAT32 file system. Reformat the card if necessary and ensure all required boot files are correctly copied.
4. **Incorrect Jumper Configuration**. Improper jumper settings can prevent the ZedBoard from booting from the SD card. Refer to Section 3.1 for the correct jumper configuration.

**Q**: The GUI is not connected to the FPGA board. What should I do?

**A**: Follow these instructions:

1. **Check the IP Address**: Ensure that the IP address shown on the FPGA board's OLED display matches exactly what you are entering in your browser's address bar.
2. **Ensure unique MAC address**: If you are using multiple boards on the same network, modify the MAC address according to section 3.2.
3. **Verify Network Connection**: Make sure your computer is connected to the same network as the FPGA board.
4. **Refresh the Browser**: Sometimes a simple refresh (Ctrl+R or Cmd+R) can help re-establish the connection.

**Q**: The ZedBoard does not acquire an address using the DHCP server. What should I do?

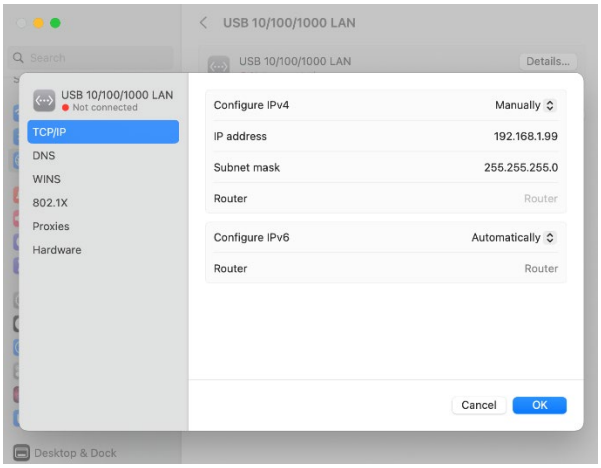
**A**: Follow these instructions:

1. **Power Cycle the Board**: Turn off the ZedBoard, wait a few seconds, and then power it back on. This will restart the DHCP request process and may resolve temporary communication issues.
2. **Verify Network Connection**: Ensure that the Ethernet cable is securely connected to both the ZedBoard and the network switch or router. Try using a different cable or port if necessary.
3. **Check DHCP Server Availability**: Confirm that a DHCP server is active and functioning on the network. If you're unsure, consult your network administrator to verify DHCP service status and network configuration.

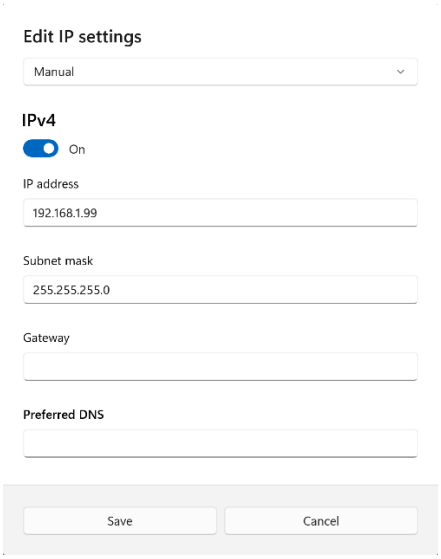
**Q**: How Do I Connect the SDA64 EVK Directly to My Computer?

**A**: If you want to connect the SDA64 Evaluation Kit (EVK) directly to your computer using an Ethernet cable (without a router or DHCP server), follow these steps to configure the network manually:

1. **Set Manual IP Configuration on the PC**: Open your computer's network settings. Locate the wired Ethernet adapter settings. Set the IP configuration mode to Manual (or Static, depending on your operating system). Assign an IP address in the range: 192.168.1.xx (e.g., 192.168.1.99.
2. **Configure Subnet Mask**: Set the Subnet Mask to 255.255.255.0
3. **Leave Gateway and DNS Blank**.




macOS




Windows

**Q:** Why does the FFT plot show large tones?

**A:** This can be caused by several factors. Check the following:

1. **High Input Amplitude**: The signal generator output may be too strong, causing distortion. Try reducing the input level.
2. **Harmonics or Spurs from the Signal Generator**: Most signal generators produce unwanted harmonics or spurious tones. Use a bandpass filter centered at your frequency of interest to suppress these.
3. **Aliasing Due to Insufficient Sampling Rate**: If the sampling rate is too low, higher-frequency components can fold into the FFT spectrum. Ensure your sampling rate is at least twice the highest frequency in your signal (Nyquist criterion).
4. **Clock Jitter**: Timing variations in the ADC clock can introduce spectral artifacts. Use a high-quality, low-jitter clock source.
5. **Improper Windowing or FFT Settings**: Using the wrong window function or FFT size can cause spectral leakage, making tones appear larger. Try applying a Han or Blackman window and experiment with different FFT lengths. If possible, make your input signal frequency coherent with your sample rate.
6. **Reflections or Impedance Mismatch**: Mismatched cables or connectors can cause signal reflections, leading to standing waves and unexpected tones. Check your connections and use proper termination.

## 7. Revision History

| Version | Date | Comment |
|---|---|---|
| 1.0 | Jul 7, 2025 | Initial Release. |
| | | |