DATASHEET

AEM00900
AEM00901

Compact PMIC with Source Voltage Level Configuration for PV Cells or Pulsed Source

Features and Benefits

Constant input voltage regulation (0.12 V to 2.73 V)
- Optimized for single/dual elements capacitive PV cell, intermittent and pulsed power sources.

Cold start from 250 mV input voltage and ultra-low input power
- Fast start-up from source;
- AEM00900: 2.47 µW cold-start power (typical);
- AEM00901: 3.99 µW cold-start power (typical).

Selectable overdischarge and overcharge protection
- Supports various types of rechargeable batteries (LiC, Li-ion, LiPo, Li-ceramic pouch, etc.).

Thermal monitoring
- Battery protection against over-temperature and under-temperature during charging.

Average power monitoring
- Easy estimation of the charging power.

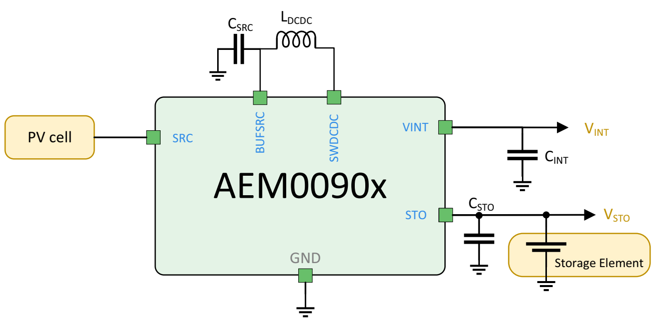
Shipping and shelf mode
- Prevents energy drain from battery when no source available (KEEP_ALIVE pin);
- Disables storage element charging (DIS_STO_CH pin).

Configuration by GPIO or I²C
- Easy setup;
- Basic settings at start-up with configuration pins;
- Advanced configuration with I²C (Fast Mode Plus).

Ultra-low power idle mode
- Stored energy is preserved when no source available.

Applications

Smart Home	Industrial Sensor
Smart Building	Retail
Edge IoT	PC Accessories



Description

The AEM0090x is a compact, fully integrated battery charger that harvests DC power to store energy in rechargeable batteries. It extends battery lifetime and removes the need for primary energy storage in a large range of applications.

Selecting the operating voltage allows the user to set a constant Maximum Power Point at which the AEM0090x operates, to charge a storage element, such as a Li-ion battery or a LiC. The boost converter operates with input voltages ranging from 120 mV to 2.73 V.

The AEM0090x has a unique cold-start circuit capable of operation with input voltages as low as 250 mV and a few micro Watts. The output voltages ranges from 2.5 V to 4.8 V, with configurable protection levels to prevent overcharging and overdischarging of the storage element. No external components are necessary to set these protection levels. Additionally, thermal monitoring safeguards the storage element, while an Average Power Monitoring system offers insights into the energy transfered to the storage element.

Thanks to the keep-alive feature, the AEM0090x internal circuit can stay powered by the storage element even in absence of a harvesting source. When keep-alive is disabled and no harvesting source is present, the AEM0090x turns off, preserving the energy of the storage element.

A shelf-mode can be obtained by disabling the keep-alive feature, thus, preventing the battery to be drained during device storage. Furthermore, enabling the DIS_STO_CH feature creates a shipping mode by preventing battery charging.

The AEM00900 application schematic is featuring small PCB size (51 mm²) and a global lower bill of material. The AEM00901 application schematic allows higher performance with a PCB area penalty as low as 6 mm², enabling small size and low cost implementation for single/dual element PV or pulsed sources versus other DCDC based solutions.

Device Information

Part Number	Package	Body size
10AEM00900C0002 10AEM00901C0002	QFN 28-pin	4x4mm

Evaluation Board

Part number
2AAEM00900C002
2AAEM00901C002

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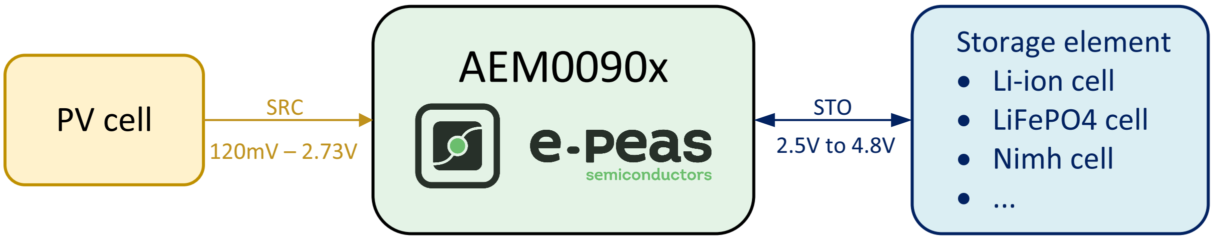


Figure 1: Simplified schematic view

1. Introduction

The AEM0090x is a full-featured energy efficient battery charger able to charge a storage element (connected to STO) from an energy source (connected to SRC).

The core of the AEM0090x is a regulated switching converter (boost) with high-power conversion efficiency.

At first start-up, as soon as a required cold-start voltage of 250 mV and a few micro Watts are available at the source (V_{STO} > 2.5 V), the AEM0090x coldstarts. After the cold start, the AEM extracts the power available from the source if the input voltage is higher than $V_{SRC,REG}$.

The AEM0090x can be fully configured through I²C or partially by configuration pins. I²C configuration is not mandatory, as the default configuration is made to fit the most common needs, along with the configuration pins for the most common settings.

Through I²C communication or through the configuration pins, the user can select a specific operating mode from a variety of modes that cover most application requirements without any dedicated external component. The battery protection thresholds (V_{OVCH} and V_{OVDIS}) can be configured with the help of the STO_CFG[2:0] pins. They can also be configured in 60 mV steps using the I²C bus.

Depending on the harvester, the source regulation voltage, $V_{SRC,REG}$, can be configured using six configuration pins (SRC_LVL_CFG[5:0]) or using I²C communication.

The ST_STO status pin provides information about the voltage level of the storage element, and thus about its readiness to supply an application. It can also be used to powergate an application circuit when sufficient energy is stored.

The AEM0090x features an optional temperature protection. It can be set through the I²C interface and allows to define a temperature range so that, when the ambient temperature is outside that range, battery charging is disabled. One additional resistor and one additional thermistor are needed for this feature.

The KEEP_ALIVE functionality sets the source from which the AEM0090x supplies its internal circuitry VINT. It can be supplied either from the harvester connected on SRC or from the battery connected to STO.

When KEEP_ALIVE is disabled, the AEM0090x internal circuitry is running as long as enough energy is available on SRC. If no energy is available on SRC, the internal voltage drops down to reset voltage and the AEM needs to go through a cold start before being able to charge the battery again. This is useful for applications with long periods without energy on SRC and when the I²C is not used. If the I²C communication is used, the AEM will need to be reconfigured after the cold-start. With this setting, only a few nA of quiescent current is taken from the storage element.

When KEEP_ALIVE is enabled, the AEM0090x is supplied by STO, the circuit stays in SUPPLY STATE or SLEEP STATE as long as the battery connected to STO is above the overdischarge threshold. It prevents losing the I²C configuration when energy harvesting is not occurring and offers faster reactivity as the AEM is not reset depending on the available energy on SRC.

2. Pin Configuration and Functions

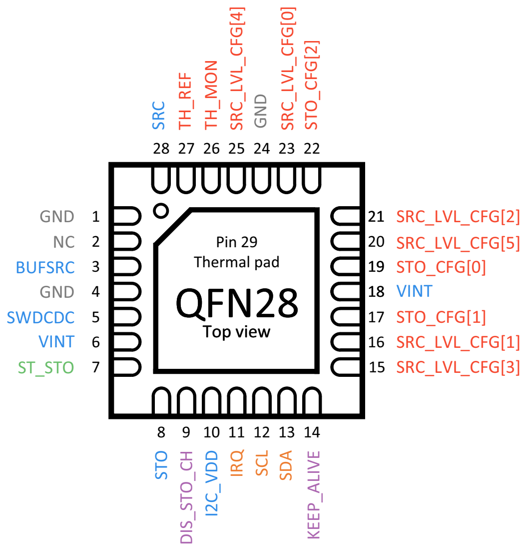


Figure 2: Pinout diagram QFN28

NAME	PIN NUMBER	Function
Power Pins		
SRC	28	Connection to the harvested energy source.
BUFSRC	3	Connection to an external capacitor buffering the boost converter input.
SWDCDC	5	Switching node of the boost converter.
VINT	6, 18	Internal supply voltage.
STO	8	Connection to the energy storage element (rechargeable only). Cannot be left floating, voltage must always be above 2.5 V.
I2C_VDD	10	Connection to supply the I²C interface. - Connect to a 1.5 V to 5.0 V power supply if I²C is used. - Connect to GND if I²C is not used.
Configuration Pins		
STO_CFG[0]	19	Used for the configuration of the threshold voltages for the energy storage element. Read as HIGH if left floating.
STO_CFG[1]	17	
STO_CFG[2]	22	
SRC_LVL_CFG[0]	23	Used for the configuration of the source voltage level. Read as HIGH if left floating.
SRC_LVL_CFG[1]	16	
SRC_LVL_CFG[2]	21	
SRC_LVL_CFG[3]	15	
SRC_LVL_CFG[4]	25	
SRC_LVL_CFG[5]	20	
TH_REF	27	Reference voltage for thermal monitoring. Leave floating if not used.
TH_MON	26	Pin for temperature monitoring. Connect to VINT if not used.
Control Pins		
DIS_STO_CH	9	When HIGH, the AEM stops charging the battery. Read as LOW if left floating.
KEEP_ALIVE	14	When HIGH, the internal circuitry is supplied from STO. When LOW, the internal circuitry is supplied from SRC. Read as HIGH if left floating.

Table 1: Pins description

NAME	PIN NUMBER	Function
I²C Pins		
SDA	13	Bidirectional data line. Connect to I2C_VDD if not used.
SCL	12	Unidirectional serial clock for I²C. Connect to I2C_VDD if not used.
IRQ	11	Output Interrupt request. Leave floating if not used.
Status Pin		
ST_STO	7	Logic output. - Rises when V_{STO} is above V_{OVDIS} + 100 mV. - Falls after V_{STO} is held under V_{OVDIS} for 2.5 s. - Logic HIGH is V_{STO}. Leave floating if not used.
Other pins		
GND	1, 4, 24, 29 (thermal pad)	Ground connection, each terminal should be strongly tied to the PCB ground plane, pin 29 (thermal pad) being the main GND connection of the AEM0090x.
NC	2	Not connected pin, leave floating.

Table 1: Pins description

3. Specifications

3.1. Absolute Maximum Ratings

Parameter	Value
Voltage on SWDCDC, STO, I2C_VDD, SDA, SCL, IRQ, ST_STO, DIS_STO_CH	5.5 V
Voltage on SRC, BUFSRC	3 V
Voltage on VINT, KEEP_ALIVE STO_CFG[2:0], SRC_LVL_CFG[5:0], TH_REF, TH_MON	2.75 V
Operating junction temperature	-40°C to 85°C
Storage temperature	-40°C to 150°C
ESD HBM voltage JEDEC JS-001-2023	2000 V ± 5 % Class-2
ESD CDM voltage JEDEC JS-002-2022	1000 V ± 5 % C2b

Table 2: Absolute maximum ratings

3.2. ESD Ratings

Parameter		Value	Unit
Electrostatic discharge V_{ESD}	Human-Body Model (HBM)[1]	± 2000	V
	Charged-Device Model (CDM)[2]	± 1000	V

Table 3: ESD ratings

1. ESD Human-Body Model (HBM) value tested according to JEDEC standard JS-001-2023.
2. ESD Charged-Device Model (CDM) value tested according to JEDEC standard JS-002-2022.

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality

3.3. Thermal Resistance

Package	θJA	θJC	Unit
QFN-28	47	4.5	°C/W

Table 4: Thermal data

3.4. Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
$P_{SRC,CS}$	Minimum source power required for cold start[1]	During cold start: AEM00900		2.47		µW
		During cold start: AEM00901		3.99		µW
$V_{SRC,CS}$	Minimum source voltage required for cold start			0.25		V
$V_{SRC,REG}$	Target regulation voltage of the source (depending on SRC_LVL_CFG[5:0] configuration or I²C register)		0.12		2.73	V
V_{OC}	Open-circuit voltage of the source				3.0	V
Timing						
$T_{STO,SUPPLY}$	Time between two V_{STO} evaluations in SUPPLY STATE			0.12		s
$T_{STO,SLEEP}$	Time between two V_{STO} evaluations in SLEEP STATE			0.96		s
$T_{GPIO,MON}$	Time between two GPIO state evaluations			1.92		s
$T_{DIS\_STO\_CH,MON}$	Time between two DIS_STO_CH IO state evaluations			1.00		s
$T_{TEMP,MON}$	Time between two temperature evaluations			7.67		s
T_{CRIT}	Time spent in SHUTDOWN STATE with V_{STO} below V_{OVDIS} before switching to OVDIS STATE			2.50		s
Storage Element						
V_{STO}	Voltage on the storage element		2.5		4.8	V
V_{OVCH}	Voltage above which the storage element is considered fully charged and must not be charged any further.		2.7	See section 6.3	4.8	V
V_{OVDIS}	Voltage below which the storage element is considered fully depleted, and must not be discharged any further.		2.5		4.05	V
Internal supply & Quiescent Current						
V_{INT}	Internal supply voltage	Auto-regulated, outside of reset and coldstart conditions.		2.2		V
$V_{INT,CS}$	Internal supply cold-start voltage	Minimum voltage on VINT to allow the AEM0090x to switch from RESET STATE to SENSE STO STATE.		2.3		V
$V_{INT,RESET}$	Internal supply reset voltage	Minimum voltage on VINT before switching to RESET STATE (from any other state).		2.0		V
$I_{QSUPPLY}$	Quiescent current on STO in SUPPLY STATE	V_{STO} = 3.7 V		242		nA
I_{QSLEEP}	Quiescent current on STO in SLEEP STATE	V_{STO} = 3.7 V		162		nA
I_{QSTO}	Quiescent current on STO when Keep-alive functionality is disabled			7.4		nA
I²C interface						
Bus frequency				400	1000	kHz
V_{I2C_VDD}	I²C interface supply pin voltage		1.5		5.0	V
SCL	I²C interface communication pins		Pull-up to I2C_VDD with resistors			
SDA						

Table 5: Electrical characteristics

1.These values are valid with the recommended BOM components (see Section 12)

3.5. Recommended Operation Conditions

Symbol	Parameter		Min	Typ	Max	Unit
External Components						
L_{DCDC}	Inductor of the boost converter	AEM00900	3.3	6.8		µH
		AEM00901	6.8	33	47	
C_{SRC}	Capacitor decoupling the BUFSRC terminal		10			µF
C_{INT}	Capacitor decoupling V_{INT}		3.3			µF
C_{STO}	Capacitor decoupling the STO terminal[1]		5	22		µF
R_{DIV}	Optional - pull-up resistor for the thermal monitoring		5k	22k	33k	Ω
R_{TH}	Optional - NTC thermistor for the thermal monitoring	R0		10k		Ω
		Beta		3380		K
R_{SCL} R_{SDA}	Optional - pull-up resistors for the I²C interface			1k		Ω
Logic input Pins						
SRC_LVL_CFG[5:0]	Configuration pins for the SRC voltage level	Logic HIGH	Connect to VINT			
		Logic LOW	Connect to GND			
STO_CFG[2:0]	Configuration pins for the storage element thresholds	Logic HIGH	Connect to VINT			
		Logic LOW	Connect to GND			
KEEP_ALIVE	Configuration for the “keep-alive” functionality	Logic HIGH	Connect to VINT			
		Logic LOW	Connect to GND			
DIS_STO_CH	Configuration for disabling the charging of the battery	Logic HIGH	Connect to STO			
		Logic LOW	Connect to GND			

Table 6: Recommended operating conditions

1.Decoupling capacitor of at least 5µF is required to avoid damaging the AEM. The decoupling capacitor is to be sized according to the storage element internal resistance (ESR) to ensure optimal efficiency of the DCDC converter. It is recommended to use a capacitor of at least 22 µF when measuring the AEM0090x efficiency with laboratory equipment such as source measurement units (SMU).

3.6. Typical Characteristics

3.6.1. Boost Converter Efficiency

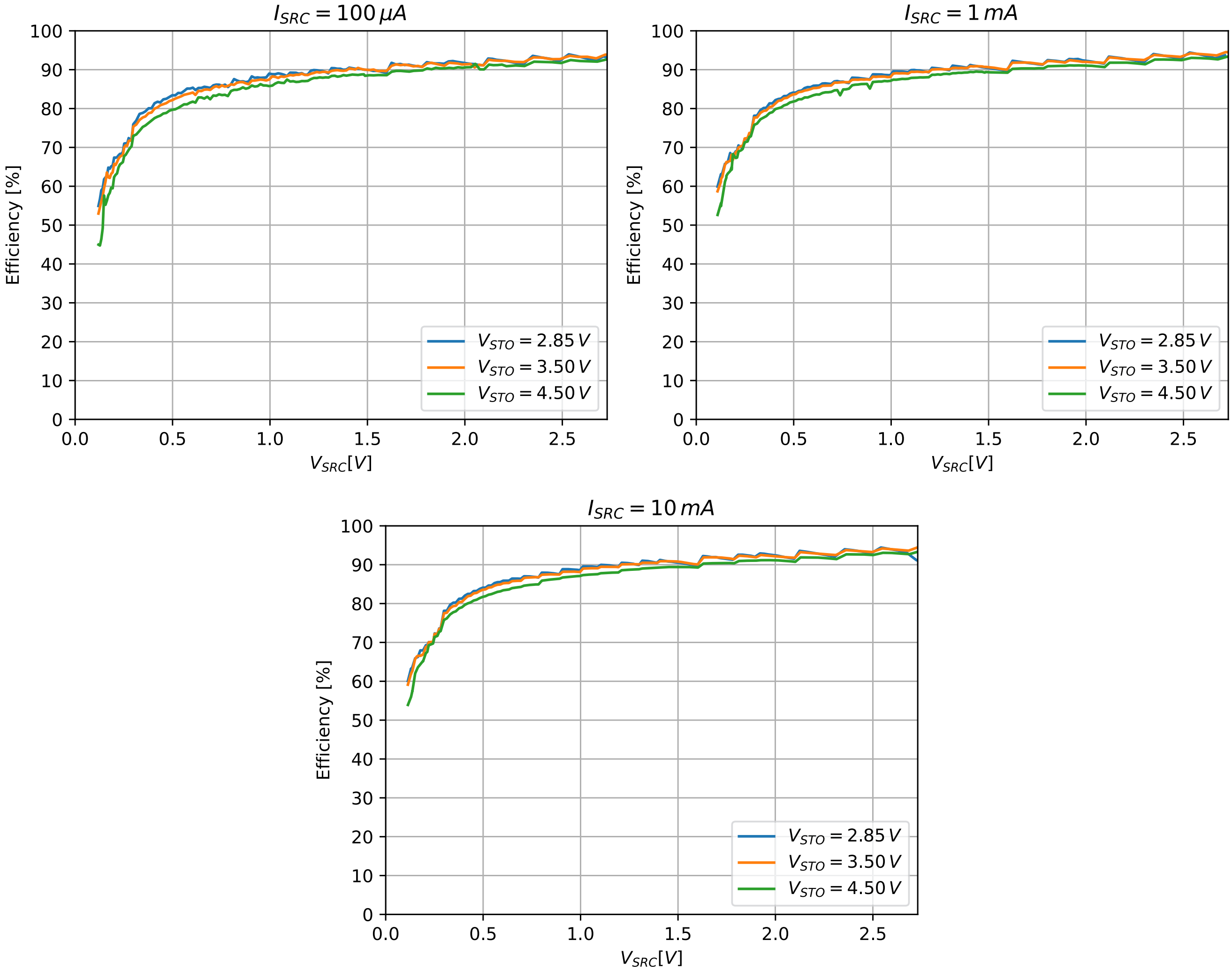


Figure 3: AEM00900 DCDC conversion efficiency (L_{DCDC}: TDK VLS252012HBX-6R8M-1)

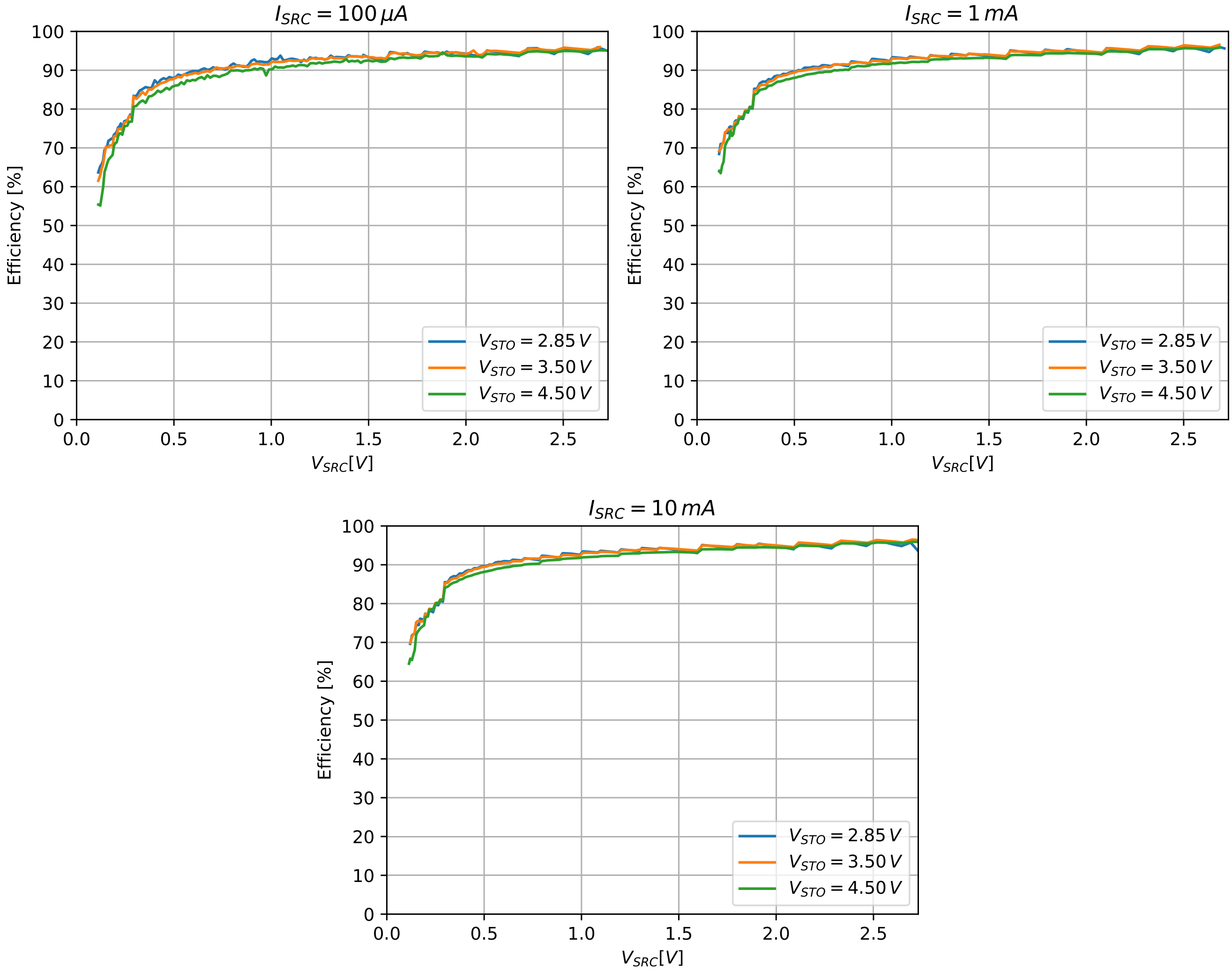


Figure 4: AEM00901 DCDC conversion efficiency (L_{DCDC}: Coilcraft LPS4018-333MRB)

3.6.2. Quiescent Current

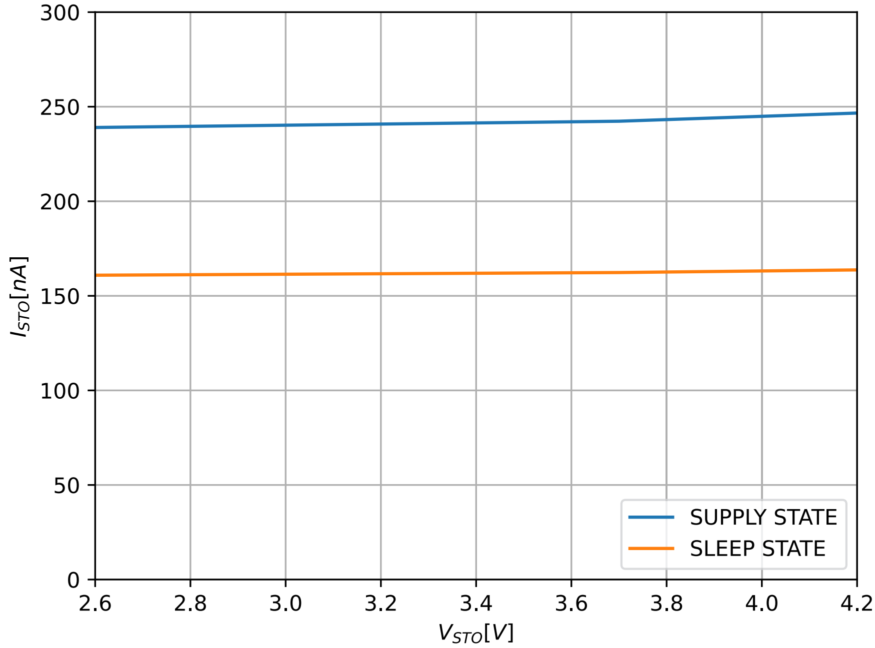


Figure 5: Quiescent current

4. Functional Block Diagram

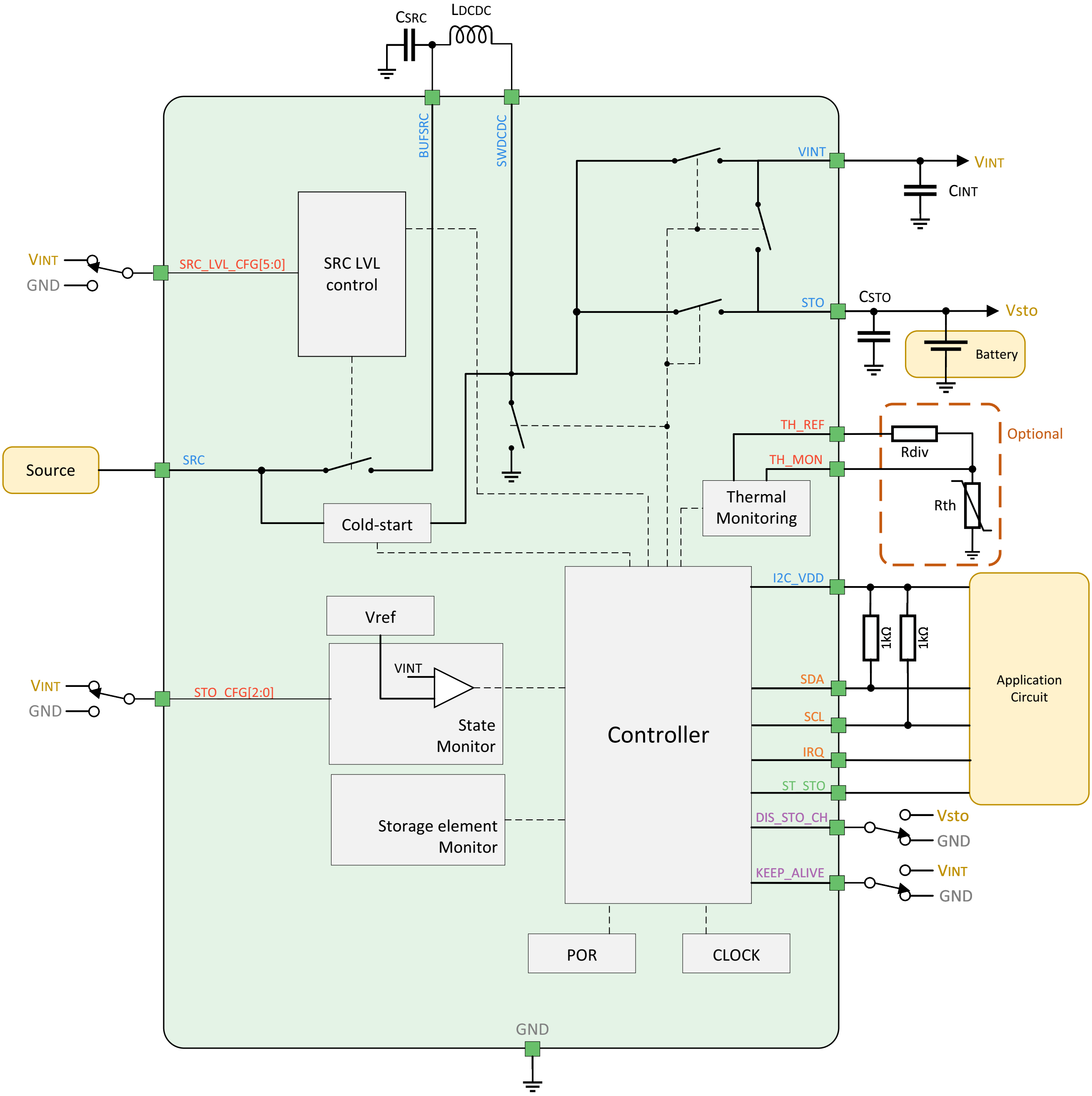


Figure 6: Functional block diagram

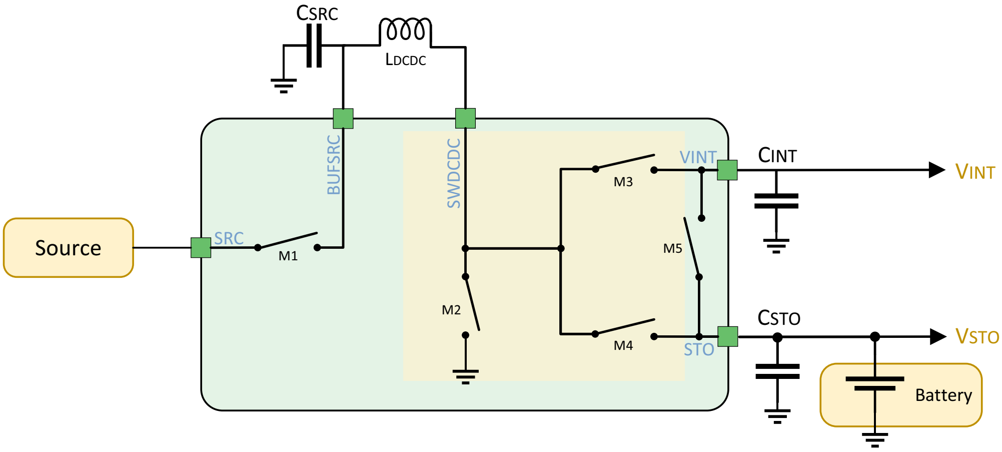


Figure 7: Simplified schematic view of the AEM0090x

5. Theory of Operation

5.1. Boost Converter

The boost (step-up) converter raises the voltage available at BUFSRC to a level suitable for charging the storage element, in the range of 2.5 V to 4.8 V, according to the system configuration. The switching transistors of the boost converter are M2, M3 and M4. The reactive power component of this converter is the external inductor L_{DCDC}.

When the boost converter is extracting energy from SRC, M1 is closed. BUFSRC is decoupled by the capacitor C_{SRC}, which smoothens the voltage against the current pulses induced by the boost converter.

The storage element is connected to STO pin, whose voltage is V_{STO}. This node is linked to the output of one of the high-side transistors (M4) of the boost converter. When energy harvesting is occurring, the boost converter charges the battery. If V_{INT} drops below its regulation value and if the Keep-alive functionality is disabled, the AEM uses M3 instead of M4 as the high-side transistor of the boost converter until V_{INT} reaches its target plus a small hysteresis. If the Keep-alive functionality is enabled, V_{INT} is instead supplied from STO by modulating the gate of M5. In that case M3 is never used.

5.2. Source Voltage Regulation

During SUPPLY STATE, the voltage on SRC is regulated to a voltage configured by the user. The AEM0090x offers a large choice of values for the source voltage. If the open-circuit voltage of the harvester is lower than $V_{SRC,REG}$, the AEM0090x does not extract the power from the source. If the SRC voltage is higher, the AEM0090x regulates V_{SRC} to $V_{SRC,REG}$ and extracts power.

5.3. Thermal Monitoring

Thermal monitoring allows to protect the storage element by disabling the charge of the storage element and setting the STATUS.TEMP register when the temperature is outside of the defined temperature range. Enabling this functionality requires the use of a resistor (R_{DIV}) and a thermistor (R_{TH}). See Figure 8 for external components connections. The TH_REF terminal allows a reference voltage to be applied to the resistive divider while TH_MON is the measuring point. An ADC is measuring the voltage on TH_MON between 0 and 1 V. The temperature evaluation is done periodically ($T_{TEMP,MON}$) to spare power. Information for the thermal monitoring is described in Section 9.5. Thermal monitoring is optional, if not used connect TH_MON to VINT and leave TH_REF floating.

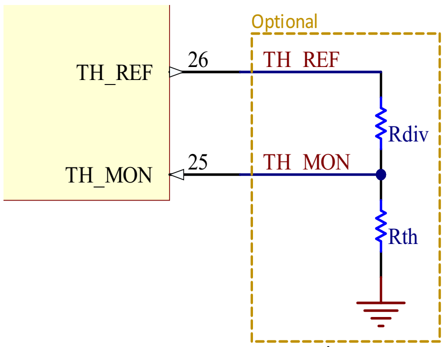


Figure 8: TH_REF and TH_MON connections

5.4. Average Power Monitoring

The Average Power Monitoring (APM) allows to evaluate the energy transfer from SRC to STO. The APM is evaluated on the storage element side, so it takes into account the efficiency of the boost converter.

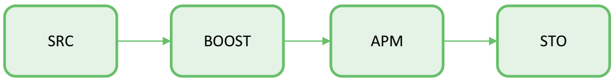


Figure 9: APM in the power chain

The APM is able to determine the transferred energy by counting the number of current pulses transferred to STO by the boost converter over a configurable time window, and thus, evaluate the corresponding energy.

Two modes are available: Pulse Counter Mode and Power Meter Mode.

The APM behavior is described in Figure 10:

- Phase A:
  - Pulse Counter Mode: APM counts the number of DCDC pulses happening during T_A
  - Power Meter Mode: APM integrates the energy transferred from SRC to STO during T_A
- Phase B: APM waits during $T_B = T_A$
- IRQ: a rising edge is triggered on the IRQ pin, if IRQEN.APMDONE field is set to 1 (see Section 9.9 and Section 9.11). A rising edge on IRQ along with the IRQFLAG.APMDONE field set to 1 indicates to the user that a new value is available and ready to be read in the APM Data Register (Section 9.13).

Refer to Sections 9.8. and 9.13 for further details about how to set modes, how to convert registers value to Joule and how to set T_A.

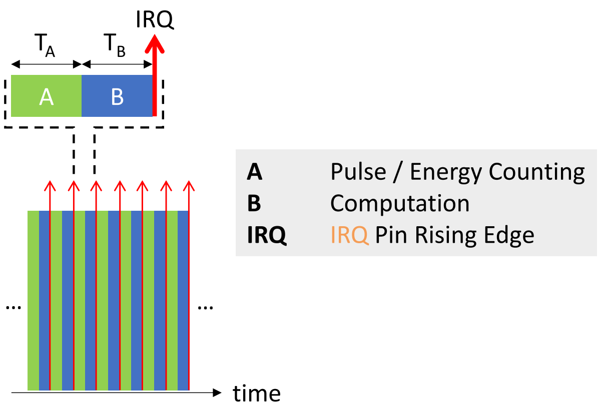


Figure 10: Average Power Monitoring behavior

5.5. Automatic High-power Mode

When the AEM detects that the energy available on SRC is high enough, the boost converter automatically switches to high-power mode, increasing the harvesting current capability at the price of a slight efficiency degradation.

Preventing the AEM to switch to high-power mode may allow to use an inductor with half peak current rating for L_{DCDC} (see Section 6.5.2). On the other hand, allowing the AEM to switch to high-power mode increases the maximum current that the AEM can harvest from SRC to STO.

Automatic high-power mode is enabled by default and can be disabled by setting the PWR.HPEN to 0 through the I²C interface.

5.6. Keep-alive

The internal circuitry connected to VINT can be supplied either by SRC through the boost converter (keep-alive disabled), or by the battery STO (keep-alive enabled).

When the keep-alive feature is disabled, the AEM0090x is supplied from SRC. The AEM will switch to RESET STATE if the energy on SRC is not sufficient.

When the keep-alive feature is enabled, the AEM0090x is supplied from STO. V_{INT} is regulated as long as $V_{STO} > V_{OVDIS}$. The keep-alive feature allows to maintain the I²C registers configuration and therefore preventing the loss of volatile memory. Referring to Table 5, the quiescent current is then $I_{QSUPPLY}$ or I_{QSLEEP}, depending on whether the AEM0090x is in SUPPLY STATE or in SLEEP STATE.

5.7. IRQ Pin

The IRQ pin allows user to get notified when various events happen (rising edge on IRQ pin). At start-up, the only flag that is enabled is I2CRDY, allowing the user to know when the AEM0090x has finished to coldstart and thus, is out of RESET STATE and is ready to be programmed through I²C. Other flags can be enabled by writing the IRQEN register (Section 9.9). When the IRQ pin shows a rising edge, the flags can be determined by reading the IRQFLG register (Section 9.11). Reading the IRQFLG register will reset the IRQ pin and clear the IRQFLG register.

5.8. State Description

NOTE: Unless stated otherwise, all values given in this section are typical.

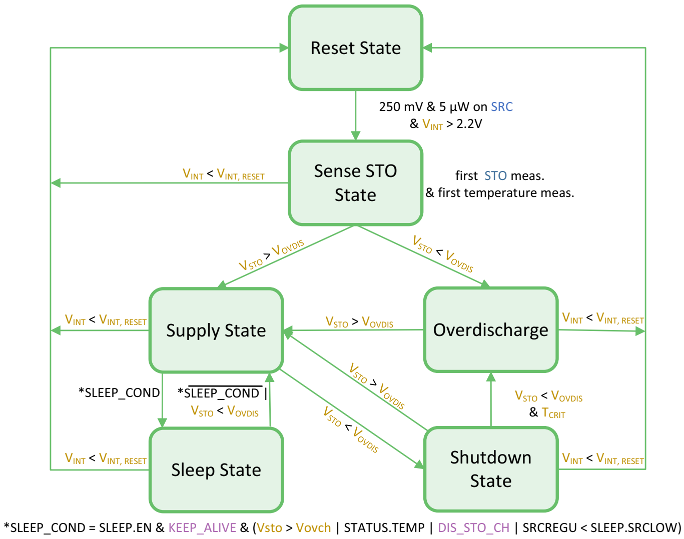


Figure 11: Diagram of the AEM0090x state machine

5.8.1. Reset State

In RESET STATE all nodes are deeply discharged and there is no available energy to be harvested, ST_STO is LOW. The AEM stays in this state until the source connected to SRC meets the cold start requirements long enough to make V_{INT} rise up to 2.3 V.

When V_{INT} has reached 2.3 V, the AEM0090x reads the configuration pins and switches to SENSE STO STATE. ST_STO stays LOW.

5.8.2. Sense STO State

In SENSE STO STATE the AEM0090x does the following measurements in order to know if the charging condition of the battery are met:

- Battery voltage on STO;
- Temperature through pins TH_MON and TH_REF (see Section 5.3. and 9.5.).

In this state, ST_STO is LOW. Once the measurements are done, if V_{STO} > V_{OVDIS}, the AEM0090x switches to SUPPLY STATE. Else, it switches to OVDIS STATE.

5.8.3. Supply State

In SUPPLY STATE, the AEM transfers charges directly from SRC to STO while maintaining V_{INT}. When coming from SENSE STO STATE with V_{STO} > V_{OVDIS}, ST_STO is LOW until V_{STO} is above V_{OVDIS} + 100 mV. Then ST_STO stays HIGH as long as the AEM does not go into OVDIS STATE.

If V_{INT} drops below $V_{INT,RESET}$ and the energy available on SRC is not sufficient to make V_{INT} rise again, there are two possible behaviors, depending on the keep-alive feature:

- If keep-alive is enabled, V_{INT} is supplied by the battery through M5, so the AEM0090x stays in SUPPLY STATE while energy is available on the battery;
- If keep-alive is disabled, V_{INT} will no longer be maintained and the AEM switches to RESET STATE.

5.8.4. Sleep State

In SLEEP STATE, the AEM power consumption is reduced. This mode may be used when the power available on the input is presumably low.

The AEM0090x enters sleep mode when the following conditions are met:

- Field SLEEP.EN in the SLEEP register is set to 1 and SRCREGU.VALUE register value is set below SLEEP.SRCLOW (I²C).
- Temperature is out of range.
- V_{STO} ≥ V_{OVCH}.
- DIS_STO_CH is HIGH.

5.8.5. Shutdown State

The AEM goes in SHUTDOWN STATE whenever V_{STO}<V_{OVDIS}. If V_{STO} < V_{OVDIS} for more than T_{CRIT}, the AEM goes in OVDIS STATE. If V_{STO} rises again above V_{OVDIS} before T_{CRIT} passed, the AEM goes back in SUPPLY STATE. ST_STO remains HIGH while in SHUTDOWN STATE.

The SHUTDOWN STATE is used to prevent the AEM from going in OVDIS STATE if there is a sudden current draw on the battery coming from the application circuit, causing the battery voltage to drop momentarily.

5.8.6. Overdischarge State

In OVDIS STATE, the AEM transfers charges directly from SRC to STO while maintaining V_{INT} from SRC. The AEM is no longer supplied from the storage element. In this state, ST_STO is LOW. If the source no longer provides energy to the AEM, it will go into RESET STATE.

6. System Configuration

6.1. Configuration Pins and I²C

6.1.1. Configuration Pins

After a cold start, the AEM0090x reads the configuration GPIOs. Those are then read periodically every $T_{GPIO,MON}$, with the exception of the DIS_STO_CH pin that is read every $T_{DIS\_STO\_CH,MON}$. The configuration pins can be changed on-the-fly and the corresponding configuration will be updated at the next IO reading. The floating configuration pins are read as HIGH, except DIS_STO_CH which is read as LOW.

6.1.2. Configuration by I²C

To configure the AEM0090x through the I²C interface after a cold start, the user must wait for the IRQ pin to rise, showing that the AEM0090x is out of RESET STATE and is ready to communicate with I²C. The interrupt is reset by reading its IRQFLG register. Please note that the IRQ pin is always low during RESET STATE. See Section 9.11 for further informations about the IRQ pin.

Once IRQ goes HIGH, the user can then write to the desired registers and validate the configuration by setting the CTRL.UPDATE register field. All configuration pins are then ignored (with the exception of DIS_STO_CH, see Section 9.6) and all the configurations are set by the register values. All registers have a reset value, that can be found in Table 9. It is possible to go back to the GPIO configuration by resetting the CTRL.UPDATE bit. To apply any modification to the configuration, simply change the wanted registers value and set the CTRL.UPDATE bit again.

Registers are stored in a volatile memory, so their value are lost when V_{INT} drops below the reset voltage ($V_{INT,RESET}$), making the AEM0090x switch to RESET STATE. Thus, when using the I²C configuration, it is highly recommended to enable the keep-alive (see section 5.6.). If keep-alive functionality is disabled, register configuration is lost every time the energy available on SRC is not sufficient to maintain V_{INT} above the reset voltage ($V_{INT,RESET}$).

6.2. Source Level Configuration

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
L	L	L	H	H	L	0.12 V[1]
L	L	L	H	H	H	0.13 V
L	L	H	L	L	L	0.15 V
L	L	H	L	L	H	0.16 V
L	L	H	L	H	L	0.18 V
L	L	H	L	H	H	0.19 V
L	L	H	H	L	L	0.21 V
L	L	H	H	L	H	0.22 V
L	L	H	H	H	L	0.24 V
L	L	H	H	H	H	0.25 V
L	H	L	L	L	L	0.27 V
L	H	L	L	L	H	0.28 V
L	H	L	L	H	L	0.30 V
L	H	L	L	H	H	0.33 V
L	H	L	H	L	L	0.36 V
L	H	L	H	L	H	0.39 V
L	H	L	H	H	L	0.42 V
L	H	L	H	H	H	0.45 V
L	H	H	L	L	L	0.48 V
L	H	H	L	L	H	0.51 V
L	H	H	L	H	L	0.54 V
L	H	H	L	H	H	0.57 V
L	H	H	H	L	L	0.60 V
L	H	H	H	L	H	0.63 V
L	H	H	H	H	L	0.66 V
L	H	H	H	H	H	0.69 V
H	L	L	L	L	L	0.72 V
H	L	L	L	L	H	0.75 V
H	L	L	L	H	L	0.78 V

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
H	L	L	L	H	H	0.81 V
H	L	L	H	L	L	0.84 V
H	L	L	H	L	H	0.90 V
H	L	L	H	H	L	1.00 V
H	L	L	H	H	H	1.05 V
H	L	H	L	L	L	1.10 V
H	L	H	L	L	H	1.14 V
H	L	H	L	H	L	1.20 V
H	L	H	L	H	H	1.25 V
H	L	H	H	L	L	1.29 V
H	L	H	H	L	H	1.35 V
H	L	H	H	H	L	1.40 V
H	L	H	H	H	H	1.44 V
H	H	L	L	L	L	1.50 V
H	H	L	L	L	H	1.59 V
H	H	L	L	H	L	1.66 V
H	H	L	L	H	H	1.70 V
H	H	L	H	L	L	1.79 V
H	H	L	H	L	H	1.90 V
H	H	L	H	H	L	1.99 V
H	H	L	H	H	H	2.10 V
H	H	H	L	L	L	2.19 V
H	H	H	L	L	H	2.25 V
H	H	H	L	H	L	2.32 V
H	H	H	L	H	H	2.41 V
H	H	H	H	L	L	2.50 V
H	H	H	H	L	H	2.59 V
H	H	H	H	H	L	2.68 V
H	H	H	H	H	H	2.73 V

Table 7: Configuration of SRC_LVL_CFG[5:0]

1.The default value of the SLEEP.SRCLOW being 0.12 V, the AEM0090x may enter SLEEP STATE if the SLEEP conditions are met. To prevent this, reset the SLEEP.EN register.

The source voltage regulation can be configured using GPIO or I²C communication.

Six dedicated configuration pins, SRC_LVL_CFG[5:0], allow selecting the $V_{SRC,REG}$ at which the source regulates its voltage. All configurations set below SRC_LVL_CFG[5:0] = LLLHHL will be set at 0.12 V.

The I²C communication allows more precision than the GPIO configuration (see Section 9.2), as SRCREGU.VALUE (0x01) is a 7-bit register.

6.3. Storage Element Thresholds Configuration

The user must set the voltage thresholds for which the storage element is considered to be discharged (V_{OVDIS}) and fully charged (V_{OVCH}). Note that the ST_STO pin is asserted when V_{STO} gets 100 mV above the V_{OVDIS} level.

V_{OVDIS} is configured on the VOVDIS (0x02) register and encoded on 6 bits. The value to be written to the register is determined using the following equation:

$$\mathrm{THRESH} = \frac{V_{OVDIS} - 0.50625}{0.05625}$$

THRESH is the integer value to be written in the register. The minimum value for V_{OVDIS} is 2.5 V. If the register value corresponds to V_{OVDIS} < 2.5 V, the threshold voltage is forced to 2.5 V.

V_{OVCH} is configured on the VOVCH (0x03) register and encoded on 6 bits. The value to be written to the register is determined using the following equation:

$$\mathrm{THRESH} = \frac{V_{OVCH} - 1.2375}{0.05625}$$

THRESH is the integer value to be written in the register. The minimum value for V_{OVCH} is 2.7 V. If the register value corresponds to V_{OVCH} < 2.7 V, the threshold voltage is forced to 2.7 V.

It is also possible to configure V_{OVDIS} and V_{OVCH} with configuration pins STO_CFG[2:0] as shown in Table 8.

Configuration			Storage element threshold		Storage element type
STO_CFG[2:0]			V_{OVCH}	V_{OVDIS}	
L	L	L	4.50 V	3.30 V	NiCd 3 cells
L	L	H	4.00 V	2.80 V	Tadrian TLI1020A
L	H	L	3.63 V	2.80 V	LiFePO4
L	H	H	3.90 V	2.80 V	Tadrian HLC1020
H	L	L	3.80 V	2.50 V	LIC
H	L	H	3.90 V	3.01 V	Li-ion (long life)
H	H	L	4.35 V	3.01 V	LiPo
H	H	H	4.12 V	3.01 V	Li-ion/solid-state/NiMH 3 cells

Table 8: Usage of STO_CFG[2:0]

DISCLAIMER: the provided storage element thresholds in the table above are indicative to support a wide range of storage element variants. They are provided as is to the best knowledge of e-peas's application laboratory. They should not replace the actual values provided in the storage element manufacturer's specifications and datasheet.

6.4. Disable Storage Element Charging

Pulling up DIS_STO_CH to V_{STO} disables the charging of the storage element connected to STO. The storage element charging can also be disabled via I²C by setting the PWR.STOCHDIS register. Pulling up DIS_STO_CH overtakes the PWR.STOCHDIS register configuration.

Please note that, if the keep-alive feature is enabled by pulling up KEEP_ALIVE to V_{INT}, VINT is supplied by STO regardless of the setting of DIS_STO_CH. To make sure that the storage element is neither charged nor used to supply VINT, user must tie both DIS_STO_CH to STO and KEEP_ALIVE to GND.

6.5. External Components

6.5.1. Storage Element

The storage element of the AEM0090x must be a rechargeable battery, which size should be chosen so that its voltage does not fall below V_{OVDIS} for longer than 2.5 s during current draw from the battery to the load connected on it. To keep the chip functionality, minimum voltage on STO pin shall remain above 2.5V.

The monitoring of the storage element is done periodically. It is therefore possible that the storage element may be overloaded if it is incorrectly sized.

It is mandatory to buffer the battery with a capacitor C_{STO} if the internal resistance of the battery is high, to ensure that the current pulled from the battery by the application circuit does not ever make the battery voltage fall below 2.5 V.

If a disconnection of the battery is expected (e.g. because of a user removable connector), the PCB must include a decoupling capacitor to avoid over-voltage and under-voltage during that battery disconnection. The minimum effective value of this capacitor is 5 µF.

A minimal decoupling capacitor of 22 µF is recommended to obtain optimal DCDC converter efficiency when using high ESR battery, or when measuring efficiency using laboratory equipments such as source measurement units (SMU).

6.5.2. External Inductor Information

L_{DCDC}

The AEM0090x operates with one standard miniature inductor. L_{DCDC} must comply to the following:

- Peak current rating must be at least 1 A for a 3.3 µH inductor in high-power mode and 500 mA if high-power mode is disabled. Current rating decreases linearly when inductor value increases.
- Switching frequency must be at least 10 MHz.
- ESR as low as possible as it has a strong influence on DCDC efficiency.
- The recommended values for optimal efficiency is:
  - 6.8 µH for AEM00900
  - 33 µH for AEM00901

6.5.3. External Capacitors Information

C_{SRC}

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage variations when the buck-boost converter is active. The recommended value is 22 µF.

C_{INT}

This capacitor acts as an energy buffer for the internal voltage supply. The minimum effective value is 3.3 µF. 22µF is recommended.

C_{STO}

This capacitor allows for buffering the current peaks of the boost converter output. While it is mandatory to connect a capacitor of minimum 5 µF to avoid damaging the AEM, it is recommended to use a capacitor with at least 22µF (real value, including derating, tolerance, etc.) to ensure best efficiency from the boost converter if the storage element has high internal series resistance (ESR).

6.5.4. Optional External Components for Thermal Monitoring

The following components are required for the thermal monitoring:

- One resistor, typ. 22 kΩ
- One NTC thermistor, typ. R0 = 10 kΩ ±5% and Beta = 3380 K ±3% (NCP15XH103J03RC)

6.5.5. Optional Pull-up Resistors for the I²C Interface

SDA and SCL must be pulled up by resistors (1 kΩ typical) if the I²C interface is used. The value must be determined according to the I²C mode used.

7. I²C Serial Interface Protocol

The AEM0090x uses I²C communication for configuration as well as to provide information about system status and measurement data. Communication requires a serial data line (SDA) and a serial clock line (SCL). A device sending data is defined as a transmitter and a device receiving data as a receiver. The device that controls the communication is called a master and the device it controls is defined as the slave.

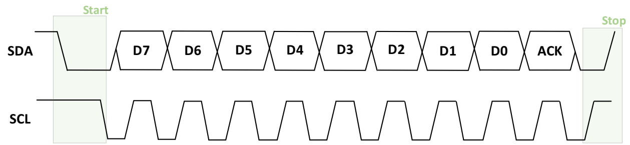


Figure 12: I²C transmission frame

The master is in charge of generating the clock, managing bus accesses and generating the start and stop bits. The AEM0090x is a slave that will receive configuration data or send the informations requested by the master.

The AEM0090x supports I²C Standard-mode (100 kHz maximum clock rate), Fast-mode (400 kHz maximum clock rate), and Fast-mode Plus (1 MHz maximum clock rate) device. Data are sent with the most significant bit first.

Here are some typical I²C interface states:

- When the communication is idle, both transmission lines are pulled up (SDA and SCL are open drain outputs);
- Start bit (S): to initiate the transmission, the master switches the SDA line low while keeping SCL high. This is called the start bit;
- Stop bit (P): to end the transmission, the master switches the SDA line from low to high while keeping SCL high. This is called a stop bit;
- Repeated Start bit (Sr): it is used as a back-to-back start and stop bit. It is similar to a start condition, but when the bus is not on idle;
- ACK: to acknowledge a transmission, the device receiving the data (master in case of a read mode transmission, slave in case of a write mode transmission) switches SDA low;
- NACK: when the device receiving data keeps SDA high after the transmission of a byte. When reading a byte, this can mean that the master is done reading bytes from the slave.

To initiate the communication, the master sends a byte with the following informations:

- Bits [7:1] is the slave address, which is 0x41;
- Bit [0] is the communication mode: 1 for 'read mode' (used when the master reads informations from the slave) and 0 for 'write mode' (when the master writes informations to the slave);
- Slave replies with an ACK to acknowledge that the address has been successfully transmitted.

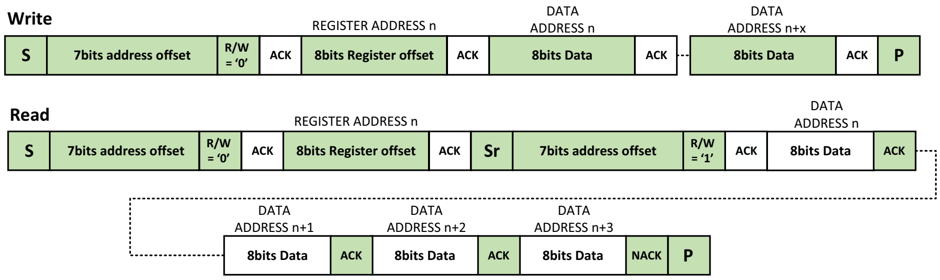
Here is the procedure for the master to write a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be written. For example, for the TEMPCOLD register, the master sends the value 0x04;
- Slave sends an ACK;
- Master sends the data to write to the register;
- Slave sends an ACK;
- If the master wants to write a register at the next address (TEMPHOT in our example), it sends next value to write, without having to specify the address again. This can be done several times in a row for writing several consecutive registers;
- Else the master sends a stop bit (P).

Here is the procedure for the master to read a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be read. For example, for the SRC_REGU register, the master sends the value 0x01;
- Slave sends an ACK;
- Master sends a repeated start bit (Sr);
- Master sends the address of the slave in 'read' mode;
- Slave sends an ACK;
- Master provides the clock on SCL to allow the slave to shift the data of the read register on SDA;
- If the master wants to read register at the next address (VOVDIS in our example), it sends an ACK and provides the clock for the slave to shift its following 8 bits of data. This can be done several times in a row for reading several registers;
- If the master wants to end the transmission, it sends a NACK to notify the slave that the transmission is over, and then sends a stop bit (P).

Both communications are described in the Figure 13. Refer to Table 9 for all register addresses.



S = START
ACK = ACKNOWLEDGE
P = STOP

R/W = READ/WRITE
NACK = NOT ACKNOWLEGDE
Sr = RESTART

Figure 13: Read and write transmission

8. Registers Map

Address	Name	Bit	Field Name	Access	Reset	Description
0x00	VERSION	[7:0]	VERSION	R	-	Version number.
0x01	SRCREGU	[7:0]	VALUE	R/W	0x77 (1.54V)	Source voltage regulation level.
0x02	VOVDIS	[5:0]	THRESH	R/W	0x2D (3.04V)	Storage element overdischarge threshold.
0x03	VOVCH	[5:0]	THRESH	R/W	0x33 (4.1V)	Storage element overcharge threshold.
0x04	TEMPCOLD	[7:0]	THRESH	R/W	0x8F (0°C)	Cold temperature level threshold.
0x05	TEMPHOT	[7:0]	THRESH	R/W	0x2F (45°C)	Hot temperature level threshold.
0x06	PWR	[0:0]	KEEPALEN	R/W	0x01	Keep-alive enable.
		[1:1]	HPEN	R/W	0x01	High-power mode enable.
		[2:2]	TMONEN	R/W	0x01	Temperature monitoring enable.
		[3:3]	CHARGEDIS	R/W	0x00	Storage element charging disable.
0x07	SLEEP	[0:0]	EN	R/W	0x01	Sleep mode enable.
		[3:1]	SRCLOW	R/W	0x00	SRC LOW threshold.
0x08	RSVD	[7:0]	-	R/W	-	This register can be written in but it will have no effect.
0x09	APM	[0:0]	EN	R/W	0x00	APM enable.
		[1:1]	MODE	R/W	0x00	APM mode
		[3:2]	WINDOW	R/W	0x00	APM computation window
0x0A	IRQEN	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable.
		[1:1]	VOVDIS	R/W	0x00	IRQ STO OVDIS enable.
		[2:2]	VOVCH	R/W	0x00	IRQ STO OVCH enable.
		[3:3]	SRCLOW	R/W	0x00	IRQ SRC LOW enable.
		[4:4]	TEMP	R/W	0x00	IRQ temperature enable.
		[5:5]	APMDONE	R/W	0x00	IRQ APM done enable.
		[6:6]	APMERR	R/W	0x00	IRQ APM error enable.
0x0B	CTRL	[0:0]	UPDATE	R/W	0x00	Load I²C registers configuration.
		[1:1]	-	R	0x00	Reserved.
		[2:2]	SYNCBUSY	R	0x00	Synchronization busy flag.
0x0C	IRQFLG	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag.
		[1:1]	VOVDIS	R	0x00	IRQ STO OVDIS flag.
		[2:2]	VOVCH	R	0x00	IRQ STO OVCH flag.
		[3:3]	SRCLOW	R	0x00	IRQ SRC LOW flag.
		[4:4]	TEMP	R	0x00	IRQ temperature flag.
		[5:5]	APMDONE	R	0x00	IRQ APM done flag.
		[6:6]	APMERR	R	0x00	IRQ APM error flag.
0x0D	STATUS	[1:1]	VOVDIS	R	0x00	Status STO OVDIS.
		[2:2]	VOVCH	R	0x00	Status STO OVCH.
		[3:3]	SRCLOW	R	0x00	Status SRC LOW.
		[4:4]	TEMP	R	0x00	Status temperature.
		[6:6]	CHARGING	R	0x00	Status STO CHARGE.
		[7:7]	CHARGEDIS	R	0x00	Status GPIO DIS_STO_CH.
0x0E	APM0	[7:0]	DATA	R	0x00	APM data 0.

Table 9: Register summary

Address	Name	Bit	Field Name	Access	Reset	Description
0x0F	APM1	[7:0]	DATA	R	0x00	APM data 1.
0x10	APM2	[7:0]	DATA	R	0x00	APM data 2.
0x11	TEMP	[7:0]	DATA	R	0x00	Temperature data.
0x12	STO	[7:0]	DATA	R	0x00	Storage element voltage.
0x13	RSVD	[7:0]	-	R	-	Reserved.
0xE0	PN0	[7:0]	DATA	R	0X30 - 0x31	Part number 0 data.
0xE1	PN1	[7:0]	DATA	R	0X30	Part number 1 data.
0xE2	PN2	[7:0]	DATA	R	0X39	Part number 2 data.
0xE3	PN3	[7:0]	DATA	R	0X30	Part number 3 data.
0xE4	PN4	[7:0]	DATA	R	0X30	Part number 4 data.

Table 9: Register summary

9. Registers Configurations

9.1. Version Register (VERSION)

The VERSION register holds the version of the chip.

VERSION Register 0x00 R
Bit [7:0]
VERSION
-

Table 10: VERSION register

9.2. Source Voltage Regulation Register (SRCREGU)

The source voltage regulation can be set thanks to the I²C communication with more precision. The register is made of 8 bits. Use the Table 13 to set the SRCREGU.VALUE register according the desired $V_{SRC,REG}$.

It is also possible to use the formulas in Table 12 to set the SRCREGU.VALUE register.

SRCREGU Register	0x01	R/W
Bit [7:0]		
VALUE		
0x77		

Table 11: SRCREGU register

$V_{SRC,REG}$ Range	SRCREGU.VALUE [7:0]
$V_{SRC,REG} < 0.112$ V	0x0C
$0.112 \leq V_{SRC,REG} < 0.315$	$\text{round}\left(3 + \frac{V_{SRC,REG} - 0.045}{0.0075}\right)$
$0.315 \leq V_{SRC,REG} < 1.478$	$\text{round}\left(37 + \frac{V_{SRC,REG} - 0.3}{0.015}\right)$
$1.478 \leq V_{SRC,REG} < 2.227$	$\text{round}\left(70 + \frac{V_{SRC,REG} - 0.45}{0.0224}\right)$
$2.227 \leq V_{SRC,REG} \leq 2.727$	$\text{round}\left(120 + \frac{V_{SRC,REG} - 0.9}{0.0455}\right)$

Table 12: Source voltage V_{SRC} from SRCREGU.VALUE register value (formula)

SRCREGU .VALUE [7:0]	$V_{SRC,REG}$ [V]	SRCREGU .VALUE [7:0]	$V_{SRC,REG}$ [V]	SRCREGU .VALUE [7:0]	$V_{SRC,REG}$ [V]	SRCREGU .VALUE [7:0]	$V_{SRC,REG}$ [V]	SRCREGU .VALUE [7:0]	$V_{SRC,REG}$ [V]
0x00	Source Low[1]	0x27	0.330	0x47	0.810	0x67	1.290	0x87	1.903
...		0x28	0.345	0x48	0.825	0x68	1.305	0x88	1.925
		0x29	0.360	0x49	0.840	0x69	1.320	0x89	1.948
		0x2A	0.375	0x4A	0.855	0x6A	1.335	0x8A	1.970
		0x2B	0.390	0x4B	0.870	0x6B	1.350	0x8B	1.993
		0x2C	0.405	0x4C	0.885	0x6C	1.365	0x8C	2.015
0x0D	0.120	0x2D	0.420	0x4D	0.900	0x6D	1.380	0x8D	2.037
0x0E	0.128	0x2E	0.435	0x4E	0.915	0x6E	1.395	0x8E	2.060
0x0F	0.135	0x2F	0.450	0x4F	0.930	0x6F	1.410	0x8F	2.082
0x10	0.143	0x30	0.465	0x50	0.945	0x70	1.425	0x90	2.104
0x11	0.150	0x31	0.480	0x51	0.960	0x71	1.440	0x91	2.127
0x12	0.158	0x32	0.495	0x52	0.975	0x72	1.455	0x92	2.149
0x13	0.165	0x33	0.510	0x53	0.990	0x73	1.470	0x93	2.172
0x14	0.173	0x34	0.525	0x54	1.005	0x74	1.478	0x94	2.194
0x15	0.180	0x35	0.540	0x55	1.020	0x75	1.500	0x95	2.227
0x16	0.188	0x36	0.555	0x56	1.035	0x76	1.522	0x96	2.273
0x17	0.195	0x37	0.570	0x57	1.050	0x77	1.545	0x97	2.318
0x18	0.203	0x38	0.585	0x58	1.065	0x78	1.567	0x98	2.364
0x19	0.210	0x39	0.600	0x59	1.080	0x79	1.590	0x99	2.409
0x1A	0.218	0x3A	0.615	0x5A	1.095	0x7A	1.612	0x9A	2.455
0x1B	0.225	0x3B	0.630	0x5B	1.110	0x7B	1.634	0x9B	2.500
0x1C	0.233	0x3C	0.645	0x5C	1.125	0x7C	1.657	0x9C	2.545
0x1D	0.240	0x3D	0.660	0x5D	1.140	0x7D	1.679	0x9D	2.591
0x1E	0.248	0x3E	0.675	0x5E	1.155	0x7E	1.701	0x9E	2.636
0x1F	0.255	0x3F	0.690	0x5F	1.170	0x7F	1.724	0x9F	2.682
0x20	0.263	0x40	0.705	0x60	1.185	0x80	1.746	0xA0	2.727
0x21	0.270	0x41	0.720	0x61	1.200	0x81	1.769	...	2.727
0x22	0.278	0x42	0.735	0x62	1.215	0x82	1.791		
0x23	0.285	0x43	0.750	0x63	1.230	0x83	1.813		
0x24	0.293	0x44	0.765	0x64	1.245	0x84	1.836		
0x25	0.300	0x45	0.780	0x65	1.260	0x85	1.858		
0x26	0.315	0x46	0.795	0x66	1.275	0x86	1.881	0xFF	2.727

Table 13: SRC constant voltage values configured by SRCREGU

1.Setting SRCREGU.VALUE to a value lower than 0x0D causes the AEM0090x to consider the SRC voltage to be lower than SLEEP.SRCLOW if the SLEEP condition is met.

9.3. Overdischarge Voltage (VOVDIS)

The VOVDIS register allows for configuring V_{OVDIS}, as shown in Table 15. The following formula can also be used:

$$V_{OVDIS} = 0.50625 + \mathrm{DEC(THRESH)} \cdot 0.05625$$

All values of V_{OVDIS} selected below 2.51 V will be set at 2.51 V

VOVDIS Register	0x02 R/W
Bit [7:6]	Bit [5:0]
RESERVED	THRESH
0x00	0x2D

Table 14: VOVDIS register

VOVDIS [5:0]	V_{OVDIS} [V]	VOVDIS [5:0]	V_{OVDIS} [V]
0x00	2.51	0x30	3.21
...	2.51	0x31	3.26
		0x32	3.32
0x23	2.51	0x33	3.38
0x24	2.53	0x34	3.43
0x25	2.59	0x35	3.49
0x26	2.64	0x36	3.54
0x27	2.70	0x37	3.60
0x28	2.76	0x38	3.66
0x29	2.81	0x39	3.71
0x2A	2.87	0x3A	3.77
0x2B	2.93	0x3B	3.83
0x2C	2.98	0x3C	3.88
0x2D	3.04	0x3D	3.94
0x2E	3.09	0x3E	3.99
0x2F	3.15	0x3F	4.05

Table 15: Storage element V_{OVDIS} configuration by VOVDIS register

9.4. Overcharge Voltage (VOVCH)

The VOVCH register allows for the configuration of V_{OVCH}, as shown in Table 17. The following formula can also be used:

$$V_{OVCH} = 1.2375 + \mathrm{DEC(THRESH)} \cdot 0.05625$$

All values of V_{OVCH} selected below 2.70 V will be set at 2.70 V

<table>
<tr><th>VOVCH Register</th><th>0x03 R/W</th></tr>
<tr><td>Bit
[7:6]</td><td>Bit
[5:0]</td></tr>
<tr><td>RESERVED</td><td>THRESH</td></tr>
<tr><td>0x00</td><td>0x33</td></tr>
</table>

Table 16: VOVCH register

VOVCH [5:0]	V_{OVCH} [V]	VOVCH [5:0]	V_{OVCH} [V]
0x00	2.70	0x2C	3.71
...	2.70	0x2D	3.77
0x1A	2.70	0x2E	3.83
0x1B	2.76	0x2F	3.88
0x1C	2.81	0x30	3.94
0x2D	2.87	0x31	3.99
0x1E	2.93	0x32	4.05
0x1F	2.98	0x33	4.11
0x20	3.04	0x34	4.16
0x21	3.09	0x35	4.22
0x22	3.15	0x36	4.28
0x23	3.21	0x37	4.33
0x24	3.26	0x38	4.39
0x25	3.32	0x39	4.44
0x26	3.38	0x3A	4.50
0x27	3.43	0x3B	4.56
0x28	3.49	0x3C	4.61
0x29	3.54	0x3D	4.67
0x2A	3.60	0x3E	4.73
0x2B	3.66	0x3F	4.78

Table 17: V_{OVCH} configuration by VOVCH register

9.5. Temperature Register (TEMPCOLD, TEMPHOT)

The configuration of the temperature thresholds is done by setting two registers through I²C communication:

- The low temperature threshold is configured in register TEMPCOLD (0x04);
- The high temperature threshold is configured in register TEMPHOT (0x05).

The temperature protection uses a voltage divider consisting of the resistor R_{DIV} and the thermistor $R_{TH}(T)$. Considering the specifications of the thermistor used, it is possible to determine the relationship between the temperature and the resistance of the thermistor. The following equation must therefore be applied to determine the value to be written to the register:

$$\mathrm{THRESH} = 256 \cdot \frac{R_{TH}(T)}{R_{TH}(T) + R_{DIV}}$$

The equation is the same for both the high and the low thresholds. THRESH is the value to be written to the registers, $R_{TH}(T)$ is the resistance of the thermistor at the threshold temperature and R_{DIV} is the resistance that creates a resistive divider with $R_{TH}(T)$, as shown on Figure 8. The AEM0090x determines if the ambient temperature is within the range previously set by measuring the voltage on pin TH_MON.

The following equations are useful to determine the temperature from the THRESH register field value:

$$R_{TH}(T) = R0 \cdot e^{B \cdot \left(\frac{1}{T} - \frac{1}{T_0}\right)}$$

$$T = \frac{B}{\ln\left(\frac{R_{TH}(T)}{R0}\right) + \frac{B}{T_0}}$$

- THRESH is the unsigned 8-bit value to be written in the registers to set the temperature threshold to the temperature T [K].
- R0 [Ω] is the resistance of the NTC thermistor at ambient temperature T_0 = 298.15 K (25 °C).
- $R_{TH}(T)$ [Ω] is the resistance of the thermistor at temperature T [K].
- T_0 [K] = 298.15 K (25 °C)
- T [K] is the current ambient temperature of the circuit.
- B is the characteristic constant of the thermistor, allowing to determine the resistance of the thermistor for a given temperature.

For example with a Murata NCP15XH103J03RC the default thresholds are 0°C and 45°C (see Table 9), which matches the specifications of most Li-Ion batteries.

9.5.1. TEMPCOLD

Minimum temperature (cold) for storage element charging register.

TEMPCOLD Register	0x04	R/W
Bit [7:0]		
THRESH		
0x8F		

Table 18: TEMPCOLD register

Bit [7:0]: THRESH (TEMPCOLD.THRESH).

This fields is used to configure the minimum temperature (cold) threshold.

9.5.2. TEMPHOT

Maximum temperature (hot) for storage element charging register.

TEMPHOT Register	0x05	R/W
Bit [7:0]		
THRESH		
0x2F		

Table 19: TEMPHOT register

Bit [7:0]: THRESH (TEMPHOT.THRESH).

This fields is used to configure the maximum temperature (hot) threshold.

9.6. Power Register (PWR)

The PWR (0x06) register is dedicated to the power settings of the AEM0090x and is constituted of 4 bits:

PWR Register	0x06		R/W	
Bit [7:4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	CHARGEDIS	TMONEN	HPEN	KEEPALEN
0x00	0	1	1	1

Table 20: PWR register

Bit [3]: Battery charging disable (PWR.CHARGEDIS).

Prevent charging the battery.

- 0: DIS - allow the charging of the battery
- 1: EN - disable the charging of the battery.

The charging of the battery is disabled if either PWR.CHARGEDIS is set or if the DIS_STO_CH pin is HIGH. The state of the DIS_STO_CH pin is not ignored when the AEM0090x switches to the I²C register configuration (see Section 6.1), as it would for all other configuration pins.

Bit [2]: Temperature monitoring enable (PWR.TMONEN).

The temperature monitoring enable bit enables the monitoring of the ambient temperature.

- 0: DIS - Disable the temperature monitoring.
- 1: EN - Enable the temperature monitoring.

Bit [1]: High-power mode enable (PWR.HPEN).

Allow the AEM to automatically enter high-power mode if needed, allowing for more power to be harvested from SRC (see section 5.5.).

- 0: DIS - Disable automatic high-power mode.
- 1: EN - Enable automatic high-power mode.

Bit [0]: Keep-alive enable (PWR.KEEPALEN).

Define the energy source from which the AEM0090x supplies VINT (internal circuitry).

- 0: DIS - VINT is supplied by SRC through the boost converter.
- 1: EN - VINT is supplied by STO.

Refer to section 5.6. for more information.

NOTE: disabling the keep-alive feature is not recommended when configuring the AEM0090x with I²C registers, see Section 5.6.

9.7. Sleep Register (SLEEP)

The Sleep register SLEEP (0x07) enables the sleep mode and sets the conditions for entering the sleep mode.

SLEEP Register	0x07 R/W	
Bit [7:4]	Bit [3:1]	Bit [0]
RESERVED	SRCLOW	EN
0x00	0x00	1

Table 21: SLEEP register

Bit [3:1]: Sleep threshold (SLEEP.SRCLOW)

This field sets the voltage threshold below which the AEM0090x enters SLEEP STATE. Table 22 shows the available settings.

For example, if the SLEEP.SRCLOW field is set to 0x02, the AEM will switch to SLEEP STATE if the source target voltage is set below 0.255 V.

The SRC threshold is set by default at 0.112 mV.

SLEEP.SRCLOW	
Configuration	SRC threshold
0x00	0.112 V
0x01	0.202 V
0x02	0.255 V
0x03	0.300 V
0x04	0.360 V
0x05	0.405 V
0x06	0.510 V
0x07	0.600 V

Table 22: Configuration of the sleep threshold

Bit [0]: Sleep mode enable (SLEEP.EN)

This field controls the SLEEP STATE behavior of the AEM0090x.

- 0: DIS - The AEM0090x will never switch to SLEEP STATE.
- 1: EN - Enable the AEM0090x to switch to SLEEP STATE if conditions are met (see below).

The AEM0090x can only go in SLEEP STATE if the following conditions are met:

SLEEP_STATE = SLEEP.EN & KEEP_ALIVE & (Vsto < Vovch |STATUS.TEMP| DIS_STO_CH | SRCREGU < SLEEP.SRCLOW) & (Vsto > Vovdis)

9.8. Average Power Monitoring Control Register (APM)

Average Power Monitoring (APM; register address 0x09) allows for estimating the energy transferred from the source to the battery.

APM Register	0x09	R/W	
Bit [7:4]	Bit [3:2]	Bit [1]	Bit [0]
RESERVED	WINDOW	MODE	EN
0x00	0x00	0	0

Table 23: APM register

Bit [3:2]: APM Computation Window (APM.WINDOW)

This field is used to select the APM computation window (noted T_A in Section 5.4). The energy transferred is integrated over this configurable time window.

APM.WINDOW		
Configuration	Configuration window	APM register refresh rate
0x00	128 ms	256 ms
0x01	64 ms	128 ms
0x02	32 ms	64 ms

Table 24: Configuration of APM computation windows

Please note that, as described in Section 5.4, measurement period is twice the computation window, meaning that a new measurement is available every 2 x T_A.

Bit [1]: APM mode (APM.MODE)

The APM implements two modes, according to the APM.MODE register field value:

- 0: COUNTER - Pulse counter mode: the AEM0090x counts the number of current pulses drawn by the boost converter. This mode is enabled by setting the APM mode bit to 0.
- 1: POWER - Power meter mode: the number of pulses during a period is multiplied by a value to obtain the energy that has been transferred taking into account the efficiency of the AEM0090x. This mode is enabled by setting the APM mode bit to 1.

Bit [0]: APM enable (APM.EN)

This field enables the APM feature.

- 0: DIS - APM feature disabled.
- 1: EN - APM feature enabled.

9.9. IRQ Enable Register (IRQEN)

IRQ enable register (0x0A): configures on which event the IRQ pin is set HIGH.

IRQEN Register				0x0A		R/W	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	APMERR	APMDONE	TEMP	SRCLOW	VOVCH	VOVDIS	I2CRDY
0	0	0	0	0	0	0	1

Table 25: IRQEN register

Bit [6]: IRQ APM error enable (IRQEN.APMERR)

Enable the IRQ pin to be asserted (HIGH) when an APM error occurs

- 0: DIS - Disable.
- 1: EN - Enable.

Bit [5]: IRQ APM done enable (IRQEN.APMDONE)

Enable the IRQ pin to be asserted (HIGH) when new APM data is available.

- 0: DIS - Disable.
- 1: EN - Enable.

Bit [4]: IRQ temperature enable (IRQEN.TEMP)

Enable the IRQ pin to be asserted (HIGH) when the temperature crosses the minimum or maximum temperature allowed to charge the battery (see section 9.5.).

- 0: DIS - Disable.
- 1: EN - Enable.

Bit [3]: IRQ source low enable (IRQEN.SRCLOW)

Enable the IRQ pin to be asserted (HIGH) when $V_{SRC,REG}$ crosses the SRC LOW threshold.

- 0: DIS - Disable.
- 1: EN - Enable.

Bit [2]: IRQ storage overcharge enable (IRQEN.VOVCH)

Enable the IRQ pin to be asserted (HIGH) when the battery voltage crosses the V_{OVCH} threshold.

- 0: DIS - Disable.
- 1: EN - Enable.

Bit [1]: IRQ storage overdischarge enable (IRQEN.VOVDIS)

Enable the IRQ pin to be asserted (HIGH) when the storage element voltage crosses the V_{OVDIS} threshold.

- 0: DIS - Disable.
- 1: EN - Enable.

Bit [0]: IRQ serial interface ready enable (IRQEN.I2CRDY)

This bit is set at 1 by default.

When the AEM0090x has coldstarted and is ready to communicate through I²C. The IRQ pin is asserted (HIGH).

- 0: DIS - Disable.
- 1: EN - Enable.

9.10. I²C Control (CTRL)

Control register (0x0B).

CTRL Register	0x0B	R/W		
Bit [7:3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	SYNCBUSY	RESERVED	UPDATE
0x00	0	0	0

Table 26: CTRL register

Bit [2]: SYNCBUSY (CTRL.SYNCBUSY).

This field indicates whether the synchronization from the I²C registers to the system registers is ongoing or not. While ongoing, it is not possible to write in the registers.

- 0: NSYNC - R: CTRL register not synchronizing.
- 1: SYNC - R: CTRL register synchronizing.

Bit [0]: UPDATE (CTRL.UPDATE).

This field is used to control the source of the AEM0090x configuration (GPIO or I²C).

Furthermore, this field is used to update the AEM0090x configuration with the current configuration from the I²C registers.

- 0: GPIO
  - W: load configurations from the GPIO.
  - R: configurations from the GPIO is currently used if read as 0.
- 1: I2C
  - W: load configurations from the I²C registers.
  - R: configurations from the I²C is currently used if read as 1.

NOTE: writing any register does not have any effect until 1 is written to the CTRL.UPDATE field, leading to the AEM0090x to read the new register values and apply them.

NOTE: when using I²C register configuration, user can switch back to GPIO configuration by writing 0 to the CTRL.UPDATE field. In that case, the settings previously written to the IRQEN registers are still valid even when using GPIO configuration, as well as the data in IRQFLG register.

9.11. IRQ Flag Register (IRQFLG)

The IRQFLG (0x0C) register contains all interrupt flags, corresponding to those enabled in the IRQEN register.

This register is reset when read.

IRQFLG Register				0x0C		R	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	APMERR	APMDONE	TEMP	SRCLOW	VOVCH	VOVDIS	I2CRDY
0	0	0	0	0	0	0	1

Table 27: IRQFLG register

Bit [6]: IRQ APM error Flag (IRQFLG.APMERR)

This interrupt flag is set when an APM error occurred.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [5]: IRQ APM done Flag (IRQFLG.APMDONE)

This interrupt flag is set when APM data is available.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [4]: IRQ temperature Flag (IRQFLG.TEMP)

This interrupt flag is set when the temperature crosses the minimum or maximum temperature (selected through the TEMPCOLD and TEMPHOT registers).

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [3]: IRQ source low Flag (IRQFLG.SRCLOW)

This interrupt flag is set when $V_{SRC,REG}$ crosses the SRC LOW voltage (selected through the SLEEP register).

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [2]: IRQ storage overcharge Flag (IRQFLG.VOVCH)

This interrupt flag is set when the battery crosses the overcharge voltage (selected through the VOVCH register).

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [1]: IRQ storage overdischarge Flag (IRQFLG.VOVDIS)

This interrupt flag is set when the battery crosses the overdischarge voltage (selected through the VOVDIS register).

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [0]: IRQ serial interface ready Flag (IRQFLG.I2CRDY)

This interrupt flag is set when the AEM0090x has coldstarted and is ready to communicate through I²C (the corresponding interrupt source is enabled by default).

- 0: NFLG - No interrupt flag raised. The AEM0090x is not ready to communicate through the I²C bus.
- 1: FLG - Interrupt flag raised. The AEM0090x is ready to communicate through the I²C bus.

9.12. Status Register (STATUS)

The STATUS (0x0D) register contains informations about the status of the AEM0090x.

STATUS Register				0x0D		R	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
CHARGEDIS	CHARGING	RESERVED	TEMP	SRCLOW	VOVCH	VOVDIS	RESERVED
0	0	0	0	0	0	0	0

Table 28: Status register

Bit [7]: CHARGEDIS Status (STATUS.CHARGEDIS)

This status indicates whether the storage charging is enabled or not via the GPIO (DIS_STO_CH).

- 0: LOW - DIS_STO_CH is LOW.
- 1: HIGH - DIS_STO_CH is HIGH.

Bit [6]: CHARGE Status (STATUS.CHARGING)

This status indicates whether the AEM is currently able to charge the battery or not.

- 0: LOW - Charging is disabled.
- 1: HIGH - Charging is enabled.

Set condition:

$$(V_{STO} < V_{OVCH})\ \&\ \overline{\text{STATUS.TEMP}}\ \&\ \overline{\text{STATUS.CHARGEDIS}}$$

$$\&\ (\text{OVDIS STATE}\ |\ \text{SUPPLY STATE}\ |\ \text{SHUTDOWN STATE})$$

Bit [4]: Temperature Status (STATUS.TEMP)

This bit is set if the temperature is outside the range defined in TEMPCOLD and TEMPHOT registers.

- 0: LOW - Temperature is in range.
- 1: HIGH - Temperature is outside of the range.

Bit [3]: Source Low Status (STATUS.SRCLOW)

This status indicates whether the source target voltage is higher or lower than the sleep level threshold (112mV).

- 0: LOW - Source target voltage is above the sleep level threshold.
- 1: HIGH - Source target voltage is below the sleep level threshold.

Bit [2]: Storage Overcharge Status (STATUS.VOVCH)

This status indicates whether the battery voltage is higher or lower than the overcharge level threshold.

- 0: LOW - $V_{STO} < V_{OVCH}$.
- 1: HIGH - $V_{STO} \geq V_{OVCH}$.

Bit [1]: Storage Overdischarge Status (STATUS.VOVDIS)

This status indicates whether the battery is higher or lower than the overdischarge level threshold.

- 0: LOW - $V_{STO} > V_{OVDIS}$.
- 1: HIGH - $V_{STO} \leq V_{OVDIS}$.

9.13. Average Power Monitoring Data Registers (APM)

- Pulse Counter Mode: in that mode, the value in the APM data registers is the number of pulses drawn by the DCDC converter during the computation window (see Section 5.4). This value can be accessed directly in the COUNTER fields as shown in Table 29.
- Power Meter mode: in that mode, the value in the APM data registers is the energy value E_{APM} in nano-Joule. It can be read by left bit-shifting (OFFSET bits) the value in the POWER field and multiplying the result by the corresponding á parameter and by the inductance of the DCDC converter L_{DCDC}.

$$E_{APM} = \frac{(POWER \ll OFFSET) \cdot \alpha}{L_{DCDC}}$$

NOTE:the α parameter varies according to application specific parameters. Please contact e-peas support for information about how to determine the α parameter in a specific application

<table>
<tr><th></th><th colspan="8">APM2</th><th colspan="8">APM1</th><th colspan="8">APM0</th></tr>
<tr><th></th><th>Bit [7]</th><th>Bit [6]</th><th>Bit [5]</th><th>Bit [4]</th><th>Bit [3]</th><th>Bit [2]</th><th>Bit [1]</th><th>Bit [0]</th><th>Bit [7]</th><th>Bit [6]</th><th>Bit [5]</th><th>Bit [4]</th><th>Bit [3]</th><th>Bit [2]</th><th>Bit [1]</th><th>Bit [0]</th><th>Bit [7]</th><th>Bit [6]</th><th>Bit [5]</th><th>Bit [4]</th><th>Bit [3]</th><th>Bit [2]</th><th>Bit [1]</th><th>Bit [0]</th></tr>
<tr><td>Register Field</td><td></td><td colspan="7">APM2SRC.DATA[22:16]</td><td colspan="8">APM1SRC.DATA[15:8]</td><td colspan="8">APM0SRC.DATA[7:0]</td></tr>
<tr><td>Global APM Field</td><td></td><td colspan="23">APM DATA [22:0]</td></tr>
<tr><td>Pulse Counter Mode</td><td></td><td></td><td colspan="6">COUNTER [21:16]</td><td colspan="8">COUNTER [15:8]</td><td colspan="8">COUNTER [7:0]</td></tr>
<tr><td>Power Meter Mode</td><td></td><td colspan="4">OFFSET [22:19]</td><td colspan="3">POWER [18:16]</td><td colspan="8">POWER [15:8]</td><td colspan="8">POWER [7:0]</td></tr>
</table>

Table 29: Summary of APMx registers fields

9.14. Temperature Data Register (TEMP)

This field contains the result of the ADC acquisition for the temperature monitoring. The voltage at the terminals of the voltage divider can be derived by applying the following equation, with V_{REF} = 1 V:

$$V_{TH} = \frac{V_{REF} \cdot DATA}{256}$$

Or, in order to make a comparison with the Table in the thermistor datasheet, it is possible to find the impedance of the thermistor:

$$R_{TH} = R_{DIV} \cdot \frac{DATA}{256 - DATA}$$

TEMP Register	0x11	R
Bit [7:0]		
DATA		
0x00		

Table 30: TEMP register

9.15. Battery Voltage Register (STO)

The STO (0x12) contains the 8-bit result from the ADC acquisition of the battery voltage. To convert the result to Volts, the following equation is applied.

$$V_{STO} = \frac{4.8 \cdot DEC(DATA)}{256}$$

STO Register	0x12	R
Bit [7:0]		
DATA		
0x00		

Table 31: STO register

9.16. Part Number Registers (PN)

PN0 Register	**0xE0**	**R**
Bit [7:0]		
DATA		
AEM00900: 0x30	AEM00901: 0x31	

Table 32: PN0 register

PN1 Register	**0xE1**	**R**
Bit [7:0]		
DATA		
0x30		

Table 33: PN1 register

PN2 Register	**0xE2**	**R**
Bit [7:0]		
DATA		
0x39		

Table 34: PN2 register

PN3 Register	**0xE3**	**R**
Bit [7:0]		
DATA		
0x30		

Table 35: PN3 register

PN4 Register	**0xE4**	**R**
Bit [7:0]		
DATA		
0X30		

Table 36: PN4 register

10. Typical Application Circuits

10.1. Example Circuit 1

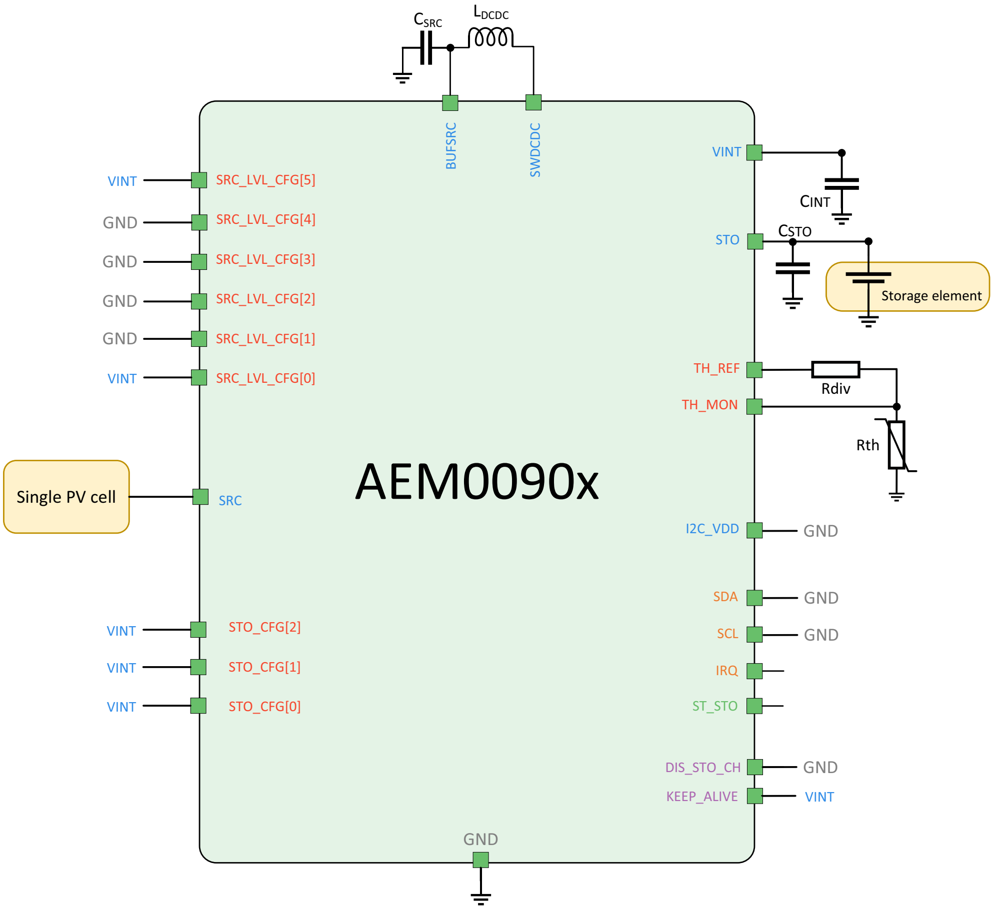


Figure 14: Typical application circuit 1

The circuit is an example of a system with solar energy harvesting with the AEM0090x. It uses a Li-ion rechargeable battery as energy storage.

- Energy source: PV cell.
- SRC_LVL_CFG[5:0] = HLLLLH: The source voltage regulation is set to 0.75 V to extract the maximum power of the PV cell.
- STO_CFG[2:0] = HHH: The storage element is a Li-ion battery.
- V_{OVCH} = 4.12 V
- V_{OVDIS} = 3.01 V
- The thermal monitoring is used with a default threshold value (TEMPCOLD = 0°C, TEMPHOT = 45°C) with R_{DIV} = 22 kΩ and R_{TH}: NCP15XH103J03RC.
- The I²C communication is not used.
- DIS_STO_CH is connected to GND: The charging of the storage element on STO is enabled.
- KEEP_ALIVE is connected to V_{INT}: The AEM is being powered from the storage element.

10.2. Example Circuit 2

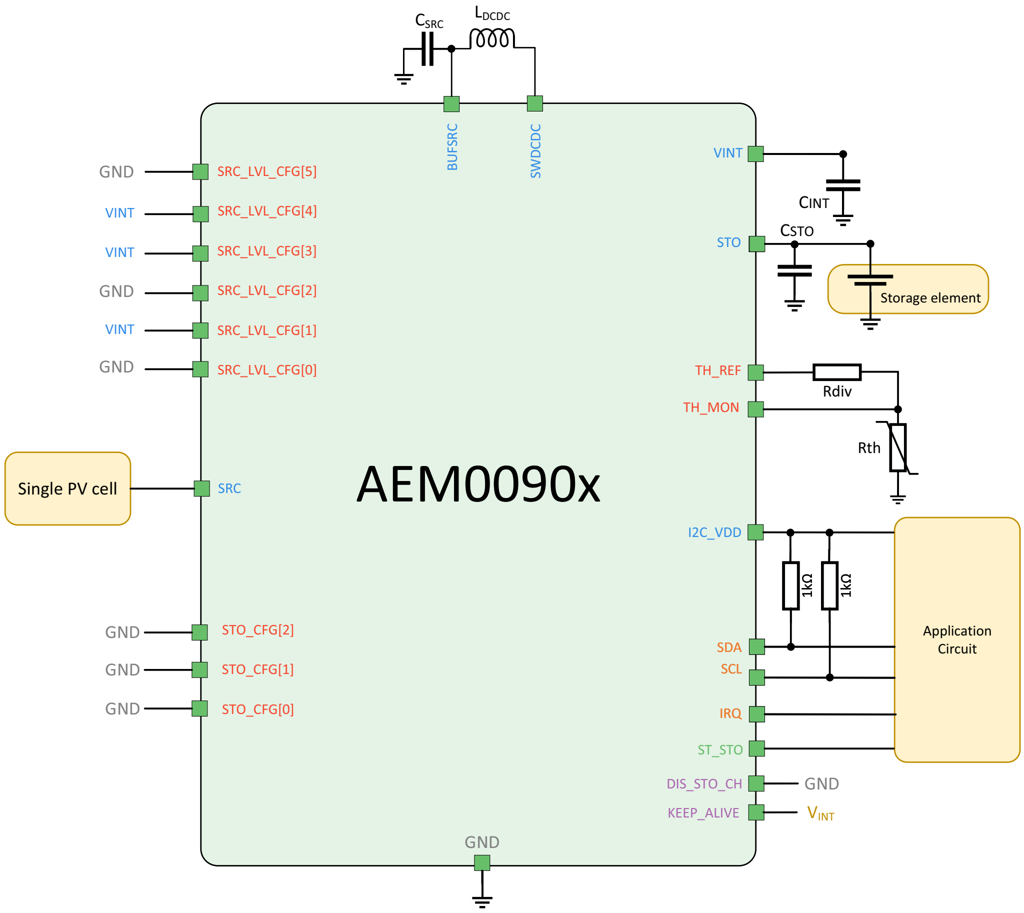


Figure 15: Typical application circuit 2

The circuit is a example of a system with solar energy harvesting with the AEM0090x. It uses a NiCd 3 cells battery as storage element.

- Energy source: PV cell
- SRC_LVL_CFG[5:0]: Configured through the I²C communication (0.555 V)
- STO_CFG[2:0]: Configured through the I²C communication
  - V_{OVCH} = 4.11 V
  - V_{OVDIS} = 3.32 V
- The thermal monitoring is used and the thresholds are configured through the I²C communication (Cold threshold = 10°C, Hot threshold = 60°C with R_{DIV} = 22 kΩ and R_{TH}: NCP15XH103J03RC).
- DIS_STO_CH is connected to GND: The charging of the storage element on STO is enabled.
- KEEP_ALIVE is connected to V_{INT}: The AEM is being powered from the storage element.

Register Address	Register Name	Value
0x01	SRCREGU	0x36
0x02	VOVDIS	0x32
0x03	VOVCH	0x33
0x04	TEMPCOLD	0x74
0x05	TEMPHOT	0x1F

Table 37: Typical application circuit 2 register settings

NOTE: a configuration tool is available on e-peas website. It helps the user to read and write registers.

11. Circuit Behavior

11.1. Start-up and Supply

11.1.1. Configuration

- SRC is supplied by a 1.0 V voltage source with 5 mA current compliance.
  - V_{OC} = 1.0 V
  - I_{SRC} = 5 mA
- SRC_LVL_CFG[5:0] = LHHLLH
  - $V_{SRC,REG}$ = 0.51 V
- STO_CFG[2:0] = HHL
  - V_{OVDIS} = 3.01 V
  - V_{OVCH} = 4.35 V
- Temperature monitoring disabled.
- DIS_STO_CH = L
  - Storage element charge is enabled.
- KEEP_ALIVE = H
  - Keep-alive functionality is enabled.

11.1.2. Observations

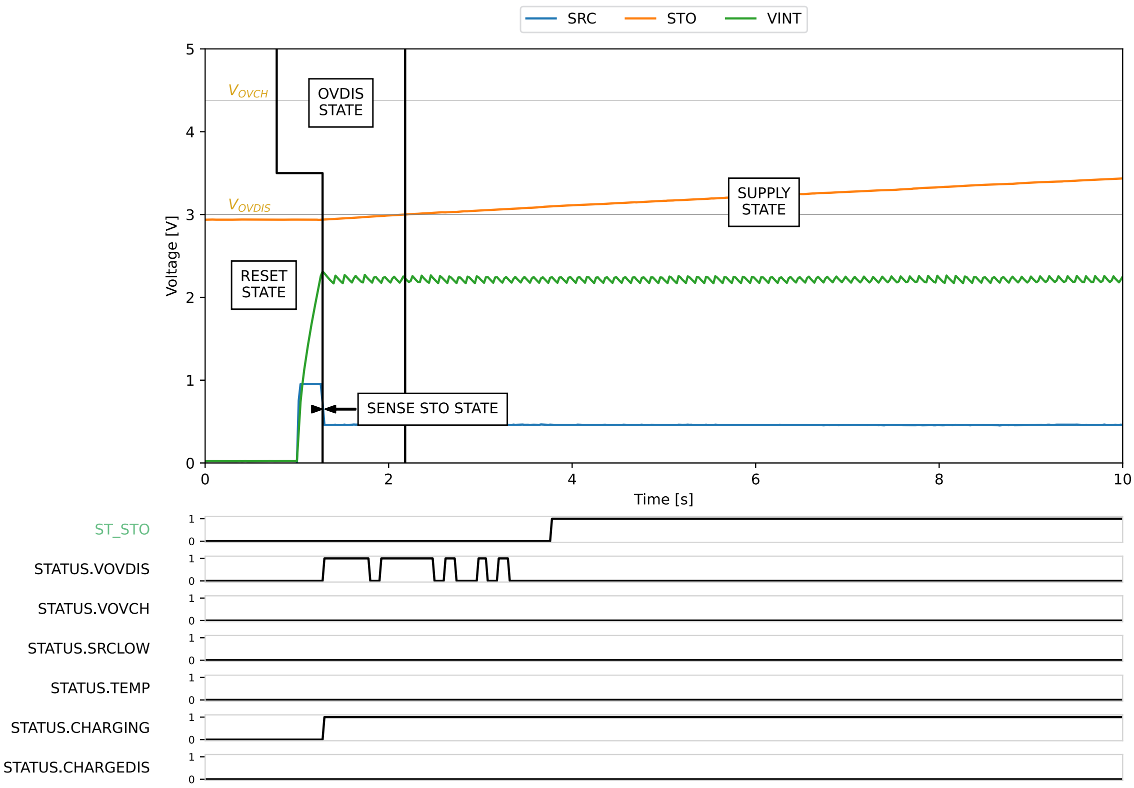


Figure 16: start-up and charge behavior

- The AEM0090x is initially in RESET STATE.
- Once the supply connected on SRC is switched on, the AEM0090x coldstarts. C_{INT} is charged until VINT reaches $V_{INT,CS}$. Then, the AEM0090x switches to SENSE STO STATE.
- In SENSE STO STATE, the AEM0090x measures V_{STO}, which is slightly below V_{OVDIS}. The AEM0090x goes into OVDIS STATE.
- In OVDIS STATE, the AEM0090x charges the storage element on STO by harvesting the energy from SRC. V_{SRC} is regulated at 0.51 V. VINT is supplied by SRC. Once V_{STO} reaches V_{OVDIS}, the AEM0090x switches to SUPPLY STATE.
- In SUPPLY STATE, the AEM0090x charges the storage element.
  - Once V_{STO} reaches V_{OVDIS} + 100 mV, the ST_STO toggles from LOW to HIGH.

11.2. Supply and Overcharge

11.2.1. Configuration

- SRC is supplied by a 1.0 V voltage source with 5 mA current compliance.
  - V_{OC} = 1.0 V
  - I_{SRC} = 5 mA
- SRC_LVL_CFG[5:0] = LHHLLH
  - $V_{SRC,REG}$ = 0.51 V
- STO_CFG[2:0] = HHL
  - V_{OVDIS} = 3.01 V
  - V_{OVCH} = 4.35 V
- Temperature monitoring disabled.
- DIS_STO_CH = L
  - Storage element charge is enabled.
- KEEP_ALIVE = H
  - Keep-alive functionality is enabled.

11.2.2. Observations

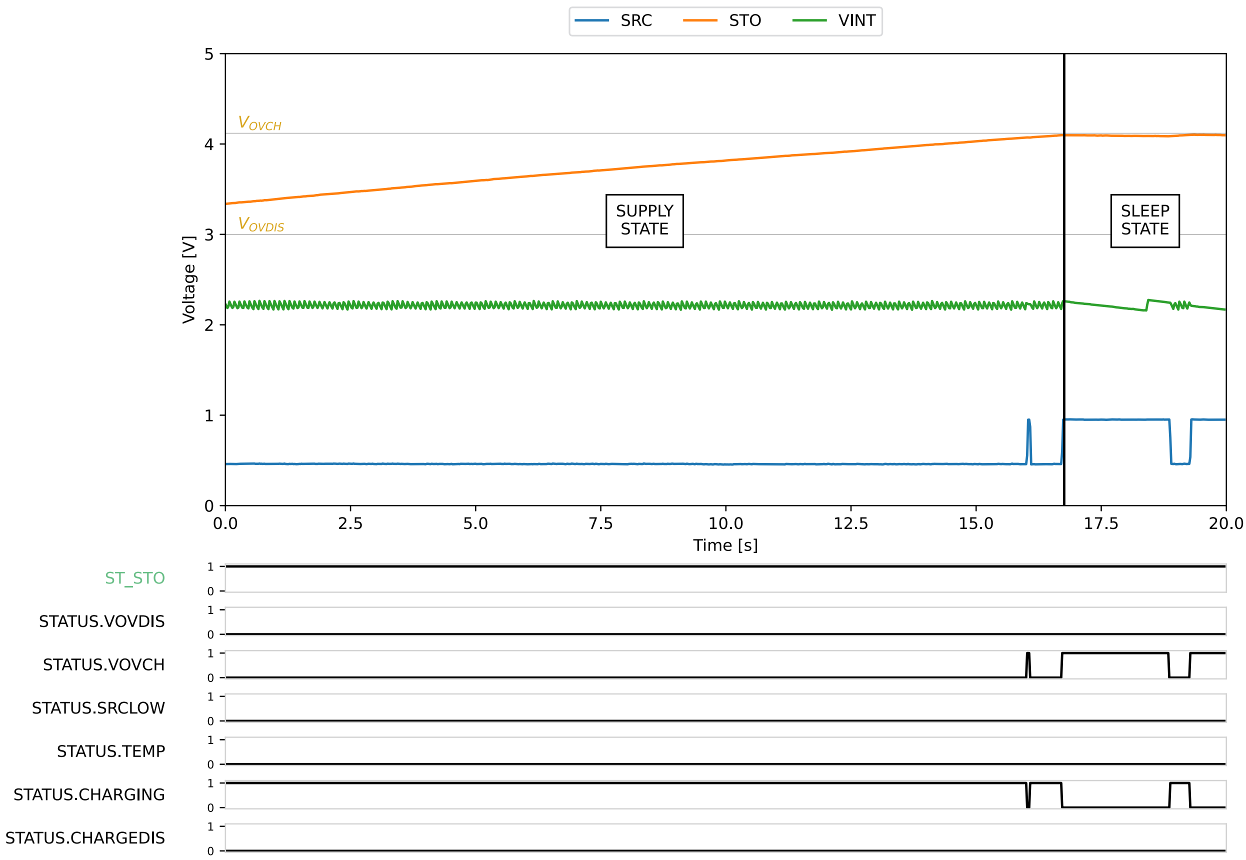


Figure 17: Supply and overcharge behavior

- In SUPPLY STATE, the AEM0090x charges the storage element.
- When the SLEEP condition is satisfied, the AEM switches to SLEEP STATE.
- In SLEEP STATE, STO and VINT are fully charged. The AEM0090x stops harvesting energy from SRC. Please note that around 19 s, the AEM0090x recharges VINT from STO, thus briefly switching to SUPPLY STATE because V_{STO} goes below V_{OVCH}.

11.3. Overdischarge

11.3.1. Configuration

- SRC is supplied by a 1.0 V voltage source with 5 mA current compliance.
  - V_{OC} = 1.0 V
  - I_{SRC} = 5 mA
- SRC_LVL_CFG[5:0] = LHHLLH
  - $V_{SRC,REG}$ = 0.51 V
- STO_CFG[2:0] = HHL
  - V_{OVDIS} = 3.01 V
  - V_{OVCH} = 4.35 V
- Temperature monitoring disabled.
- DIS_STO_CH = L
  - Storage element charge is enabled.
- KEEP_ALIVE = H
  - Keep-alive functionality is enabled.

11.3.2. Observations

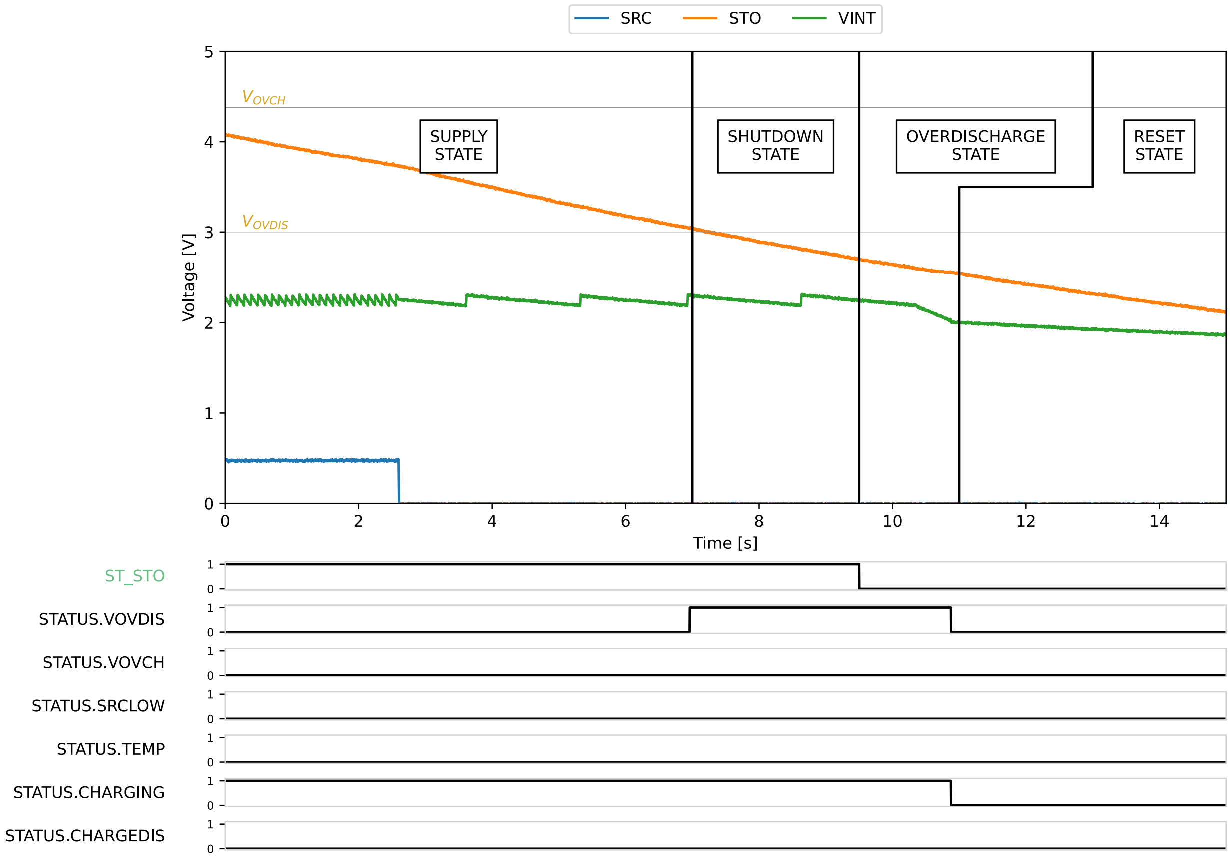


Figure 18: Overdischarge behavior

- The AEM0090x is initially in SUPPLY STATE.
- After the source is cut off, V_{STO} decreases while maintaining V_{INT} until it reaches V_{OVDIS}, the AEM0090x enters SHUTDOWN STATE.
- After T_{CRIT} in SHUTDOWN STATE, the AEM0090x goes in OVDIS STATE and ST_STO toggles from HIGH to LOW. V_{INT} is no longer supplied and C_{INT} starts to discharge.
- Once V_{INT} falls below $V_{INT,RESET}$, the AEM0090x goes in RESET STATE. All STATUS signals are set to LOW.

11.4. Keep-alive

11.4.1. Configuration

- SRC is supplied by a 1.0 V voltage source with 5 mA current compliance.
  - V_{OC} = 1.0 V
  - I_{SRC} = 5 mA
- SRC_LVL_CFG[5:0] = LHHLLH
  - $V_{SRC,REG}$ = 0.51 V
- STO_CFG[2:0] = HHL
  - V_{OVDIS} = 3.01 V
  - V_{OVCH} = 4.35 V
- Temperature monitoring disabled.
- DIS_STO_CH = L
  - Storage element charge is enabled.
- KEEP_ALIVE: is enabled on Figure 19 and disabled on Figure 20.

11.4.2. Observations

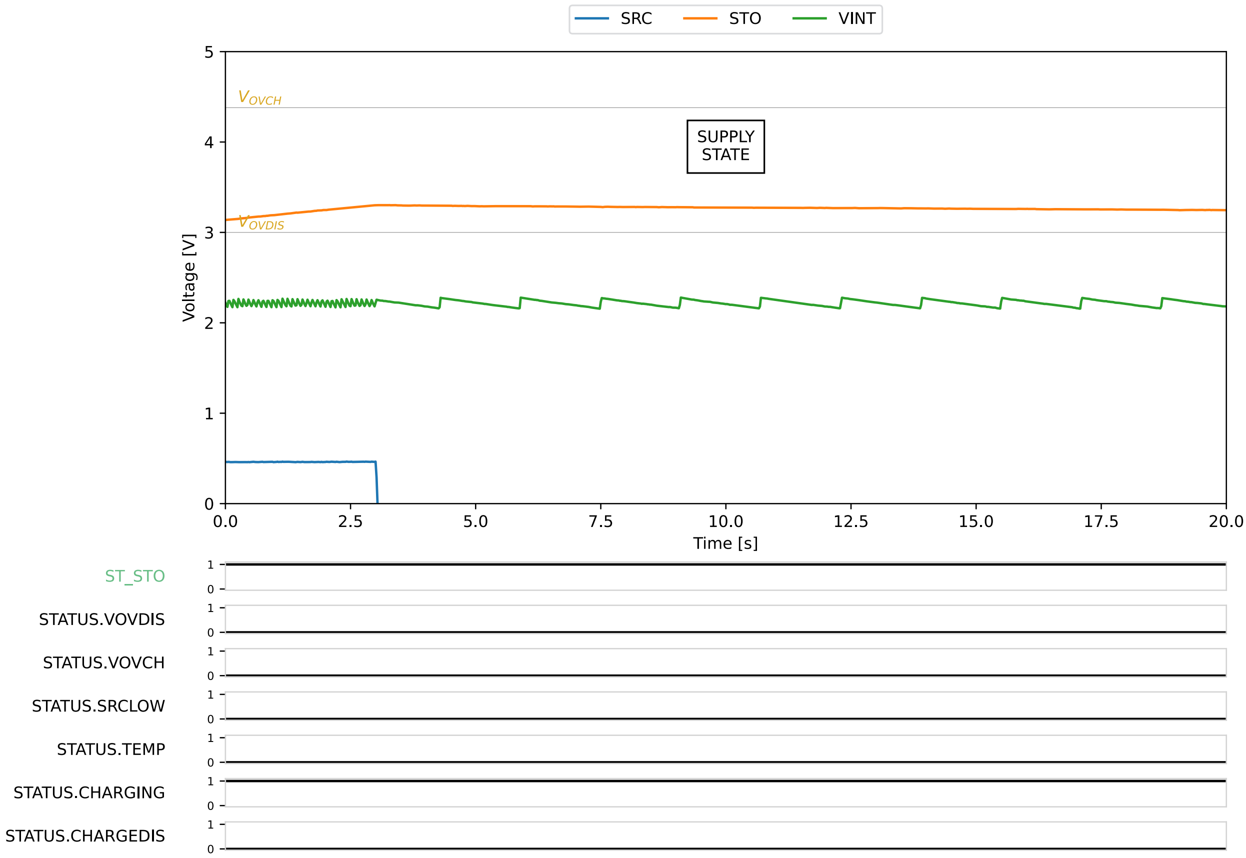


Figure 19: KEEP_ALIVE HIGH behavior

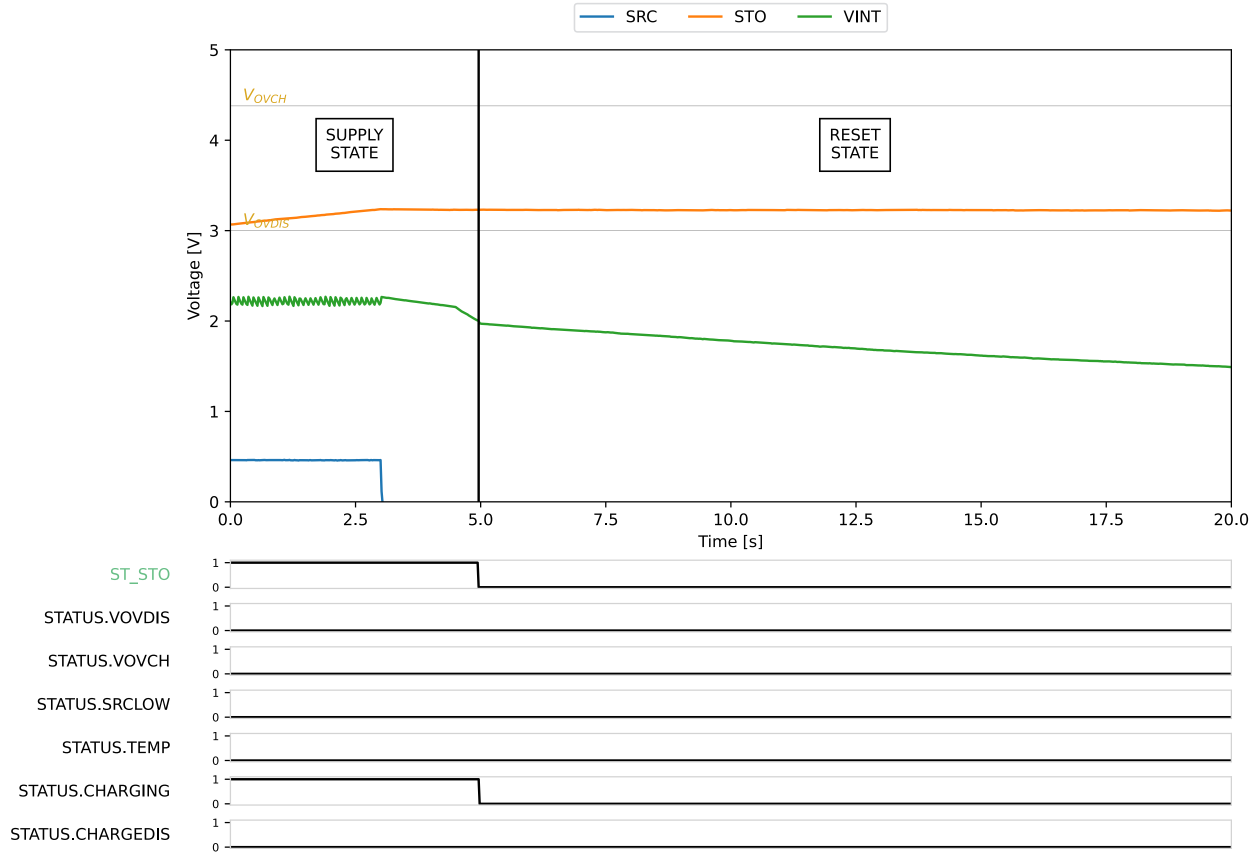


Figure 20: KEEP_ALIVE LOW behavior

In both cases, the AEM0090x is first in SUPPLY STATE. The storage element connected to STO is charged by extracting power from SRC.

At 3 s, the energy source connected to the SRC pin is switched off in both cases. The behavior after that depends on whether the keep-alive functionality is enabled or not:

- KEEP_ALIVE = H (Keep-alive enabled, Figure 19): VINT keeps being supplied from the storage element connected to STO. The AEM0090x will be able to harvest again as soon as power is restored to the SRC pin. On the other hand, a small current is pulled from the storage element (I_{QSLEEP}, see Table 5).
- KEEP_ALIVE = L (Keep-alive disabled, Figure 20): VINT can only be supplied from the energy available on SRC, so as soon as the power source is switched off, VINT stops being supplied. Once V_{INT} falls below $V_{INT,RESET}$, the AEM0090x switches to RESET STATE, so that no current is pulled from the storage element. The stored energy is thus preserved. On the other hand, when power is restored to the SRC pin, the AEM0090x must perform a cold start to resume harvesting.

11.5. Temperature Monitoring

11.5.1. Configuration

- SRC is supplied by a 1.0 V voltage source with 5 mA current compliance.
  - V_{OC} = 1.0 V
  - I_{SRC} = 5 mA
- SRC_LVL_CFG[5:0] = LHHLLH
  - $V_{SRC,REG}$ = 0.51 V
- STO_CFG[2:0] = HHL
  - V_{OVDIS} = 3.01 V
  - V_{OVCH} = 4.35 V
- Temperature monitoring is enabled with default values:
  - The temperature range in which the AEM0090x charges the storage element is 0 °C to 45 °C.
- DIS_STO_CH = L
  - Storage element charge is enabled.
- KEEP_ALIVE = H
  - keep-alive feature is enabled.

11.5.2. Observations

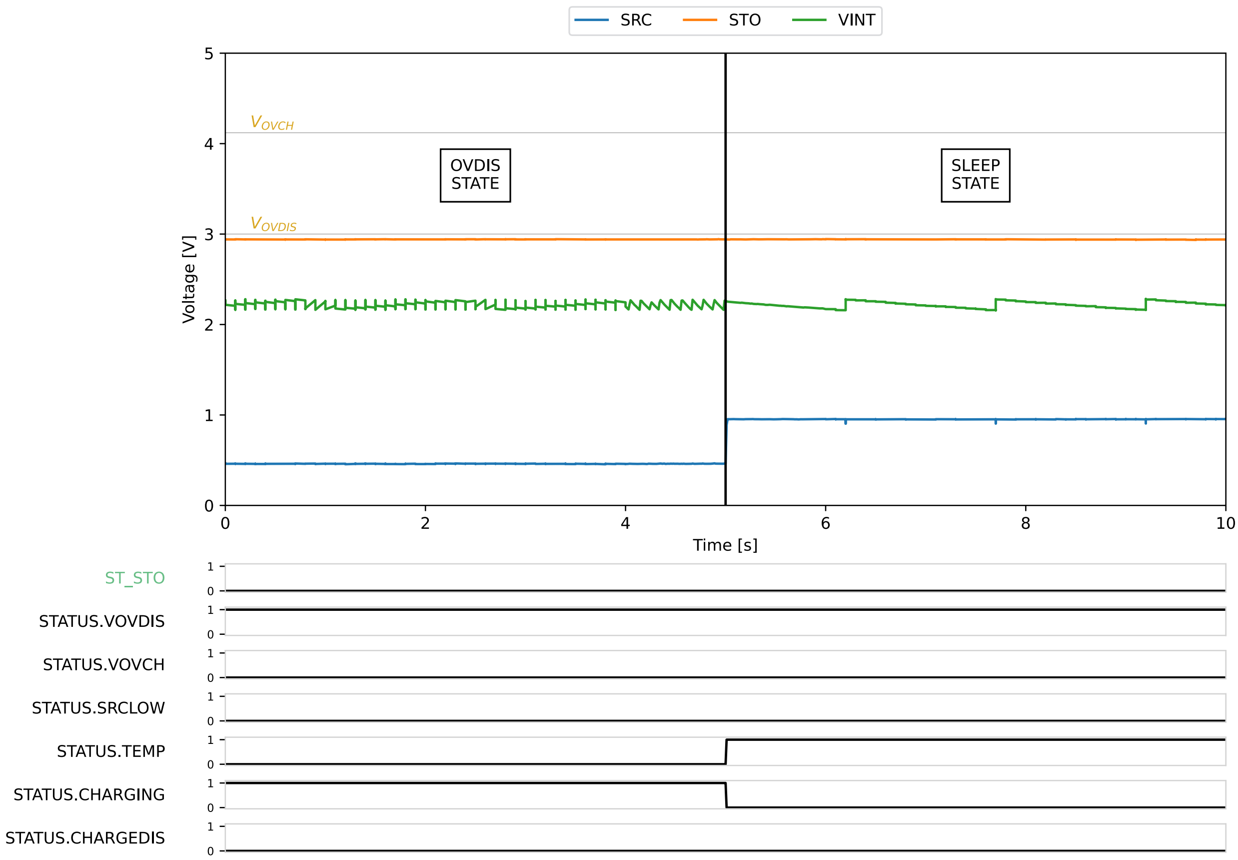


Figure 21: Temperature monitoring behavior

Figure 21 shows the AEM0090x charging the storage element (V_{SRC} is regulated) while being in OVDIS STATE. At 5 s, the temperature drops below 0 °C, causing the AEM0090x to stop charging (V_{SRC} goes to V_{OC}) the storage element. The AEM0090x goes in SLEEP STATE.

12. Minimum BOM

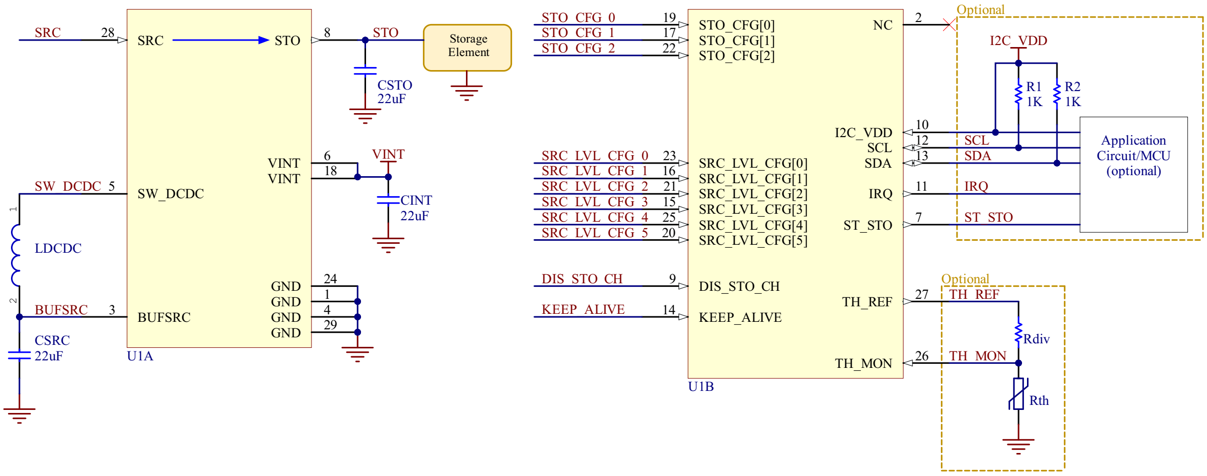


Figure 22: AEM0090x schematic

	Designator	Description	Quantity	Manufacturer	Part number
Mandatory	U1	AEM0090x	1	e-peas	order at sales@e-peas.com
	Battery	Storage element with 2.5 V min. voltage	1	To be defined by the user	
	LDCDC (AEM00900)	Power inductor 6.8 µH 1.15A 1008	1	TDK	VLS252012HBX-6R8M-1
	LDCDC (AEM00901)	Power inductor 33 µH 680 mA 1515	1	Coilcraft	LPS4018-333MRB
	CSRC	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
	CINT	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
	CSTO	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
Optional	R1, R2	Pull-up 1 kΩ Resistors for I²C interface	2	Yageo	AC0603FR-071KL
	Rth	10 kΩ NTC thermistor for temperature monitoring	1	Murata	NCP15XH103J03RC
	Rdiv	Resistor 22 kΩ 1%	1	Yageo	RC0402FR-0722KL

Table 38: AEM0090x bill of material

13. Layout

The following Figures are showcasing layout examples of the AEM0090x.

The following guidelines must be applied for best performances:

- Make sure that ground and power signals are routed with large tracks. If an internal ground plane is used, place via as close as possible to the components, especially for decoupling capacitors.
- Reactive components related to the boost converter must be placed as close as possible to the corresponding pins (SWDCDC, BUFSRC and STO), and be routed with large tracks/polygons.
- PCB track capacitance must be reduced as much as possible on the boost converter switching node SWDCDC. This is done as follows:
  - Keep the connection between the SWDCDC pin and the inductor short.
  - Remove the ground and power planes under the SWDCDC node. The polygon on the opposite external layer may also be removed.
  - Increase the distance between SWDCDC and the ground polygon on the external PCB layer where the AEM0090x is mounted.
- PCB track capacitance must be reduced as much as possible on the TH_REF node. Same principle as for SWDCDC may be applied.

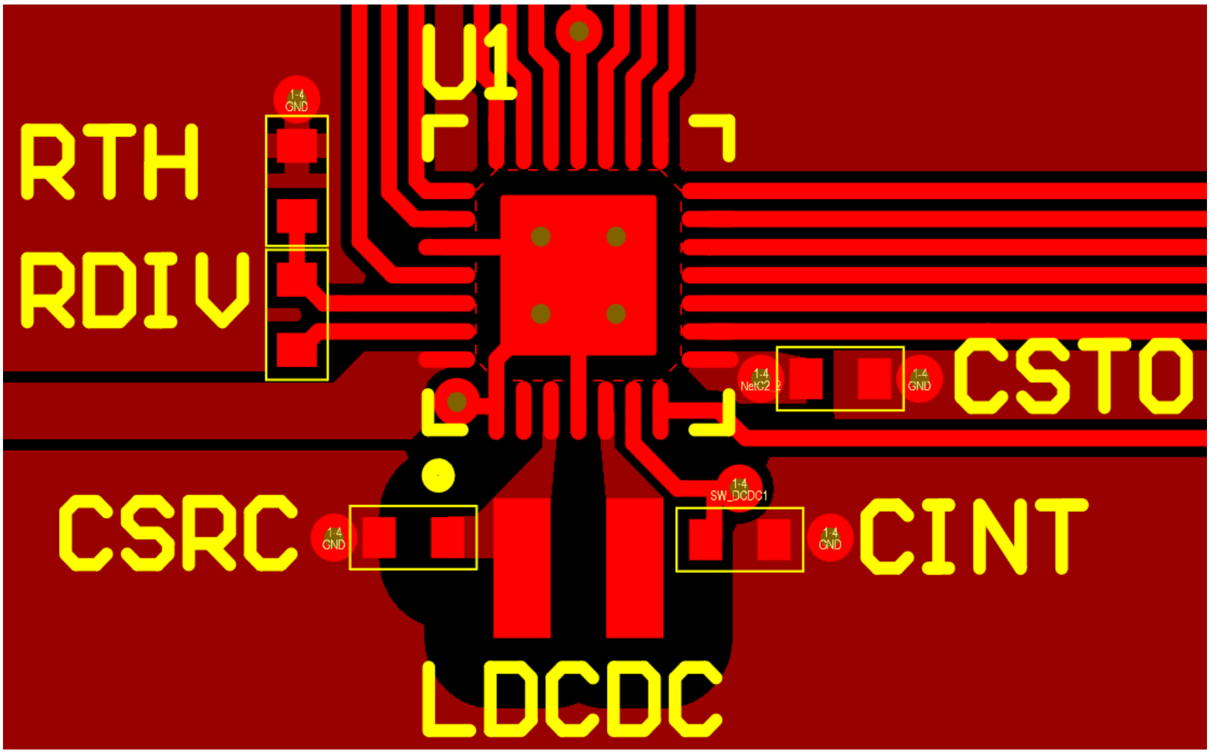


Figure 23: AEM00900 QFN28 layout example

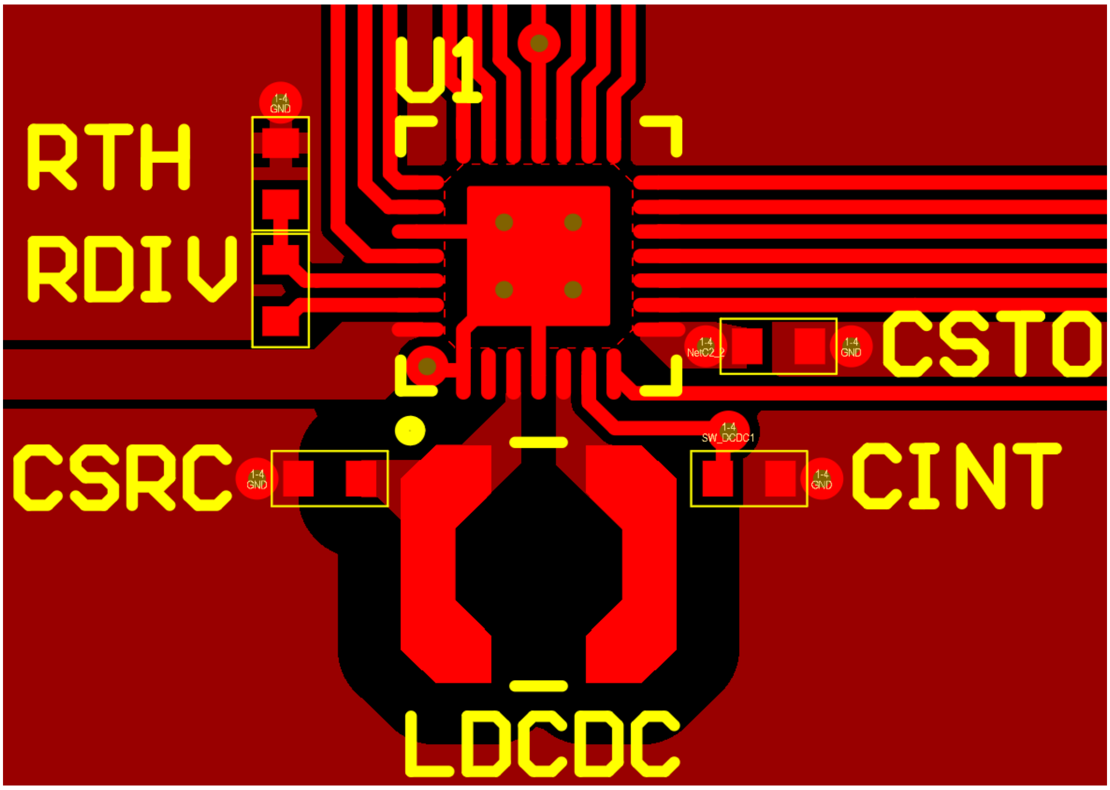


Figure 24: AEM00901 QFN28 layout example

14. Package Information

14.1. Moisture Sensitivity Level

Package	Moisture Sensitivity Level (MSL)[1]
QFN-28	Level 1

Table 39: Moisture sensitivity level

1. According to JEDEC 22-A113 standard.

14.2. RoHS Compliance

e-peas product complies with RoHS requirement.

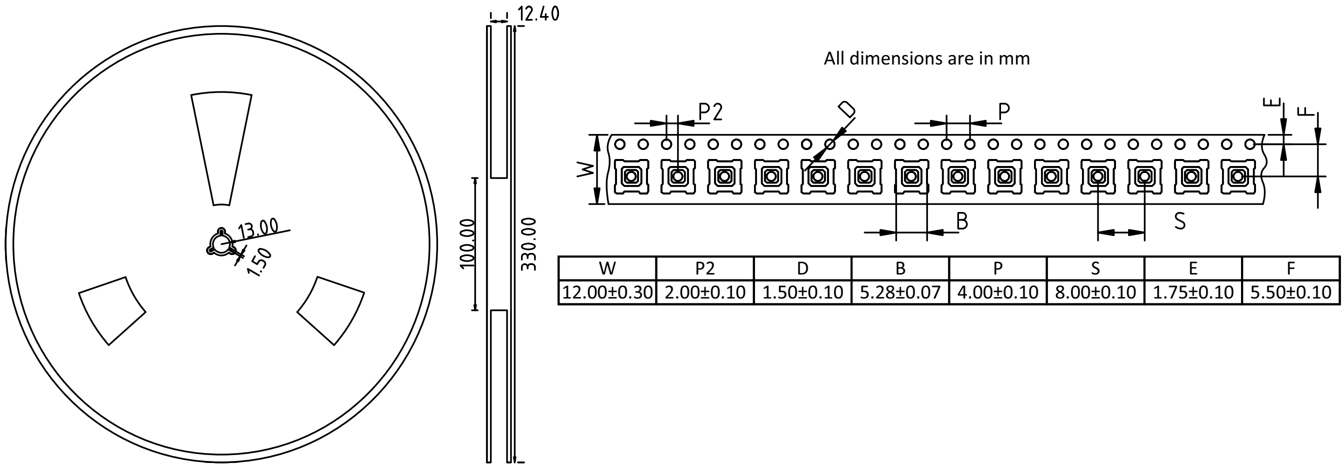
e-peas defines "RoHS" to mean that semiconductor end-products are compliant with RoHS regulation for all 10 RoHS substances.

This applies to silicon, die attached adhesive, gold wire bonding, lead frames, mold compound, and lead finish (pure tin).

14.3. REACH Compliance

The component and elements used by e-peas subcontractors to manufacture e-peas PMICs and devices are REACH compliant. For more detailed information, please contact e-peas sales team.

14.4. Tape and Reel Dimensions



W	P2	D	B	P	S	E	F
12.00±0.30	2.00±0.10	1.50±0.10	5.28±0.07	4.00±0.10	8.00±0.10	1.75±0.10	5.50±0.10

Figure 25: Tape and reel dimensions

14.5. Package Dimensions

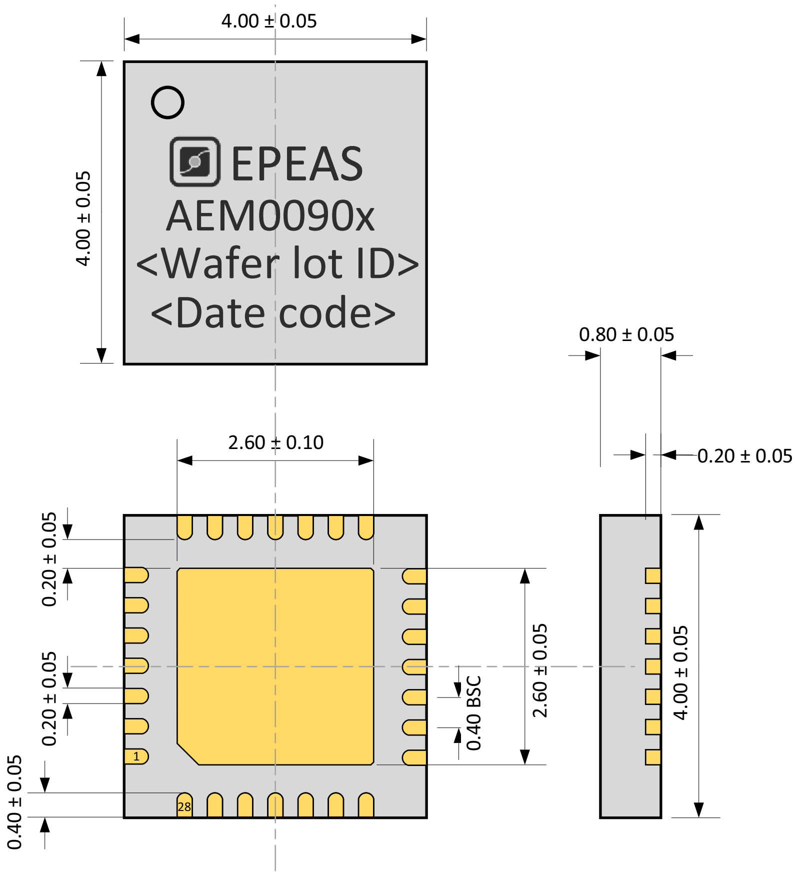


Figure 26: QFN28 4x4 mm drawaing (all dimensions in mm)

14.6. Board Layout

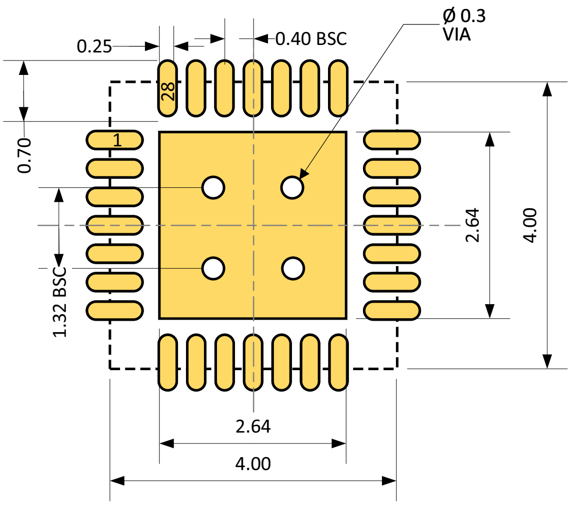


Figure 27: Recommended board layout for QFN28 package (all dimensions in mm)

15. Glossary

15.1. SRC Acronyms

V_{SRC}

Voltage at SRC pin.

$V_{SRC,CS}$

Minimum source voltage required for cold start.

$V_{SRC,REG}$

Target regulation voltage at the SRC pin.

V_{OC}

Open-circuit voltage of the harvester connected to the SRC pin.

$P_{SRC,CS}$

Minimum power available on SRC for the AEM0090x to coldstart.

I_{SRC}

Current drawn at the SRC pin.

C_{SRC}

BUFSRC pin decoupling capacitor.

L_{DCDC}

DCDC converter inductor.

15.2. STO Acronyms

V_{STO}

Voltage at STO pin.

V_{OVDIS}

Overdischarge voltage at STO pin.

V_{OVCH}

Overcharge voltage at STO pin.

$I_{QSUPPLY}$

Quiescent current on VINT when the AEM0090x is in SUPPLY STATE.

I_{QSLEEP}

Quiescent current on VINT when the AEM0090x is in SLEEP STATE.

I_{QSTO}

Quiescent current on STO when Keep-alive functionality is disabled.

$T_{STO,SUPPLY}$

Time between two V_{STO} evaluations in SUPPLY STATE

$T_{STO,SLEEP}$

Time between two V_{STO} evaluations in SLEEP STATE

T_{CRIT}

Time spent in SHUTDOWN STATE with V_{STO} below V_{OVDIS} before switching to OVDIS STATE

15.3. VINT Acronyms

V_{INT}

AEM0090x internal circuit voltage supply.

$V_{INT,RESET}$

Minimum voltage on VINT before switching to RESET STATE (from any other state).

$V_{INT,CS}$

Minimum voltage on VINT to allow the AEM0090x to switch from RESET STATE to SENSE STO STATE.

C_{INT}

VINT pin decoupling capacitor.

15.4. I²C Acronyms

R_{SCL} / R_{SDA}

Respectively, I²C SCL and SDA pin pull-up resistors.

15.5. Various Acronyms

R_{DIV}

Resistor that creates a resistive voltage divider with R_{TH}.

$T_{GPIO,MON}$

Time between two GPIO state evaluations

$T_{DIS\_STO\_CH,MON}$

Time between two DIS_STO_CH IO state evaluations

$T_{TEMP,MON}$

Time between two temperature evaluations

16. Revision History

Revision	Date	Description
1.0	January, 2022	Creation of the document.
1.1	February, 2023	- I2C_VDD: max. voltage to 2.2 V. - I2C_VDD: more explanation about pin use when using I²C and not using I²C. - Added component part number. - LDCDC from 4.7 µH to 6.8 µH in typical application circuits and in efficiency graphs (AEM00900). - Explanations about CSTO influence on efficiency.
2.0	July, 2024	- Small fixes. - Thermal pad (back plane) renamed as pin 29. - Added ST_STO - Changed APM register - Increased SRC voltage range - Removed necessity for STO protection - Improved SRCREGU register lookup table for more clarity - Updated FSM diagram. - Updated efficiency graphs. - Improved register description. - Cleaner “circuit behavior” section - Removed SRC register - Updated IQ graph

2.1	September, 2024	- Small fixes
		- Changed default value of version register
		- Changed BUFSRC max voltage to 3 V
		- Added ESD and latch-up value in “Absolute Maximum Ratings” table.
		- Created a “Specification” section and moved the following sections in it:
		    - “Absolute Maximum Ratings”.
		    - ”Typical Electrical Characteristics at 25 °C”, renamed as “Electrical Characteristics at 25 °C”.
		    - “Recommended Operating Conditions”.
		    - “Performance Data”, renamed as “Typical Characteristics”.
		- Renamed the “Thermal Resistance” section and moved it in the “Package information” section.
		- “Pin description” table: added KEEP_ALIVE pin state when left floating.
		- Fixed APM register value to energy formula and removed the α table and added a note to contact support for more information.
		- Added precisions about the behavior of the DIS_STO_CH pin combined with the PWR.STOCHDIS register field.
		- One register per page for a clearer text flow.
		- Added Cold-start power graphs.
		- Updated IQ values.
		- Added STO, GPIO and THMON monitoring period.

Table 40: Revision history (part 1)

Revision	Date	Description
2.2	March, 2025	- Changed “Features and Benefits” order. - Changed first page applications. - Removed latch-up values in “Absolute Maximum Ratings”. - Corrected operating temperature and added storage temperature in “Absolute Maximum Ratings”. - Renamed SRCTHRES to SRCLOW. - Renamed STATUS.CHARGE to STATUS.CHARGING - Renamed STATUS.BSTDIS to STATUS.CHAREGEDIS - Changed register description in “Register Map”. - Changed default value of VOVDIS/VOVCH registers in “Register Map”. - Corrected $V_{SRC,REG}$ hex value calculation formula. - Unsplited VOVDIS/VOVCH table. - Updated “Package Information” figure. - Added tape and reel dimensions. - Small fixes.

Table 40: Revision history (part 2)