ES9082

8 Channel High Performance SMART DAC with Line Driver and Mixer

Product Datasheet

Analog Reinvented

The SABRE® ES9082 High Performance SMART DAC is an 8 channel audio digital to analog converter (DAC) incorporating an integrated line driver and 2nd generation ESS Audio Signal Processor (ASP2) that targets professional and consumer applications while reducing the Bill-Of-Material (BOM).

Using ESS' patented HyperStream® IV architecture and advanced SABRE HIFI® technology, the ES9082 delivers a True DNR of +120dB and –108dB THD+N per channel and provides the listener with the legendary SABRE® sound quality with improved audio performance and a refined and enjoyable listening experience.

The ES9082 SMART DAC incorporates a 2nd generation ESS Audio Signal Processor (ASP2) that allows customers to integrate their preferred audio algorithms. For example, customers can integrate multi-band PEQs, MIXERs, Audio Expansion and Compression, stereo widening, specialty filters such RIAA de-emphasis and cross-over filters, DRC, AGL, etc. This reduces or may eliminate the need for an external DSP which will simplify programming and lowers BOM requirements. In addition, a 2-channel input is available to mix a secondary stereo source such as a microphone monitor into ASP2.

The serial data interface supports TDM, TDM Daisy Chain, I²S, LJ, DoP and DSD input formats with sample rates of up to 768kHz (using 64FS mode) and DSD1024. The integrated TDM & S/PDIF output encoders allow for a variety of systems design considerations.

The ES9082 also incorporates:

- Digital Volume range from +1dB to -126dB in 0.5dB steps with 0 to +42dB pre-gain in +6dB Steps
- SPI or I²C slave interface and a Hardware (HW) mode for ease of use
- SPI master interface with an optional external SPI Flash memory for fast program loading of the ASP2
- 8 selectable internal digital FIR filters and 8 input channels of PDM are supported

With the integrated line drivers, the ES9082 reduces BOM costs by eliminating the need for external amplifiers to produce a line level $2V_{rms}$ output on each of the 8 channels. Channels can be summed to improve performance in an application requiring fewer channels. A 2-channel differential configuration can achieve up to +127dB DNR with a $4V_{RMS}$ output. A 4-channel sum configuration can achieve +123dB DNR with 2Vrms single-ended output.

The ES9082 SMART DAC sets a new standard for high-quality audio performance in a cost-effective, compact, easy to use form factor for today's most demanding digital audio applications.

FEATURE	DESCRIPTION
+120dB DNR per channel -108dB THD+N per channel	Ultra-low noise and distortion
High Sample Rates	Support for sample rates up to and including 768kHz & DSD1024
8-channel DAC + 2Vrms Line Driver	The ground centered line driver reduces BOM costs w/o required external amplifier. Reduced footprint and simplifies board layout
Versatile Digital Audio Ports	Supports Serial Data Interface inputs such as TDM, I²S, LJ, DoP, and DSD formats, TDM & S/PDIF encoders are available for external use
Integrated Audio Signal Processor (ASP)	2nd generation ASP2 that can handle custom algorithms including AGL, DRC, PEQ, MIXER functions and de-emphasis filters
I²C,SPI and HW mode Interfaces	Standard I²S and SPI interfaces for programming desired settings with additional support for HW mode
Integrated Low Noise DAC Reference Regulators	Reduced BOM cost, PCB area and improved DNR
Customizable Filter Selection	8 preset digital filters
Low Pin Count Standardized Packages	7mm x 7mm, 48 pin QFN

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Functional Block Diagram

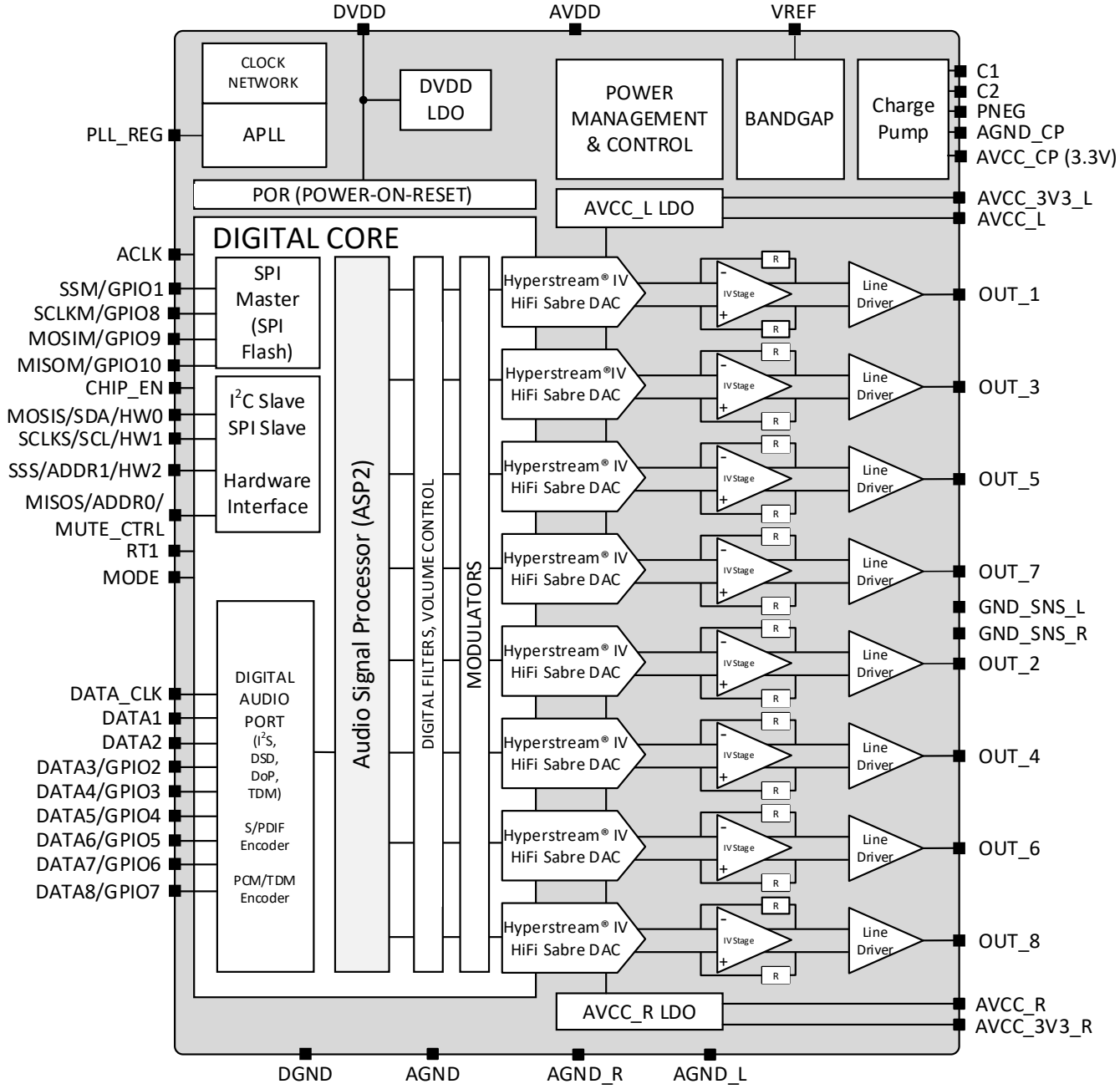


Figure 1 - ES9082 Block Diagram

ES9082 Package

48 QFN Pinout

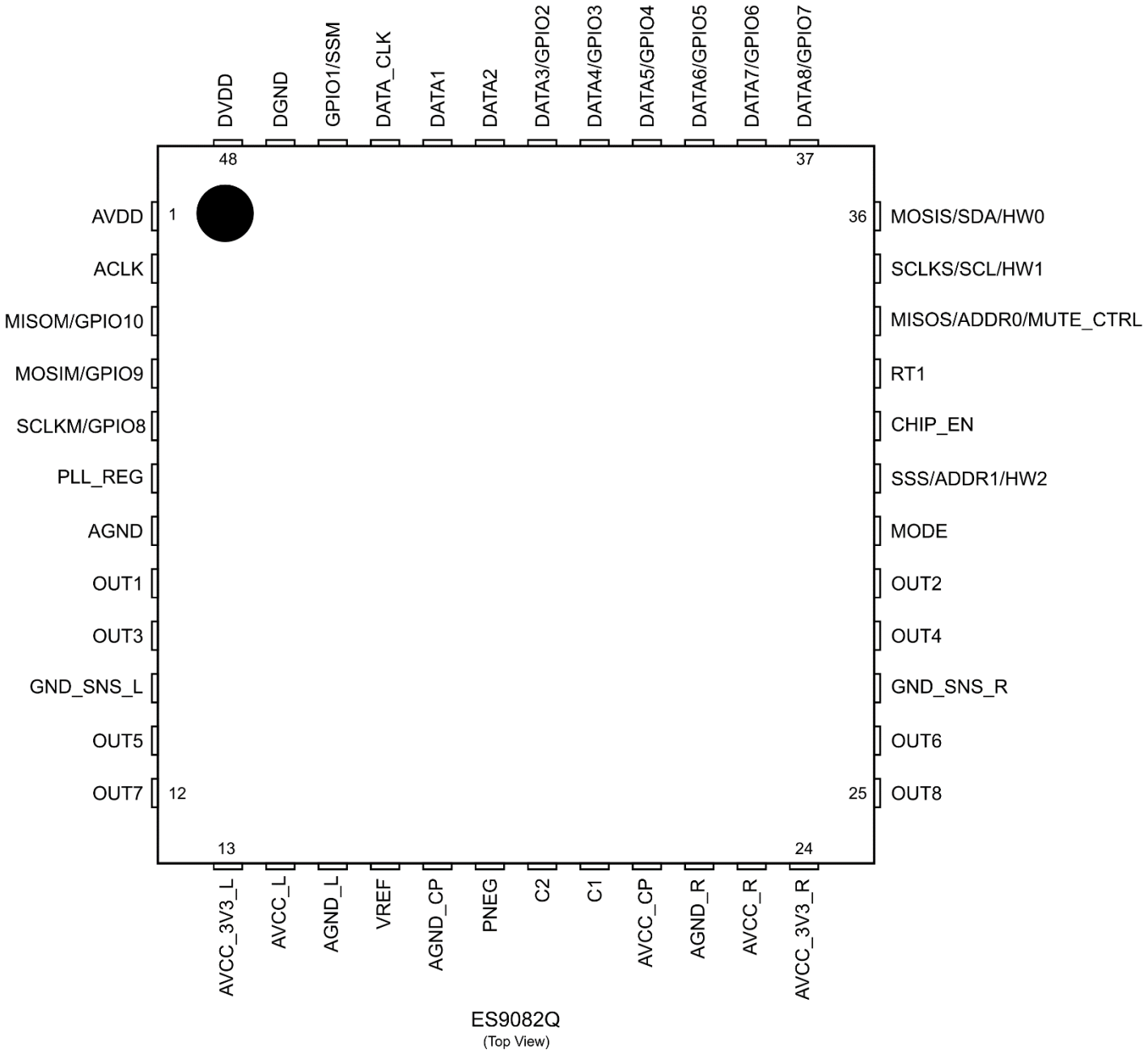


Figure 2 – ES9082 48QFN Pinout

48 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	AVDD	Power	Power	3.3V I/O supply
2	ACLK	Clock I	HiZ	Clock input
3	GPIO10	D I/O	HiZ	General I/O 10
	MISOM			SPI Main In Sub Out pin (Master), controlled by MODE
4	GPIO9	D I/O	HiZ	General I/O 9
	MOSIM			SPI Main Out Sub In pin (Master), controlled by MODE
5	GPIO8	D I/O	HiZ	General I/O 8
	SCLKM			SPI Serial Clock pin (Master), controlled by MODE
6	PLL_REG	A O	Ground	PLL Voltage Reference, Capacitor to ground
7	AGND	Ground	Ground	Analog ground
8	OUT1	A O	Ground	Output channel 1
9	OUT3	A O	Ground	Output channel 3
10	GND_SNS_L	A I	Ground	Line driver load ground voltage sense (left, CH 1,3,5,7)
11	OUT5	A O	Ground	Output channel 5
12	OUT7	A O	Ground	Output channel 7
13	AVCC_3V3_L	Power	Power	Analog Regulator 3.3V Supply (left)
14	AVCC_L	A O	P/D	Analog Regulator Output (left), internally supplied
15	AGND_L	Ground	Ground	Analog Ground (left)
16	VREF	A O	Ground	Bandgap Voltage reference
17	AGND_CP	Ground	Ground	Analog Ground for charge pump
18	PNEG	A O	P/D	Integrated charge pump output. Line driver negative supply.
19	C2	-	-	Line driver negative flying capacitor
20	C1	-	-	Line driver positive flying capacitor
21	AVCC_CP	Power	Power	Analog Supply for charge Pump
22	AGND_R	Ground	Ground	Analog Ground (right)
23	AVCC_R	A O	P/D	Analog regulator output (right), internally supplied
24	AVCC_3V3_R	Power	Power	Analog Regulator 3.3V Supply (right)
25	OUT8	A O	Ground	Output channel 8
26	OUT6	A O	Ground	Output channel 6
27	GND_SNS_R	A I	Ground	Line driver load ground voltage sense (right, CH 2,4,6,8)
28	OUT4	A O	Ground	Output channel 4
29	OUT2	A O	Ground	Output channel 2
30	MODE	D I/O	HiZ	I2C/SPI Control selection or HW mode
31	SSS	D I/O	HiZ	SPI Slave Select (Slave) pin, controlled by MODE

	ADDR1			I2C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
32	CHIP_EN	Reset	HiZ	Active-high Chip Enable
33	RT1	D I	HiZ	Reserved. **Must be connected to DGND for normal operation**.
34	MISOS	D I/O	HiZ	SPI Main In Sub Out pin (Slave), controlled by MODE
	ADDR0			I2C Address 0 pin, controlled by MODE
	MUTE_CTRL			Hardware Mute Control pin, controlled by MODE
35	SCLKS	D I/O	HiZ	SPI Serial Clock pin (Slave), controlled by MODE
	SCL			I2C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
36	MOSIS	D I/O	HiZ	SPI Main Out Sub In pin (Slave), controlled by MODE
	SDA			I2C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
37	DATA8	D I/O	HiZ	Serial DATA8
	GPIO7			General I/O 7
38	DATA7	D I/O	HiZ	Serial DATA7
	GPIO6			General I/O 6
39	DATA6	D I/O	HiZ	Serial DATA6
	GPIO5			General I/O 5
40	DATA5	D I/O	HiZ	Serial DATA5
	GPIO4			General I/O 4
41	DATA4	D I/O	HiZ	Serial DATA4
	GPIO3			General I/O 3
42	DATA3	D I/O	HiZ	Serial DATA3
	GPIO2			General I/O 2
43	DATA2	D I/O	HiZ	Serial DATA2
44	DATA1	D I/O	HiZ	Serial DATA1
45	DATA_CLK	D I/O	HiZ	Serial Data Clock pin
46	GPIO1	D I/O	HiZ	General I/O 1
	SSM			SPI Slave Select (Master) pin, controlled by MODE
47	DGND	Ground	Ground	Digital core ground
48	DVDD	A O	P/D	Digital core supply, internally supplied
49	Package Pad	-	-	Not electrically connected, used for heat dissipation

Table 1 – ES9082 48QFN Pin Descriptions

Configuration Modes

The ES9082 has 4 control programming modes which are controlled by the state of the MODE pin (Pin 30).

MODE PIN	Configuration
0	I²C Interface
Pull 0	HW control mode (see Hardware Mode Table)
Pull 1	HW control mode (see Hardware Mode Table)
1	SPI Interface

Table 2 - Mode Pin Configuration Options

Design Information

Hardware pins can be configured in 4 different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. These 4 options also apply to MUTE_CTRL.

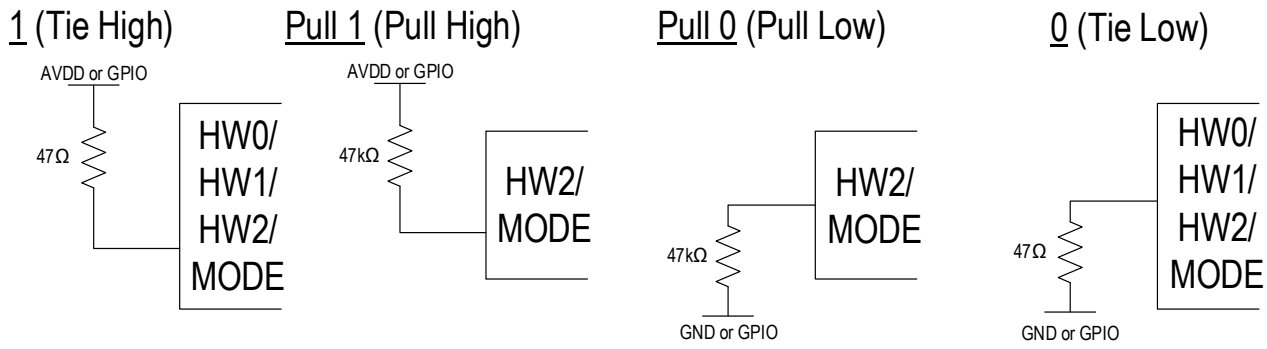


Figure 3 - Example Hardware Mode Pin Configurations

Software Mode

The ES9082 supports a slave I²C or SPI serial communication in software mode. There are two types of registers, read/write registers and read-only registers. Software modes are set when the MODE pin is a 0 (0V) for I²C or a 1 (AVDD) for SPI.

A system clock is not required to read and write registers.

I²C Slave Interface Commands

- MODE (Pin 30) – 0 (Tied-Low)
- Connect per I²C standard
  - SDA (Pin 36)
  - SCL (Pin 35)
  - ADDR0 (Pin 34)
  - ADDR1 (Pin 31)

I²C Address	ADDR1	ADDR0
0x90	GND	GND
0x92	GND	AVDD
0x94	AVDD	GND
0x96	AVDD	AVDD

Table 3 - I²C Addresses

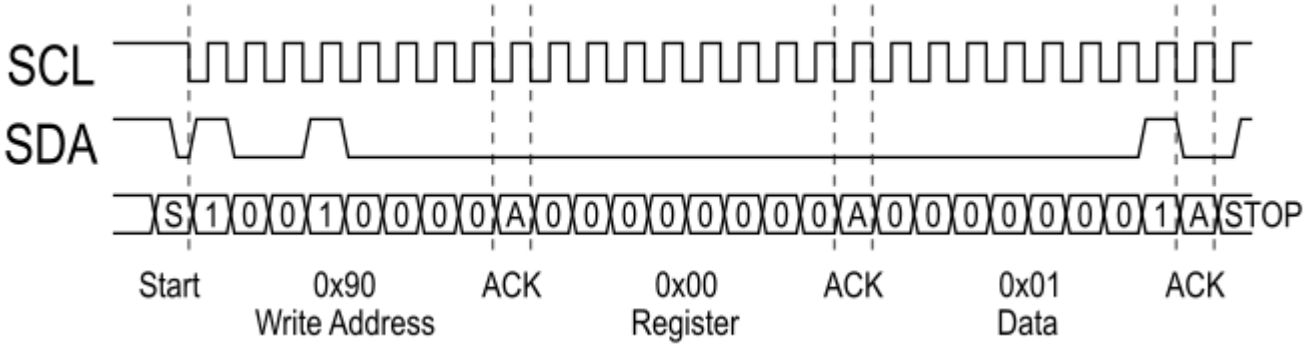


Figure 4 - I²C Write Example

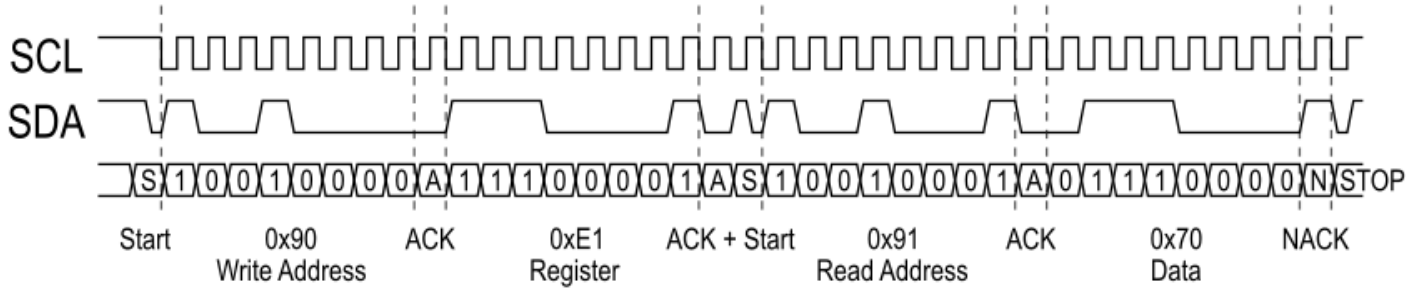


Figure 5 - I²C Read Example

Note: CHIP_ID is 0x70 in Register 225 (0xE1)

SPI Slave Interface Commands

- MODE (Pin 18) – 1 (Tied-High)
- Connect per SPI standard
  - MOSI (Pin 36)
  - SCLK (Pin 35)
  - MISO (Pin 34)
  - SS (Pin 31)

SPI Command	First Byte
Write	0x03
Read	0x01

Table 4 - SPI Commands

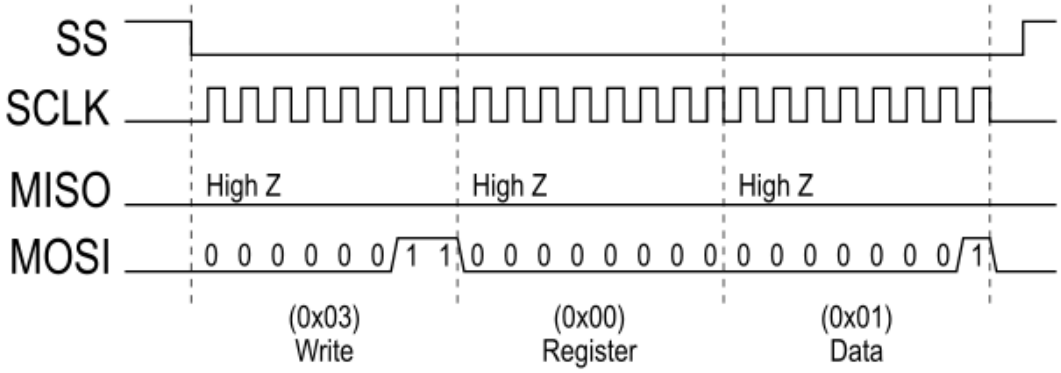


Figure 6 - SPI Single Byte Write

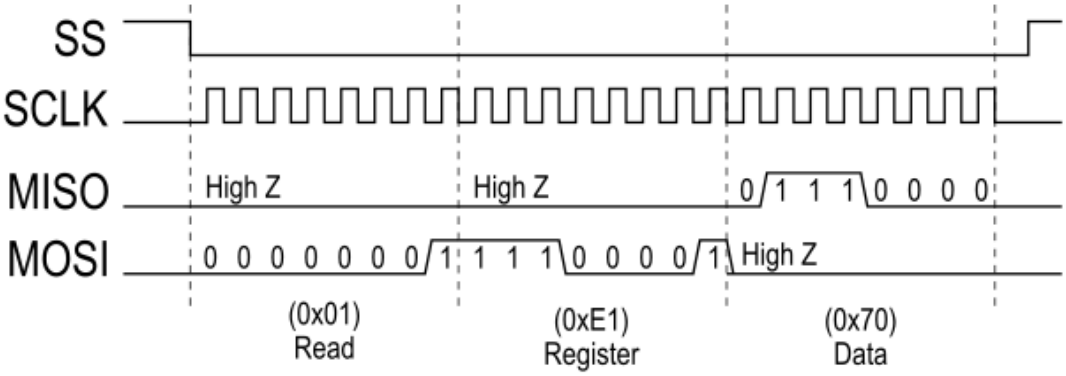


Figure 7 - SPI Single Byte Read

Note: CHIP_ID is 0x70 in Register 225 (0xE1)

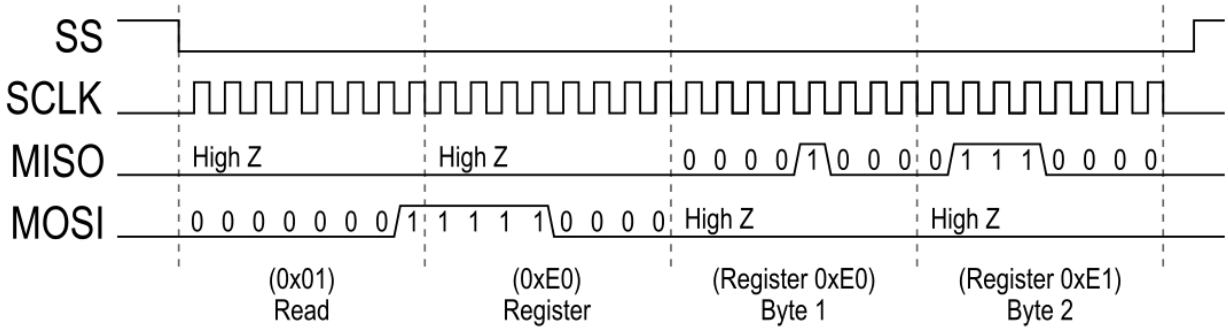


Figure 8 - SPI Multi Byte Read

Hardware Mode

The ES9082 has pre-configured modes that can be set with an external pin configuration. These modes configure the DAC for different input/output serial data rates and set the mute control. Hardware modes also support stereo digital PDM microphones as inputs. Each hardware mode pin has 4 states that can be found in Design Information.

These modes are set with pins:

- MODE (Pin 30)
- HW0 (Pin 36)
- HW1 (Pin 35)
- HW2 (Pin 31)
- MUTE_CTRL (Pin 34)

Recommended Hardware Mode Setup Sequence

The Hardware Mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

Note: MUTE_CTRL should be set to muted until the HW mode is finalized and after CHIP_EN is asserted, then it may be set to the correct clock rate and unmuted last. See Mute Control for more information.

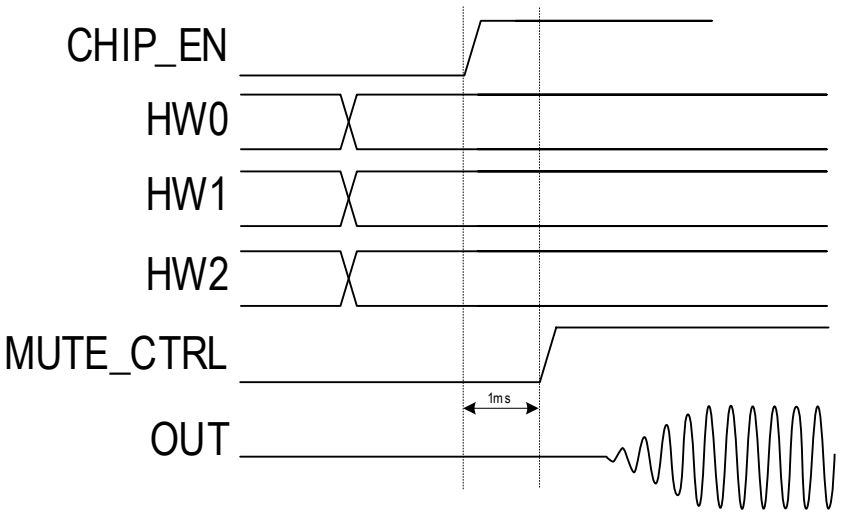


Figure 9 - Hardware Mode Startup Sequence

Hardware Pin Configurations

HW Mode	Mode Description	MCLK Source	PCM FS [kHz]	DoP Rate	DSD Rate	PDM Clock [MHz]	BCK[1] [MHz]	MODE	HW2	HW1	HW0
32-bit PCM/DoP/DSD/PCM Master Modes (Ext MCLK)											
0	I²S / DoP / DSD / PDM	Ext. MCLK	MCLK/128	DoP128/256	DSD512/1024	PDM24/49	MCLK/2 (64*FS)	Pull 0	0	0	0
1			MCLK/256	DoP64/128	DSD256/512	PDM12/24	MCLK/4 (64*FS)	Pull 0	0	0	1
2	I²S / DSD / PDM		MCLK/512	-	DSD128/256	PDM6/12	MCLK/8 (64*FS)	Pull 0	0	1	0
3			MCLK/1024	-	DSD64/128	PDM3/6	MCLK/16 (64*FS)	Pull 0	0	1	1
4	LJ / DoP / DSD / PDM		MCLK/128	DoP128/256	DSD512/1024	PDM24/49	MCLK/2 (64*FS)	Pull 0	Pull 0	0	0
5			MCLK/256	DoP64/128	DSD256/512	PDM12/24	MCLK/4 (64*FS)	Pull 0	Pull 0	0	1
6	LJ / DSD / PDM		MCLK/512	-	DSD128/256	PDM6/12	MCLK/8 (64*FS)	Pull 0	Pull 0	1	0
7			MCLK/1024	-	DSD64/128	PDM3/6	MCLK/16 (64*FS)	Pull 0	Pull 0	1	1
32-bit PCM/DoP/DSD/PCM Slave Modes (PLL and Ext MCLK)											
8	I²S / DoP / DSD / PDM Auto FS	Ext. MCLK	8 ≤ FS ≤ 768	DoP64 - 256	DSD64 - DSD1024	0.375 ≤ PDM ≤ 24	64*FS	Pull 0	Pull 1	0	0
9	I²S / DSD / PDM	PLL from BCK	48	-	DSD64	PDM3	3.072	Pull 0	Pull 1	0	1
10			96	-	DSD128	PDM6	6.144	Pull 0	Pull 1	1	0
11			192	-	DSD256	PDM12	12.288	Pull 0	Pull 1	1	1
12	LJ / DoP / DSD / PDM Auto FS	Ext. MCLK	8 ≤ FS ≤ 768	DoP64 - 256	DSD64 - DSD1024	0.375 ≤ PDM ≤ 24	64*FS	Pull 0	1	0	0
13	LJ / DSD / PDM	PLL from BCK	48	-	DSD64	PDM3	3.072	Pull 0	1	0	1
14			96	-	DSD128	PDM6	6.144	Pull 0	1	1	0
15			192	-	DSD256	PDM12	12.288	Pull 0	1	1	1

Table 5 - Hardware Pin Configurations, Modes 0-15

See Table Continuation on next page.

[1] For master mode DoP, DSD, and PDM, the BCKs frequency is doubled.

Hardware Pin Configurations Pt2.

HW Mode	Mode Description	MCLK Source	TDM Mode	PCM FS [kHz]	BCK [MHz]	TDM Channels	TDM Slots	MODE	HW2	HW1	HW0
32-bit TDM LJ Slave Modes, Autodetect FS & CH Num											
16	32-Bit TDM LJ Slave Auto FS Auto CH num	Ext. MCLK	Daisy Chain	8 ≤ FS ≤ 192	Auto (256FS, 512FS, 1024FS)	8 ≤ CH ≤ 32	1 - 8	Pull 1	0	0	0
17				8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	16 ≤ CH ≤ 32	9 - 16	Pull 1	0	0	1
18				8 ≤ FS ≤ 48	Auto (1024FS)	32	17 - 24	Pull 1	0	1	0
19				8 ≤ FS ≤ 48	Auto (1024FS)	32	25 - 32	Pull 1	0	1	1
20			Parallel	8 ≤ FS ≤ 192	Auto (256FS, 512FS, 1024FS)	8 ≤ CH ≤ 32	1 - 8	Pull 1	Pull 0	0	0
21				8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	16 ≤ CH ≤ 32	9 - 16	Pull 1	Pull 0	0	1
22				8 ≤ FS ≤ 48	Auto (1024FS)	32	17 - 24	Pull 1	Pull 0	1	0
23				8 ≤ FS ≤ 48	Auto (1024FS)	32	25 - 32	Pull 1	Pull 0	1	1
16-bit TDM LJ Slave Modes, Autodetect FS & CH Num											
24	16-Bit TDM LJ Slave Auto FS Auto CH num	Ext. MCLK	Daisy Chain	8 ≤ FS ≤ 384	Auto (128FS, 256FS, 512FS)	8 ≤ CH ≤ 32	1 - 8	Pull 1	Pull 1	0	0
25				8 ≤ FS ≤ 192	Auto (256FS, 512FS)	16 ≤ CH ≤ 32	9 - 16	Pull 1	Pull 1	0	1
26				8 ≤ FS ≤ 96	Auto (512FS)	32	17 - 24	Pull 1	Pull 1	1	0
27				8 ≤ FS ≤ 48	Auto (512FS)	32	25 - 32	Pull 1	Pull 1	1	1
28			Parallel	8 ≤ FS ≤ 384	Auto (128FS, 256FS, 512FS)	8 ≤ CH ≤ 32	1 - 8	Pull 1	1	0	0
29				8 ≤ FS ≤ 192	Auto (256FS, 512FS)	16 ≤ CH ≤ 32	9 - 16	Pull 1	1	0	1
30				8 ≤ FS ≤ 96	Auto (512FS)	32	17 - 24	Pull 1	1	1	0
31				8 ≤ FS ≤ 48	Auto (512FS)	32	25 - 32	Pull 1	1	1	1

Table 6 - Hardware Pin Configurations, Modes 16-31

GPIO Functions in Hardware Mode

The ES9082 supports specific functions using GPIO pins in hardware mode. The tables below show the available options including DAC Input Select, Automute, and the choice between two digital filters in various input modes.

Input Format	Supported HW Modes	[GPIO9, GPIO10]	Input/Output
I²S/LJ	0 - 15	2'b00	Input
DSD		2'b10	Input
PDM		2'b11	Input
DoP	0, 1, 4, 5, 8, 12	2'b01	Input
TDM (Daisy Chain)	16 - 19 & 24 - 27	-	High Z
TDM (Parallel)	20 - 23 & 28 - 31	-	High Z

Table 7 - DAC Input Select with GPIO9 & GPIO10 in Hardware Mode

GPIO1	Input Format	Filter
1'b0	I²S/LJ, TDM	Filter 0 Minimum Phase
1'b1		Filter 2 Linear Phase Fast Roll-Off

Table 8 - DAC Filter Select with GPIO1 in Hardware Mode

GPIO8	Automute
1'b0	Disabled
1'b1	Enabled

Table 9 - DAC Automute with GPIO8 in Hardware Mode

Mute Control

Set MUTE_CTRL (Pin 34) to mute the output while in Hardware Mode:

HW MUTE Control (Pin 34)	Condition	MCLK
0	Mute	24.576MHz
1	Unmute	24.576MHz
Pull 0	Mute	49.152MHz
Pull 1	Unmute	49.152MHz

Table 10 - Mute Control in Hardware Mode

Note: If MUTE_CTRL (Pin 34) is set to the incorrect MCLK rate, the DAC may have less output performance.

Digital Features

Audio Input/Output Formats

The ES9082 supports multiple serial input data formats. Input format is selected either through Hardware Mode or Software Mode.

The ES9082 can automatically determine the input data format (PCM, DSD and DoP Only) by enabling Register 1[0] AUTO_INPUT_SEL, data must be provided on the DATA2 pin to properly decode the input format. The input data format can also be selected using Register 1[2:1] INPUT_SEL.

The formats include:

- PCM
  - Slave and master mode in 16, 24, 32 - bit widths
  - I²S, and Left Justified (LJ)
  - Sample rates up to 768kHz (64fs mode)
  - Channel remapping & invert
- TDM
  - Up to 32 slots including daisy chain mode
  - Slave mode in hardware mode. Slave and master modes in software mode
  - LJ format in hardware modes. I²S or LJ in software modes
  - Channel remapping & invert
- DoP (DSD Over PCM)
  - Slave and master mode
  - Sample rates to DoP256 (24bit, 705.5kHz PCM)
  - Channel mapping & invert
- DSD
  - Slave and master mode
  - Sample rates from DSD64 (2.8224Mbits/s, 64x44.1kHz) to DSD1024
  - Channel mapping & invert
- PDM
  - Slave and master mode
  - Channel mapping & invert
- S/PDIF
  - Stereo 2 Channel output
  - Channel Select
  - Sample rates up to 192kHz

PCM/TDM Decoder

The ES9082 integrates a PCM/TDM Decoder whose input has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The decoder allows for I²S, LJ, and TDM input streams.

The PCM/TDM decoder can support up to 32 different slots and each channel of the DAC can be mapped to any of the 32 slots.

PCM/TDM Decoder/Encoder Registers

- Register 6[7] TDM_RESYNC
- Register 6[6] AUTO_CH_DETECT
- Register 6[4:0] TDM_CH_NUM
- Register 7[7] ENABLE_WS_MONITOR
- Register 7[6] ENABLE_BCK_MONITOR
- Register 7[5:4] TDM_WORD_WIDTH
- Register 7[3:2] TDM_BIT_DEPTH
- Register 7[1] TDM_VALID_EDGE
- Register 7[0] TDM_LJ

PCM/TDM Decoder Mapping Registers

- Register 8-15[6:5] TDM_LINE_SEL_CHx
- Register 8-15[4:0] TDM_SLOT_SEL_CHx

Daisy Chain Registers

- Register 18[7] TDM_DAISY_CHAIN
- Register 18[6:5] TDM_DAISY_CHAIN_LINE_IN
- Register 18[4:0] TDM_DATA_LATCH_ADJ

PCM/TDM Encoder

The ES9082 integrates a PCM/TDM Encoder whose output has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The decoder can output a single line through DATA7 and allows for I²S, LJ, and TDM output streams.

The PCM/TDM Encoder can support up to 32 different slots and each channel of the DAC can be mapped to any of the 32 slots.

The PCM/TDM Encoder and PCM/TDM Decoder use the same format settings but have independent slot and line settings.

Note: Daisy Chain is not supported on the PCM/TDM Encoder.

PCM/TDM Encoder Mapping Registers

- Register 23[0] ENABLE_TDM_ENCODE
- Register 26-33[4:0] TDM_ENC_SLOT_SEL_CHx

PCM (I²S, LJ) Format

The input data is organized into 2 channels per data line, on up to 5 data lines. Each input data slot can be mapped to any DAC channel using Register 8-15[4:0] TDM_SLOT_SEL_CHx. Input data is latched on the positive edge of BCLK.

PCM Pin Connections:

Pin Name	Function	Description
DATA_CLK	PCM BCLK	PCM Clock (Bit Clock), Master or Slave
DATA1	PCM WS	PCM WS (Word Select/Frame Select), Master or Slave
DATA2	PCM DATA1	PCM Data Channel 1 & 2 (default)
DATA3	PCM DATA2	PCM Data Channel 3 & 4 (default)
DATA4	PCM DATA3	PCM Data Channel 5 & 6 (default)
DATA5	PCM DATA4	PCM Data Channel 7 & 8 (default)
DATA6	PCM MIX DATA	PCM Mix Channel 1 & 2

Table 11 - PCM Pin Connections

The ES9082 can accommodate an additional 2 channels of data (DATA6) using either I²S or TDM formats with the 8 normal DAC channels. These 2 channels can be incorporated into the ASP functionality for the purpose of mixing with other channels. See Figure 10 - ES9082 I2S 10 Channel Configuration for a 10 channel I²S configuration.

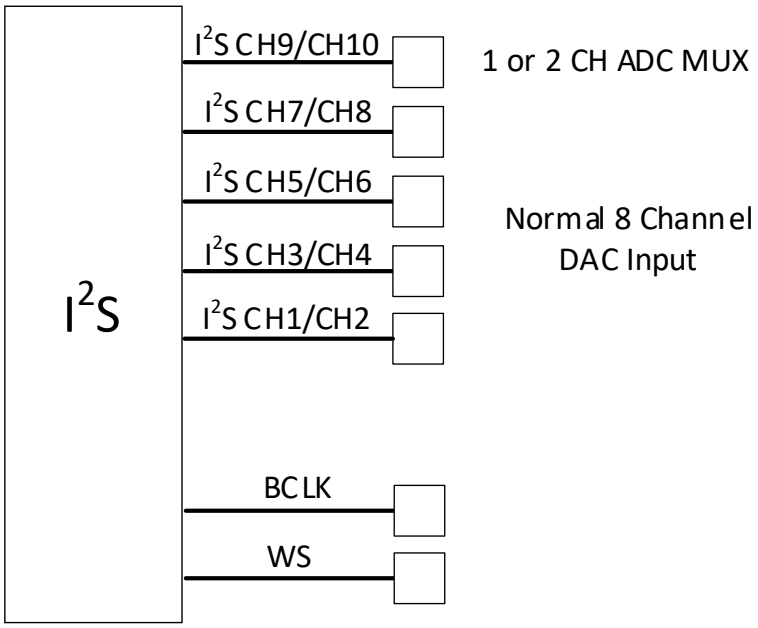


Figure 10 - ES9082 I²S 10 Channel Configuration

Note: To enable the Mix input on DATA6, Register 16-17[13] TDM_MIX_DATA6_EN must be set.

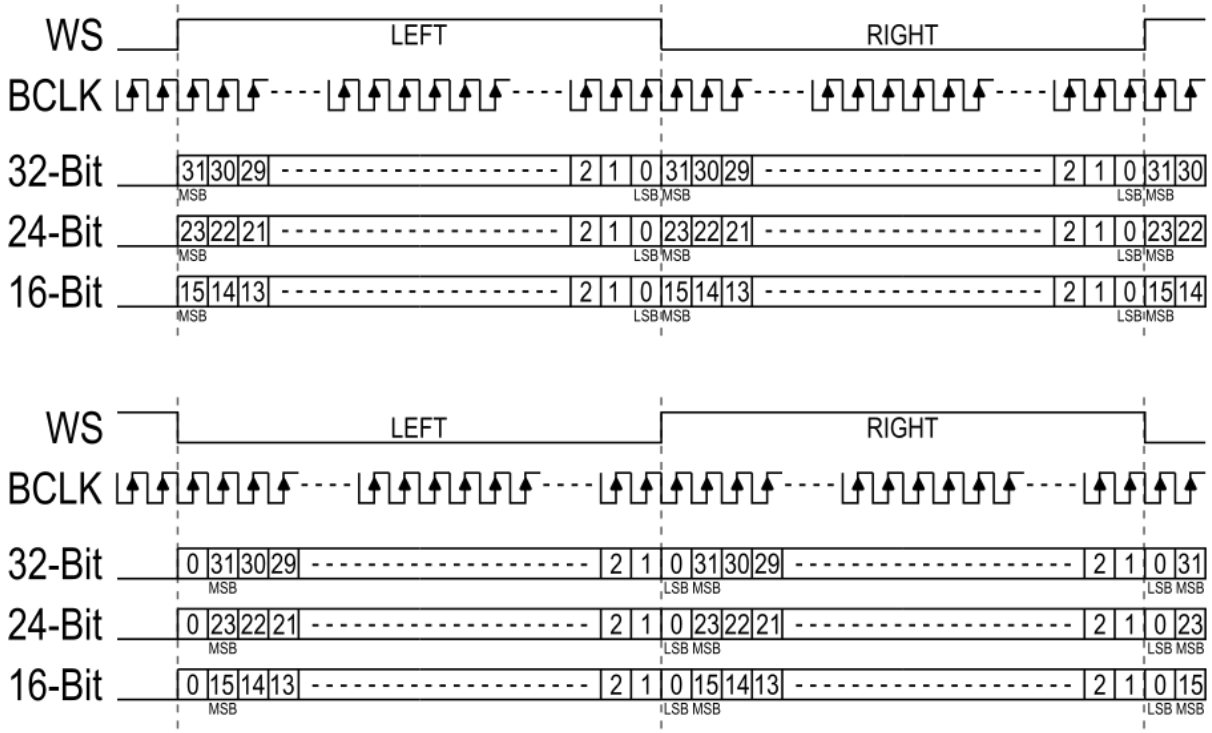


Figure 11 - LJ (top) & I²S (bottom) for 16,24, and 32-bit Word Widths

TDM Format

The ES9082 supports TDM format, allowing for 2 to 32 channels on a single data line. TDM is supported in both software and hardware modes with the TDM data line to be input through DATA2. Input data is latched on the positive edge of BCLK.

Hardware modes each have their own slots that the eight audio channels maps to. For example, in the case of TDM32 (32CH), the hardware mode will be configured so that slots 1 through 8 will map to one device (HW mode #16), slots 9 through 16 will map to a second device (HW mode #17), slots 17 through 24 will map to a third device (HW mode #18), up to slots 25 through 32 mapping to a 4th device respectively (HW mode #19).

In software mode, Registers 8-15 [4:0] TDM_SLOT_SEL_CHx can be set to internally map any slot to any DAC channel.

TDM Pin Connections:

Pin Name	Function	Description
DATA_CLK	TDM BCLK	TDM Clock, Master, or Slave
DATA1	TDM WS	TDM WS (Word Select/Frame Select), Master or Slave
DATA2	TDM DATA1	TDM DATA Channel 1 & 2 (default)
DATA3	TDM DATA2	TDM DATA Channel 3 & 4 (default)
DATA4	TDM DATA3	TDM DATA Channel 5 & 6 (default)
DATA5	TDM DATA4	TDM DATA Channel 7 & 8 (default)

Table 12 - TDM Pin Connections

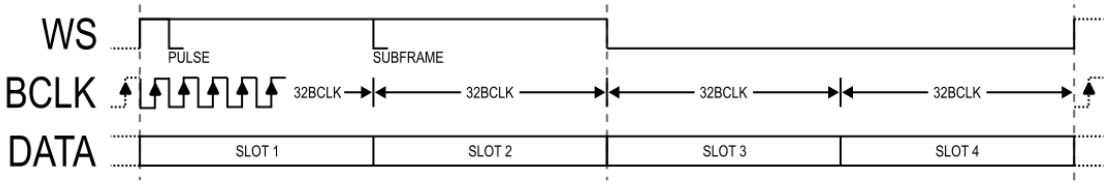


Figure 12 - TDM4 Mode

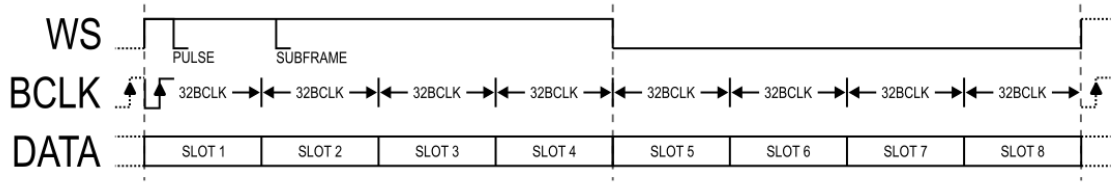


Figure 13 - TDM8 Mode

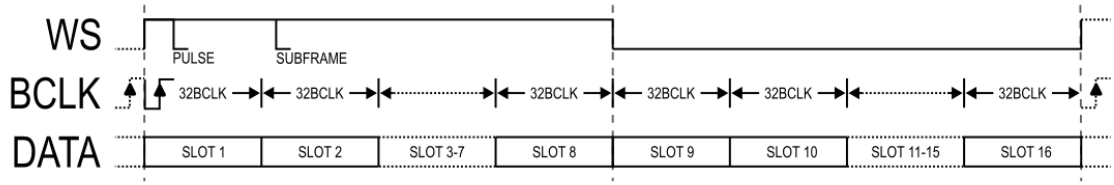


Figure 14 - TDM16 Mode

DSD Format

In DSD mode, there is a single DSD clock line, and each channel of data is an additional DSD data line. Each DSD source can be remapped to any DAC channel by using the below registers.

DSD Channel Mapping Registers

- Register 19-22[5:3][2:0] DSD_LINE_SEL_CHx

DSD Pin Connections:

Pin Name	Function	Description
DATA_CLK	DSD CLK	DSD Clock
DATA1	DSD CH1	DSD DATA Channel 1
DATA2	DSD CH2	DSD DATA Channel 2
DATA3	DSD CH3	DSD DATA Channel 3
DATA4	DSD CH4	DSD DATA Channel 4
DATA5	DSD CH5	DSD DATA Channel 5
DATA6	DSD CH6	DSD DATA Channel 6
DATA7	DSD CH7	DSD DATA Channel 7
DATA8	DSD CH8	DSD DATA Channel 8

Table 13 - DSD Pin Connections

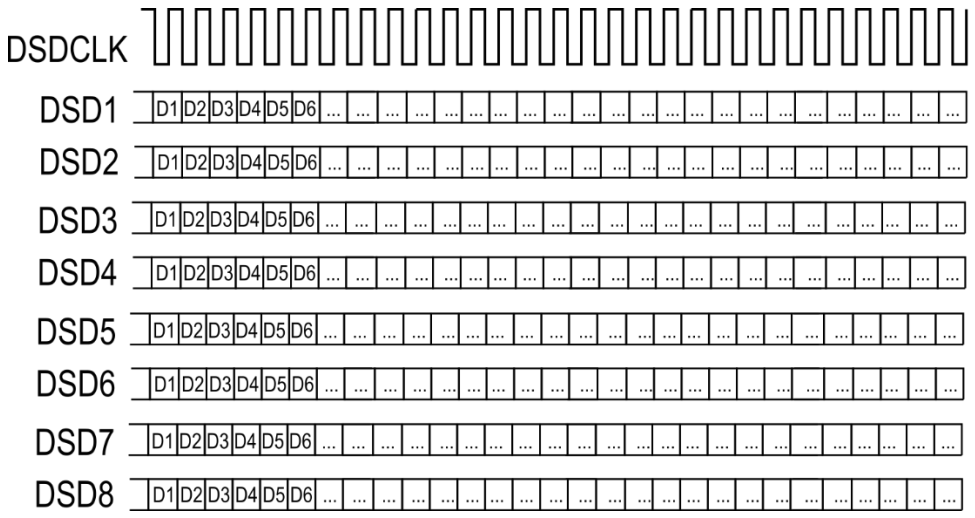


Figure 15 - DSD Format, 1-bit stream

PDM Decoder

PDM Data is input through the PDM decoder to be converted to DSD internally, following the rest of the respective internal data path including the DSD Channel Mapping, Automute, and DSD FIR and Volume blocks.

PDM Decoder Registers

- Register 1[7] ENABLE_PDM_DECODE
- Register 19[7] PDM_DATA_PHASE
- Register 19[6] PDM_FRAME_EDGE
- Register 20[6] PDM_2X_GAIN_EN

PDM Format

In PDM mode, there is a single PDM clock line and a multiple PDM data lines containing two channels of data each. The channels can be swapped by setting Register 19[7] PDM_DATA_PHASE.

Pin Name	Function	Description
DATA_CLK	PDM CLK	PDM Clock
DATA1	PDM DATA1	PDM Data Channel 1 & 2
DATA2	PDM DATA2	PDM Data Channel 3 & 4
DATA3	PDM DATA3	PDM Data Channel 5 & 6
DATA4	PDM DATA4	PDM Data Channel 7 & 8

Table 14 - PDM Pin Connections

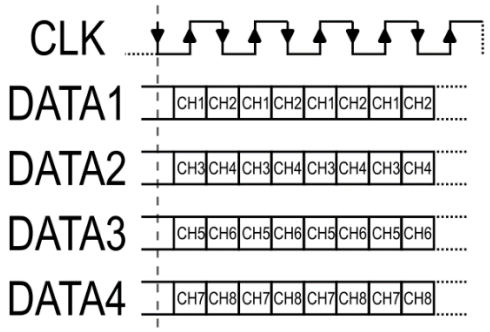


Figure 16 - PDM 8 Channel Format

S/PDIF Encoder

The ES9082 features a stereo S/PDIF encoder that can directly output a pair of channels (1/2, 3/4, 5/6, 7/8) from after the ASP or the TDM mix signal being output by the PCM/TDM Decoder. The S/PDIF channel status bits can be updated one byte at a time using the below address and data registers and toggling the write enable register to set the status bits.

S/PDIF Encoder Registers

- Register 23[4] SPDIF_MIX_DATA_SEL
- Register 23[3:2] SPDIF_CH_PAIR_SEL
- Register 23[1] ENABLE_SPDIF_ENCODE
- Register 24[7] SPDIF_CS_WE
- Register 24[2:0] SPDIF_CS_BYTE_ADDR
- Register 25[7:0] SPDIF_CS_BYTE_DATA

Digital Signal Path

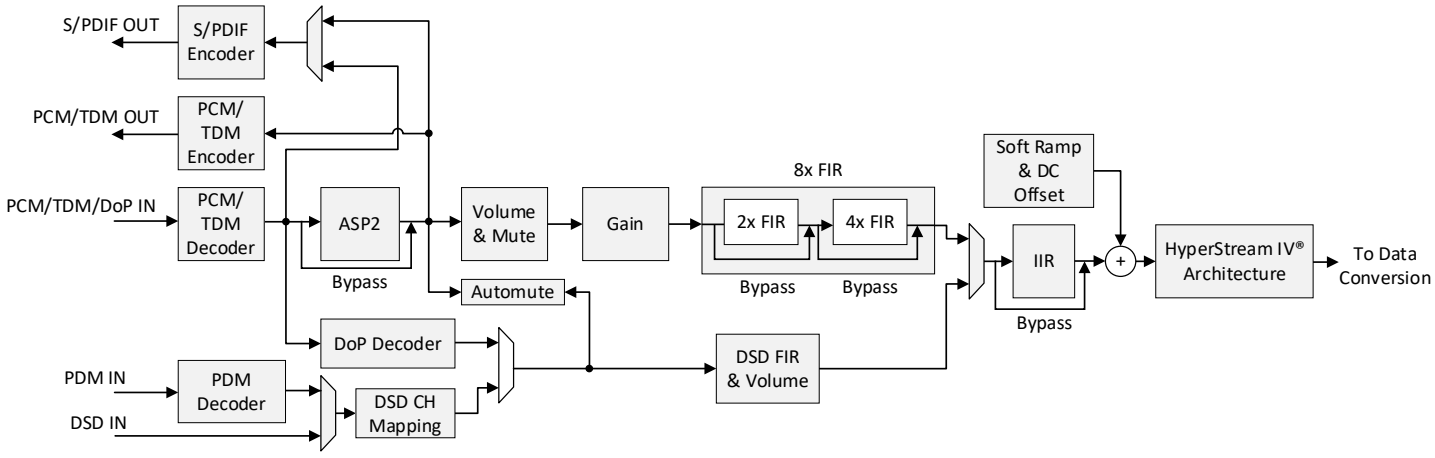


Figure 17 - Digital Signal Path

ASP2 (Audio Signal Processor)

The ES9082 SMART DAC incorporates a 2nd generation ESS Audio Signal Processor (ASP2) that allows customers to integrate their preferred audio algorithms by using ESS' proprietary SABRE Intelligence Studio (SIS) graphical software tool. In addition, a 2-channel input is available to mix a secondary stereo source such as a microphone monitor into ASP2

The ES9082 ASP2 is a very versatile Audio Signal Processor that can allow up to 512 instructions per sample depending on sample rate. It has a 32-bit internal data path with real-time operation. The ASP2 can be programmed using the slave I²C, slave SPI interfaces or with the SPI master interface with an optional external SPI Flash memory for very fast program loading and for storing multiple configuration programs.

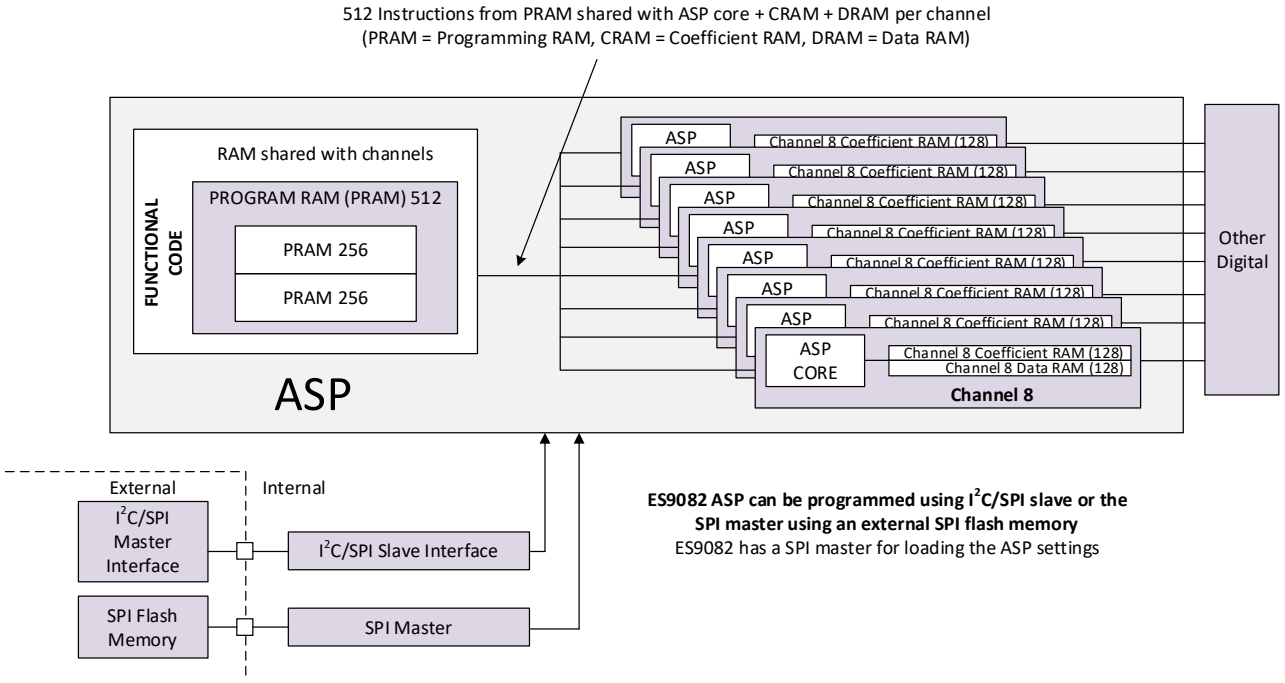


Figure 18 - Top level view of ES9082 ASP2

The ASP2 can be programmed to represent (among others):

- High-efficiency IIR/Biquad filters
- Mixers
- Parametric Equalizers (PEQ), including 25 band PEQs
- Multi-band Dynamic Range Compression (DRC) operations
- Automatic Gain Limiters (AGL)
- Specialty filters including Crossovers & RIAA Equalization de-emphasis filters
- Stereo Widening
- Audio Expansion and Compression

The integration of the ASP2 into the datapath alleviates processing requirements on the system processor and helps simplify system design.

The ES9082 can be programmed using ESS' proprietary SABRE Intelligence Studio (SIS) graphical software tool. For more information on the ASP2 or SIS tool, please contact your local ESS FAE or distributor for availability.

SPI Master Flash

The ES9082 features an SPI master interface for programming an ASP program quickly from a SPI Flash device. The SPI master can receive I²C or SPI slave commands, convert them to the SPI master and program/burn the SPI flash. In addition, the SPI master can read from the SPI flash and program the ASP at SPI high speed clock rates (up to MCLK/2).

Any SPI Serial Flash can be used to store the programmable instructions and coefficients for the ASP. The programming will change depending on the specific architecture of the SPI flash and the MCU used to send the instructions. To program the SPI flash with an ASP program, the memory offset, the 32-bit array of instructions and the 32-bit arrays of coefficients must be known.

Note: Figure 31 - Example SPI Flash Schematic shows the connections to the ES9082 using the W25X40CLSNIG 4-Mbit, 3.3V, SPI Serial Flash.

Volume Control

The Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

The ES9082 also features the ability to manually mute specific channels, invert the volume control phase as well as control all channel volumes with the CH1 volume control.

Volume Control Registers

- Register 87-94 VOLUME CHx
- Register 102 VOLUME UP RAMP RATE
- Register 103 VOLUME DOWN RAMP RATE
- Register 100 MUTE
- Register 95 PHASE INVERSION
- Register 101[6] MONO_VOLUME

Gain

The ES9082 has a digital pre-gain of up to +42dB in 6 dB (+6,+12,+18,+24,+30,+36,+42) steps.

Gain Registers

- Register 99-96 DIGITAL GAIN

The digital pre-gain and volume control can be used together for finer resolution. Figure 19 shows the available ranges:

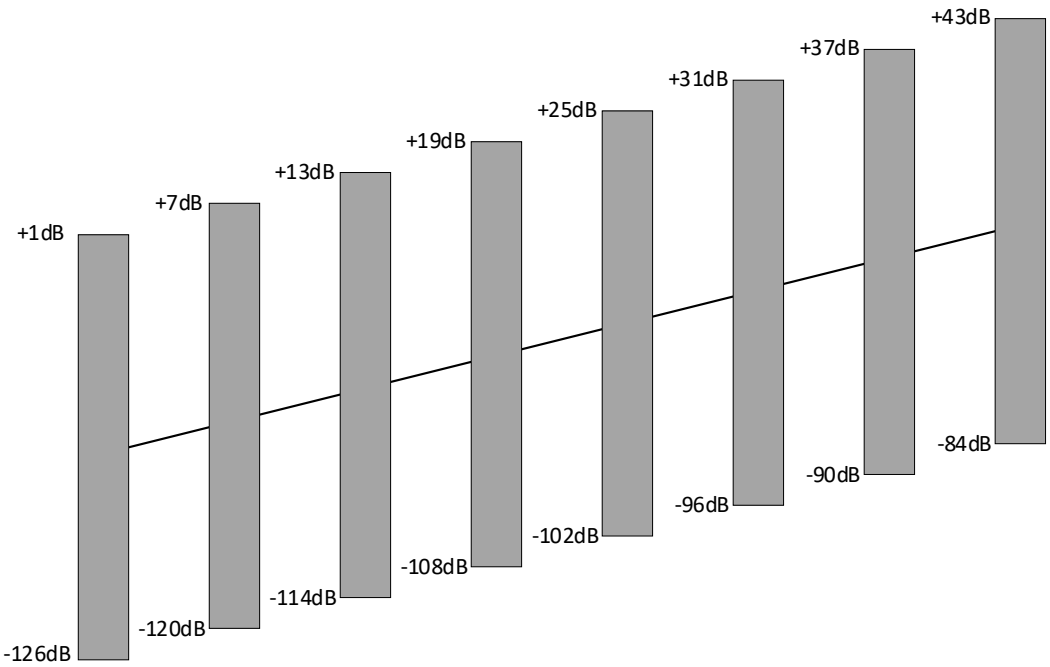


Figure 19 - ES9082 Volume Range

Automute

The ES9082 features an automute that triggers when the signal is below the specified level for longer than the specified time. The automute will disengage when the signal is above the specified off value for the same amount of time.

Note: Automute in DSD mode has additional registers that require configuration. Automute will trigger if it detects a DC level or automute patterns for the duration of AUTOMUTE_TIME.

$$Time[s] = \frac{2^{18} * 2^{64FS\_MODE}}{AUTOMUTE\_TIME * FS}$$

$$Level[dB] = \frac{20 * log_{10}(AUTOMUTE\_LEVEL)}{(2^{16} - 1) * 2^{7}}$$

$$Level_{OFF}[dB] = \frac{20 * log_{10}(AUTOMUTE\_OFF\_LEVEL)}{(2^{16} - 1) * 2^{7}}$$

Automute Registers

- Register 105 AUTOMUTE ENABLE
- Register 106-107 [10:0] AUTOMUTE_TIME
- Register 108-109 AUTOMUTE_LEVEL
- Register 110-111 AUTOMUTE_OFF_LEVEL

DSD Automute Settings Registers

- Register 106-107[15] DSD_FAULT_DETECT_EN
- Register 106-107[14] DSD_DC_AM_ENB
- Register 106-107[13] DSD_MUTE_AM_ENB

8x FIR Filter

Selection of the 8x interpolation filter is chosen from 8 pre-programmed filters. The 2x and 4x filter can be bypassed individually or together. For more information on filters see the Pre-Programmed Digital Filters section.

8x FIR Registers

- Register 86[2:0] FILTER_SHAPE
- Register 86[3] BYPASS_FIR2X
- Register 86[4] BYPASS_FIR4X

IIR Filter

The IIR filter can be bypassed using Register 86[5] BYPASS_IIR

Soft Ramp & DC Offset

The ES9082 saves power by ramping to ground during a normal mute condition. This includes automute, register mute, and GPIO mute.

A DC offset can be added to the CH1 datapath signal in 100uV increments.

Soft Ramp & DC Offset Registers

- Register 101[5] MUTE_RAMP_TO_GROUND
- Register 101[4:0] SOFT_RAMP_TIME
- Register 104 DC_OFFSET

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	Analog Outputs Off	Shutdown
1	Output 1'b0	Output
2	Output 1'b1	Output
3	Clock Valid	Output
4	PLL Locked Flag	Output
5	DAC Minimum Volume Flag	Output
6	DAC Automute Status	Output
7	DAC Soft Ramp Done Flag	Output
8	Mute DAC	Input
9	System Mode Control	Input
10	OR of Status Bits	Output
11	S/PDIF Stream	Output
12	PWM Signal	Output
13	MCLK_128FS	Output
14	Reserved	-
15	Reserved	-

Table 15 - GPIO Configuration

Analog Outputs Off

The GPIO is shutdown and has no functionality.

Output 1'b0

Outputs a constant 1'b0.

Output 1'b1

Outputs a constant 1'b1.

Clock Valid

Outputs HIGH if a MCLK source is detected. Outputs LOW when clock is removed or not present.

Note: Must have Register 3[1] EN_CLK_DET set for detection circuit to function.

PLL Locked Flag

Outputs HIGH if the PLL is locked.

DAC Minimum Volume Flag

Outputs HIGH when the DAC is muted. This can occur from manually muting via GPIO or a register, automuting, setting volume to 0xFF, loss of PLL lock, or an invalid MCLK/BCK ratio is detected via Register 7[6] ENABLE_BCK_MONITOR.

Relevant Registers

- Register 74-75[13] GPIO_AND_VOL_MIN sets the output to be the logical AND of both channels' mute flags.
- Register 76-77[13] GPIO_OR_VOL_MIN sets the output to be the logical OR of both channels' mute flags.

DAC Automute Status

Outputs HIGH when the DACs automute condition is met.

Relevant Registers

- Register 74-75[14] GPIO_AND_AUTOMUTE sets the output to be the logical AND of both channels' automute flags.
- Register 76-77[14] GPIO_OR_AUTOMUTE sets the output to be the logical OR of both channels' automute flags.

DAC Soft Ramp Done Flag

Outputs HIGH when the DAC is neither ramping up nor down.

Relevant Registers

- Register 74-75[15] GPIO_AND_SS_RAMP sets the output to be the logical AND of both channels' automute flags.
- Register 76-77[15] GPIO_OR_SS_RAMP sets the output to be the logical OR of both channels' automute flags.

Mute DAC

Mute all DAC channels.

System Mode Control

Sets the ability to turn the DAC on and off via a GPIO.

Relevant Registers

- Register 72-73[14] GPIO_FSM_MODE sets whether the GPIO has an enable or enable-bar (disable) functionality
  - GPIO_FSM_MODE = 1'b0: Disable datapath when the GPIO input is 1'b1
  - GPIO_FSM_MODE = 1'b1: Enable datapath when the GPIO input is 1'b1.
- Note: When GPIO_FSM_MODE = 1'b0, the system mode will be determined by Register 0[0] ENABLE_DAC_REG

OR of Status Bits

Outputs the logical OR of all the currently masked status flags.

Relevant Registers

- Registers 36-38 STATUS BITS MASKP 1-4
- Registers 39-43 STATUS BITS MASKN 1-4
- Registers 44-47 STATUS BITS CLEAR 1-4

S/PDIF Stream

Outputs the S/PDIF stream. Requires Register 23[1] ENABLE_SPDIF_ENCODE to be set.

PWM Signal

Outputs a configurable PWM signal. The frequency and duty cycle of the PWM signal can be calculated with the following equations:

$$frequency\ [Hz] = \frac{MCLK}{PWM\_FREQ + 1}$$

$$Duty\ Cycle\ [\%] = \left(\frac{PWM\_COUNT}{PWM\_FREQ + 1}\right) \times 100$$

Relevant Registers

- Register 82 PWM COUNT
- Register 83-84 PWM FREQUENCY

MCLK_128FS

Outputs the MCLK_128FS clock. Requires the DAC to be on.

$$\text{MCLK\_128FS} = \frac{\text{FS} * 2^7}{2^{64\text{FS\_MODE}}}$$

Pre-Programmed Digital Filters

The ES9082 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 86[2:0] FILTER_SHAPE for configuration)

#	Filter	Description
1	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection
2	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55FS
4	Linear Phase Fast Roll-Off Low-Ripple	Sabre legacy filter, optimized for in-band ripple
5	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
6	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
7	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
8	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 16 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase (default)	5.34 / FS
Linear Phase Apodizing Fast Roll-Off	34.7 / FS
Linear Phase Fast Roll-Off	35.33 / FS
Linear Phase Fast Roll-Off Low-Ripple	33.27 / FS
Linear Phase Slow Roll-Off	7.78 / FS
Minimum Phase Fast Roll-Off	5.32 / FS
Minimum Phase Slow Roll-Off	4.36 / FS
Minimum Phase Fast Roll-Off Low Dispersion	11.3 / FS

Table 17 - PCM Filter Latency

PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-96.61 dB	0.55 FS			Hz
Group Delay		2.91/FS		9.01/FS	s
Flatness (ripple)	0.0013				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 FS	Hz
Stop band	-106.1 dB	0.50 FS			Hz
Group Delay			32.81 FS		s
Flatness (ripple)	0.0029				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 FS	Hz
Stop band	-110.5 dB	0.55 FS			Hz
Group Delay			33.43/FS		s
Flatness (ripple)	0.0032				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-89.1 dB	0.55 FS			Hz
Group Delay			31.37/FS		s
Flatness (ripple)	0.0013				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.44 FS	Hz
Stop band	-90.7	0.75 FS			Hz
Group Delay			5.87/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-97.96 dB	0.55 FS			Hz
Group Delay		2.91/FS		9.14/FS	s
Flatness (ripple)	0.0023				dB

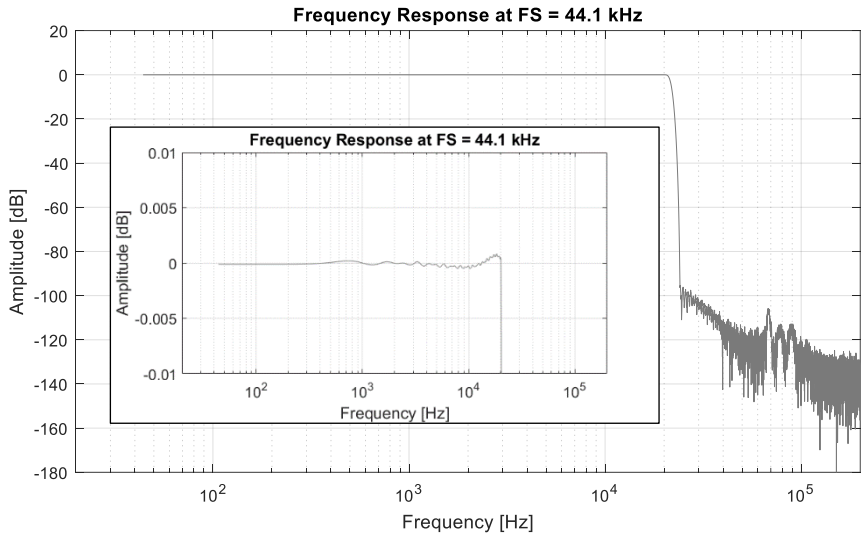
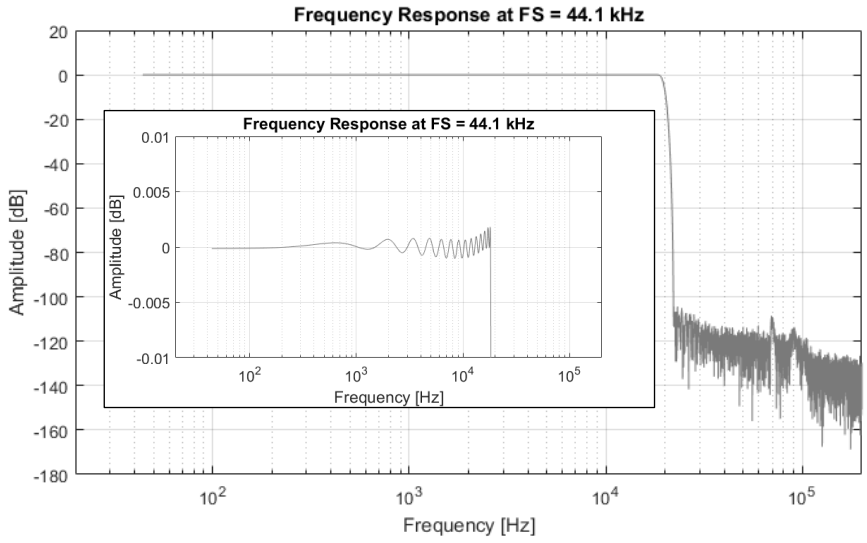
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 FS	Hz
Stop band	-90.9 dB	0.80 FS			Hz
Group Delay		2.08/FS		3.56/FS	s
Flatness (ripple)					dB

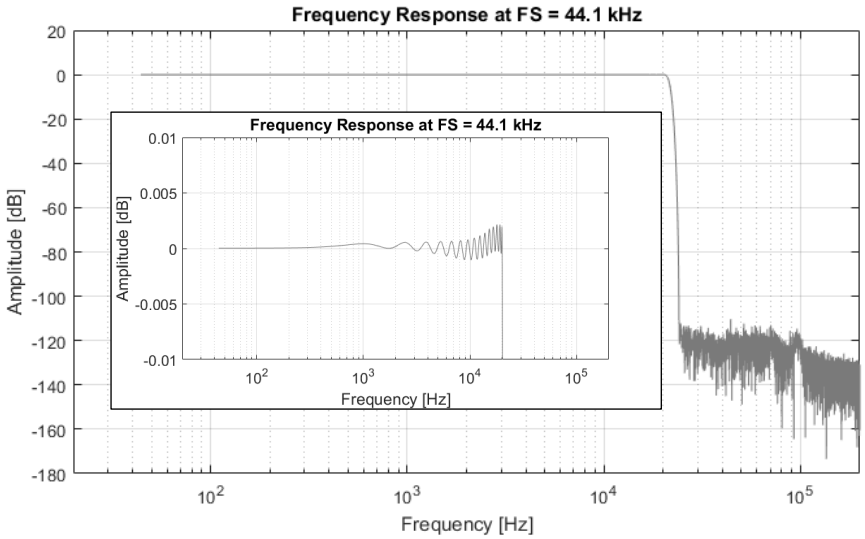
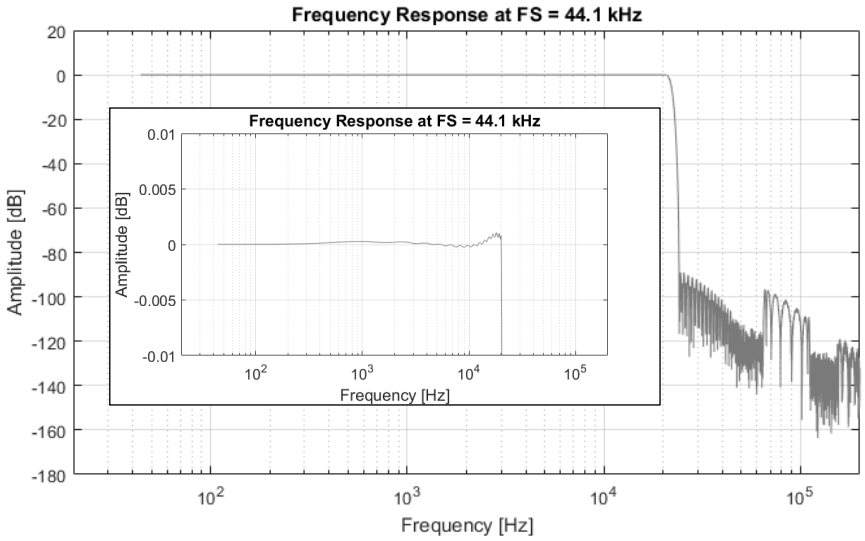
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 FS	Hz
Stop band	-91 dB	0.80 FS			Hz
Group Delay		9.23/FS		9.75/FS	s
Flatness (ripple)					dB

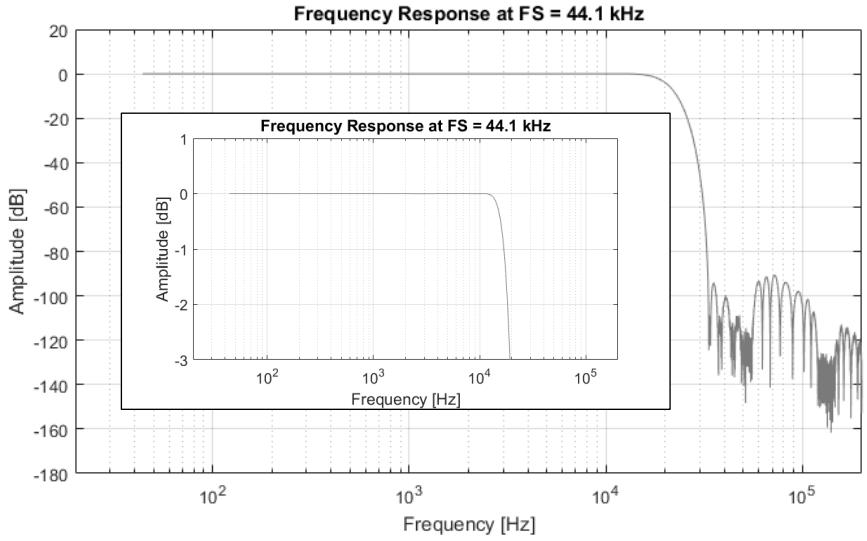
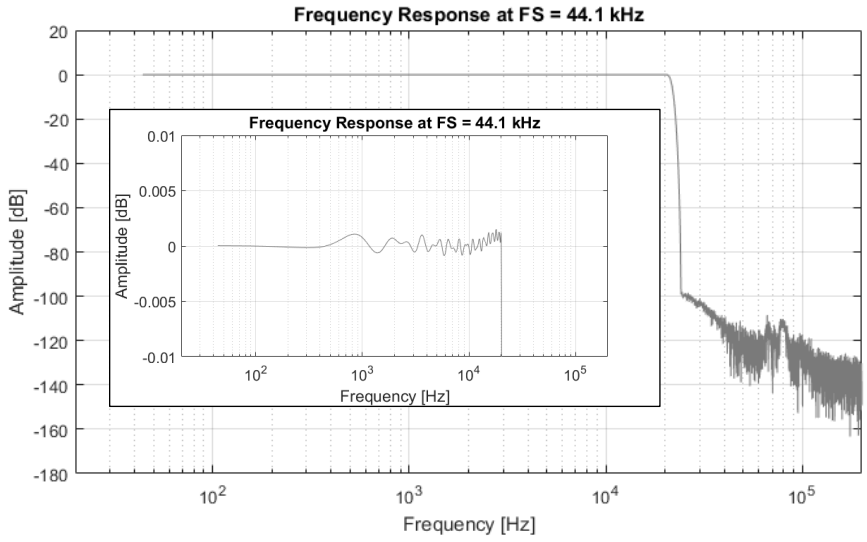
Table 18 - PCM Filter Properties

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

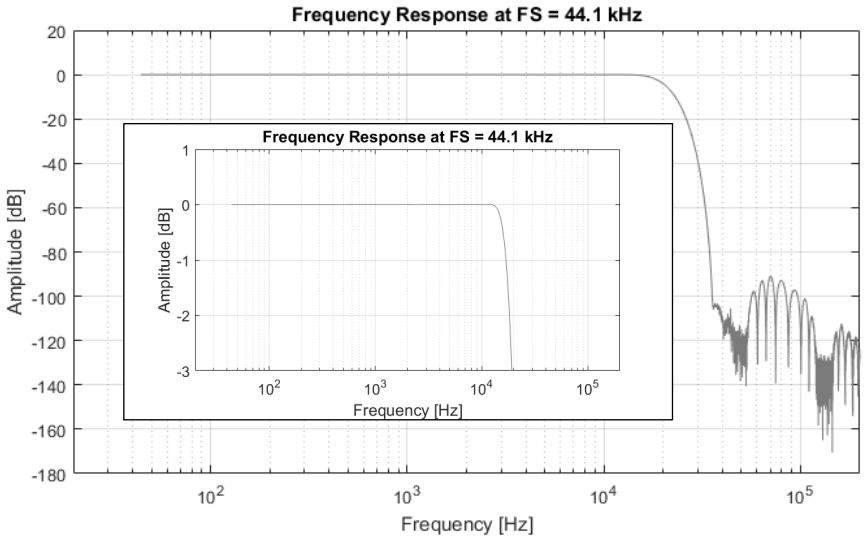
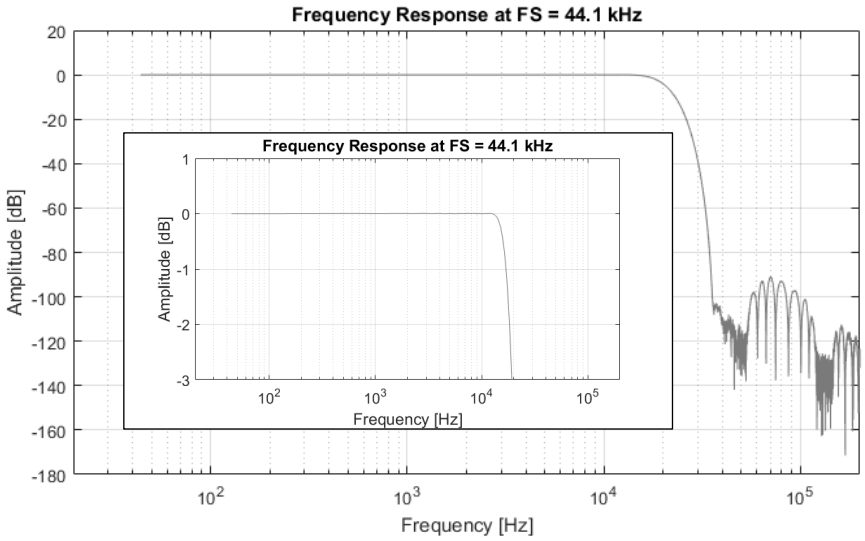
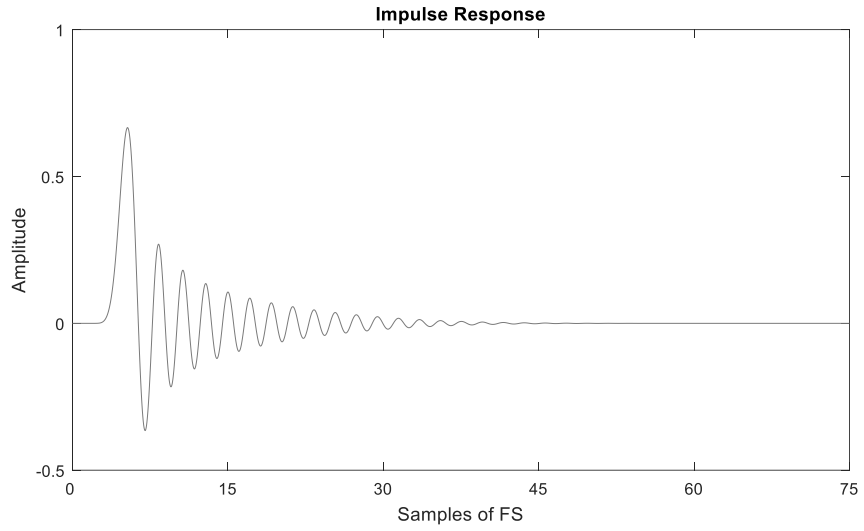
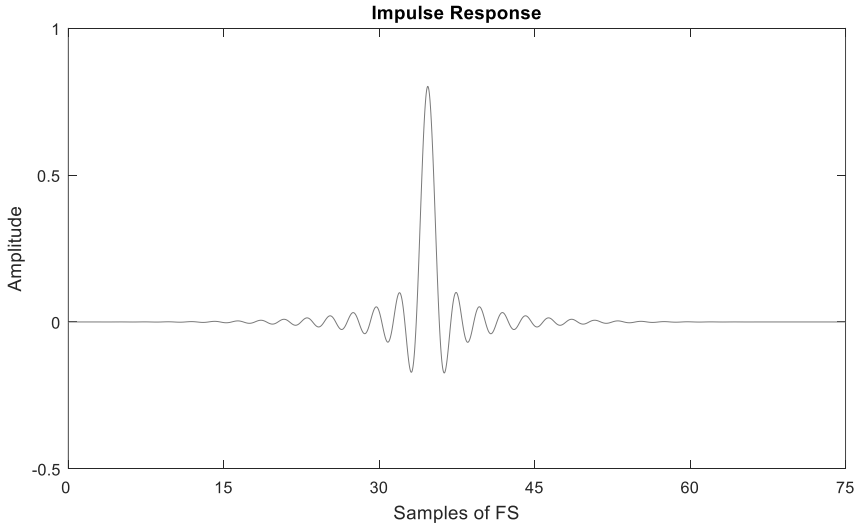
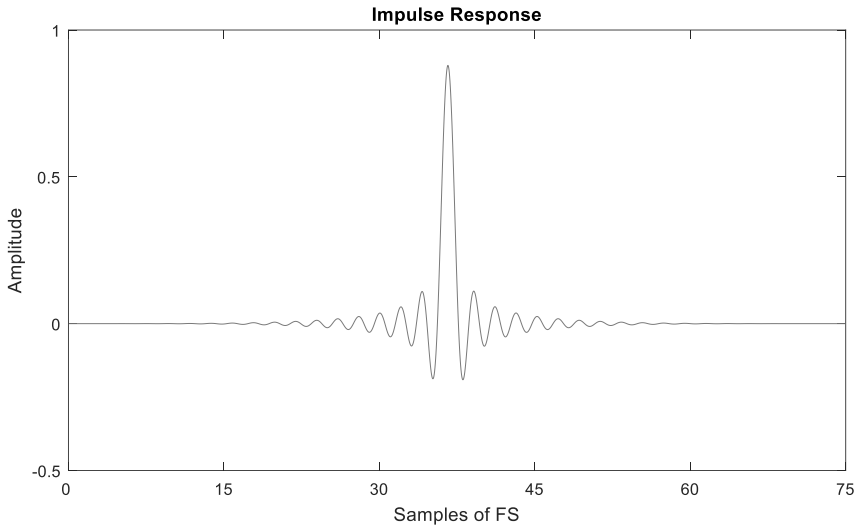
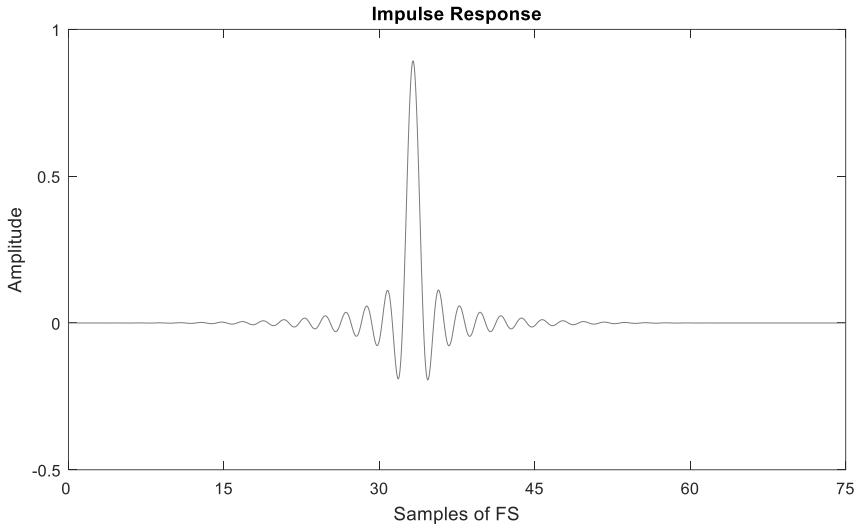
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

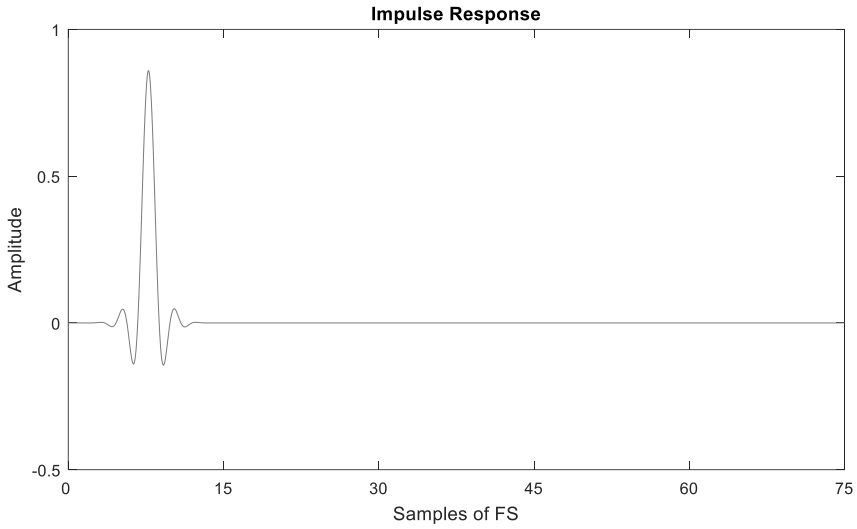
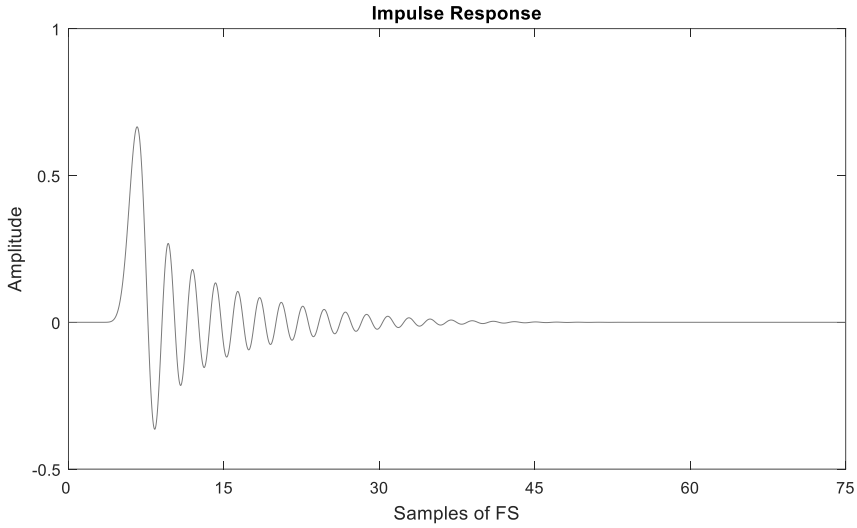
Table 19 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

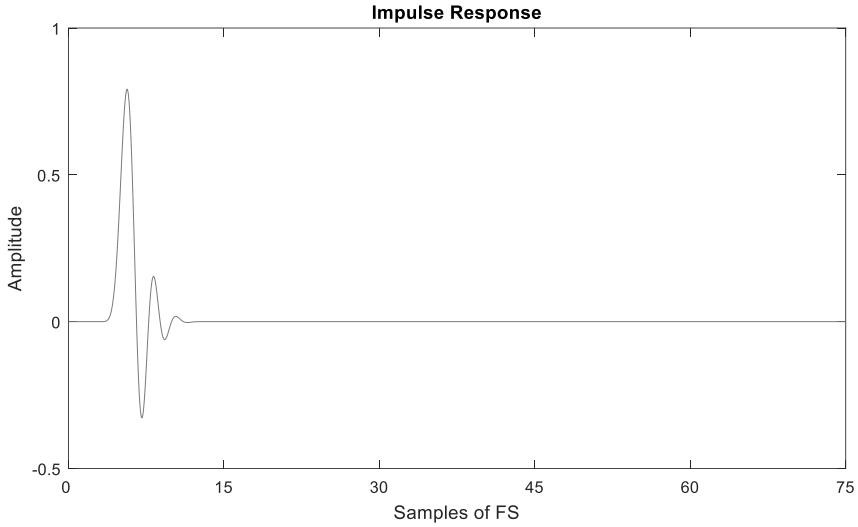
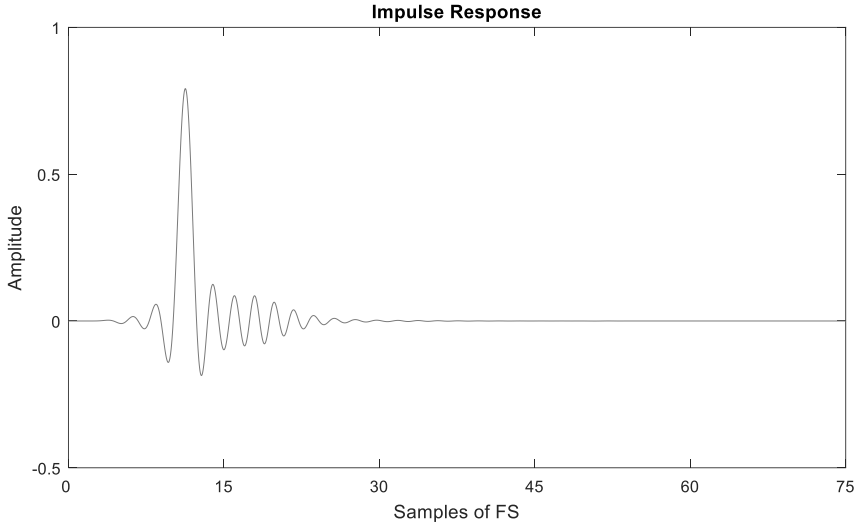
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 20 - PCM Filter Impulse Response

64FS Mode

When the MCLK/FS ratio is required to be 64, it is necessary for the ES9082 to be in 64FS mode. 64FS Mode can be enabled by setting:

Software Register

- Register 0[1] ENABLE_64FS_MODE = 1'b1
  - Manually enables 64FS mode
  - Should be used with high sample rates like 705.6kHz & 768kHz
- Register 0[2] AUTO_FS_DETECT = 1'b1
  - Sets the MCLK_128FS divider according to MCLK/FS ratio
  - Automatically enables 64FS mode when MCLK/MCLK_128FS ratio is 64
- 64FS mode can be blocked when AUTO_FS_DETECT is enabled by setting:
  - Register 0[3] AUTO_FS_BLOCK_64FS = 1'b1

Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase 64FS	3.67 / FS

Table 21 - Minimum Phase 64FS Latency

Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.45 FS	Hz
Stop band	-61.29 dB	0.68 FS			Hz
Group Delay		1.54/FS		2.35/FS	s
Flatness (ripple)					dB

Table 22 - Minimum Phase 64FS Properties

Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

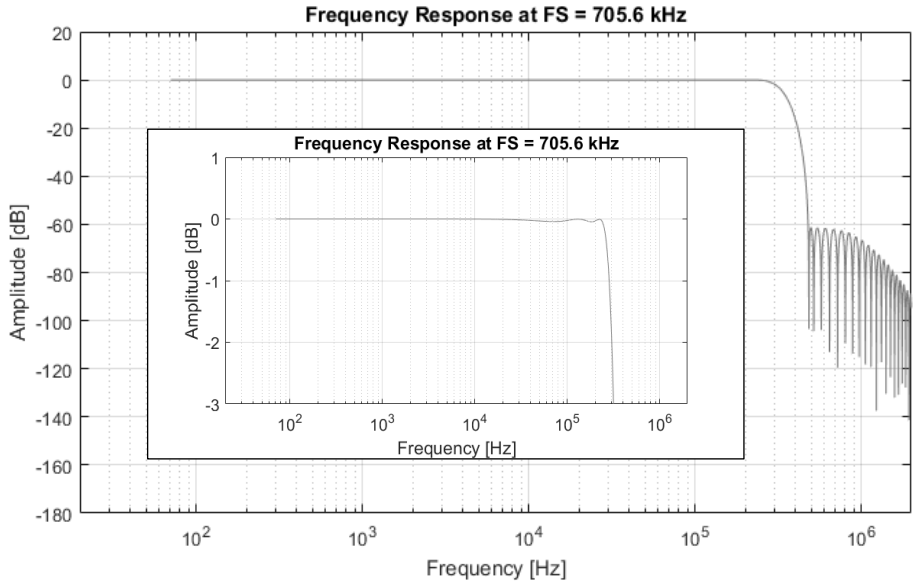


Figure 20 - Minimum Phase 64FS Frequency Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

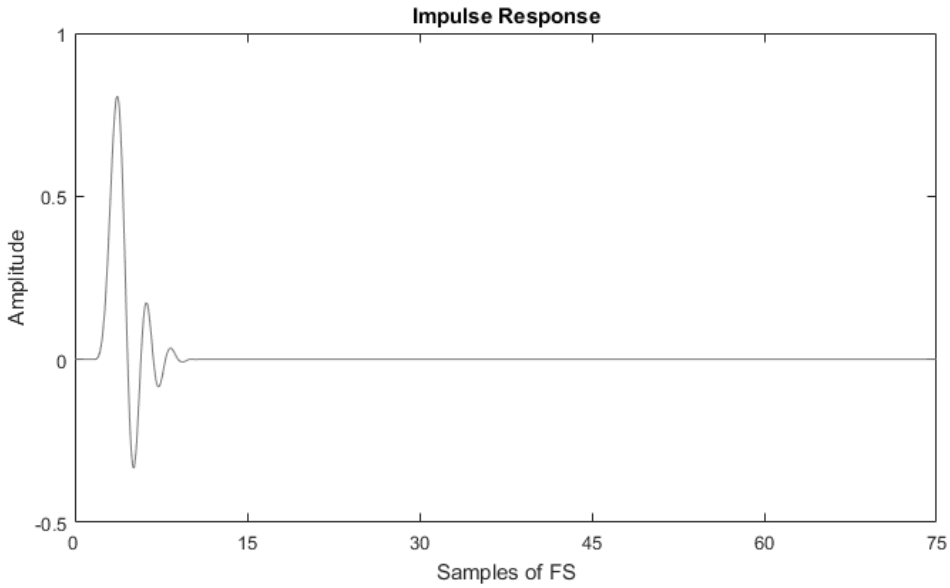


Figure 21 - Minimum Phase 64FS Impulse Response

Analog Features

APLL

The ES9082 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally. For an application note on the APLL, please ask your FAE or distributor for availability.

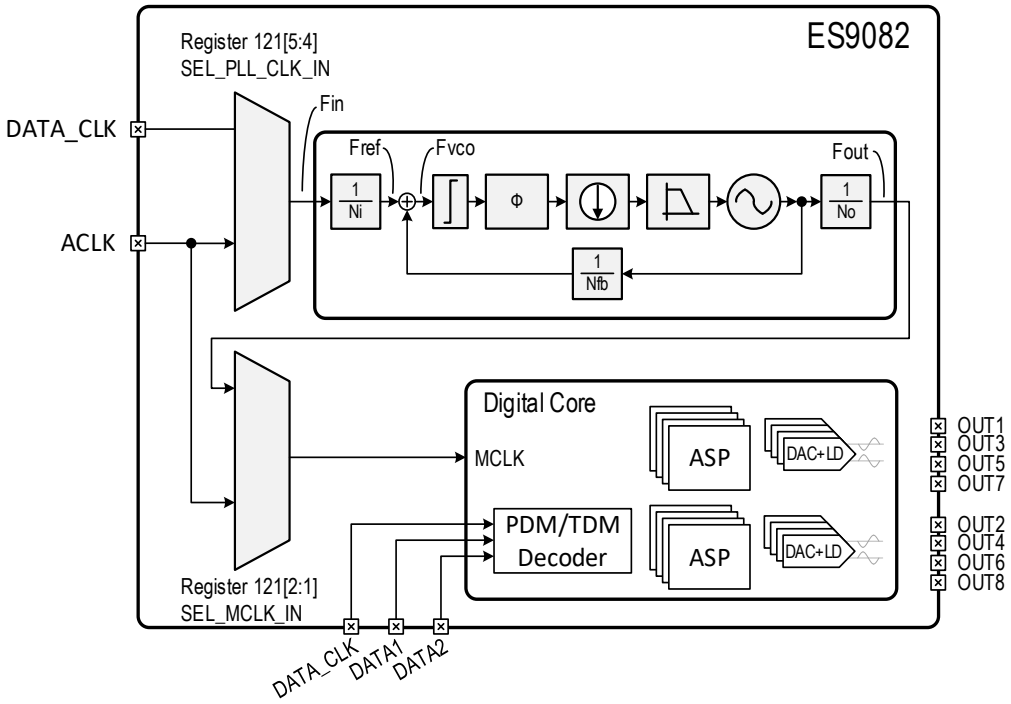


Figure 22 - Functional Block Diagram of ES9082 APLL

The input clock (F_{in}) source to the APLL is chosen between ACLK or DATA_CLK with Register 121[5:4] SEL_PLL_CLK_IN. The input MCLK source to the chip is chosen between the APLLs output or the ACLK pin with Register 121[2:1] SEL_MCLK_IN.

For calculation of the PLL frequency output, use the following formulas:

$$F_{ref} = \left(\frac{F_{in}}{N_i}\right) \qquad F_{vco} = \left(\frac{F_{in}}{N_i}\right) * N_{fb} \qquad N_{fb} = \frac{2^{25}}{FBDIV} \qquad F_{out} = \left(\frac{F_{in}}{N_i}\right) * \frac{N_{fb}}{N_o}$$

Where:

a. FBDIV is a 24-bit number
b. PLL frequency range requirements:
    a. Fref requirement: 2.5MHz < Fref < 12 MHz
    b. Fvco requirement: 90MHz < Fvco < 110MHz
    c. Fout requirement: 22.5792/24.576MHz & 45.1584/49.152Mhz
c. Ni = input divider
    - Accessible from Reg 127-129[8:0], PLL_CLK_IN_DIV
d. No = output divider
    - Accessible from Reg 127-129[15:12], PLL_CLK_OUT_DIV
e. Nfb = feedback divider
    - Accessible from Reg 124-126[23:0], PLL_CLK_FB_DIV
        - Note: Toggle Reg 127-129 PLL_FB_DIV_LOAD to load PLL_CLK_FB_DIV value

44.1kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	DATA_CLK (MHz)	Ni	Fref (MHz)	FBDIV	Fvco (MHz)	No	Fout (MHz)
32-Bit Frame							
352.8	22.5792	2	11.2896	4194304	90.3168	4	22.5792
176.4	11.2896	1	11.2896	4194304	90.3168	4	22.5792
88.2	5.6448	1	5.6448	2097152	90.3168	4	22.5792
44.1	2.8224	1	2.8224	1048576	90.3168	4	22.5792
16-Bit Frame							
352.8	11.2896	1	11.2896	4194304	90.3168	4	22.5792
176.4	5.6448	1	5.6448	2097152	90.3168	4	22.5792
88.2	2.8224	1	2.8224	1048576	90.3168	4	22.5792
44.1	1.4112	1	1.4112	524288	90.3168	4	22.5792

Table 23 - APLL Divider Values for 44.1kHz Base Rates

48kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	DATA_CLK (MHz)	Ni	Fref (MHz)	FBDIV	Fvco (MHz)	No	Fout (MHz)
32-Bit Frame							
384	24.576	2	12.288	4194304	98.304	4	24.576
192	12.288	1	12.288	4194304	98.304	4	24.576
96	6.144	1	6.144	2097152	98.304	4	24.576
48	3.072	1	3.072	1048576	98.304	4	24.576
16-Bit Frame							
384	12.288	1	12.288	4194304	98.304	4	24.576
192	6.144	1	6.144	2097152	98.304	4	24.576
96	3.072	1	3.072	1048576	98.304	4	24.576
48	1.536	1	1.536	524288	98.304	4	24.576

Table 24 - APLL Divider Values for 48kHz Base Rates

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_3V3_L • AVCC_3V3_R • AVCC_CP • AVDD • DVDD	 • +3.7V with respect to ground • +3.7V with respect to ground • +3.7V with respect to ground • +3.7V with respect to ground • +1.4V with respect to ground
Storage Temperature	-65ºC to +150ºC
Operating Junction Temperature	+125ºC
Voltage Range for Digital Input Pins	-0.3V to AVDD (nom) +0.3V

Table 25 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

ESD Ratings

ESD Standard	Rating
Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001	2kV
Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002	500V

Table 26 - ESD Ratings

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-level input voltage	VIH	(AVDD / 2) + 0.4		V
Low-level input voltage	VIL		0.4	V
High-level output voltage	VOH	AVDD – 0.2		V
Low-level output voltage	VOL		0.2	V

Table 27 - I/O Electrical Characteristics

Switching Characteristics

Parameter	Notes	Min.	Typ.	Max.	Unit
MCLK[1]					
Frequency		6.144	-	49.152	MHz
Duty Cycle		45	-	55	%
PCM Mode[2]					
WS Frequency (Word Select Clock)		8	-	MCLK/128	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	TDM_WORD_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
WS Frequency (Word Select Clock)	64FS Mode[3]	352.8	MCLK/64	768	kHz
BCLK Frequency (Bit Clock)		22.5792	MCLK	49.152	MHz
TDM Mode					
WS Frequency (Word Select Clock)	TDM4	8	-	MCLK/128	kHz
	TDM8		-	MCLK/256	kHz
	TDM16		-	MCLK/512	kHz
	TDM32		-	MCLK/1024	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	(TDM_WORD_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
DSD Mode					
DSD Clock Frequency		2.8224	-	MCLK/2	MHz

Table 28 - Switching Characteristics

[1] MCLK must be synchronous to the digital audio clock

[2] In hardware mode, only 32-bit word widths are supported for both PCM, 32-bit and 16-bit for TDM.

[3] 64FS mode is for 705.6/768kHz with 45.1584/49.152MHz or 352.8/384kHz with 22.5792/24.576MHz.

Timing Characteristics

Bit-Clock (BCLK) and Word-Select (WS) Timing

Test Conditions 1 (unless otherwise noted)
T_A = 25ºC, AVCC_3V3_L = AVCC_3V3_R = AVCC_CP = AVDD = +3.3V, DVDD= Internal, fs = 48kHz, DAC enabled, 1kHz sine full scale.

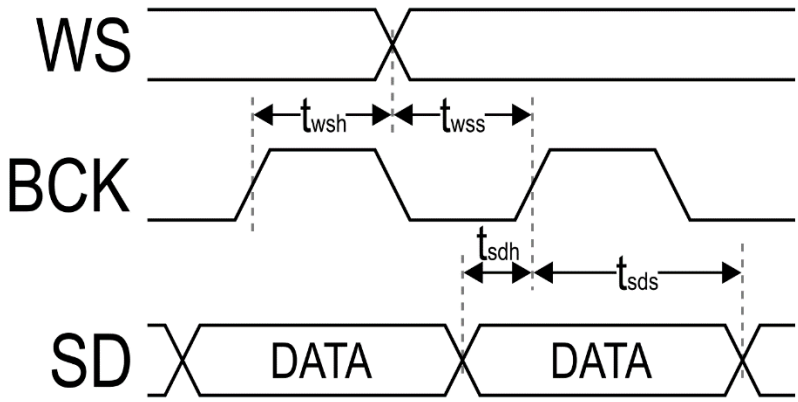


Figure 23 - Bit-Clock and Word-Select Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
WS setup time	t_{wss}	-	0.3	-	ns
WS hold time	t_{wsh}	-	0.3	-	ns
SD setup time	t_{sds}	-	-0.4	-	ns
SD hold time	t_{sdh}	-	0.8	-	ns

Table 29 - Bit-Clock and Word-Select Timing Definitions

I²C Slave Interface Timing

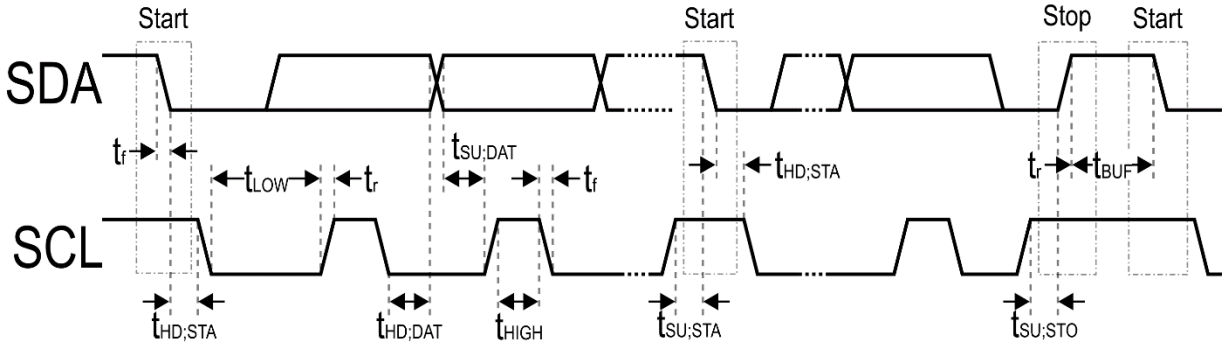


Figure 24 - I²C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000	-	300	ns
Fall time of SDA and SCL	t_f		-	300	-	300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 30 - I²C Slave/Synchronous Slave Interface Timing Definitions

SPI Slave Interface Timing

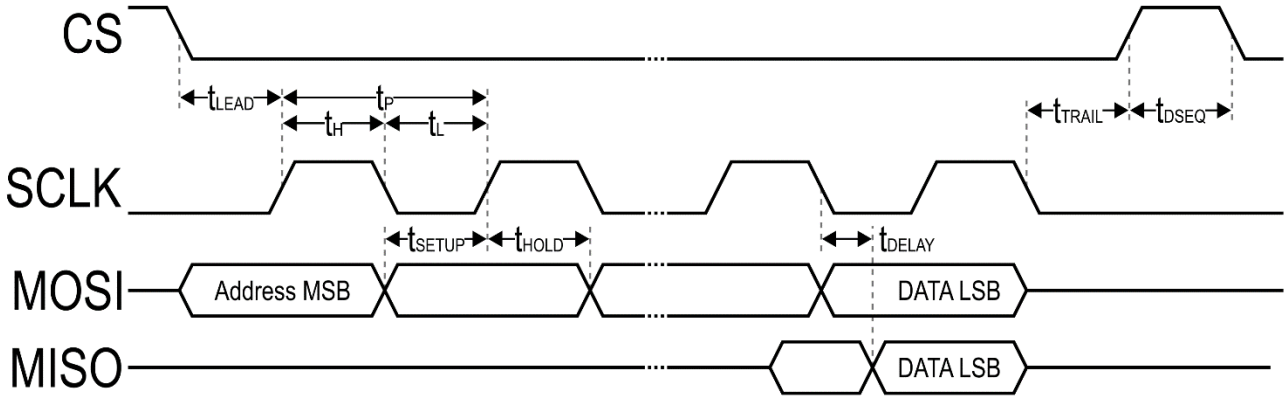


Figure 25 - SPI Slave Interface Timing

Parameter	Symbol	Min [ns]	Max [ns]
CS Lead Time (SCLK rising edge)	t_{LEAD}	4	-
CS Trail Time (SCLK falling edge)	t_{TRAIL}	4	-
MOSI Data Setup Time	t_{SETUP_MOSI}	-36	-
MOSI Data Hold Time	t_{HOLD_MOSI}	60	-
SCLK-MISO Delay Time	t_{DELAY_MISO}	-	74
SCLK Period	t_{P_SCLK}	122	-
SCLK High Pulse Duration	t_{H_SCLK}	94	-
SCLK Low Pulse Duration	t_{L_SCLK}	60	-
Sequential Transfer Delay	t_{DSEQ}	38	-

Table 31 - SPI Slave Interface Timing

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	-20°C to +85°C
AVDD		+3.3V
AVCC_3V3_L		+3.3V
AVCC_3V3_R		+3.3V
AVCC_CP		+3.3V
AVCC_L		Internal
AVCC_R		Internal
DVDD		Internal
PLL_REG		Internal
VREF		Internal
PNEG		Internal

Charge Pump

The ES9082 features an integrated Charge Pump (CP) that produces the internal negative supply required for the "ground centered" line drivers, on pin 18 (PNEG). The CP will automatically shut down, saving power, when a mute condition is detected. This function can be disabled by setting Reg 48[0] CP_MUTE_PD_EN = 1'b0.

The charge pump clock must be set to 705.6kHz or 768kHz depending on the sample rate multiple (44.1kHz/48kHz respectively). This is done by setting the value of CP_CLK_DIV to result in a charge pump clock of 705.1kHz/768kHz. CP_CLK_DIV (default 8d'31) is not required to change when the MCLK rate is 22.5792MHz/24.576MHz or 45.1584MHz/49.152MHz when the MCLK_RATE_SEL register is selected correctly. It will divide the clock automatically according to the equation below. If MCLK is another frequency, then the CP_CLK_DIV must also be set to ensure CP_CLK is in the required range.

$$\text{CP\_CLK [Hz]} = \frac{\text{MCLK}}{2^{\sim \text{MCLK\_RATE\_SEL}} \cdot (\text{CP\_CLK\_DIV} + 1)}$$

$$\text{CP\_CLK\_DIV} = \frac{\text{MCLK}}{2^{\sim \text{MCLK\_RATE\_SEL}} \cdot \text{CP\_CLK}} - 1$$

Charge Pump Registers

- Register 2[7] MCLK_RATE_SEL
- Register 51[7:0] CP_CLK_DIV (Default is 8'd31)
- Register 49[0] CP_MUTE_PD_EN

Recommended Power Up/Down Sequence

The recommended power up sequence for the ES9082, the AVCC supply is enabled ~200us before AVCC_3V3_L, AVCC_3V3_R, and AVCC_CP are enabled.

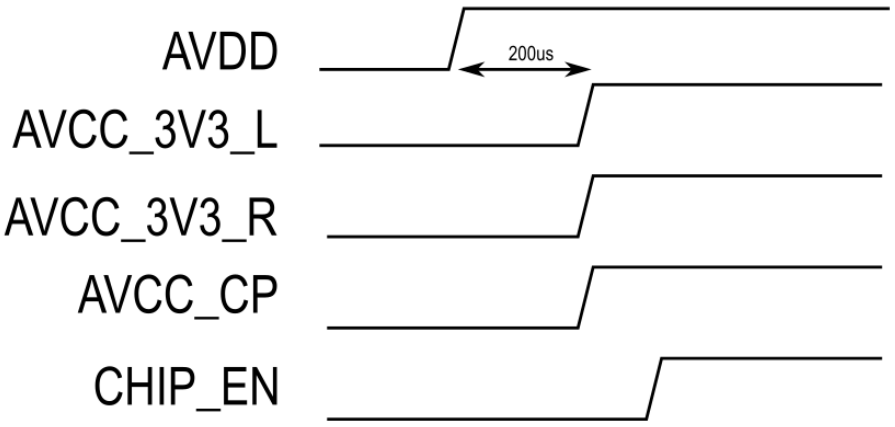


Figure 26 – Recommended Power Up Sequence

On power down, after CHIP_EN is disabled, AVCC_3V3_L, AVCC_3V3_R, AVCC_CP, and AVCC supplies are disabled.

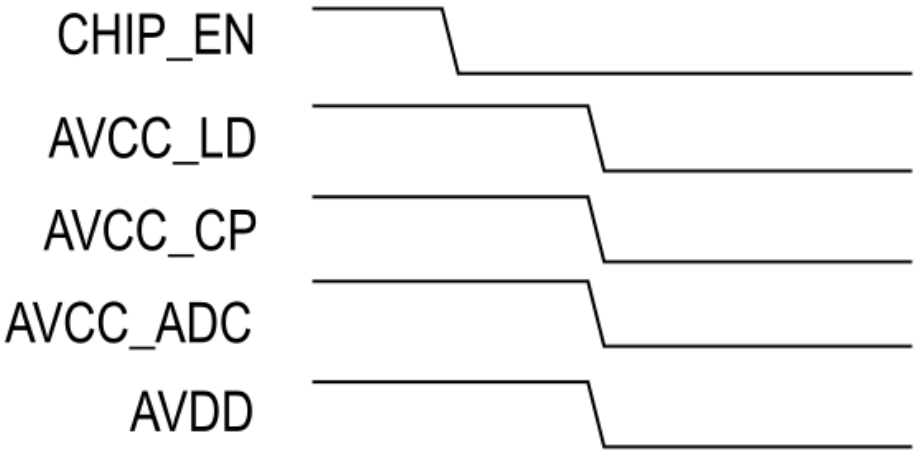


Figure 27 – Recommended Power Down Sequence

Power Consumption

Test Conditions (unless otherwise noted)

T_A = 25ºC, AVCC_3V3_L = AVCC_3V3_R = AVCC_CP = AVDD = +3.3V, 0dBFS input. AVDD supply includes DVDD current.

Parameter	Min	Typ.	Max	Unit
Standby (CHIP_EN=0)				
AVCC_3V3_L		0.1		mA
AVCC_3V3_R		0.1		mA
AVCC_CP		0		mA
AVDD		0.1		mA
Fs = 48kHz, MCLK = 24.576MHz				
AVCC_3V3_L		30.9		mA
AVCC_3V3_R		30.9		mA
AVCC_CP		39.5		mA
AVDD		15.6		mA
Fs = 384kHz, MCLK = 24.576MHz				
AVCC_3V3_L		30.9		mA
AVCC_3V3_R		30.9		mA
AVCC_CP		39.5		mA
AVDD		25.1		mA

Table 32 - Power Consumption

Performance

Test Conditions 1 (unless otherwise noted)

T_A = 25ºC, AVCC_3V3_L = AVCC_3V3_R = AVCC_CP = AVDD = +3.3V, fs = 48kHz, HW mode (I^2S Master Mode)

Note: Performance numbers were measured using the ESS ES9082 5v0 evaluation board.

Parameter		Min	Typ.	Max	Unit
Resolution			32		Bit
Max MCLK frequency	Note: Synchronous clocks required		49.152		MHz
THD+N Ratio 0dBFS BW=20Hz-20kHz	8 ch single-ended		-108		dB
	4 ch differential		-110		dB
	4 ch single-ended		-108		dB
DNR (A-weighted) -60dBFS BW=20Hz-20kHz	8 ch single-ended		120		dB
	4 ch differential		124		dB
	4 ch single-ended		123		dB
	2 ch differential		127		dB
	2 ch single-ended		126		dB
Voltage output amplitude	0dBFS input		2		Vrms

Table 33 – ES9082 Performance

Register Overview

A system clock is not required to access registers.

Read/Write Register Addresses

Registers 0-179 (0x00 - 0xB3) are read and write registers.

Read-Only Register Addresses

Register 224-250 (0xE0 - 0xFA) are read only registers.

Multi-Byte Registers

Multi-Byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-Byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	RESERVED			AUTO_FS_BLOCK_64FS	AUTO_FS_DETECT	EN_64FS_MODE	ENABLE_DAC
0x01	1	DIGITAL INPUT CONFIG	ENABLE_PDM_DECODE	ENABLE_DSD_DECODE	ENABLE_DOP_DECODE	ENABLE_TDM_DECODE	RESERVED	INPUT_SEL		AUTO_INPUT_SEL
0x02	2	CLOCK CONTROL	MCLK_RATE_SEL	MCLK_128FS_HALF_DIV	MCLK_128FS_DIV					
0x03	3	MISC CLOCK CONTROLS	RESERVED					DAC_CLK_INV	EN_CLK_DET	FORCE_PLL_LOCK
0x04	4	PCM MASTER CLK CONFIG	MASTER_BCK_DIV							
0x05	5	PCM MASTER MODE CONFIG	SLAVE_BCK_INVERT	RESERVED		MASTER_WS_PULSE_MODE	MASTER_WS_INVERT	MASTER_BCK_INVERT	DSD_MASTER_MODE_EN	PCM_MASTER_MODE_EN
0x06	6	TDM CONFIG 1	TDM_RESYNC	AUTO_CH_DETECT	RESERVED	TDM_CH_NUM				
0x07	7	TDM CONFIG 2	ENABLE_WS_MONITOR	ENABLE_BCK_MONITOR	TDM_WORD_WIDTH		TDM_BIT_DEPTH		TDM_VALID_EDGE	TDM_LJ
0x08	8	TDM CH1 SLOT CONFIG	RESERVED	TDM_LINE_SEL_CH1		TDM_SLOT_SEL_CH1				
0x09	9	TDM CH2 SLOT CONFIG	RESERVED	TDM_LINE_SEL_CH2		TDM_SLOT_SEL_CH2				
0x0A	10	TDM CH3 SLOT CONFIG	RESERVED	TDM_LINE_SEL_CH3		TDM_SLOT_SEL_CH3				
0x0B	11	TDM CH4 SLOT CONFIG	RESERVED	TDM_LINE_SEL_CH4		TDM_SLOT_SEL_CH4				
0x0C	12	TDM CH5 SLOT CONFIG	RESERVED	TDM_LINE_SEL_CH5		TDM_SLOT_SEL_CH5				
0x0D	13	TDM CH6 SLOT CONFIG	RESERVED	TDM_LINE_SEL_CH6		TDM_SLOT_SEL_CH6				
0x0E	14	TDM CH7 SLOT CONFIG	RESERVED	TDM_LINE_SEL_CH7		TDM_SLOT_SEL_CH7				
0x0F	15	TDM CH8 SLOT CONFIG	RESERVED	TDM_LINE_SEL_CH8		TDM_SLOT_SEL_CH8				
0x10	16	TDM MIX CONFIG	TDM_MIX_LINE_SEL			TDM_MIX_SLOT_SEL_CH1				
0x11	17	TDM MIX CONFIG	RESERVED		TDM_MIX_DATA6_EN	TDM_MIX_SLOT_SEL_CH2				
0x12	18	TDM DAISY CHAIN	TDM_DAISY_CHAIN	TDM_DAISY_CHAIN_LINE_IN		TDM_DATA_LATCH_ADJ				
0x13	19	DSD CH1/2 LINE SELECT	PDM_DATA_PHASE	PDM_FRAME_EDGE	DSD_LINE_SEL_CH2			DSD_LINE_SEL_CH1		
0x14	20	DSD CH3/4 LINE SELECT	RESERVED	PDM_2X_GAIN_EN	DSD_LINE_SEL_CH4			DSD_LINE_SEL_CH3		
0x15	21	DSD CH5/6 LINE SELECT	RESERVED		DSD_LINE_SEL_CH6			DSD_LINE_SEL_CH5		
0x16	22	DSD CH7/8 LINE SELECT	RESERVED		DSD_LINE_SEL_CH8			DSD_LINE_SEL_CH7		
0x17	23	ENCODER CONFIG	RESERVED			SPDIF_MIX_DATA_SEL	SPDIF_CH_PAIR_SEL		ENABLE_SPDIF_ENCODE	ENABLE_TDM_ENCODE
0x18	24	S/PDIF CS ADDR	SPDIF_CS_WE	RESERVED				SPDIF_CS_BYTE_ADDR		
0x19	25	S/PDIF CS DATA	SPDIF_CS_BYTE_DATA							
0x1A	26	TDM ENC SLOT SEL CH1	RESERVED			TDM_ENC_SLOT_SEL_CH1				
0x1B	27	TDM ENC SLOT SEL CH2	RESERVED			TDM_ENC_SLOT_SEL_CH2				
0x1C	28	TDM ENC SLOT SEL CH3	RESERVED			TDM_ENC_SLOT_SEL_CH3				
0x1D	29	TDM ENC SLOT SEL CH4	RESERVED			TDM_ENC_SLOT_SEL_CH4				
0x1E	30	TDM ENC SLOT SEL CH5	RESERVED			TDM_ENC_SLOT_SEL_CH5				
0x1F	31	TDM ENC SLOT SEL CH6	RESERVED			TDM_ENC_SLOT_SEL_CH6				
0x20	32	TDM ENC SLOT SEL CH7	RESERVED			TDM_ENC_SLOT_SEL_CH7				
0x21	33	TDM ENC SLOT SEL CH8	RESERVED			TDM_ENC_SLOT_SEL_CH8				
0x22-0x23	34-35	RESERVED	RESERVED							
0x24	36	STATUS BITS MASKP 1	VOL_MIN_CH8_MASKP	VOL_MIN_CH7_MASKP	VOL_MIN_CH6_MASKP	VOL_MIN_CH5_MASKP	VOL_MIN_CH4_MASKP	VOL_MIN_CH3_MASKP	VOL_MIN_CH2_MASKP	VOL_MIN_CH1_MASKP
0x25	37	STATUS BITS MASKP 2	AUTOMUTE_CH8_MASKP	AUTOMUTE_CH7_MASKP	AUTOMUTE_CH6_MASKP	AUTOMUTE_CH5_MASKP	AUTOMUTE_CH4_MASKP	AUTOMUTE_CH3_MASKP	AUTOMUTE_CH2_MASKP	AUTOMUTE_CH1_MASKP
0x26	38	STATUS BITS MASKP 3	SS_FULL_RAMP_CH8_MASKP	SS_FULL_RAMP_CH7_MASKP	SS_FULL_RAMP_CH6_MASKP	SS_FULL_RAMP_CH5_MASKP	SS_FULL_RAMP_CH4_MASKP	SS_FULL_RAMP_CH3_MASKP	SS_FULL_RAMP_CH2_MASKP	SS_FULL_RAMP_CH1_MASKP
0x27	39	STATUS BITS MASKP 4	RESERVED	INPUT_SEL_OVR_MASKP		DOP_VALID_CH12_MASKP	TDM_DATA_VALID_MASKP	BCK_WS_FAIL_MASKP	RESERVED	PLL_LOCKED_MASKP
0x28	40	STATUS BITS MASKN 1	VOL_MIN_CH8_MASKN	VOL_MIN_CH7_MASKN	VOL_MIN_CH6_MASKN	VOL_MIN_CH5_MASKN	VOL_MIN_CH4_MASKN	VOL_MIN_CH3_MASKN	VOL_MIN_CH2_MASKN	VOL_MIN_CH1_MASKN
0x29	41	STATUS BITS MASKN 2	AUTOMUTE_CH8_MASKN	AUTOMUTE_CH7_MASKN	AUTOMUTE_CH6_MASKN	AUTOMUTE_CH5_MASKN	AUTOMUTE_CH4_MASKN	AUTOMUTE_CH3_MASKN	AUTOMUTE_CH2_MASKN	AUTOMUTE_CH1_MASKN
0x2A	42	STATUS BITS MASKN 3	SS_FULL_RAMP_CH8_MASKN	SS_FULL_RAMP_CH7_MASKN	SS_FULL_RAMP_CH6_MASKN	SS_FULL_RAMP_CH5_MASKN	SS_FULL_RAMP_CH4_MASKN	SS_FULL_RAMP_CH3_MASKN	SS_FULL_RAMP_CH2_MASKN	SS_FULL_RAMP_CH1_MASKN
0x2B	43	STATUS BITS MASKN 4	RESERVED	INPUT_SEL_OVR_MASKN		DOP_VALID_CH12_MASKN	TDM_DATA_VALID_MASKN	BCK_WS_FAIL_MASKN	RESERVED	PLL_LOCKED_MASKN
0x2C	44	STATUS BITS CLEAR 1	VOL_MIN_CH8_CLEAR	VOL_MIN_CH7_CLEAR	VOL_MIN_CH6_CLEAR	VOL_MIN_CH5_CLEAR	VOL_MIN_CH4_CLEAR	VOL_MIN_CH3_CLEAR	VOL_MIN_CH2_CLEAR	VOL_MIN_CH1_CLEAR
0x2D	45	STATUS BITS CLEAR 2	AUTOMUTE_CH8_CLEAR	AUTOMUTE_CH7_CLEAR	AUTOMUTE_CH6_CLEAR	AUTOMUTE_CH5_CLEAR	AUTOMUTE_CH4_CLEAR	AUTOMUTE_CH3_CLEAR	AUTOMUTE_CH2_CLEAR	AUTOMUTE_CH1_CLEAR
0x2E	46	STATUS BITS CLEAR 3	SS_FULL_RAMP_CH8_CLEAR	SS_FULL_RAMP_CH7_CLEAR	SS_FULL_RAMP_CH6_CLEAR	SS_FULL_RAMP_CH5_CLEAR	SS_FULL_RAMP_CH4_CLEAR	SS_FULL_RAMP_CH3_CLEAR	SS_FULL_RAMP_CH2_CLEAR	SS_FULL_RAMP_CH1_CLEAR
0x2F	47	STATUS BITS CLEAR 4	RESERVED	INPUT_SEL_OVR_CLEAR		DOP_VALID_CH12_CLEAR	TDM_DATA_VALID_CLEAR	BCK_WS_FAIL_CLEAR	CLK_AVALID_CLEAR	PLL_LOCKED_CLEAR
0x30	48	RESERVED	RESERVED							
0x31	49	CHARGE PUMP CONFIG	RESERVED							CP_MUTE_PD_EN
0x32	50	RESERVED	RESERVED							
0x33	51	CHARGE PUMP CLOCK DIV	CP_CLK_DIV							
0x34-0x42	52-66	RESERVED	RESERVED							
0x43	67	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x44	68	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x45	69	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x46	70	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG			
0x47	71	GPIO9/10 CONFIG	GPIO10_CFG				GPIO9_CFG			
0x48	72	GPIO INPUT CONTROL	GPIO8_SDB	GPIO7_SDB	GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB
0x49	73		RESERVED	GPIO_SYSTEM_MODE	RESERVED				GPIO10_SDB	GPIO9_SDB
0x4A	74	GPIO OUTPUT CONTROL	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x4B	75		GPIO_AND_SS_RAMP	GPIO_AND_AUTOMUTE	GPIO_AND_VOL_MIN	RESERVED			GPIO10_OE	GPIO9_OE
0x4C	76	GPIO INVERT CONTROL	GPIO8_INV	GPIO7_INV	GPIO6_INV	GPIO5_INV	GPIO4_INV	GPIO3_INV	GPIO2_INV	GPIO1_INV

0x4D	77		GPIO_OR_SS_RAMP	GPIO_OR_AUTOMUTE	GPIO_OR_VOL_MIN	RESERVED			GPIO10_INV	GPIO9_INV
0x4E	78	GPIO KEEPER CONTROL	GPIO8_WK_EN	GPIO7_WK_EN	GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x4F	79		RESERVED						GPIO10_WK_EN	GPIO9_WK_EN
0x50	80	GPIO READ CONTROL	GPIO8_READ	GPIO7_READ	GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x51	81		RESERVED						GPIO10_READ	GPIO9_READ
0x52	82	PWM COUNT	PWM_COUNT							
0x53	83	PWM FREQUENCY	PWM_FREQ							
0x54	84		PWM_FREQ							
0x55	85	RESERVED	RESERVED							
0x56	86	DAC FILTER CONFIG	RESERVED		BYPASS_IIR	BYPASS_FIR4X	BYPASS_FIR2X	FILTER_SHAPE		
0x57	87	VOLUME CH1	VOLUME_CH1							
0x58	88	VOLUME CH2	VOLUME_CH2							
0x59	89	VOLUME CH3	VOLUME_CH3							
0x5A	90	VOLUME CH4	VOLUME_CH4							
0x5B	91	VOLUME CH5	VOLUME_CH5							
0x5C	92	VOLUME CH6	VOLUME_CH6							
0x5D	93	VOLUME CH7	VOLUME_CH7							
0x5E	94	VOLUME CH8	VOLUME_CH8							
0x5F	95	PHASE INVERSION	VOL_PHASE_INV_CH8	VOL_PHASE_INV_CH7	VOL_PHASE_INV_CH6	VOL_PHASE_INV_CH5	VOL_PHASE_INV_CH4	VOL_PHASE_INV_CH3	VOL_PHASE_INV_CH2	VOL_PHASE_INV_CH1
0x60	96	DIGITAL GAIN	RESERVED		DIGITAL_GAIN_CH2			DIGITAL_GAIN_CH1		
0x61	97		RESERVED		DIGITAL_GAIN_CH4			DIGITAL_GAIN_CH3		
0x62	98		RESERVED		DIGITAL_GAIN_CH6			DIGITAL_GAIN_CH5		
0x63	99		RESERVED		DIGITAL_GAIN_CH8			DIGITAL_GAIN_CH7		
0x64	100	MUTE	MUTE_CH8	MUTE_CH7	MUTE_CH6	MUTE_CH5	MUTE_CH4	MUTE_CH3	MUTE_CH2	MUTE_CH1
0x65	101	SOFT RAMP CONFIG	RESERVED	MONO_VOLUME	MUTE_RAMP_TO_GROUND	SOFT_RAMP_TIME				
0x66	102	VOLUME UP RAMP RATE	VOL_RAMP_RATE_UP							
0x67	103	VOLUME DOWN RAMP RATE	VOL_RAMP_RATE_DOWN							
0x68	104	DC OFFSET	DC_OFFSET							
0x69	105	AUTOMUTE ENABLE	AUTOMUTE_EN_CH8	AUTOMUTE_EN_CH7	AUTOMUTE_EN_CH6	AUTOMUTE_EN_CH5	AUTOMUTE_EN_CH4	AUTOMUTE_EN_CH3	AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x6A	106	AUTOMUTE TIME	AUTOMUTE_TIME							
0x6B	107		DSD_FAULT_DETECT_EN	DSD_DC_AM_ENB	DSD_MUTE_AM_ENB	RESERVED		AUTOMUTE_TIME		
0x6C	108	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x6D	109		AUTOMUTE_LEVEL							
0x6E	110	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x6F	111		AUTOMUTE_OFF_LEVEL							
0x70-0x78	112-120	RESERVED	RESERVED							
0x79	121	PLL CLOCK SELECT	RESERVED	PLL_CLK_PHASE_INV	SEL_PLL_CLK_IN		EN_PLL_CLK_IN	SEL_MCLK_IN		EN_MCLK_IN
0x7A	122	PLL VCO & CP	RESERVED				PLL_CP_EN	PLL_VCO_EN	PLL_CLKSMP_EN	PLL_DIG_RSTB
0x7B	123	PLL REGULATOR	RESERVED				PLL_REG_EN	RESERVED		
0x7C	124	PLL FEEDBACK DIV	PLL_CLK_FB_DIV							
0x7D	125		PLL_CLK_FB_DIV							
0x7E	126		PLL_CLK_FB_DIV							
0x7F	127	PLL IN & OUT DIV	PLL_CLK_IN_DIV							
0x80	128		PLL_CLK_OUT_DIV				RESERVED		PLL_FB_DIV_LOAD	PLL_CLK_IN_DIV
0x81-0x87	129-135	RESERVED	RESERVED							
0x88	136	ASP CONTROL	RESERVED					ASP_FLUSH_MEMS	ASP_PROG_EN	ASP_CORE_EN
0x89	137	ASP BYPASS	ASP_BYPASS_CH8	ASP_BYPASS_CH7	ASP_BYPASS_CH6	ASP_BYPASS_CH5	ASP_BYPASS_CH4	ASP_BYPASS_CH3	ASP_BYPASS_CH2	ASP_BYPASS_CH1
0x8A-0xB1	138-177	RESERVED	RESERVED							
0xB2	178	SPI MASTER CONFIG	SPI_M_PULSE_WIDTH				SPI_M_EN	RESERVED		SPI_M_START
0xB3	179	SPI MASTER DATA OUT	SPI_M_DATA_O							
0xE0	224	INPUT FORMAT READ	DOP_VALID				DAC_TDM_VALID	INPUT_SEL_OVERRIDE		PLL_LOCKED
0xE1	225	CHIP ID	CHIP_ID							
0xE2-0xE4	226-228	RESERVED	RESERVED							
0xE5	229	STATUS BITS STATE	VOL_MIN_STATE							
0xE6	230		AUTOMUTE_STATE							
0xE7	231		SS_FULL_RAMP_STATE							
0xE8	232		RESERVED	INPUT_SEL_OVR_STATE		DOP_VALID_CH12_STATE	TDM_DATA_VALID_STATE	BCK_WS_FAIL_STATE	CLK_AVALID_STATE	PLL_LOCKED_STATE
0xE9	233	RESERVED	RESERVED							
0xEA	234	AUTO FS READ	EN_64FS_MODE_AUTO	MCLK_128FS_HALF_DIV_AUTO	MCLK_128FS_DIV_AUTO					
0xEB	235	CLOCK VALIDITY	RATIO_VALID	BCK_INVALID	WS_INVALID	AUTO_CH_NUM				
0xEC	236	GPIO READBACK	GPIO8_R	GPIO7_R	GPIO6_R	GPIO5_R	GPIO4_R	GPIO3_R	GPIO2_R	GPIO1_R
0xED	237		RESERVED						GPIO10_R	GPIO9_R
0xEE	238	VOL MIN READ	VOL_MIN_CH8	VOL_MIN_CH7	VOL_MIN_CH6	VOL_MIN_CH5	VOL_MIN_CH4	VOL_MIN_CH3	VOL_MIN_CH2	VOL_MIN_CH1
0xEF	239	AUTOMUTE READ	AUTOMUTE_CH8	AUTOMUTE_CH7	AUTOMUTE_CH6	AUTOMUTE_CH5	AUTOMUTE_CH4	AUTOMUTE_CH3	AUTOMUTE_CH2	AUTOMUTE_CH1
0xF0	240	SOFT RAMP UP READ	SS_RAMP_UP_CH8	SS_RAMP_UP_CH7	SS_RAMP_UP_CH6	SS_RAMP_UP_CH5	SS_RAMP_UP_CH4	SS_RAMP_UP_CH3	SS_RAMP_UP_CH2	SS_RAMP_UP_CH1
0xF1	241	SOFT RAMP DOWN READ	SS_RAMP_DOWN_CH8	SS_RAMP_DOWN_CH7	SS_RAMP_DOWN_CH6	SS_RAMP_DOWN_CH5	SS_RAMP_DOWN_CH4	SS_RAMP_DOWN_CH3	SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1
0xF2-0xF9	242-249	RESERVED	ASP_DONE_CH8	ASP_DONE_CH7	ASP_DONE_CH6	ASP_DONE_CH5	ASP_DONE_CH4	ASP_DONE_CH3	ASP_DONE_CH2	ASP_DONE_CH1
0xFA	250	SPI MASTER DATA IN	SPI_M_DATA_I							

Table 34 - Register Map

Register Listing

System Registers

Register 0: SYS CONFIG

Bits	[7]	[6:4]	[3]	[2]	[1]	[0]
Default	1'b0	3'b000	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core, resetting all registers to their power-on defaults.
[6:4]	RESERVED	N/A
[3]	AUTO_FS_BLOCK_64FS	Block AUTO_FS_DETECT from transitioning to 64FS mode when the detected MCLK/MCLK_128FS ratio is 64. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	AUTO_FS_DETECT	Automatically determine optimal (MCLK/MCLK_128FS ratio) according to detected FS. • 1'b0: Disabled, use SELECT_MCLK_128FS_NUM to set ratio. • 1'b1: Enabled, overrides SELECT_MCLK_128FS_NUM (default)
[1]	EN_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_DAC	Enables the DAC interpolation path. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 1: DIGITAL INPUT CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'd0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	ENABLE_PDM_DECODE	Enables PDM decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ENABLE_TDM_DECODE	Enables I2S/TDM decoding. • 1'b0: Disabled • 1'b1: Enabled (default)
[3]	RESERVED	N/A
[2:1]	INPUT_SEL	Selects input data format when AUTO_INPUT_SEL is disabled. • 2'd0: PCM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: Reserved
[0]	AUTO_INPUT_SEL	Automatic input data selection config. • 1'b0: Disables auto input select. Input data format is set by INPUT_SEL (default) • 1'b1: Automatically determine the input data format.

Register 2: CLOCK CONTROL

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd3

Bits	Mnemonic	Description
[7]	MCLK_RATE_SEL	Sets the frequency of MCLK, allowing controls to automatically scale between MCLK rates. • 1'b0: MCLK = 22.5792MHz / 24.576MHz (default) • 1'b1: MCLK = 45.1584MHz / 49.152MHz
[6]	MCLK_128FS_HALF_DIV	• 1'b0: Divide by MCLK_128FS_DIV + 1 (default) • 1'b1: Divide by half of MCLK_128FS_DIV + 1 Note: Can only produce half of an odd number divide
[5:0]	MCLK_128FS_DIV	Whole number divide value + 1 for MCLK_128FS (MCLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd3: Whole number divide value + 1 = 4 (default)

Register 3: MISC CLOCK CONTROLS

Bits	[7:3]	[2]	[1]	[0]
Default	5'd0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	DAC_CLK_INV	Inverts the phase of the analog DAC_CLK. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	EN_CLK_DET	Enable Clock Detection circuit • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	FORCE_PLL_LOCK	Clock locking status control with PLL_LOCKED. • 1'b0: clock locking status is determined by PLL_LOCKED • 1'b1: ignores PLL_LOCKED signal from PLL and sets clock locking status to 1'b1

Register 4: PCM MASTER CLK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_BCK_DIV	Master mode DCLK and WS generation clock divider. Whole number divide value + 1 for CLK_BCK_WS_GEN (MCLK/divide_value).

Register 5: PCM MASTER MODE CONFIG

Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	2'b01	1'b0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SLAVE_BCK_INVERT	• 1'b0: Non-inverted (default) • 1'b1: Invert BCK input
[6:5]	RESERVED	N/A
[4]	MASTER_WS_PULSE_MODE	When enabled, master WS is a 1 BCK pulse signal instead of a 50% duty cycle signal. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[3]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	MASTER_BCK_INVERT	Inverts master BCK. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[1]	DSD_MASTER_MODE_EN	Enables DSD master mode, generating DATA_CLK. • 1'b0: Disabled, slave mode (default) • 1'b1: Enabled
[0]	PCM_MASTER_MODE_EN	Enables PCM master mode, generating BCK and WS. • 1'b0: Disabled, slave mode (default) • 1'b1: Enabled

Register 6: TDM CONFIG 1

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM encoder & decoder to resync. • 1'b0: Enable TDM codec synchronization (default) • 1'b1: Force TDM codec to desynchronize.
[6]	AUTO_CH_DETECT	• 1'b0: Disabled (default) • 1'b1: Auto detect BCK/FRAME ratio to determine the number of TDM channels Note: Only active in TDM slave mode.
[5]	RESERVED	N/A
[4:0]	TDM_CH_NUM	Sets number of channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 7: TDM CONFIG 2

Bits	[7]	[6]	[5:4]	[3:2]	[1]	[0]
Default	1'b1	1'b1	2'b00	2'b00	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ENABLE_WS_MONITOR	Enable WS monitor, used to detect the validity of the WS signal. WS is considered invalid if BCK/WS > 1024. • 1'b0: Disabled • 1'b1: Enabled (default)
[6]	ENABLE_BCK_MONITOR	Enable BCK monitor, used to detect the validity of the BCK signal. BCK is considered invalid if MCLK/BCK > 256. • 1'b0: Disabled • 1'b1: Enabled (default)
[5:4]	TDM_WORD_WIDTH	Sets the width, in bits, of one data word / subframe. A subframe is a frame divided by the number of channels. • 2'b00: 32-bits (default) • 2'b01: 24-bits • 2'b10: 16-bits
[3:2]	TDM_BIT_DEPTH	Sets the bit depth, number of data bits, in one data word / subframe. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit
[1]	TDM_VALID_EDGE	Sets which WS edge the frame starts on. • 1'b0: Frame starts on negedge of WS (default) • 1'b1: Frame starts on posedge of WS
[0]	TDM_LJ	Sets left-justified mode. • 1'b0: One BCK period delay (default) • 1'b1: Left-justified

Register 8: TDM CH1 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH1	CH1 data line selection. CH1 receives the data from: • 2'd0: DATA2 (default) • 2'd1: DATA3/GPIO2 • 2'd2: DATA4/GPIO3 • 2'd3: DATA5/GPIO4
[4:0]	TDM_SLOT_SEL_CH1	Selects which TDM channel slot is latched into CH1. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 9: TDM CH2 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH2	CH2 data line selection. CH2 receives the data from: • 2'd0: DATA2 (default) • 2'd1: DATA3/GPIO2 • 2'd2: DATA4/GPIO3 • 2'd3: DATA5/GPIO4
[4:0]	TDM_SLOT_SEL_CH2	Selects which TDM channel slot is latched into CH2. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 10: TDM CH3 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd1	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH3	CH3 data line selection. CH3 receives the data from: • 2'd0: DATA2 • 2'd1: DATA3/GPIO2 (default) • 2'd2: DATA4/GPIO3 • 2'd3: DATA5/GPIO4
[4:0]	TDM_SLOT_SEL_CH3	Selects which TDM channel slot is latched into CH3. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 11: TDM CH4 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd1	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH4	CH4 data line selection. CH4 receives the data from: • 2'd0: DATA2 • 2'd1: DATA3/GPIO2 (default) • 2'd2: DATA4/GPIO3 • 2'd3: DATA5/GPIO4
[4:0]	TDM_SLOT_SEL_CH4	Selects which TDM channel slot is latched into CH4. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 12: TDM CH5 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd2	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH5	CH5 data line selection. CH5 receives the data from: • 2'd0: DATA2 • 2'd1: DATA3/GPIO2 • 2'd2: DATA4/GPIO3 (default) • 2'd3: DATA5/GPIO4
[4:0]	TDM_SLOT_SEL_CH5	Selects which TDM channel slot is latched into CH5. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 13: TDM CH6 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd2	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH6	CH6 data line selection. CH6 receives the data from: • 2'd0: DATA2 • 2'd1: DATA3/GPIO2 • 2'd2: DATA4/GPIO3 (default) • 2'd3: DATA5/GPIO4
[4:0]	TDM_SLOT_SEL_CH6	Selects which TDM channel slot is latched into CH6. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 14: TDM CH7 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd3	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH7	CH7 data line selection. CH7 receives the data from: • 2'd0: DATA2 • 2'd1: DATA3/GPIO2 • 2'd2: DATA4/GPIO3 • 2'd3: DATA5/GPIO4 (default)
[4:0]	TDM_SLOT_SEL_CH7	Selects which TDM channel slot is latched into CH7. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 15: TDM CH8 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd3	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH8	CH8 data line selection. CH8 receives the data from: • 2'd0: DATA2 • 2'd1: DATA3/GPIO2 • 2'd2: DATA4/GPIO3 • 2'd3: DATA5/GPIO4 (default)
[4:0]	TDM_SLOT_SEL_CH8	Selects which TDM channel slot is latched into CH8. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 17-16: TDM MIX CONFIG

Bits	[15:14]	[13]	[12:8]	[7:5]	[4:0]
Default	2'd0	1'b0	5'd1	3'd4	5'd0

Bits	Mnemonic	Description
[15:14]	RESERVED	N/A
[13]	TDM_MIX_DATA6_EN	Enables the TDM MIX interface on DATA6. • 1'b0: Disabled, DATA6 is TDM Daisy Chain output (default) • 1'b1: Enabled
[12:8]	TDM_MIX_SLOT_SEL_CH2	Selects which TDM channel slot is latched into CH8. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32
[7:5]	TDM_MIX_LINE_SEL	Mix interface data line selection. Mix channels receives the data from: • 3'd0: DATA2 • 3'd1: DATA3/GPIO2 • 3'd2: DATA4/GPIO3 • 3'd3: DATA5/GPIO4 • 3'd4: DATA6/GPIO5 (default) • Others: Reserved
[4:0]	TDM_MIX_SLOT_SEL_CH1	Selects which TDM channel slot is latched into MIX CH1. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 18: TDM DAISY CHAIN

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	TDM_DAISY_CHAIN	DAC TDM daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6:5]	TDM_DAISY_CHAIN_LINE_IN	Daisy chain input data line selection, chains the data from: • 2'd0: DATA2 (default) • 2'd1: DATA3/GPIO2 • 2'd2: DATA4/GPIO3 • 2'd3: DATA5/GPIO4
[4:0]	TDM_DATA_LATCH_ADJ	Adjusts the position of the MSB within each TDM slot by TDM_DATA_LATCH_ADJ clock cycles. • 5'd0: Normal position • 5'd1-31: Number of clock cycles to wait

Register 19: DSD CH1/2 LINE SELECT

Bits	[7]	[6]	[5:3]	[2:0]
Default	1'b0	1'b1	3'd1	3'd0

Bits	Mnemonic	Description
[7]	PDM_DATA_PHASE	• 1'b0: CH1 on the rising edge of PDM clock, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge of PDM clock, CH1 on the falling edge
[6]	PDM_FRAME_EDGE	Sets the edge of PDM_CLK where the PDM sample increments. • 1'b0: Rising edge • 1'b1: Falling edge (default)
[5:3]	DSD_LINE_SEL_CH2	Selects the source for the CH2 DSD data. • 3'd0: DATA1 • 3'd1: DATA2 (default) • 3'd2: DATA3/GPIO2 • 3'd3: DATA4/GPIO3 • 3'd4: DATA5/GPIO4 • 3'd5: DATA6/GPIO5 • 3'd6: DATA7/GPIO6 • 3'd7: DATA8/GPIO1
[2:0]	DSD_LINE_SEL_CH1	Selects the source for the CH1 DSD data. • 3'd0: DATA1 (default) • 3'd1: DATA2 • 3'd2: DATA3/GPIO2 • 3'd3: DATA4/GPIO3 • 3'd4: DATA5/GPIO4 • 3'd5: DATA6/GPIO5 • 3'd6: DATA7/GPIO6 • 3'd7: DATA8/GPIO1

Register 20: DSD CH3/4 LINE SELECT

Bits	[7]	[6]	[5:3]	[2:0]
Default	1'd0	1'b0	3'd3	3'd2

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PDM_2X_GAIN_EN	Sets the overall gain of the PDM datapath. • 1'b0: 1x gain (default) • 1'b1: 2x gain
[5:3]	DSD_LINE_SEL_CH4	Selects the source for the CH4 DSD data. • 3'd0: DATA1 • 3'd1: DATA2 • 3'd2: DATA3/GPIO2 • 3'd3: DATA4/GPIO3 (default) • 3'd4: DATA5/GPIO4 • 3'd5: DATA6/GPIO5 • 3'd6: DATA7/GPIO6 • 3'd7: DATA8/GPIO1
[2:0]	DSD_LINE_SEL_CH3	Selects the source for the CH3 DSD data. • 3'd0: DATA1 • 3'd1: DATA2 • 3'd2: DATA3/GPIO2 (default) • 3'd3: DATA4/GPIO3 • 3'd4: DATA5/GPIO4 • 3'd5: DATA6/GPIO5 • 3'd6: DATA7/GPIO6 • 3'd7: DATA8/GPIO1

Register 21: DSD CH5/6 LINE SELECT

Bits	[7:6]	[5:3]	[2:0]
Default	2'd0	3'd5	3'd4

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:3]	DSD_LINE_SEL_CH6	Selects the source for the CH6 DSD data. • 3'd0: DATA1 • 3'd1: DATA2 • 3'd2: DATA3/GPIO2 • 3'd3: DATA4/GPIO3 • 3'd4: DATA5/GPIO4 • 3'd5: DATA6/GPIO5 (default) • 3'd6: DATA7/GPIO6 • 3'd7: DATA8/GPIO1
[2:0]	DSD_LINE_SEL_CH5	Selects the source for the CH5 DSD data. • 3'd0: DATA1 • 3'd1: DATA2 • 3'd2: DATA3/GPIO2 • 3'd3: DATA4/GPIO3 • 3'd4: DATA5/GPIO4 (default) • 3'd5: DATA6/GPIO5 • 3'd6: DATA7/GPIO6 • 3'd7: DATA8/GPIO1

Register 22: DSD CH7/8 LINE SELECT

Bits	[7:6]	[5:3]	[2:0]
Default	2'd0	3'd7	3'd6

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:3]	DSD_LINE_SEL_CH8	Selects the source for the CH8 DSD data. • 3'd0: DATA1 • 3'd1: DATA2 • 3'd2: DATA3/GPIO2 • 3'd3: DATA4/GPIO3 • 3'd4: DATA5/GPIO4 • 3'd5: DATA6/GPIO5 • 3'd6: DATA7/GPIO6 • 3'd7: DATA8/GPIO1 (default)
[2:0]	DSD_LINE_SEL_CH7	Selects the source for the CH7 DSD data. • 3'd0: DATA1 • 3'd1: DATA2 • 3'd2: DATA3/GPIO2 • 3'd3: DATA4/GPIO3 • 3'd4: DATA5/GPIO4 • 3'd5: DATA6/GPIO5 • 3'd6: DATA7/GPIO6 (default) • 3'd7: DATA8/GPIO1

Register 23: ENCODER CONFIG

Bits	[7:5]	[4]	[3:2]	[1]	[0]
Default	3'd0	1'b0	2'b00	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	SPDIF_MIX_DATA_SEL	Selects whether the S/PDIF encoder receives the MIX channel pair data, or the data from CH_PAIR_SEL. • 1'b0: CH_PAIR_SEL data (default) • 1'b1: MIX data
[3:2]	SPDIF_CH_PAIR_SEL	Selects the channel pair sent to the S/PDIF encoder. • 2'b00: CH1/2 (default) • 2'b01: CH3/4 • 2'b10: CH5/6 • 2'b11: CH7/8
[1]	ENABLE_SPDIF_ENCODE	Enables the S/PDIF encoder. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_TDM_ENCODE	Enables the 2 channel TDM encoder. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 24: S/PDIF CS ADDR

Bits	[7]	[6:3]	[2:0]
Default	1'b0	4'd0	3'd0

Bits	Mnemonic	Description
[7]	SPDIF_CS_WE	Write enable for the S/PDIF channel status bits. Writes the SPDIF_CS_DATA to the byte at address SPDIF_CS_BYTE_SEL. Toggle high-low to perform a write.
[6:3]	RESERVED	N/A
[2:0]	SPDIF_CS_BYTE_ADDR	Byte of the 40-bit S/PDIF Channel Status register to write to.

Register 25: S/PDIF CS DATA

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	SPDIF_CS_BYTE_DATA	Data to write into the 40-bit S/PDIF Channel Status register.

Register 26: TDM ENC SLOT SEL CH1

Bits	[7:5]	[4:0]
Default	3'd0	5'd0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH1	Selects which TDM channel slot is filled by the CH1 data. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 27: TDM ENC SLOT SEL CH2

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH2	Selects which TDM channel slot is filled by the CH2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 28: TDM ENC SLOT SEL CH3

Bits	[7:5]	[4:0]
Default	3'd0	5'd2

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH3	Selects which TDM channel slot is filled by the CH3 data. • 5'd0: Slot 1 • 5'd2: Slot 3 (default) • 5'd31: Slot 32

Register 29: TDM ENC SLOT SEL CH4

Bits	[7:5]	[4:0]
Default	3'd0	5'd3

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH4	Selects which TDM channel slot is filled by the CH4 data. • 5'd0: Slot 1 • 5'd3: Slot 4 (default) • 5'd31: Slot 32

Register 30: TDM ENC SLOT SEL CH5

Bits	[7:5]	[4:0]
Default	3'd0	5'd4

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH5	Selects which TDM channel slot is filled by the CH5 data. • 5'd0: Slot 1 • 5'd4: Slot 5 (default) • 5'd31: Slot 32

Register 31: TDM ENC SLOT SEL CH6

Bits	[7:5]	[4:0]
Default	3'd0	5'd5

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH6	Selects which TDM channel slot is filled by the CH6 data. • 5'd0: Slot 1 • 5'd5: Slot 6 (default) • 5'd31: Slot 32

Register 32: TDM ENC SLOT SEL CH7

Bits	[7:5]	[4:0]
Default	3'd0	5'd6

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH7	Selects which TDM channel slot is filled by the CH7 data. • 5'd0: Slot 1 • 5'd6: Slot 7 (default) • 5'd31: Slot 32

Register 33: TDM ENC SLOT SEL CH8

Bits	[7:5]	[4:0]
Default	3'd0	5'd7

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH8	Selects which TDM channel slot is filled by the CH8 data. • 5'd0: Slot 1 • 5'd7: Slot 8 (default) • 5'd31: Slot 32

Register 35-34: RESERVED

Register 36: STATUS BITS MASKP 1

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_MASKP	Masks negative to positive transitions of the CH8 "Minimum Volume" flag.
[6]	VOL_MIN_CH7_MASKP	Masks negative to positive transitions of the CH7 "Minimum Volume" flag.
[5]	VOL_MIN_CH6_MASKP	Masks negative to positive transitions of the CH6 "Minimum Volume" flag.
[4]	VOL_MIN_CH5_MASKP	Masks negative to positive transitions of the CH5 "Minimum Volume" flag.
[3]	VOL_MIN_CH4_MASKP	Masks negative to positive transitions of the CH4 "Minimum Volume" flag.
[2]	VOL_MIN_CH3_MASKP	Masks negative to positive transitions of the CH3 "Minimum Volume" flag.
[1]	VOL_MIN_CH2_MASKP	Masks negative to positive transitions of the CH2 "Minimum Volume" flag.
[0]	VOL_MIN_CH1_MASKP	Masks negative to positive transitions of the CH1 "Minimum Volume" flag.

Register 37: STATUS BITS MASKP 2

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_CH8_MASKP	Masks negative to positive transitions of the CH8 "Automute Status" flag.
[6]	AUTOMUTE_CH7_MASKP	Masks negative to positive transitions of the CH7 "Automute Status" flag.
[5]	AUTOMUTE_CH6_MASKP	Masks negative to positive transitions of the CH6 "Automute Status" flag.
[4]	AUTOMUTE_CH5_MASKP	Masks negative to positive transitions of the CH5 "Automute Status" flag.
[3]	AUTOMUTE_CH4_MASKP	Masks negative to positive transitions of the CH4 "Automute Status" flag.
[2]	AUTOMUTE_CH3_MASKP	Masks negative to positive transitions of the CH3 "Automute Status" flag.
[1]	AUTOMUTE_CH2_MASKP	Masks negative to positive transitions of the CH2 "Automute Status" flag.
[0]	AUTOMUTE_CH1_MASKP	Masks negative to positive transitions of the CH1 "Automute Status" flag.

Register 38: STATUS BITS MASKP 3

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_MASKP	Masks negative to positive transitions of the CH8 "Soft Ramp Done" flag.
[6]	SS_FULL_RAMP_CH7_MASKP	Masks negative to positive transitions of the CH7 "Soft Ramp Done" flag.
[5]	SS_FULL_RAMP_CH6_MASKP	Masks negative to positive transitions of the CH6 "Soft Ramp Done" flag.
[4]	SS_FULL_RAMP_CH5_MASKP	Masks negative to positive transitions of the CH5 "Soft Ramp Done" flag.
[3]	SS_FULL_RAMP_CH4_MASKP	Masks negative to positive transitions of the CH4 "Soft Ramp Done" flag.
[2]	SS_FULL_RAMP_CH3_MASKP	Masks negative to positive transitions of the CH3 "Soft Ramp Done" flag.
[1]	SS_FULL_RAMP_CH2_MASKP	Masks negative to positive transitions of the CH2 "Soft Ramp Done" flag.
[0]	SS_FULL_RAMP_CH1_MASKP	Masks negative to positive transitions of the CH1 "Soft Ramp Done" flag.

Register 39: STATUS BITS MASKP 4

Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	INPUT_SEL_OVR_MASKP	Masks negative to positive transitions of either bit of the "INPUT_SEL_OVERRIDE" flag.
[4]	DOP_VALID_CH12_MASKP	Masks negative to positive transitions of CH1/2 channel pair "DOP_VALID" flag.
[3]	TDM_DATA_VALID_MASKP	Masks negative to positive transitions of the "TDM_DATA_VALID" flag.
[2]	BCK_WS_FAIL_MASKP	Masks negative to positive transitions of the "BCK_WS_FAIL" flag.
[1]	RESERVED	N/A
[0]	PLL_LOCKED_MASKP	Masks negative to positive transitions of the "PLL_LOCKED" flag.

Register 40: STATUS BITS MASKN 1

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_MASKN	Masks positive to negative transitions of the CH8 "Minimum Volume" flag.
[6]	VOL_MIN_CH7_MASKN	Masks positive to negative transitions of the CH7 "Minimum Volume" flag.
[5]	VOL_MIN_CH6_MASKN	Masks positive to negative transitions of the CH6 "Minimum Volume" flag.
[4]	VOL_MIN_CH5_MASKN	Masks positive to negative transitions of the CH5 "Minimum Volume" flag.
[3]	VOL_MIN_CH4_MASKN	Masks positive to negative transitions of the CH4 "Minimum Volume" flag.
[2]	VOL_MIN_CH3_MASKN	Masks positive to negative transitions of the CH3 "Minimum Volume" flag.
[1]	VOL_MIN_CH2_MASKN	Masks positive to negative transitions of the CH2 "Minimum Volume" flag.
[0]	VOL_MIN_CH1_MASKN	Masks positive to negative transitions of the CH1 "Minimum Volume" flag.

Register 41: STATUS BITS MASKN 2

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_CH8_MASKN	Masks positive to negative transitions of the CH8 "Automute Status" flag.
[6]	AUTOMUTE_CH7_MASKN	Masks positive to negative transitions of the CH7 "Automute Status" flag.
[5]	AUTOMUTE_CH6_MASKN	Masks positive to negative transitions of the CH6 "Automute Status" flag.
[4]	AUTOMUTE_CH5_MASKN	Masks positive to negative transitions of the CH5 "Automute Status" flag.
[3]	AUTOMUTE_CH4_MASKN	Masks positive to negative transitions of the CH4 "Automute Status" flag.
[2]	AUTOMUTE_CH3_MASKN	Masks positive to negative transitions of the CH3 "Automute Status" flag.
[1]	AUTOMUTE_CH2_MASKN	Masks positive to negative transitions of the CH2 "Automute Status" flag.
[0]	AUTOMUTE_CH1_MASKN	Masks positive to negative transitions of the CH1 "Automute Status" flag.

Register 42: STATUS BITS MASKN 3

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_MASKN	Masks positive to negative transitions of the CH8 "Soft Ramp Done" flag.
[6]	SS_FULL_RAMP_CH7_MASKN	Masks positive to negative transitions of the CH7 "Soft Ramp Done" flag.
[5]	SS_FULL_RAMP_CH6_MASKN	Masks positive to negative transitions of the CH6 "Soft Ramp Done" flag.
[4]	SS_FULL_RAMP_CH5_MASKN	Masks positive to negative transitions of the CH5 "Soft Ramp Done" flag.
[3]	SS_FULL_RAMP_CH4_MASKN	Masks positive to negative transitions of the CH4 "Soft Ramp Done" flag.
[2]	SS_FULL_RAMP_CH3_MASKN	Masks positive to negative transitions of the CH3 "Soft Ramp Done" flag.
[1]	SS_FULL_RAMP_CH2_MASKN	Masks positive to negative transitions of the CH2 "Soft Ramp Done" flag.
[0]	SS_FULL_RAMP_CH1_MASKN	Masks positive to negative transitions of the CH1 "Soft Ramp Done" flag.

Register 43: STATUS BITS MASKN 4

Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	INPUT_SEL_OVR_MASKN	Masks positive to negative transitions of either bit of the "INPUT_SEL_OVERRIDE" flag.
[4]	DOP_VALID_CH12_MASKN	Masks positive to negative transitions of CH1/2 channel pair "DOP_VALID" flag.
[3]	TDM_DATA_VALID_MASKN	Masks positive to negative transitions of the "TDM_DATA_VALID" flag.
[2]	BCK_WS_FAIL_MASKN	Masks positive to negative transitions of the "BCK_WS_FAIL" flag.
[1]	RESERVED	N/A
[0]	PLL_LOCKED_MASKN	Masks positive to negative transitions of the "PLL_LOCKED" flag.

Register 44: STATUS BITS CLEAR 1

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_CLEAR	Toggle high-low to clear and re-arm status bit.
[6]	VOL_MIN_CH7_CLEAR	Toggle high-low to clear and re-arm status bit.
[5]	VOL_MIN_CH6_CLEAR	Toggle high-low to clear and re-arm status bit.
[4]	VOL_MIN_CH5_CLEAR	Toggle high-low to clear and re-arm status bit.
[3]	VOL_MIN_CH4_CLEAR	Toggle high-low to clear and re-arm status bit.
[2]	VOL_MIN_CH3_CLEAR	Toggle high-low to clear and re-arm status bit.
[1]	VOL_MIN_CH2_CLEAR	Toggle high-low to clear and re-arm status bit.
[0]	VOL_MIN_CH1_CLEAR	Toggle high-low to clear and re-arm status bit.

Register 45: STATUS BITS CLEAR 2

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_CH8_CLEAR	Toggle high-low to clear and re-arm status bit.
[6]	AUTOMUTE_CH7_CLEAR	Toggle high-low to clear and re-arm status bit.
[5]	AUTOMUTE_CH6_CLEAR	Toggle high-low to clear and re-arm status bit.
[4]	AUTOMUTE_CH5_CLEAR	Toggle high-low to clear and re-arm status bit.
[3]	AUTOMUTE_CH4_CLEAR	Toggle high-low to clear and re-arm status bit.
[2]	AUTOMUTE_CH3_CLEAR	Toggle high-low to clear and re-arm status bit.
[1]	AUTOMUTE_CH2_CLEAR	Toggle high-low to clear and re-arm status bit.
[0]	AUTOMUTE_CH1_CLEAR	Toggle high-low to clear and re-arm status bit.

Register 46: STATUS BITS CLEAR 3

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_CLEAR	Toggle high-low to clear and re-arm status bit.
[6]	SS_FULL_RAMP_CH7_CLEAR	Toggle high-low to clear and re-arm status bit.
[5]	SS_FULL_RAMP_CH6_CLEAR	Toggle high-low to clear and re-arm status bit.
[4]	SS_FULL_RAMP_CH5_CLEAR	Toggle high-low to clear and re-arm status bit.
[3]	SS_FULL_RAMP_CH4_CLEAR	Toggle high-low to clear and re-arm status bit.
[2]	SS_FULL_RAMP_CH3_CLEAR	Toggle high-low to clear and re-arm status bit.
[1]	SS_FULL_RAMP_CH2_CLEAR	Toggle high-low to clear and re-arm status bit.
[0]	SS_FULL_RAMP_CH1_CLEAR	Toggle high-low to clear and re-arm status bit.

Register 47: STATUS BITS CLEAR 4

Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	INPUT_SEL_OVR_CLEAR	Toggle high-low to clear and re-arm status bit.
[4]	DOP_VALID_CH12_CLEAR	Toggle high-low to clear and re-arm status bit.
[3]	TDM_DATA_VALID_CLEAR	Toggle high-low to clear and re-arm status bit.
[2]	BCK_WS_FAIL_CLEAR	Toggle high-low to clear and re-arm status bit.
[1]	CLK_AVALID_CLEAR	Toggle high-low to clear and re-arm status bit.
[0]	PLL_LOCKED_CLEAR	Toggle high-low to clear and re-arm status bit.

Register 48: RESERVED

Register 49: CHARGE PUMP CONFIG

Bits	[7:1]	[0]
Default	7'b0000000	1'b1

Bits	Mnemonic	Description
[7:1]	RESERVED	N/A
[0]	CP_MUTE_PD_EN	Charge pump state control when the DAC mutes. • 1'b0: Keep charge pump on when DAC mutes • 1'b1: Power down charge pump when DAC mutes (default)

Register 50: RESERVED

Register 51: CHARGE PUMP CLOCK DIV

Bits	[7:0]
Default	8'd31

Bits	Mnemonic	Description
[7:0]	CP_CLK_DIV	Specifies the clk divider for the CP clock source. Valid from 8'd0 to 8'd255. $\text{CP\_CLK [Hz]} = \frac{\text{MCLK}}{2^{\sim \text{MCLK\_RATE\_SEL}} \cdot (\text{CP\_CLK\_DIV} + 1)}$

Register 66-52: RESERVED

GPIO Registers

Register 67: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configure GPIO2 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Reserved • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved
[3:0]	GPIO1_CFG	Configure GPIO1 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Reserved • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved

Register 68: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Reserved • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved
[3:0]	GPIO3_CFG	Configure GPIO3 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Reserved • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved

Register 69: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configure GPIO6 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Reserved • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved
[3:0]	GPIO5_CFG	Configure GPIO5 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Reserved • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved

Register 70: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO8_CFG	Configure GPIO8 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Reserved • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved
[3:0]	GPIO7_CFG	Configure GPIO7 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Reserved • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved

Register 71: GPIO9/10 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO10_CFG	Configure GPIO10 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Clock valid flag – output • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved
[3:0]	GPIO9_CFG	Configure GPIO9 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: Clock valid flag – output • 4'd4: PLL locked flag – output • 4'd5: DAC Minimum Volume flag – output • 4'd6: DAC Automute status – output • 4'd7: DAC Soft Ramp Done flag – output • 4'd8: Mute all channels – input • 4'd9: System Mode control – input • 4'd10: OR of Status Bits – output • 4'd11: S/PDIF stream – output • 4'd12: PWM signal – output • 4'd13: MCLK_128FS – output • 4'd14: Reserved • 4'd15: Reserved

Register 73-72: GPIO INPUT CONTROL

Bits	[15]	[14]	[13:10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	4'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[15]	RESERVED	N/A
[14]	GPIO_SYSTEM_MODE	When any GPIO_CFG is "System mode control": • 1'b0: Disable DAC when GPIOx input is 1'b1 • 1'b1: Enable DAC when GPIO input is 1'b1 When GPIOx input is 1'b0, system mode is determined by register 0[0] ENABLE_DAC.
[13:10]	RESERVED	N/A
[9]	GPIO10_SDB	• 1'b0: Disables GPIO10 input (default) • 1'b1: Enables GPIO10 input
[8]	GPIO9_SDB	• 1'b0: Disables GPIO9 input (default) • 1'b1: Enables GPIO9 input
[7]	GPIO8_SDB	• 1'b0: Disables GPIO8 input (default) • 1'b1: Enables GPIO8 input
[6]	GPIO7_SDB	• 1'b0: Disables GPIO7 input (default) • 1'b1: Enables GPIO7 input
[5]	GPIO6_SDB	• 1'b0: Disables GPIO6 input (default) • 1'b1: Enables GPIO6 input
[4]	GPIO5_SDB	• 1'b0: Disables GPIO5 input (default) • 1'b1: Enables GPIO5 input
[3]	GPIO4_SDB	• 1'b0: Disables GPIO4 input (default) • 1'b1: Enables GPIO4 input
[2]	GPIO3_SDB	• 1'b0: Disables GPIO3 input (default) • 1'b1: Enables GPIO3 input
[1]	GPIO2_SDB	• 1'b0: Disables GPIO2 input (default) • 1'b1: Enables GPIO2 input
[0]	GPIO1_SDB	• 1'b0: Disables GPIO1 input • 1'b1: Enables GPIO1 input (default)

Register 75-74: GPIO OUTPUT CONTROL

Bits	[15]	[14]	[13]	[12:10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b1	1'b1	3'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15]	GPIO_AND_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(ss_full_ramp[CHx]) (default) Note: overridden by GPIO_OR_SS_RAMP.
[14]	GPIO_AND_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise AND of both channel's statuses. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(automute[CHx]) (default) Note: overridden by GPIO_OR_AUTOMUTE.
[13]	GPIO_AND_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(vol_min[CHx]) (default) Note: overridden by GPIO_OR_VOL_MIN.
[12:10]	RESERVED	N/A
[9]	GPIO10_OE	• 1'b0: Tristate GPIO10 (default) • 1'b1: GPIO10 Output enabled
[8]	GPIO9_OE	• 1'b0: Tristate GPIO9 (default) • 1'b1: GPIO9 Output enabled
[7]	GPIO8_OE	• 1'b0: Tristate GPIO8 (default) • 1'b1: GPIO8 Output enabled
[6]	GPIO7_OE	• 1'b0: Tristate GPIO7 (default) • 1'b1: GPIO7 Output enabled
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 (default) • 1'b1: GPIO6 Output enabled
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 (default) • 1'b1: GPIO5 Output enabled
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 (default) • 1'b1: GPIO4 Output enabled
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 (default) • 1'b1: GPIO3 Output enabled
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 (default) • 1'b1: GPIO2 Output enabled
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 (default) • 1'b1: GPIO1 Output enabled

Register 77-76: GPIO INVERT CONTROL

Bits	[15]	[14]	[13]	[12:10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	3'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15]	GPIO_OR_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(ss_full_ramp[CHx])
[14]	GPIO_OR_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise OR of both channel's statuses. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(automute[CHx])
[13]	GPIO_OR_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(vol_min[CHx])
[12:10]	RESERVED	N/A
[9]	GPIO10_INV	Invert the GPIO10 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[8]	GPIO9_INV	Invert the GPIO9 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[7]	GPIO8_INV	Invert the GPIO8 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6]	GPIO7_INV	Invert the GPIO7 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[5]	GPIO6_INV	Invert the GPIO6 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[4]	GPIO5_INV	Invert the GPIO5 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[3]	GPIO4_INV	Invert the GPIO4 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	GPIO3_INV	Invert the GPIO3 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	GPIO2_INV	Invert the GPIO2 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	GPIO1_INV	Invert the GPIO1 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 79-78: GPIO KEEPER CONTROL

Bits	[15:10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	6'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:10]	RESERVED	N/A
[9]	GPIO10_WK_EN	• 1'b0: GPIO10 weak keeper disabled (default) • 1'b1: GPIO10 weak keeper enabled
[8]	GPIO9_WK_EN	• 1'b0: GPIO9 weak keeper disabled (default) • 1'b1: GPIO9 weak keeper enabled
[7]	GPIO8_WK_EN	• 1'b0: GPIO8 weak keeper disabled (default) • 1'b1: GPIO8 weak keeper enabled
[6]	GPIO7_WK_EN	• 1'b0: GPIO7 weak keeper disabled (default) • 1'b1: GPIO7 weak keeper enabled
[5]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[4]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 81-80: GPIO READ CONTROL

Bits	[15:10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	6'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:10]	RESERVED	N/A
[9]	GPIO10_READ	Enables readback of the GPIO10 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[8]	GPIO9_READ	Enables readback of the GPIO9 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[7]	GPIO8_READ	Enables readback of the GPIO8 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	GPIO7_READ	Enables readback of the GPIO7 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	GPIO6_READ	Enables readback of the GPIO6 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	GPIO5_READ	Enables readback of the GPIO5 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	GPIO4_READ	Enables readback of the GPIO4 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	GPIO3_READ	Enables readback of the GPIO3 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	GPIO2_READ	Enables readback of the GPIO2 input. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	GPIO1_READ	Enables readback of the GPIO1 input. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 82: PWM COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM_COUNT	8-bit value setting the number of MCLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 84-83: PWM FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM_FREQ	16-bit value to set the frequency of the PWM signal in terms of MCLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $$\text{Frequency [Hz]} = \frac{\text{MCLK}}{\text{PWM\_FREQ} + 1}$$ $$\text{Duty Cycle [\%]} = \frac{\text{PWM\_COUNT}}{\text{PWM\_FREQ} + 1} \cdot 100$$

DAC Registers

Register 85: RESERVED

Register 86: DAC FILTER CONFIG

Bits	[7:6]	[5]	[4]	[3]	[2:0]
Default	2'd0	1'b0	1'b0	1'b0	3'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	BYPASS_IIR	Bypass the IIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[4]	BYPASS_FIR4X	Bypass the 4X FIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[3]	BYPASS_FIR2X	Bypass the 2X FIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 87: VOLUME CH1

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	VOLUME_CH1	DAC CH1 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 88: VOLUME CH2

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	VOLUME_CH2	DAC CH2 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 89: VOLUME CH3

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	VOLUME_CH3	DAC CH3 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 90: VOLUME CH4

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	VOLUME_CH4	DAC CH4 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 91: VOLUME CH5

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	VOLUME_CH5	DAC CH5 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 92: VOLUME CH6

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	VOLUME_CH6	DAC CH6 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 93: VOLUME CH7

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	VOLUME_CH7	DAC CH7 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 94: VOLUME CH8

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	VOLUME_CH8	DAC CH8 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 95: PHASE INVERSION

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_PHASE_INV_CH8	Inverts the phase of VOLUME_CH8. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6]	VOL_PHASE_INV_CH7	Inverts the phase of VOLUME_CH7. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[5]	VOL_PHASE_INV_CH6	Inverts the phase of VOLUME_CH6. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[4]	VOL_PHASE_INV_CH5	Inverts the phase of VOLUME_CH5. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[3]	VOL_PHASE_INV_CH4	Inverts the phase of VOLUME_CH4. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	VOL_PHASE_INV_CH3	Inverts the phase of VOLUME_CH3. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	VOL_PHASE_INV_CH2	Inverts the phase of VOLUME_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	VOL_PHASE_INV_CH1	Inverts the phase of VOLUME_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 99-96: DIGITAL GAIN

Bits	[31:30]	[29:27]	[26:24]	[23:22]	[21:19]	[18:16]	[15:14]	[13:11]	[10:8]	[7:6]	[5:3]	[2:0]
Default	2'd0	3'd0	3'd0	2'd0	3'd0	3'd0	2'd0	3'd0	3'd0	2'd0	3'd0	3'd0

Bits	Mnemonic	Description
[31:30]	RESERVED	N/A
[29:27]	DIGITAL_GAIN_CH8	DAC CH8 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd7: +42dB
[26:24]	DIGITAL_GAIN_CH7	DAC CH7 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd7: +42dB
[23:22]	RESERVED	N/A
[21:19]	DIGITAL_GAIN_CH6	DAC CH6 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd7: +42dB
[18:16]	DIGITAL_GAIN_CH5	DAC CH5 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd7: +42dB
[15:14]	RESERVED	N/A
[13:11]	DIGITAL_GAIN_CH4	DAC CH4 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd7: +42dB
[10:8]	DIGITAL_GAIN_CH3	DAC CH3 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd7: +42dB
[7:6]	RESERVED	N/A
[5:3]	DIGITAL_GAIN_CH2	DAC CH2 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd7: +42dB
[2:0]	DIGITAL_GAIN_CH1	DAC CH1 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd7: +42dB

Register 100: MUTE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	MUTE_CH8	Mutes the CH8 datapath. • 1'b0: Normal CH8 operation (default) • 1'b1: Mute CH8
[6]	MUTE_CH7	Mutes the CH7 datapath. • 1'b0: Normal CH7 operation (default) • 1'b1: Mute CH7
[5]	MUTE_CH6	Mutes the CH6 datapath. • 1'b0: Normal CH6 operation (default) • 1'b1: Mute CH6
[4]	MUTE_CH5	Mutes the CH5 datapath. • 1'b0: Normal CH5 operation (default) • 1'b1: Mute CH5
[3]	MUTE_CH4	Mutes the CH4 datapath. • 1'b0: Normal CH4 operation (default) • 1'b1: Mute CH4
[2]	MUTE_CH3	Mutes the CH3 datapath. • 1'b0: Normal CH3 operation (default) • 1'b1: Mute CH3
[1]	MUTE_CH2	Mutes the CH2 datapath. • 1'b0: Normal CH2 operation (default) • 1'b1: Mute CH2
[0]	MUTE_CH1	Mutes the CH1 datapath. • 1'b0: Normal CH1 operation (default) • 1'b1: Mute CH1

Register 101: SOFT RAMP CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b1	5'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	MONO_VOLUME	All channel volumes controlled by the CH1 volume control. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	MUTE_RAMP_TO_GROUND	• 1'b0: When ramped to min volume during normal mute, do not soft ramp to ground • 1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default) normal mute includes: automute, mute by register, mute by GPIO
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 20 (inclusive). $\text{Time [s]} = \frac{2^{15} \cdot 2^{\text{SOFT\_RAMP\_TIME}} \cdot 2^{\sim\text{MCLK\_RATE\_SEL}}}{MCLK}$

Register 102: VOLUME UP RAMP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	VOL_RAMP_RATE_UP	Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{Ramp\_rate [dB/s]} = 20\log_{10}\left(\frac{\text{VOL\_RAMP\_RATE\_UP} \cdot FS}{2^{12}}\right)$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 103: VOLUME DOWN RAMP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	VOL_RAMP_RATE_DOWN	Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{Ramp\_rate [dB/s]} = 20\log_{10}\left(\frac{\text{VOL\_RAMP\_RATE\_DOWN}}{2^{12}}\right)$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 104: DC OFFSET

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	DC_OFFSET	Signed 8-bit DC offset value added to all 8 datapath signals, 100 uV/step. • 8'hFF: -12.7mV DC Offset • 8'h00: 0mV DC Offset (default) • 8'h7F: 12.6mV DC Offset

Register 105: AUTOMUTE ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	AUTOMUTE_EN_CH8	Enables CH8 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[6]	AUTOMUTE_EN_CH7	Enables CH7 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[5]	AUTOMUTE_EN_CH6	Enables CH6 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[4]	AUTOMUTE_EN_CH5	Enables CH5 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[3]	AUTOMUTE_EN_CH4	Enables CH4 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[2]	AUTOMUTE_EN_CH3	Enables CH3 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[1]	AUTOMUTE_EN_CH2	Enables CH2 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[0]	AUTOMUTE_EN_CH1	Enables CH1 automute. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 107-106: AUTOMUTE TIME

Bits	[15]	[14]	[13]	[12:11]	[10:0]
Default	1'b1	1'b0	1'b0	2'd0	11'h0F

Bits	Mnemonic	Description
[15]	DSD_FAULT_DETECT_EN	Sets a channel to a DSD mute pattern (0x96) if the DSD data has no changes in 64 DATA_CLKs. • 1'b0: Disabled • 1'b1: Enabled (default)
[14]	DSD_DC_AM_ENB	Disables the DSD automute condition, if a DC signal is detected. • 1'b0: Enabled (default) • 1'b1: Disabled
[13]	DSD_MUTE_AM_ENB	Disables the DSD automute condition, if a DSD mute pattern is detected. • 1'b0: Enabled (default) • 1'b1: Disabled
[12:11]	RESERVED	N/A
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. • 11'h000: Disabled • 11'h001: Slowest • 11'h00F: Default • 11'h7FF: Fastest $\text{Time [s]} = \frac{2^{18} \cdot 2^{64\text{FS\_MODE}}}{\text{AUTOMUTE\_TIME} \cdot \text{FS}}$

Register 109-108: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'h0008

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	The threshold which the audio must be below before an automute condition is flagged. • 16'h0001: -138dB • 16'h0008: -120dB (default) • 16'hFFFF: -42dB $\text{Level [dB]} = 20 \cdot \log_{10}\left(\frac{\text{AUTOMUTE\_LEVEL}}{(2^{16}-1) \cdot 2^{7}}\right)$

Register 111-110: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'h000A

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	The threshold which the audio must be above before the automute condition is immediately cleared. • 16'h0001: -138dB • 16'h000A: -118dB (default) • 16'hFFFF: -42dB $\text{Level [dB]} = 20 \cdot \log_{10}\left(\frac{\text{AUTOMUTE\_OFF\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$

Register 120-112: RESERVED

PLL Registers

Register 121: PLL CLOCK SELECT

Bits	[7]	[6]	[5:4]	[3]	[2:1]	[0]
Default	1'b0	1'b0	2'b10	1'b0	2'b00	1'b1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PLL_CLK_PHASE_INV	Digital/analog DAC clock invert phase enable. • 1'b0: Digital/analog DAC clocks have inverted phase (default) • 1'b1: Digital/analog DAC clocks have the same phase
[5:4]	SEL_PLL_CLK_IN	Selects PLL input clock source when EN_PLL_CLK_IN is set. • 2'b00: ACLK • 2'b10: DCLK (default) • Others: Reserved
[3]	EN_PLL_CLK_IN	Allows SEL_PLL_CLK_IN to select PLL input clocks. • 1'b0: Disables SEL_PLL_CLK_IN (default) • 1'b1: Enables SEL_PLL_CLK_IN
[2:1]	SEL_MCLK_IN	Selects digital core clock source when EN_MCLK_IN is set. • 2'b00: ACLK (default) • 2'b10: PLL_CLK • Others: Reserved
[0]	EN_MCLK_IN	Enables clock inputs to the digital core. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 122: PLL VCO & CP

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'b0011	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PLL_CP_EN	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	PLL_VCO_EN	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	PLL_CLKSMP_EN	Enables/disables the PLL circuitry. • 1'b0: PLL Block disabled (default) • 1'b1: PLL Block enabled
[0]	PLL_DIG_RSTB	Resets the Digital core of the PLL.

Register 123: PLL REGULATOR

Bits	[7:4]	[3]	[2:0]
Default	4'd0	1'b0	3'b010

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PLL_REG_EN	Enables/disables the PLL HV regulator (1.8V). • 1'b0: Disable the PLL regulator (default) • 1'b1: Enable the PLL regulator
[2:0]	RESERVED	N/A

Register 126-124: PLL FEEDBACK DIV

Bits	[23:0]
Default	24'h100000

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider (Nfb). • 24'h000000: Reserved • 24'h100000: Default • 24'hn: Divide by 2^"25"/n

Register 129-127: PLL IN & OUT DIV

Bits	[23:16]	[15:12]	[11:10]	[9]	[8:0]
Default	8'b00010000	4'd3	2'd0	1'b1	9'd0

Bits	Mnemonic	Description
[23:16]	RESERVED	N/A
[15:12]	PLL_CLK_OUT_DIV	Sets the PLL clock output divider (No). • 4'd0: Reserved • 4'd3: Divide by 4. (default) • 4'dn: Divide by (n + 1).
[11:10]	RESERVED	N/A
[9]	PLL_FB_DIV_LOAD	Write 1'b1 then write 1'b0 to load CLK_FB_DIV.
[8:0]	PLL_CLK_IN_DIV	Sets the PLL clock input divider (Ni). • 9'd0: Reserved (default) • 9'dn: Divide by (n + 1).

Register 135-130: RESERVED

ASP Registers

Register 136: ASP CONTROL

Bits	[7:3]	[2]	[1]	[0]
Default	5'd0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	ASP_FLUSH_MEMS	Flushes the ASP memories, clearing any existing programming. Requires ASP_CORE_EN to not be set.
[1]	ASP_PROG_EN	Enables ASP programming. Programmed functionality overridden. • 1'b0: Programming disabled (default) • 1'b1: Programming enabled
[0]	ASP_CORE_EN	Enables programmed ASP functionality. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 137: ASP BYPASS

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ASP_BYPASS_CH8	Bypasses the ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[6]	ASP_BYPASS_CH7	Bypasses the ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[5]	ASP_BYPASS_CH6	Bypasses the ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[4]	ASP_BYPASS_CH5	Bypasses the ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[3]	ASP_BYPASS_CH4	Bypasses the ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[2]	ASP_BYPASS_CH3	Bypasses the ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[1]	ASP_BYPASS_CH2	Bypasses the ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[0]	ASP_BYPASS_CH1	Bypasses the ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed

Register 138-177: RESERVED

Register 178: SPI MASTER CONFIG

Bits	[7:4]	[3]	[2:1]	[0]
Default	4'd0	1'b0	2'b00	1'b0

Bits	Mnemonic	Description
[7:4]	SPI_M_PULSE_WIDTH	Sets the master SCLK frequency. $\text{SCLK [Hz]} = \frac{\text{MCLK}}{2 \cdot \text{SPI\_M\_PULSE\_WIDTH}}$
[3]	SPI_M_EN	Enable the SPI Master • 1'b0: Disabled (default) • 1'b1: Enabled
[2:1]	RESERVED	N/A
[0]	SPI_M_START	Start/stop SPI master transactions. • 1'b0: Transactions stopped (default) • 1'b1: Transactions started

Register 179: SPI MASTER DATA OUT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	SPI_M_DATA_O	Data byte to send over the SPI master interface.

Readback Registers

Register 224: INPUT FORMAT READ

Bits	[7:4]	[3]	[2:1]	[0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7:4]	DOP_VALID	DoP Valid flags, per channel pair.
[3]	DAC_TDM_VALID	TDM decoder valid flag.
[2:1]	INPUT_SEL_OVERRIDE	Readback of the current input data format. • 2'd0: PCM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: Reserved
[0]	PLL_LOCKED	PLL locked flag.

Register 225: CHIP ID

Bits	[7:0]
Default	8'h70

Bits	Mnemonic	Description
[7:0]	CHIP_ID	Chip ID • ES9082: 0x70

Register 228-226: RESERVED

Register 232-229: STATUS BITS STATE

Bits	[31]	[30:29]	[28]	[27]	[26]	[25]	[24]	[23:16]	[15:8]	[7:0]
Default	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[31]	RESERVED	N/A
[30:29]	INPUT_SEL_OVR_STATE	State of the masked INPUT_SELECT_OVERRIDE status bits. Note: Clear bits are required to reset value.
[28]	DOP_VALID_CH12_STATE	State of the masked DOP_VALID status bit. Note: Clear bits are required to reset value.
[27]	TDM_DATA_VALID_STATE	State of the masked TDM_DATA_VALID status bit. Note: Clear bits are required to reset value.
[26]	BCK_WS_FAIL_STATE	State of the masked BCK_WS_FAIL status bit. Note: Clear bits are required to reset value.
[25]	CLK_AVALID_STATE	State of the masked CLK_AVALID status bit. Note: Clear bits are required to reset value.
[24]	PLL_LOCKED_STATE	State of the masked PLL_LOCKED status bit. Note: Clear bits are required to reset value.
[23:16]	SS_FULL_RAMP_STATE	State of each channel's "Soft Ramp Done" status bit. Note: Clear bits are required to reset value.
[15:8]	AUTOMUTE_STATE	State of each channel's "Automute Status" status bit. Note: Clear bits are required to reset value.
[7:0]	VOL_MIN_STATE	State of each channel's "Minimum Volume" status bit. Note: Clear bits are required to reset value.

Register 233: RESERVED

Register 234: AUTO FS READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	EN_64FS_MODE_AUTO	Result {Z} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic, running the device in 64FS mode. • 1'b0: 64FS disabled • 1'b1: 64FS enabled
[6]	MCLK_128FS_HALF_DIV_AUTO	Result {Y} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. • 1'b0: MCLK_128FS is an integer multiple of MCLK, Y = 1. • 1'b1: MCLK_128FS is a (X+1)*0.5 multiple of MCLK, Y = 2.
[5:0]	MCLK_128FS_DIV_AUTO	Result {X} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. $\text{FS [Hz]} = \frac{Y \cdot MCLK}{(X+1) \cdot \left(\frac{128^Z}{2}\right)}$

Register 235: CLOCK VALIDITY

Bits	[7]	[6]	[5]	[4:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	Validity of the MCLK/MCLK_128FS ratio. • 1'b0: Invalid ratio • 1'b1: Valid ratio
[6]	BCK_INVALID	Validity of the BCK signal, requires BCK_MONITOR to be enabled.
[5]	WS_INVALID	Validity of the WS signal, requires WS_MONITOR to be enabled.
[4:0]	AUTO_CH_NUM	Automatic TDM channel number tuning result.

Register 237-236: GPIO READBACK

Bits	[15:10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[15:10]	RESERVED	N/A
[9]	GPIO10_R	GPIO10 input readback.
[8]	GPIO9_R	GPIO9 input readback.
[7]	GPIO8_R	GPIO8 input readback.
[6]	GPIO7_R	GPIO7 input readback.
[5]	GPIO6_R	GPIO6 input readback.
[4]	GPIO5_R	GPIO5 input readback.
[3]	GPIO4_R	GPIO4 input readback.
[2]	GPIO3_R	GPIO3 input readback.
[1]	GPIO2_R	GPIO2 input readback.
[0]	GPIO1_R	GPIO1 input readback.

Register 238: VOL MIN READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8	CH8 minimum volume flag.
[6]	VOL_MIN_CH7	CH7 minimum volume flag.
[5]	VOL_MIN_CH6	CH6 minimum volume flag.
[4]	VOL_MIN_CH5	CH5 minimum volume flag.
[3]	VOL_MIN_CH4	CH4 minimum volume flag.
[2]	VOL_MIN_CH3	CH3 minimum volume flag.
[1]	VOL_MIN_CH2	CH2 minimum volume flag.
[0]	VOL_MIN_CH1	CH1 minimum volume flag.

Register 239: AUTOMUTE READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	AUTOMUTE_CH8	CH2 automute status flag.
[6]	AUTOMUTE_CH7	CH1 automute status flag.
[5]	AUTOMUTE_CH6	CH2 automute status flag.
[4]	AUTOMUTE_CH5	CH1 automute status flag.
[3]	AUTOMUTE_CH4	CH2 automute status flag.
[2]	AUTOMUTE_CH3	CH1 automute status flag.
[1]	AUTOMUTE_CH2	CH2 automute status flag.
[0]	AUTOMUTE_CH1	CH1 automute status flag.

Register 240: SOFT RAMP UP READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_UP_CH8	CH2 soft ramped up flag.
[6]	SS_RAMP_UP_CH7	CH1 soft ramped up flag.
[5]	SS_RAMP_UP_CH6	CH2 soft ramped up flag.
[4]	SS_RAMP_UP_CH5	CH1 soft ramped up flag.
[3]	SS_RAMP_UP_CH4	CH2 soft ramped up flag.
[2]	SS_RAMP_UP_CH3	CH1 soft ramped up flag.
[1]	SS_RAMP_UP_CH2	CH2 soft ramped up flag.
[0]	SS_RAMP_UP_CH1	CH1 soft ramped up flag.

Register 241: SOFT RAMP DOWN READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_DOWN_CH8	CH2 soft ramped down flag.
[6]	SS_RAMP_DOWN_CH7	CH1 soft ramped down flag.
[5]	SS_RAMP_DOWN_CH6	CH2 soft ramped down flag.
[4]	SS_RAMP_DOWN_CH5	CH1 soft ramped down flag.
[3]	SS_RAMP_DOWN_CH4	CH2 soft ramped down flag.
[2]	SS_RAMP_DOWN_CH3	CH1 soft ramped down flag.
[1]	SS_RAMP_DOWN_CH2	CH2 soft ramped down flag.
[0]	SS_RAMP_DOWN_CH1	CH1 soft ramped down flag.

Register 250: SPI MASTER DATA IN

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	SPI_M_DATA_I	Byte of data read from the SPI slave device.

ES9082 Reference Schematic

Hardware (HW) Mode

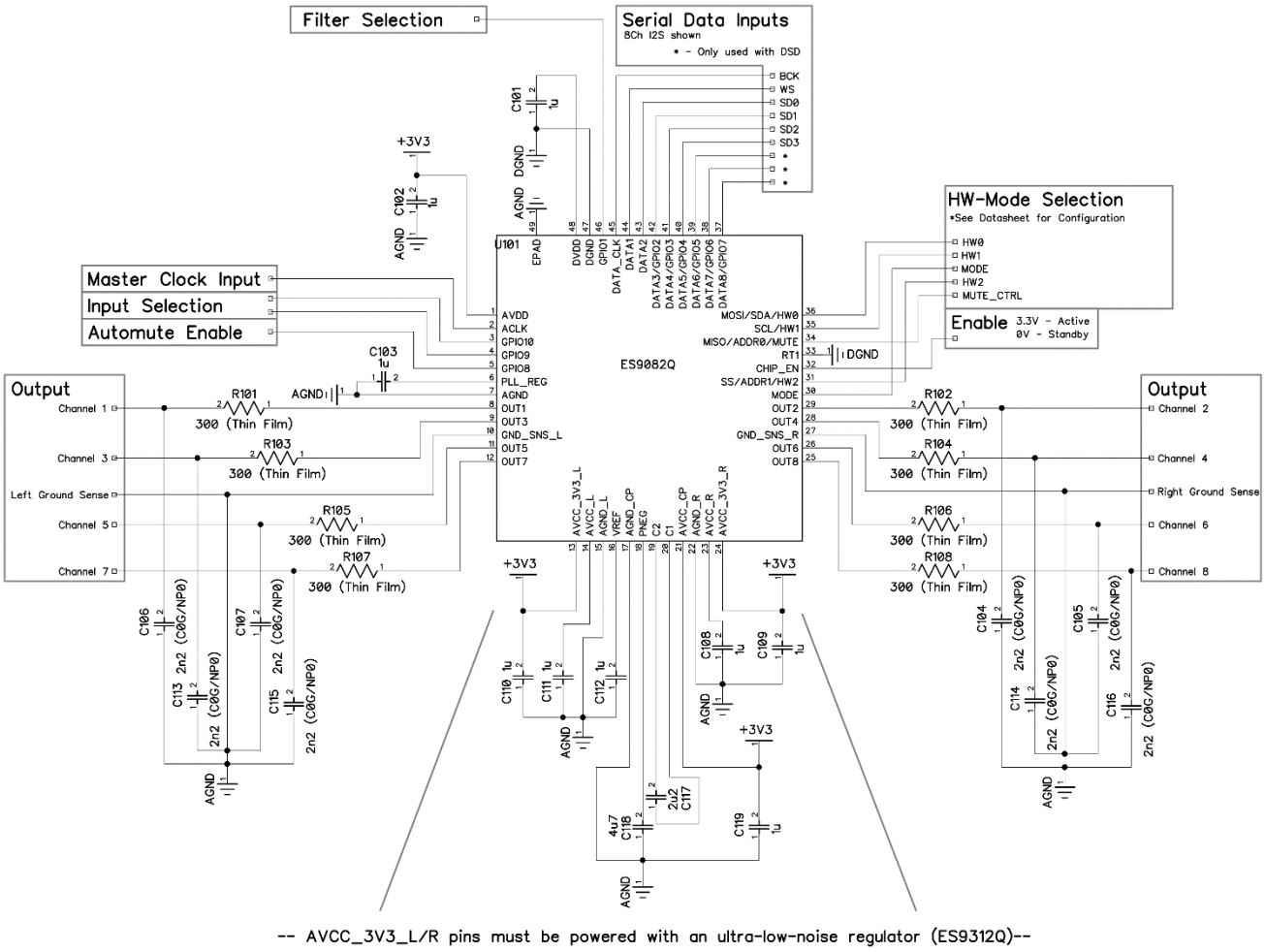


Figure 28 - ES9082 Hardware Mode Reference Schematic

Note: The ES9082 48QFN package has an exposed pad (Pin 49) that should be connected to ground.

Software (SW) Mode

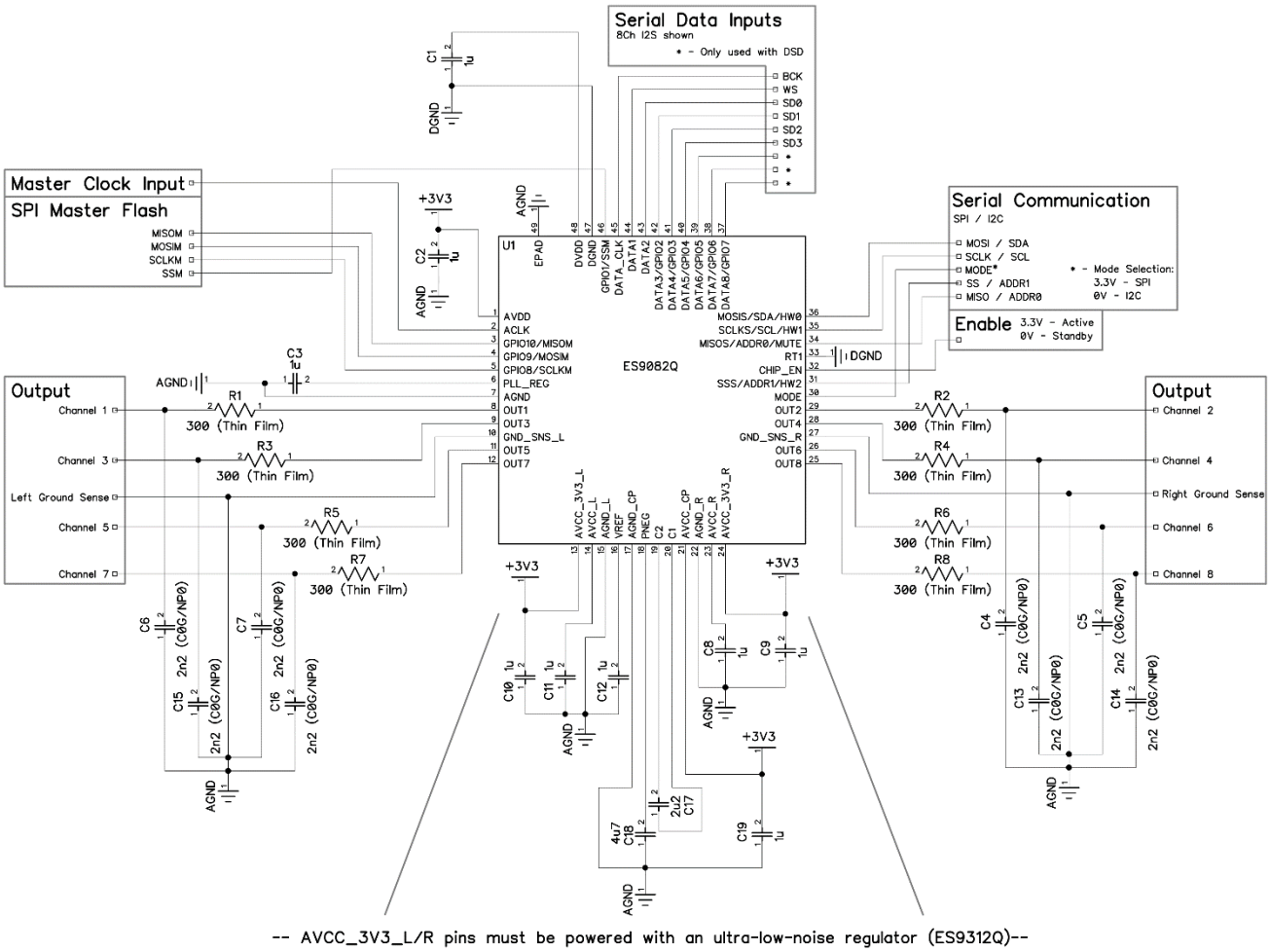


Figure 29 - ES9082 Software Mode Reference Schematic

Note: The ES9082 48QFN package has an exposed pad (Pin 49) that should be connected to ground.

Recommended Power Supply

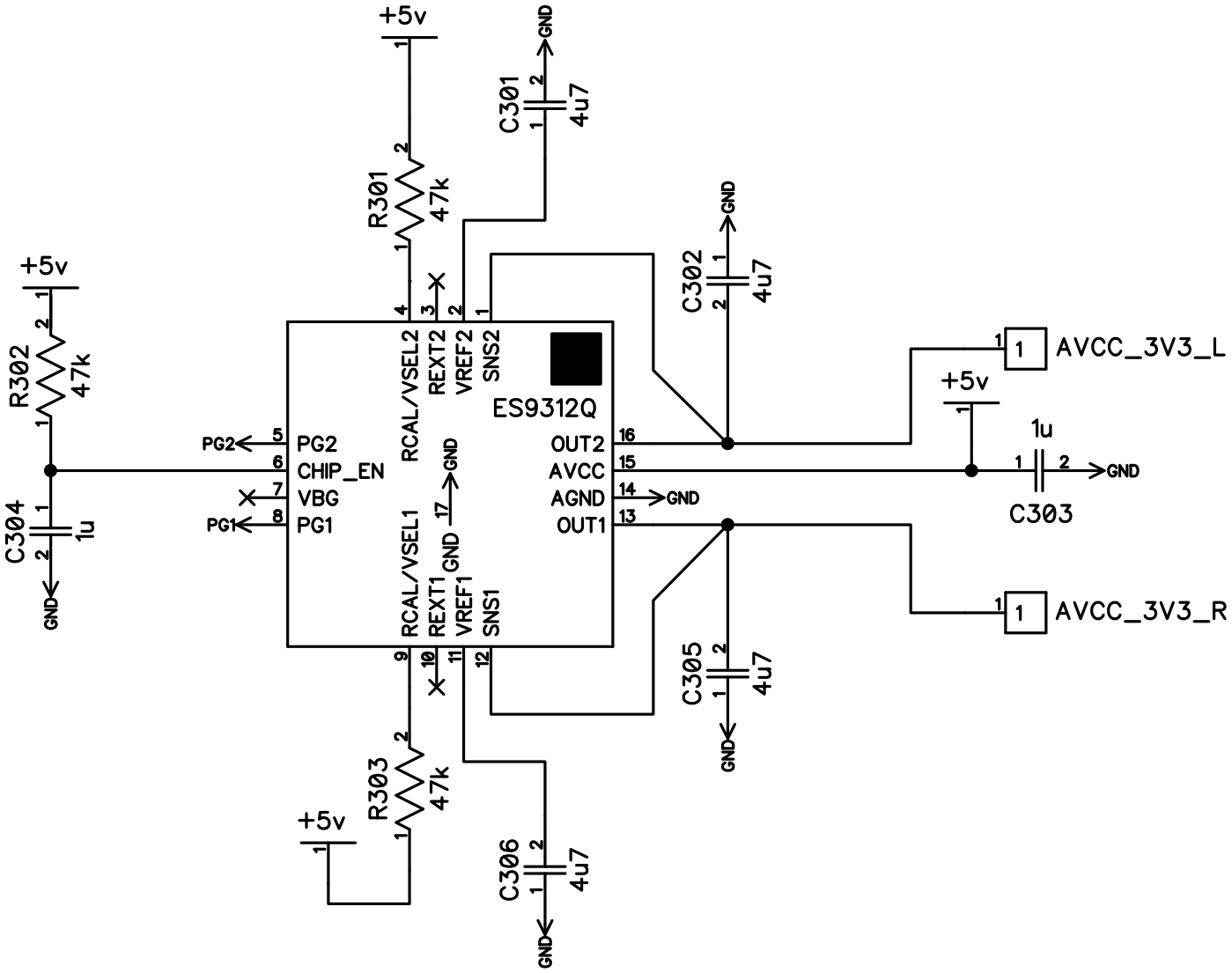


Figure 30 - ES9082 Power Supply Schematic

SPI Master Flash

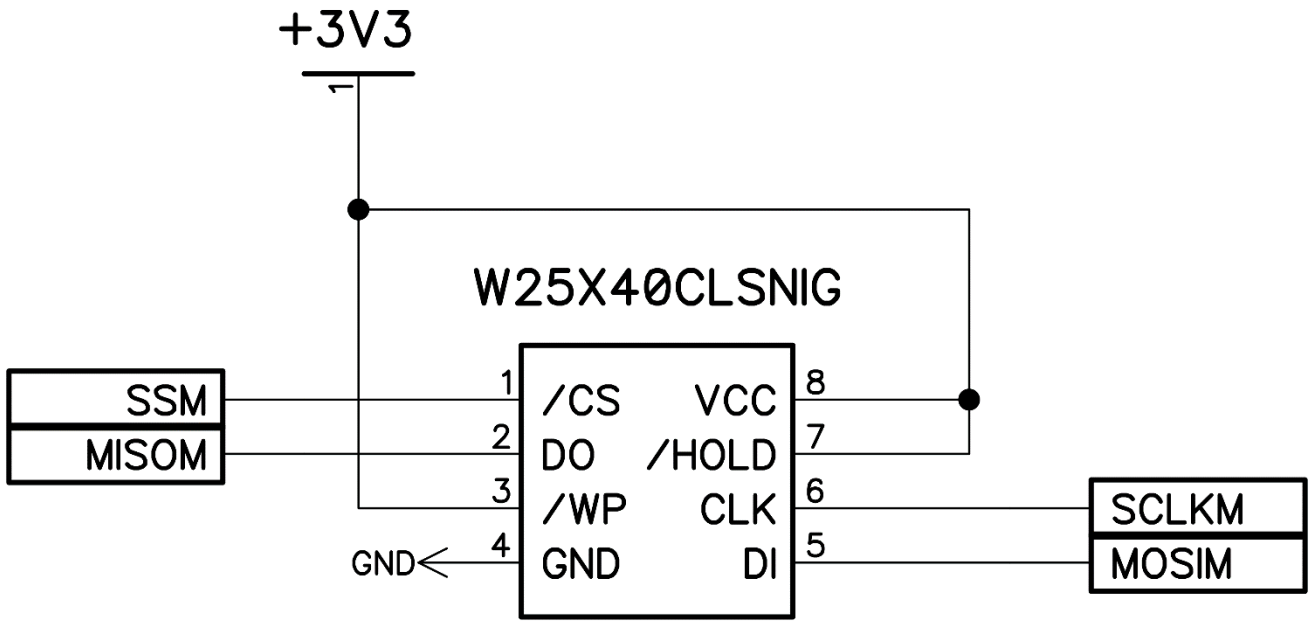
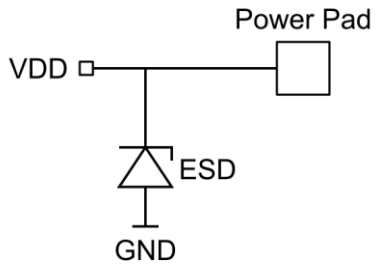
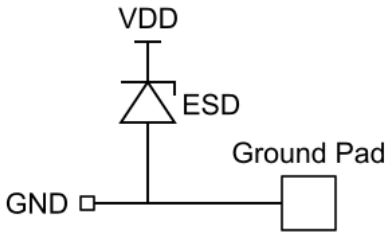
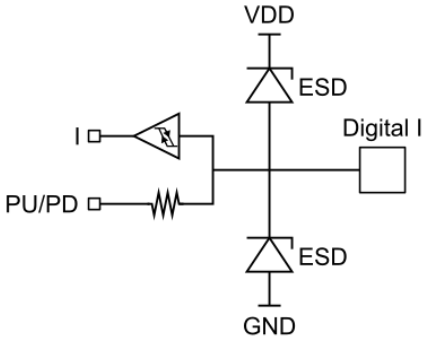
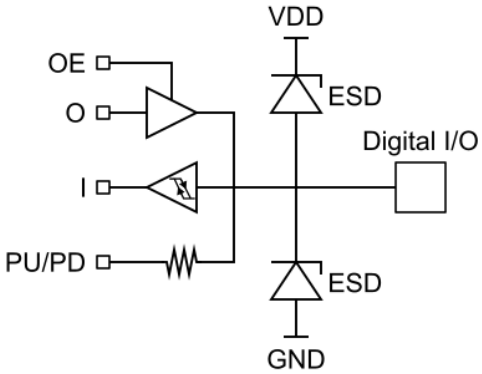


Figure 31 - Example SPI Flash Schematic

Internal Pad Circuitry

Pin Name	Type	Pin	Equivalent Circuit
AVDD AVCC_3V3_L AVCC_CP AVCC_3V3_R	Power	1 13 21 24	
AGND_L AGND_CP AGND_R DGND	Ground	15 17 22 47	
CHIP_EN	Reset	32	
GPIO10/MISOM GPIO9/MOSIM GPIO8/SCLKM MODE SSS/ADDR1/HW2 RT1 MISOS/ADDR0/MUTE_CTRL SCLKS/SCL/HW1 MOSIS/SDA/HW0 DATA8/GPIO7 DATA7/GPIO6 DATA6/GPIO5 DATA5/GPIO4 DATA4/GPIO3 DATA3/GPIO2 DATA2 DATA1 DATA_CLK GPIO1/SSM	Digital I/O	3 4 5 30 31 33 34 35 36 37 38 39 40 41 42 43 44 45 46	

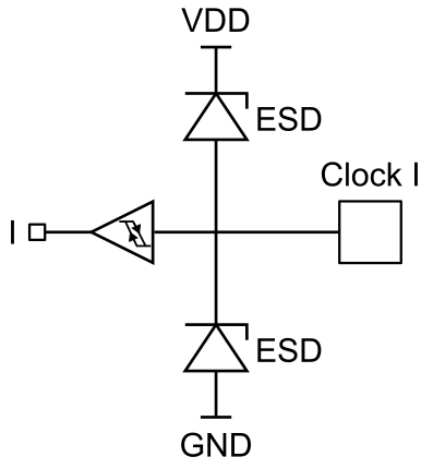
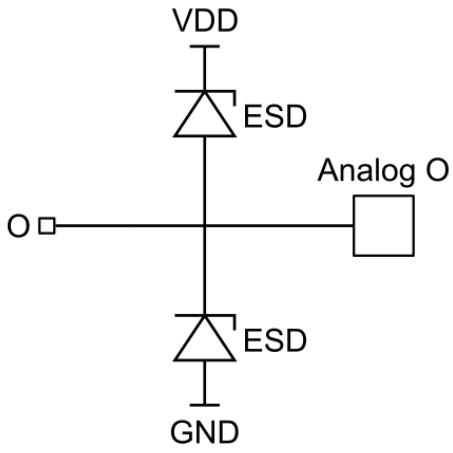
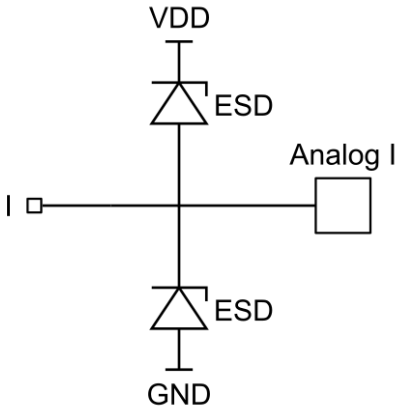
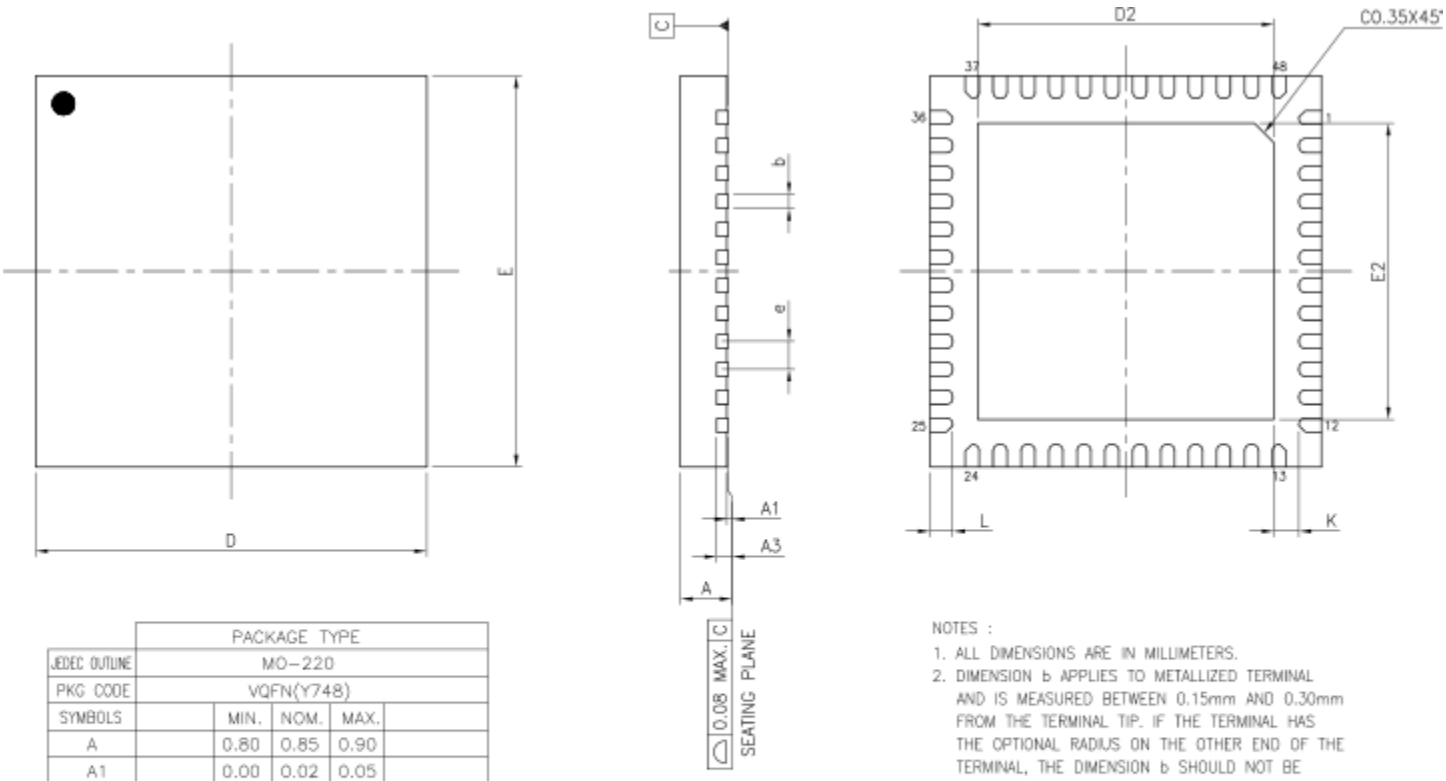
ACLK	Clock I	2	
OUT1 OUT3 OUT5 OUT7 AVCC_L VREF PNEG AVCC_R OUT8 OUT6 OUT4 OUT2 DVDD	Analog O	8 9 11 12 14 16 18 23 25 26 28 29 48	
GND_SNS_L GND_SNS_R	Analog I	10 27	

Table 35 – Internal Pad Circuitry

48 QFN Package Dimensions



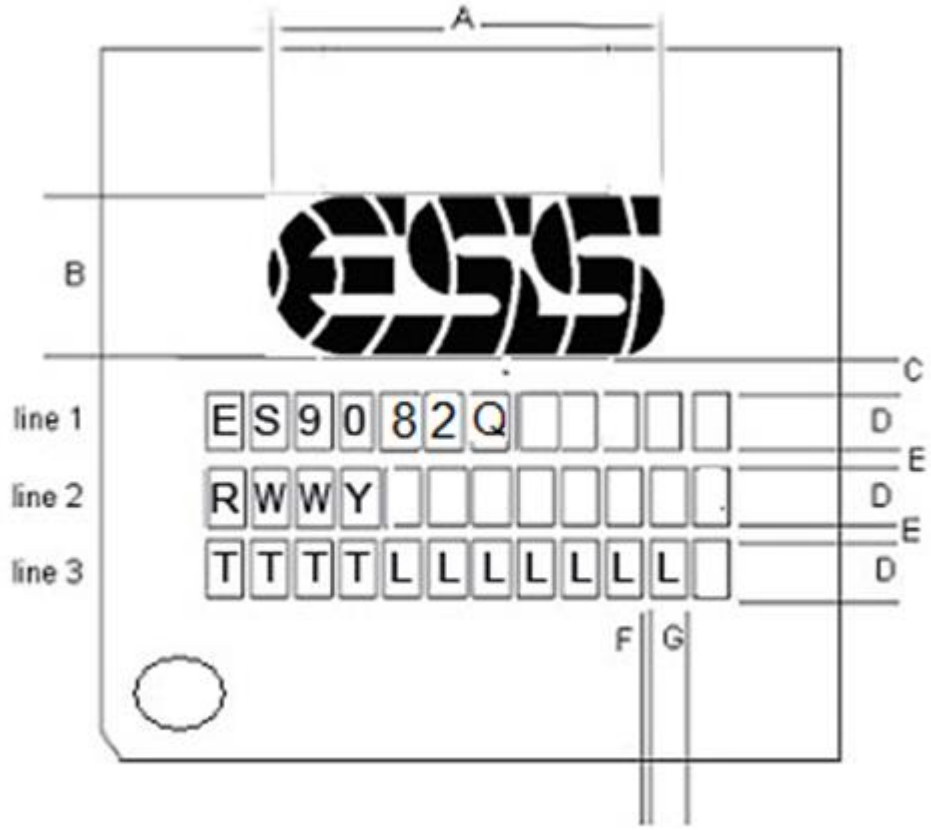
	PACKAGE TYPE				
JEDEC OUTLINE	MO-220				
PKG CODE	VQFN(Y748)				
SYMBOLS		MIN.	NOM.	MAX.	
A		0.80	0.85	0.90	
A1		0.00	0.02	0.05	
A3		0.203 REF.			
b		0.20	0.25	0.30	
D		7.00 BSC			
E		7.00 BSC			
e		0.50 BSC			
L		0.35	0.40	0.45	
K		0.20	–	–	

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
224X224 MIL	5.25	5.30	5.35	5.25	5.30	5.35	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 32 – ES9082 48 QFN Package Dimensions

48 QFN Top View Marking



	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 7mm x 7mm	5.0	2.0	0.3	0.56	0.2	0.08	0.33

T	Tracking number
W	Work week
Y	Last digit of year
L	Lot number
R	Silicon Revision

Marking is subject to change. This drawing is not to scale.

Figure 33 - ES9082 48 QFN Top View Markings

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (Table 37 - RPC-2 Pb Free Classification Temperature). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

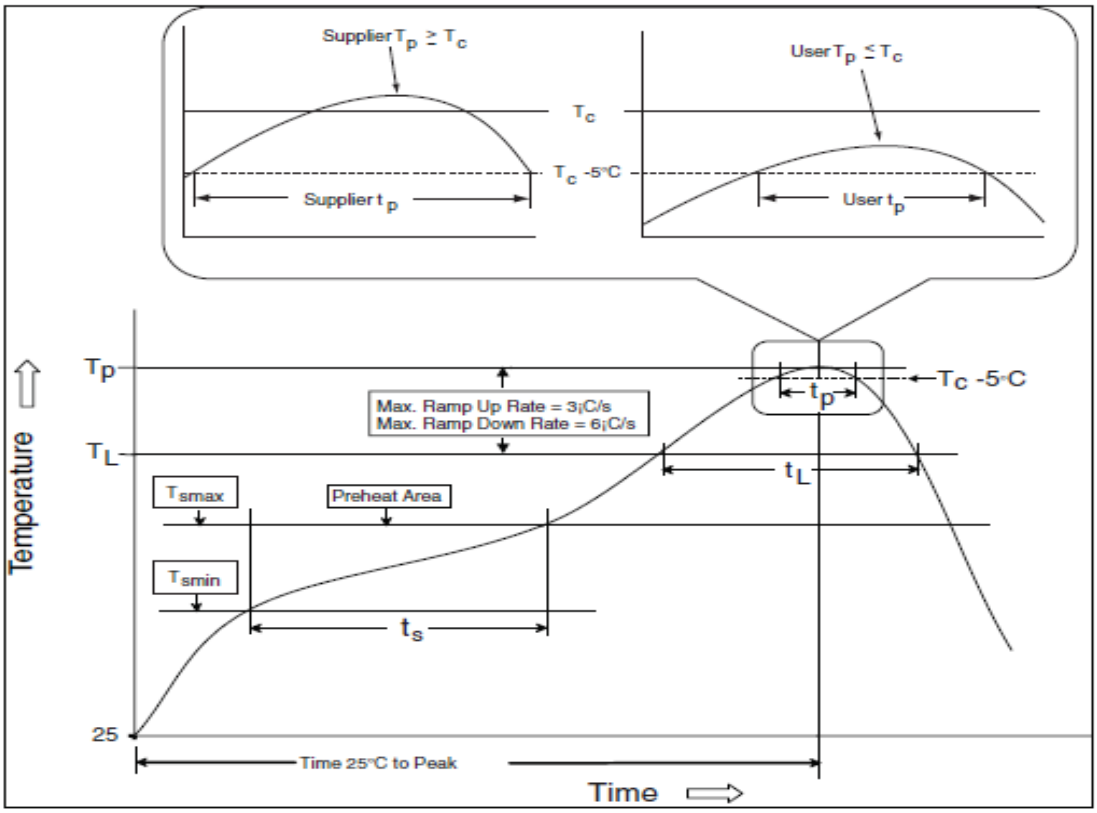


Figure 34 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 36 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2-Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 37 - RPC-2 Pb Free Classification Temperature

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9082Q	SABRE 32-bit 8 Channel SMART DAC with Line Driver & ASP2	7mm x 7mm 48 QFN

Table 38 - Ordering Information

Revision History

Current Version 0.2

Rev.	Date	Notes
0.2	September, 2024	Initial release