



Analog Reinvented

ES9020

## SABRE 2 Channel High Performance DAC Product Datasheet

The ESS SABRE® ES9020 is a 2 channel high performance audio digital-to-analog converter (DAC) that offers unsurpassed performance/cost for receivers, personal audio devices, professional audio applications such as recording systems, mixer consoles and digital audio workstations (DAW).

The ES9020 incorporates ESS' new patented Hyperstream® IV DAC Architecture and advanced SABRE HIFI® technology. It delivers incredible audio sound quality and specifications, including a True Dynamic Range (DNR) of +122dB and -110dB THD+N per channel.

The ES9020 SABRE® DAC improves on previous designs to include:

- Integrated analog low noise regulator to reduce BOM cost and design complexity.
- TDM audio format in addition to PCM, allowing for 4, 8, 16 or 32 channels per data line.
- SPI serial communication, as well as I<sup>2</sup>C are both supported in Software mode.
- Hardware modes for simple configuration of the DAC without a microcontroller.
- Integrated high-quality analog phase locked loop (APLL) to reduce BOM cost and design complexity.

The ES9020 is a synchronous DAC and can use the APLL to allow for simple configuration from the input bit clock or DSD clock. Daisy chain is supported to simplify routing when combining several chips in parallel.

| FEATURE                                                 | DESCRIPTION                                                                                           |
|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| Patented Hyperstream® IV Architecture DAC Technology    | Next-gen ESS SABRE® 2 Channel audio DAC                                                               |
| +122dB True DNR per channel<br>-110dB THD+N per channel | High dynamic range & low distortion                                                                   |
| High input sample rates                                 | Up to PCM 768kHz, DSD1024, DoP256 in 64*FS mode                                                       |
| Multiple input formats are available                    | I <sup>2</sup> S, LJ, TDM (including daisy chain), DSD, DoP                                           |
| Customizable filter characteristics                     | 8 pre-programmed digital filters as well as DC blocking and de-emphasis filters                       |
| Volume Control                                          | Volume set from +1dB to -126dB in 0.5dB steps<br>Additional gain with up to +42 dB gain in +6dB steps |
| Integrated Analog Phase Locked Loop (APLL)              | No loss in performance APLL reduces BOM requirements                                                  |
| Small standardized packaging                            | 5mm x 5mm, 28 pin QFN for reduced PCB board space                                                     |

## Applications

- Professional Audio
- Digital musical instruments
- PA/Broadcast applications
- Audiophile equipment
- Network streamers
- Powered Speakers

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## Functional Block Diagram

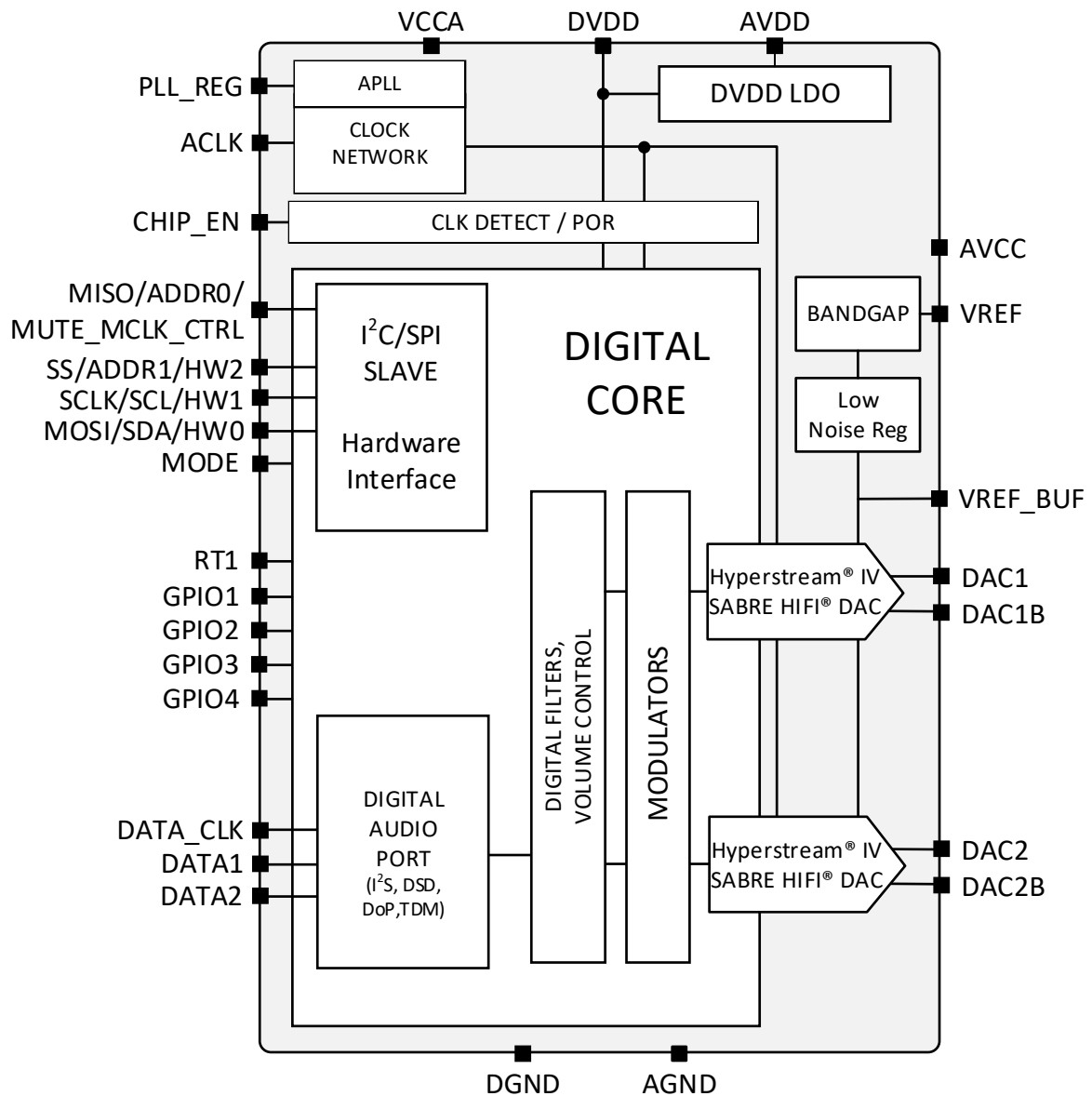
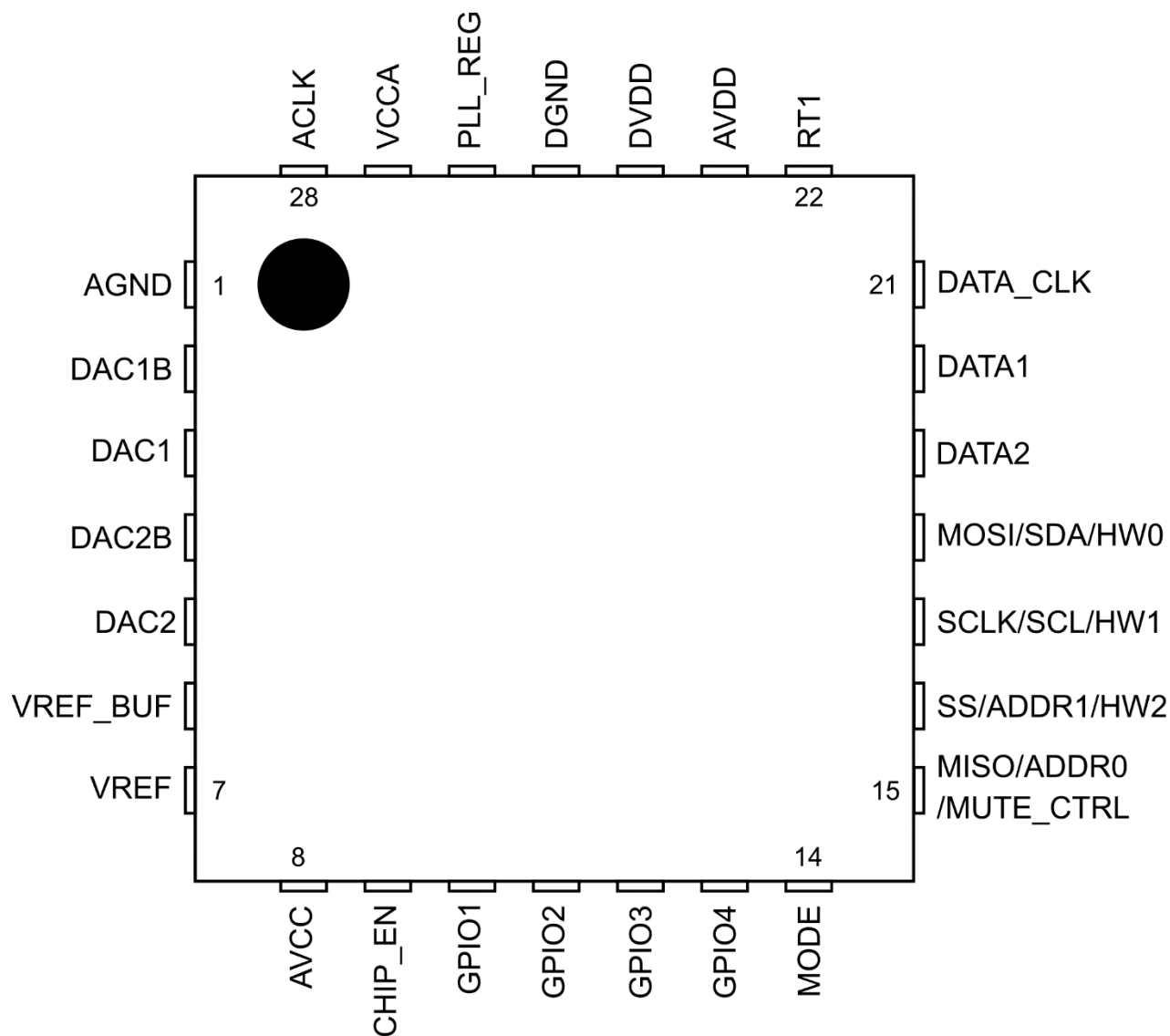


Figure 1 - ES9020 Block Diagram

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### ES9020 Pinout

#### 28 QFN Pinout



ES9020  
(Top View)

Figure 2 - 28 pin QFN Pinout

\*Note: ES9020 has an exposed pad (pin 29) that should be connected to ground.

## 28 QFN Pin Descriptions

| Pin | Name           | Pin Type | Reset State | Pin Description                                           |
|-----|----------------|----------|-------------|-----------------------------------------------------------|
| 1   | AGND           | Ground   | Ground      | DAC analog output stage ground                            |
| 2   | DAC1B          | A I/O    | Ground      | Differential Negative Output for Channel 1                |
| 3   | DAC1           | A I/O    | Ground      | Differential Positive Output for Channel 1                |
| 4   | DAC2B          | A I/O    | Ground      | Differential Negative Output for Channel 2                |
| 5   | DAC2           | A I/O    | Ground      | Differential Positive Output for Channel 2                |
| 6   | VREF_BUF       | A O      | P/D         | Analog Regulator Output, internally generated             |
| 7   | VREF           | A O      | P/D         | Voltage Reference Output, internally generated            |
| 8   | AVCC           | Power    | Power       | 3.3V DAC analog output stage reference supply             |
| 9   | CHIP_EN        | D I      | HiZ         | Active-high Chip Enable                                   |
| 10  | GPIO1          | D I/O    | HiZ         | General I/O w/extended functions                          |
| 11  | GPIO2          | D I/O    | HiZ         | General I/O w/extended functions                          |
| 12  | GPIO3          | D I/O    | HiZ         | General I/O w/extended functions                          |
| 13  | GPIO4          | D I/O    | HiZ         | General I/O w/extended functions                          |
| 14  | MODE           | D I/O    | HiZ         | I <sup>2</sup> C /SPI Control selection or HW mode        |
| 15  | MISO           | D I/O    | HiZ         | SPI Main In Sub Out pin, controlled by MODE               |
|     | ADDR0          |          |             | I <sup>2</sup> C Address 0 pin, controlled by MODE        |
|     | MUTE_MCLK_CTRL |          |             | Hardware Mute Control pin, controlled by MODE             |
| 16  | SS             | D I/O    | HiZ         | SPI Slave Select pin, controlled by MODE                  |
|     | ADDR1          |          |             | I <sup>2</sup> C Address 1 pin, controlled by MODE        |
|     | HW2            |          |             | Hardware 2 interface pin, controlled by MODE              |
| 17  | SCLK           | D I/O    | HiZ         | SPI Serial Clock pin, controlled by MODE                  |
|     | SCL            |          |             | I <sup>2</sup> C Serial Clock pin, controlled by MODE     |
|     | HW1            |          |             | Hardware 1 interface pin, controlled by MODE              |
| 18  | MOSI           | D I/O    | HiZ         | SPI Main Out Sub In pin, controlled by MODE               |
|     | SDA            |          |             | I <sup>2</sup> C Serial Data pin, controlled by MODE      |
|     | HW0            |          |             | Hardware 0 interface pin, controlled by MODE              |
| 19  | DATA2          | D I/O    | HiZ         | Serial DATA2 pin                                          |
| 20  | DATA1          | D I/O    | HiZ         | Serial DATA1 pin                                          |
| 21  | DATA_CLK       | D I/O    | HiZ         | Serial Data Clock pin                                     |
| 22  | RT1            | D I/O    | HiZ         | Reserved. Must be connected to DGND for normal operation. |
| 23  | AVDD           | Power    | Power       | 3.3V I/O Supply                                           |
| 24  | DVDD           | A O      | P/D         | 1.2V Supply for Digital Core, internally generated        |
| 25  | DGND           | Ground   | Ground      | Digital Core Ground                                       |
| 26  | PLL_REG        | A O      | P/D         | Low Noise Supply for PLL, internally generated            |
| 27  | VCCA           | Power    | Power       | Analog Supply, 3.3V                                       |
| 28  | ACLK           | Clock I  | HiZ         | Clock Input                                               |
| 29  | External PAD   | -        | -           | External Pad, connect to GND                              |

\* Note: A I/O = Analog Input/Output, D I/O = Digital Input/Output

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### Configuration Modes

The ES9020 supports 2 different software modes (SPI or I<sup>2</sup>C) and supports 2 different sets of hardware modes (PCM or TDM/DSD). These modes are controlled by the state of the MODE Pin (Pin 14).

| MODE PIN | Configuration | Description                |
|----------|---------------|----------------------------|
| 1        | Software Mode | SPI interface              |
| Pull 1   | Hardware Mode | TDM, DSD Modes             |
| Pull 0   | Hardware Mode | PCM Slave or Master Modes  |
| 0        | Software Mode | I <sup>2</sup> C interface |

Table 1 - Mode Pin Configuration Options

### Design Information

Hardware pins can be configured four different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. This also applies to MUTE\_CTRL.

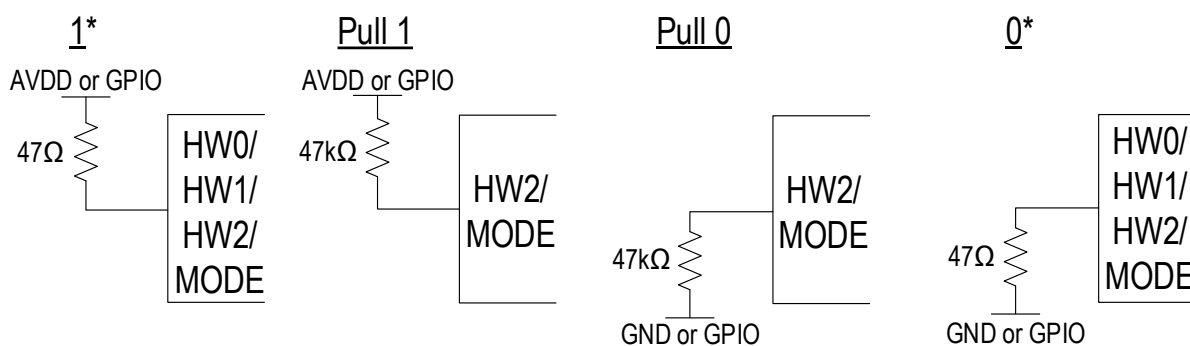


Figure 3 - Hardware Mode Pin Configurations

\* Note: Hardware mode pin states 0 and 1 can be directly connected to GND or AVDD.

## Software Mode

The ES9020 support I<sup>2</sup>C or SPI serial communication. The ES9020 have read/write register and read-only register. Software modes are set with the MODE pin (Pin 14)

### I<sup>2</sup>C Slave Interface Commands

The I<sup>2</sup>C slave interface is enabled when the MODE pin (Pin 14) is tied low (MODE=0). In I<sup>2</sup>C mode, ADDR1 (Pin 16) and ADDR0 (Pin 15) determine the I<sup>2</sup>C address and the R/W bit controls reading or writing.

For I<sup>2</sup>C Timing information, see I<sup>2</sup>C Slave Interface Timing.

The I<sup>2</sup>C Slave Interface can be accessed by:

- Pin 18 SDA
- Pin 17 SCL
- Pin 16 ADDR1
- Pin 15 ADDR0

I<sup>2</sup>C Slave Address = [5'b10010, ADDR1, ADDR0, R/W]

| I <sup>2</sup> C Slave Address | ADDR1 | ADDR0 |
|--------------------------------|-------|-------|
| 0x90                           | 0     | 0     |
| 0x92                           | 0     | 1     |
| 0x94                           | 1     | 0     |
| 0x96                           | 1     | 1     |

Table 2 - I<sup>2</sup>C Slave Addresses

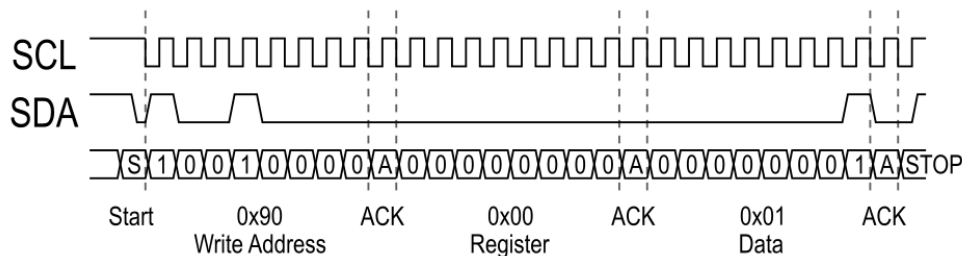


Figure 4 - I<sup>2</sup>C Write Example

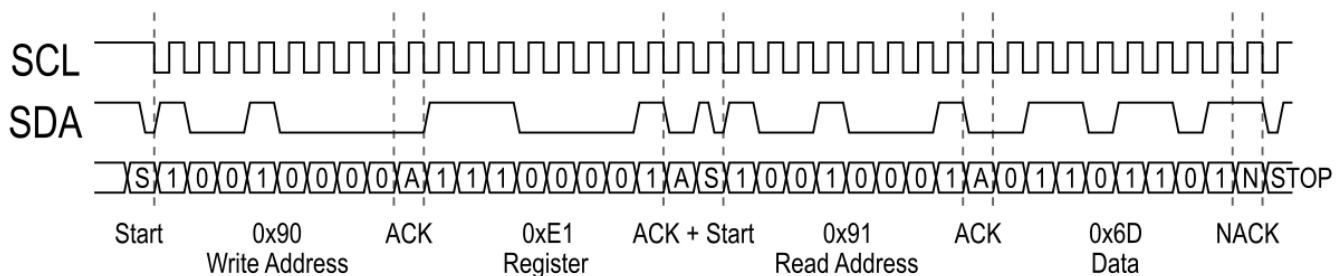


Figure 5 - I<sup>2</sup>C Read Example

Note: CHIP\_ID is 0x6D in Register 225 (0xE1)

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### SPI Slave Interface Commands

The SPI slave interface is used when the MODE pin (Pin 14) is pulled high.

The SPI slave interface can be accessed using Pins 15, 16, 17, and 18.

- Pin 18 MOSI
- Pin 17 SCLK
- Pin 16 SS
- Pin 15 MISO

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data.

SPI Commands:

- 0x01: Read
- 0x03: Write

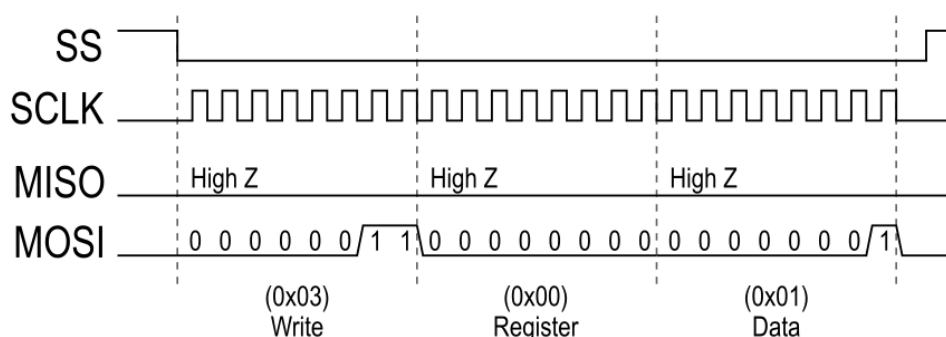


Figure 6 - SPI Single Byte Write

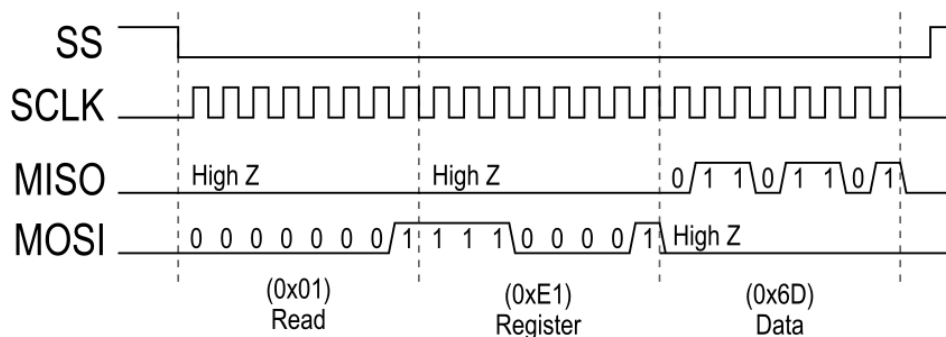


Figure 7 - SPI Single Byte Read

Note: CHIP\_ID is 0x6D in Register 225 (0xE1)

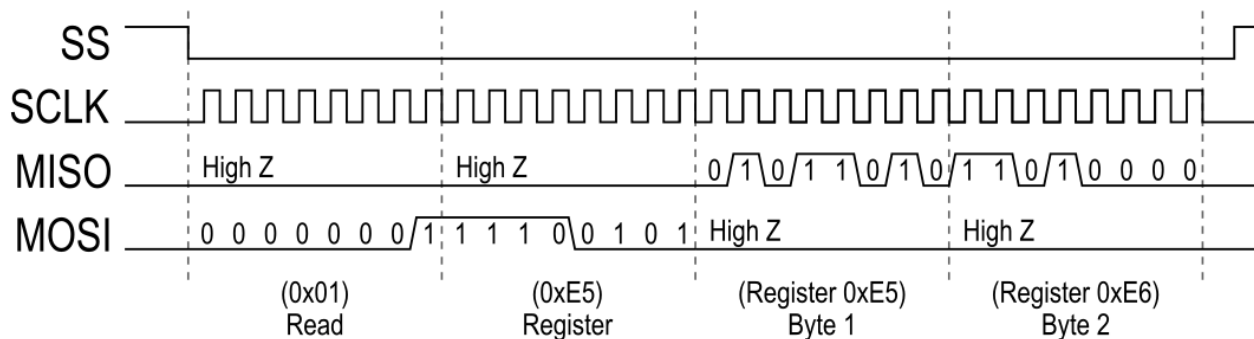


Figure 8 - SPI Multibyte Read

## Hardware Mode

The ES9020 has pre-configured modes that can be set with external pin configuration. These modes configure the DAC for different input/output serial data rates and set the muting. Hardware modes also support stereo digital PDM microphones as inputs. Each hardware mode pin has 4 states that can be found in Design Information.

These modes are set with pins:

- MODE (Pin 14)
- HW0 (Pin 18)
- HW1 (Pin 17)
- HW2 (Pin 16)
- MUTE\_CTRL (Pin 15)

### Recommended Hardware Mode Setup Sequence

The Hardware Mode setup sequence is shown below with all hardware pins being defined after CHIP\_EN is asserted.

Note: It is recommended that MUTE\_CTRL is set low until the HW mode is finalized and after CHIP\_EN is asserted, then asserted last.

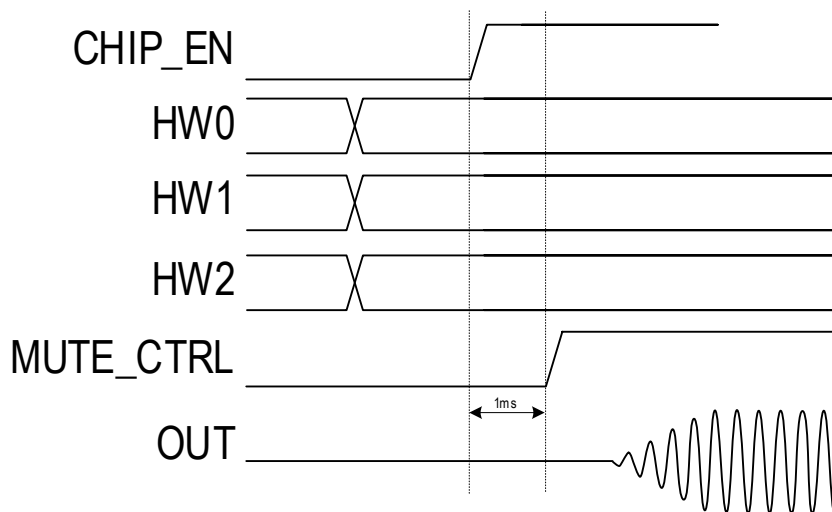


Figure 9 - Hardware Mode Startup Sequence

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### Hardware Mode Pin Configurations

| HW Mode                                               | Mode Description                              | MCLK Source               | PCM FS [kHz] | DoP Rate    | DSD Rate        | PDM Clock [MHz]  | BCK <sup>1</sup> [MHz] | MODE   | HW2    | HW1 | HW0 |
|-------------------------------------------------------|-----------------------------------------------|---------------------------|--------------|-------------|-----------------|------------------|------------------------|--------|--------|-----|-----|
| 32-bit PCM/DoP/DSD/PCM Master Modes (Ext MCLK)        |                                               |                           |              |             |                 |                  |                        |        |        |     |     |
| 0                                                     | I <sup>2</sup> S / DoP / DSD / PDM            | Ext. MCLK                 | MCLK/128     | DoP64 - 256 | DSD512/1024     | PDM24/49         | MCLK/2 (64*FS)         | Pull 0 | 0      | 0   | 0   |
| 1                                                     |                                               |                           | MCLK/256     | DoP64 - 128 | DSD256/512      | PDM12/24         | MCLK/4 (64*FS)         | Pull 0 | 0      | 0   | 1   |
| 2                                                     |                                               |                           | MCLK/512     | DoP64       | DSD128/256      | PDM6/12          | MCLK/8 (64*FS)         | Pull 0 | 0      | 1   | 0   |
| 3                                                     | I <sup>2</sup> S / DSD / PDM                  |                           | MCLK/1024    | -           | DSD64/128       | PDM3/6           | MCLK/16 (64*FS)        | Pull 0 | 0      | 1   | 1   |
| 4                                                     | LJ / DoP / DSD / PDM                          |                           | MCLK/128     | DoP64 - 256 | DSD512/1024     | PDM24/49         | MCLK/2 (64*FS)         | Pull 0 | Pull 0 | 0   | 0   |
| 5                                                     |                                               |                           | MCLK/256     | DoP64 - 128 | DSD256/512      | PDM12/24         | MCLK/4 (64*FS)         | Pull 0 | Pull 0 | 0   | 1   |
| 6                                                     |                                               |                           | MCLK/512     | DoP64       | DSD128/256      | PDM6/12          | MCLK/8 (64*FS)         | Pull 0 | Pull 0 | 1   | 0   |
| 7                                                     | LJ / DSD / PDM                                |                           | MCLK/1024    | -           | DSD64/128       | PDM3/6           | MCLK/16 (64*FS)        | Pull 0 | Pull 0 | 1   | 1   |
| 32-bit PCM/DoP/DSD/PCM Slave Modes (PLL and Ext MCLK) |                                               |                           |              |             |                 |                  |                        |        |        |     |     |
| 8                                                     | I <sup>2</sup> S / DoP / DSD / PDM<br>Auto FS | Ext. MCLK                 | 8 ≤ FS ≤ 768 | DoP64 - 256 | DSD64 - DSD1024 | 0.375 ≤ PDM ≤ 49 | 64*FS                  | Pull 0 | Pull 1 | 0   | 0   |
| 9                                                     | I <sup>2</sup> S / DSD / PDM                  | PLL from BCK <sup>2</sup> | 48           | -           | DSD64           | PDM3             | 3.072                  | Pull 0 | Pull 1 | 0   | 1   |
| 10                                                    |                                               |                           | 96           | -           | DSD128          | PDM6             | 6.144                  | Pull 0 | Pull 1 | 1   | 0   |
| 11                                                    | I <sup>2</sup> S / DoP / DSD / PDM            | BCK <sup>2</sup>          | 192          | DoP64       | DSD256          | PDM12            | 12.288                 | Pull 0 | Pull 1 | 1   | 1   |
| 12                                                    | LJ / DoP / DSD / PDM<br>Auto FS               | Ext. MCLK                 | 8 ≤ FS ≤ 768 | DoP64 - 256 | DSD64 - DSD1024 | 0.375 ≤ PDM ≤ 49 | 64*FS                  | Pull 0 | 1      | 0   | 0   |
| 13                                                    | LJ / DSD / PDM                                | PLL from BCK <sup>2</sup> | 48           | -           | DSD64           | PDM3             | 3.072                  | Pull 0 | 1      | 0   | 1   |
| 14                                                    |                                               |                           | 96           | -           | DSD128          | PDM6             | 6.144                  | Pull 0 | 1      | 1   | 0   |
| 15                                                    | LJ / DoP / DSD / PDM                          | BCK <sup>2</sup>          | 192          | DoP64       | DSD256          | PDM12            | 12.288                 | Pull 0 | 1      | 1   | 1   |

Table 3 - Hardware Pin Configurations, Modes 0-15

See table continuation on next page.

<sup>1</sup> For master mode DoP, DSD, and PDM, the BCKs frequency is doubled.<sup>2</sup> Ensure MUTE\_CTRL pin (Pin 15) is set to Pull 0 or Pull 1.

**Hardware Pin Configurations (Continued)**

| HW Mode                                           | Mode Description                        | MCLK Source | TDM Mode <sup>1</sup>                 | PCM FS [kHz] | BCK [MHz]             | TDM Channels | TDM Slots | MODE   | HW2    | HW1 | HW0 |
|---------------------------------------------------|-----------------------------------------|-------------|---------------------------------------|--------------|-----------------------|--------------|-----------|--------|--------|-----|-----|
| 32-bit TDM LJ Slave Modes, Autodetect FS & CH Num |                                         |             |                                       |              |                       |              |           |        |        |     |     |
| 16                                                | 32-Bit TDM LJ Slave Auto FS Auto CH num | Ext. MCLK   | Parallel and Daisy Chain <sup>1</sup> | 8 ≤ FS ≤ 768 | Auto (64FS - 1024FS)  | 2 ≤ CH ≤ 32  | 1, 2      | Pull 1 | 0      | 0   | 0   |
| 17                                                |                                         |             |                                       | 8 ≤ FS ≤ 384 | Auto (128FS - 1024FS) | 4 ≤ CH ≤ 32  | 3, 4      | Pull 1 | 0      | 0   | 1   |
| 18                                                |                                         |             |                                       | 8 ≤ FS ≤ 192 | Auto (256FS - 1024FS) | 8 ≤ CH ≤ 32  | 5, 6      | Pull 1 | 0      | 1   | 0   |
| 19                                                |                                         |             |                                       | 8 ≤ FS ≤ 192 | Auto (256FS - 1024FS) | 8 ≤ CH ≤ 32  | 7, 8      | Pull 1 | 0      | 1   | 1   |
| 20                                                |                                         |             |                                       | 8 ≤ FS ≤ 96  | Auto (512FS, 1024FS)  | 16 ≤ CH ≤ 32 | 9, 10     | Pull 1 | Pull 0 | 0   | 0   |
| 21                                                |                                         |             |                                       | 8 ≤ FS ≤ 96  | Auto (512FS, 1024FS)  | 16 ≤ CH ≤ 32 | 11, 12    | Pull 1 | Pull 0 | 0   | 1   |
| 22                                                |                                         |             |                                       | 8 ≤ FS ≤ 96  | Auto (512FS, 1024FS)  | 16 ≤ CH ≤ 32 | 13, 14    | Pull 1 | Pull 0 | 1   | 0   |
| 23                                                |                                         |             |                                       | 8 ≤ FS ≤ 96  | Auto (512FS, 1024FS)  | 16 ≤ CH ≤ 32 | 15, 16    | Pull 1 | Pull 0 | 1   | 1   |
| 16-bit TDM LJ Slave Modes, Autodetect FS & CH Num |                                         |             |                                       |              |                       |              |           |        |        |     |     |
| 24                                                | 16-Bit TDM LJ Slave Auto FS Auto CH num | Ext. MCLK   | Parallel and Daisy Chain <sup>1</sup> | 8 ≤ FS ≤ 768 | Auto (64FS - 512FS)   | 2 ≤ CH ≤ 32  | 1, 2      | Pull 1 | Pull 1 | 0   | 0   |
| 25                                                |                                         |             |                                       | 8 ≤ FS ≤ 384 | Auto (128FS - 512FS)  | 4 ≤ CH ≤ 32  | 3, 4      | Pull 1 | Pull 1 | 0   | 1   |
| 26                                                |                                         |             |                                       | 8 ≤ FS ≤ 192 | Auto (256FS - 512FS)  | 8 ≤ CH ≤ 32  | 5, 6      | Pull 1 | Pull 1 | 1   | 0   |
| 27                                                |                                         |             |                                       | 8 ≤ FS ≤ 192 | Auto (256FS - 512FS)  | 8 ≤ CH ≤ 32  | 7, 8      | Pull 1 | Pull 1 | 1   | 1   |
| 28                                                |                                         |             |                                       | 8 ≤ FS ≤ 96  | Auto (512FS)          | 16 ≤ CH ≤ 32 | 9, 10     | Pull 1 | 1      | 0   | 0   |
| 29                                                |                                         |             |                                       | 8 ≤ FS ≤ 96  | Auto (512FS)          | 16 ≤ CH ≤ 32 | 11, 12    | Pull 1 | 1      | 0   | 1   |
| 30                                                |                                         |             |                                       | 8 ≤ FS ≤ 96  | Auto (512FS)          | 16 ≤ CH ≤ 32 | 13, 14    | Pull 1 | 1      | 1   | 0   |
| 31                                                |                                         |             |                                       | 8 ≤ FS ≤ 96  | Auto (512FS)          | 16 ≤ CH ≤ 32 | 15, 16    | Pull 1 | 1      | 1   | 1   |

Table 4 - Hardware Pin Configurations, Modes 16-31

<sup>1</sup> TDM Mode is selected via GPIO2

## ES9020 Product Datasheet

### GPIO Functions in Hardware Mode

The ES9020 supports specific functions through the GPIO pins in hardware modes. The tables below show the available controls in hardware modes. These include DAC Input Select, Automute, and the ability to choose between two different filters in various input modes. These functions are supported in hardware modes.

| Input Format        | Supported HW Modes  | GPIO3   | GPIO2 | Input/Output |
|---------------------|---------------------|---------|-------|--------------|
| I <sup>2</sup> S/LJ | 0 - 15              | 1'b0    | 1'b0  | Input        |
| DSD                 |                     | 1'b1    | 1'b0  | Input        |
| PDM                 |                     | 1'b0    | 1'b1  | Input        |
| DoP                 | 0-2, 4-6, 8, 12, 15 | 1'b1    | 1'b1  | Input        |
| TDM (Parallel)      | 16 - 31             | -       | 1'b0  | Input        |
| TDM (Daisy Chain)   |                     | TSD Pin | 1'b1  | Input/Output |

Table 5 - DAC Input Select with GPIO3 & GPIO2 in Hardware Mode

| GPIO4 | Input Format             | Filter                                 |
|-------|--------------------------|----------------------------------------|
| 1'b0  | I <sup>2</sup> S/LJ, TDM | Filter 0<br>Minimum Phase              |
| 1'b1  |                          | Filter 2<br>Linear Phase Fast Roll-Off |

Table 6 - DAC Filter Select with GPIO4 in Hardware Mode

| GPIO1 | Automute |
|-------|----------|
| 1'b0  | Disabled |
| 1'b1  | Enabled  |

Table 7 - DAC Automute with GPIO1 in Hardware Mode

### Mute Control

Set MUTE\_CTRL (Pin 15) to mute the output while in Hardware Mode:

| HW MUTE Control (Pin 15) | Mute Condition | Automute Condition |
|--------------------------|----------------|--------------------|
| 0                        | Mute           | Automute Off       |
| 1                        | Unmute         | Automute Off       |
| Pull 0                   | Mute           | Automute On        |
| Pull 1                   | Unmute         | Automute On        |

Table 8 - Mute Control in Hardware Mode

Note: If using the PLL from BCK Hardware Modes (9-11, 13-15), MUTE\_CTRL must be set to Pull 0 or Pull 1.

## Digital Features

### Audio Input Formats

The ES9020 input format is selected either through Hardware Mode or Software Mode.

The ES9020 can automatically determine the input data format (PCM, DSD and DoP Only) by enabling Register 1[0] `AUTO_INPUT_SEL`, data must be provided on the DATA2 pin to properly decode the input format. The input data format can also be selected using Register 1[2:1] `INPUT_SEL`.

The formats include:

- **PCM/TDM** Register 1[2:1] = 2'd0
  - Slave and master mode in 16, 24, 32 - bit widths
  - I<sup>2</sup>S, Left Justified (LJ) refer to 2 channels per frame.
  - Sample rates up to 768kHz (64fs mode) for PCM
  - TDM supports up to 32 channels/slots per frame with auto channel number detect
  - TDM supported in parallel or daisy chain mode
  - TDM LJ in hardware mode, or TDM I<sup>2</sup>S and TDM LJ in software mode
  - Channel remapping through `TDM_SLOT_SEL_CHx` & invert
- **DSD/PDM** Register 1[2:1] = 2'd1
  - Set through `ENABLE_PDM_DECODER` and/or `ENABLE_DSD_DECODER`
  - PDM allows for double data rate, 2 channels per data line and remapping using `PDM_PHASE`
  - DSD uses a single channel per data line
  - Slave or master mode
  - Sample rates from DSD64 (2.8224Mbits/s) to DSD1024
  - Channel mapping through `DSD_LINE_SEL_CHx` & invert
- **DoP (DSD Over PCM)** Register 1[2:1] = 2'd2
  - Slave and master mode
  - Sample rates from DoP256 (24bit, 705.5kHz PCM)
  - Channel mapping & invert

## ES9020 Product Datasheet

### PCM (I<sup>2</sup>S, LJ)

For Pulse Code Modulation (PCM), data is organized into 2 channels per frame on a single data line for I<sup>2</sup>S or Left Justified (LJ) formats. Data is latched on the positive edge of BCLK.

PCM Pin Connections:

| Pin Name | Function | Description                                        |
|----------|----------|----------------------------------------------------|
| DATA_CLK | PCM BCLK | PCM Clock (Bit Clock), Master or Slave             |
| DATA1    | PCM WS   | PCM WS (Word Select/Frame Select), Master or Slave |
| DATA2    | PCM DATA | PCM Data Channel 1 & 2                             |

Table 9 - PCM Pin Connections

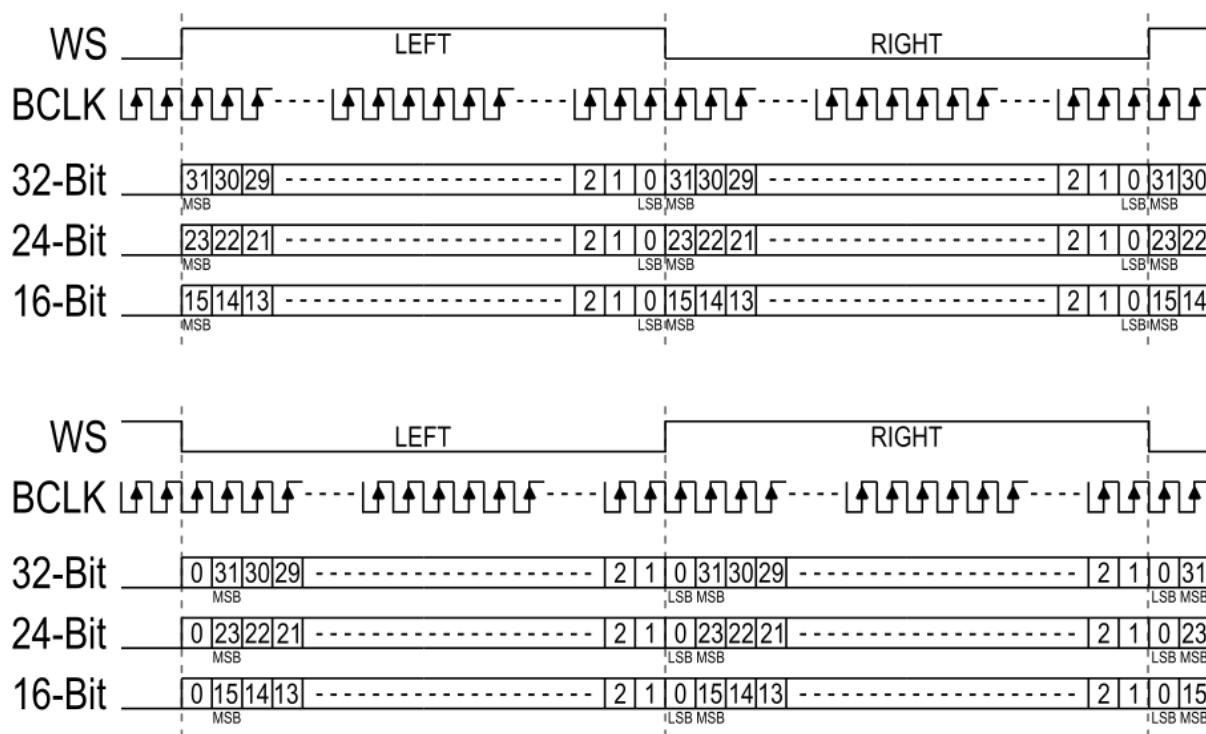


Figure 10 - LJ (top) & I<sup>2</sup>S (bottom) for 16, 24, and 32-bit Word Widths

**Note:** Right Justified is only supported in software mode

## TDM

The ES9020 supports Time Division Multiplexing (TDM) format, allowing 4 to 32 channels per frame on a single data line. TDM is supported in both software and hardware modes. Data is latched on the positive edge of BCLK.

In hardware mode, each TDM mode have their own TDM slot mapping. For example, in the case of TDM16 (16CH), the hardware mode will be configured so that slots 1 and 2 will map to one device (HW mode #16), slots 3 and 4 will map to a second device (HW mode #17), up to slots 15 and 16 mapping to an 8<sup>th</sup> device respectively.

In software mode, Registers 8-9[4:0] TDM\_SLOT\_SEL\_CHx can be set to internally map any slot to either DAC channel.

### TDM Pin Connection

| Pin Name | Function | Description                                        |
|----------|----------|----------------------------------------------------|
| DATA_CLK | TDM BCLK | TDM Clock, Master, or Slave                        |
| DATA1    | TDM WS   | TDM WS (Word Select/Frame Select), Master or Slave |
| DATA2    | TDM DATA | TDM DATA Channel 1 & 2 (default)                   |

Table 10 - TDM Pin Connections

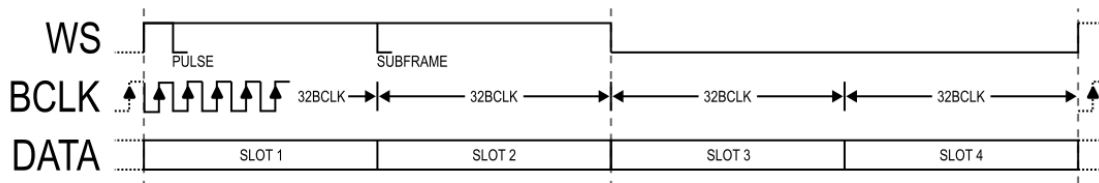


Figure 11 - TDM4 Mode

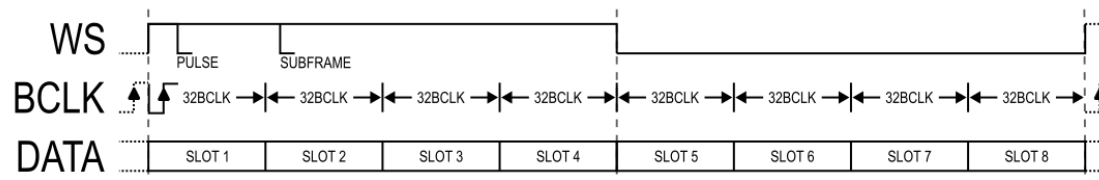


Figure 12 - TDM8 Mode

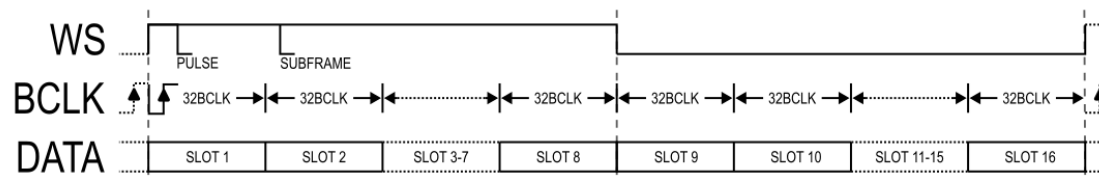


Figure 13 - TDM16 Mode

## ES9020 Product Datasheet

### DSD

In DSD mode, there is a single DSD clock line, and each channel of data is an additional DSD data line.

In hardware mode for DSD, input DSD data on DATA1 goes to CH1 and input on DATA2 goes to CH2.

In software mode, DSD data can be mapped through DSD\_LINE\_SEL\_CHx,

DSD Pin Connections (default configuration):

| Pin Name | Function | Description        |
|----------|----------|--------------------|
| DATA_CLK | DSD CLK  | DSD Clock          |
| DATA1    | DSD CH1  | DSD Data Channel 1 |
| DATA2    | DSD CH2  | DSD Data Channel 2 |

Table 11 - DSD Pin Connections

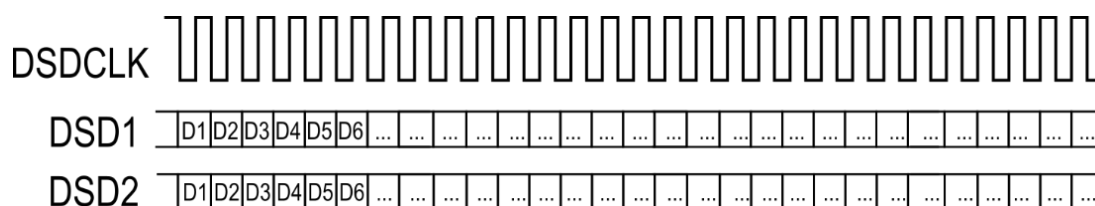


Figure 14 - DSD Format, 1-bit stream

### PDM

In PDM mode, there is a PDM clock line and a single PDM data line containing data on both edges of the PDM clock.

In Hardware mode, Channel 1 is sampled on the rising edge and Channel 2 is sampled on the falling edge of PDM clock.

In Software mode, the channel mapping can be swapped by setting Register 19[7] PDM\_PHASE. The channels can also be remapped using Register 8,9[5] DSD\_LINE\_SEL\_CHx.

See PDM Decoder for more information.

| Pin Name | Function  | Description            |
|----------|-----------|------------------------|
| DATA_CLK | PDM CLK   | PDM Clock              |
| DATA1    | PDM DATA1 | PDM Data Channel 1 & 2 |

Table 12 - PDM Pin Connections

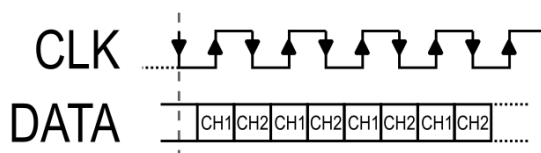


Figure 15 - PDM Dual Channel Format

Note: If a one sample phase shift is present between channels, invert PDM\_SAMPLE\_EDGE to resolve the shift.

Note: ENABLE\_DSD\_DECODE must also be set when using the PDM Decoder.

## DoP (DSD Over PCM)

DoP Encodes 16 bits of DSD data into a 24-bit PCM frame, with the 8 most significant bits containing the DSD marker. The marker alternates between 0x05 and 0xFA every sample. The DSD data is inserted into the frame such that the oldest bit is in the  $t_0$  position.

The PCM/TDM Decoder must be enabled and set up for a 24- or 32-bit word width and bit depth when using the DoP Decoder. I<sup>2</sup>S and LJ are supported for the PCM format. When using a 32-bit word width the 8 LSBs are dropped when decoding.

| Pin Name | Function  | Description                                        |
|----------|-----------|----------------------------------------------------|
| DATA_CLK | DoP BCLK  | DoP Clock (Bit Clock), Master or Slave             |
| DATA1    | DoP WS    | DoP WS (Word Select/Frame Select), Master or Slave |
| DATA2    | DoP DATA1 | DoP Data Channel 1 & 2 (default)                   |

Table 13 - DoP Pin Connections

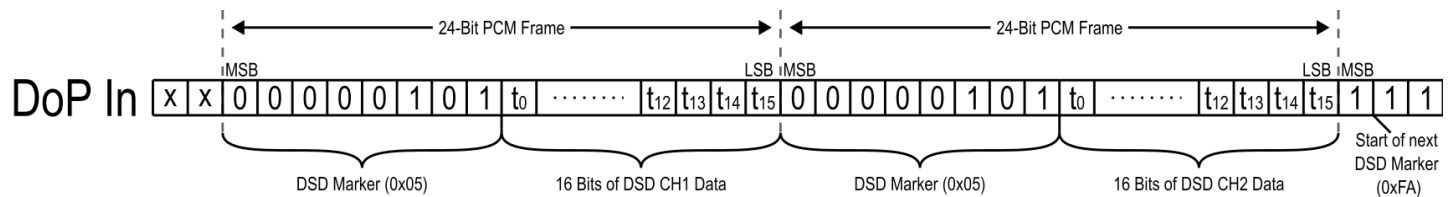


Figure 16 - DoP Format

## ES9020 Product Datasheet

### Digital Signal Path

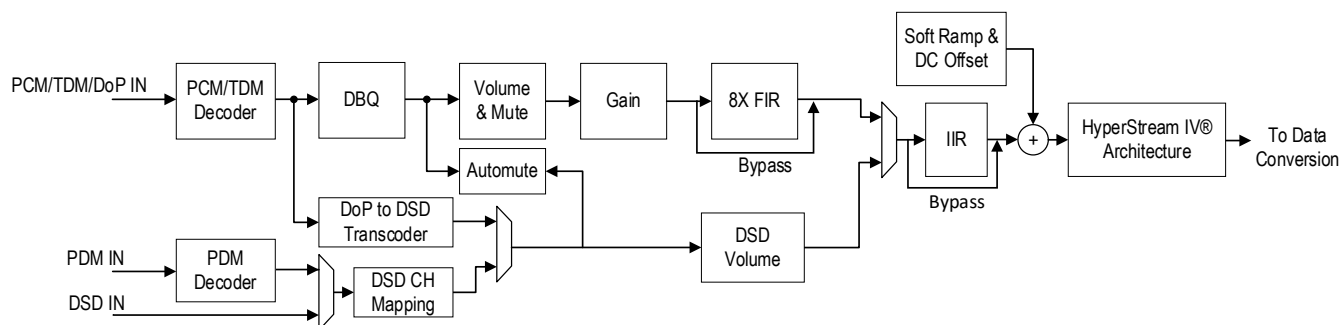


Figure 17 - Digital Signal Path

### PCM/TDM Decoder

The ES9020 integrates a PCM/TDM decoder. The input has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The decoder allows for I<sup>2</sup>S, LJ, RJ and TDM input streams.

The PCM/TDM decoder can support up to 32 different slots and each channel of the DAC can be mapped to any of the 32 slots.

#### PCM/TDM Decoder Registers

- Register 6[7] TDM\_RESYNC
- Register 6[6] AUTO\_CH\_DETECT
- Register 6[4:0] TDM\_CH\_NUM
- Register 7[7] ENABLE\_WS\_MONITOR
- Register 7[6] ENABLE\_BCK\_MONITOR
- Register 7[5:4] TDM\_WORD\_WIDTH
- Register 7[3:2] TDM\_BIT\_DEPTH
- Register 7[1] TDM\_VALID\_EDGE
- Register 7[0] TDM\_LJ

#### TDM Mapping Registers

- Register 8-9[4:0] TDM\_SLOT\_SEL\_CHx

#### Daisy Chain Registers

- Register 10[7] TDM\_DAISY\_CHAIN
- Register 10[4:0] TDM\_DATA\_LATCH\_ADJ

**PDM Decoder**

The ES9020 can receive input audio from a PDM microphone using the integrated PDM Decoder. To use the PDM signal in software mode, INPUT\_SEL must be set to 2'd1 (DSD) and ENABLE\_DPM\_DECODE must be set to 1'b1. PDM is also supported in hardware modes. The PDM Data is input into DATA1 and PDM Clock is output through DATA\_CLK.

PDM Decoder Register

- Register 1[7] ENABLE\_PDM\_DECODE
- Register 8[7] PDM\_SAMPLE\_EDGE
- Register 8[8] PDM\_PHASE
- Register 9[7] PDM\_2X\_GAIN\_EN

Note: Register 1[7] ENABLE\_PDM\_DECODE must be set to 1'b0 to use DSD

**DSD Channel Mapping**

The ES9020 features the ability to remap DSD channel sources using registers. This includes the incoming signal from the PDM decoder. Either channel can be mapped to either channel.

DSD Channel Mapping Registers

- Register 8-9[5] DSD\_LINE\_SEL\_CHx

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### DBQ

The ES9020 features a Digital Full Biquad (DBQ) filter for the DAC datapath for TDM or PCM input modes. The filter comes with 16 preset filters and the ability to make a custom filter via user input coefficients.

The custom filter uses 5 signed 24-bit coefficients to shape the filter:  $-A2$ ,  $-A1$ ,  $B2$ ,  $B1$ , and  $B0$ .

#### DBQ Filter Registers

- Register 51[4:0] DBQ\_COEFF\_SEL (preset filter selection)
- Register 52-54 PROG DBQ A2 COEFF
- Register 55-57 PROG DBQ A1 COEFF
- Register 58-60 PROG DBQ B2 COEFF
- Register 61-63 PROG DBQ B1 COEFF
- Register 64-66 PROG DBQ B0 COEFF

The DBQ is arranged in a transposed direct form 2 format.

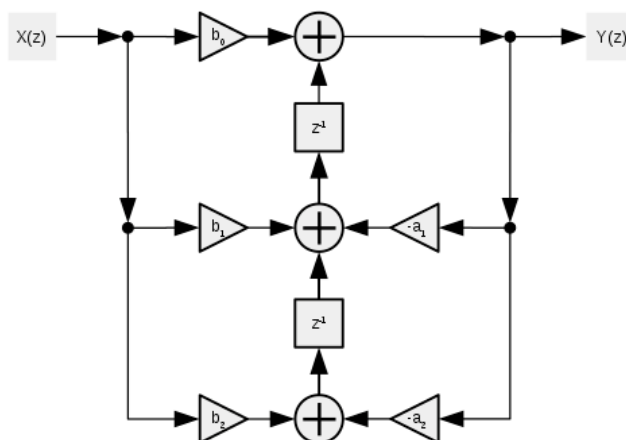


Figure 18 - DBQ format

Note: The ES9020 Digital Full Biquad is only supported for TDM or PCM input modes.

## Volume Control & Mute

The Volume Control and Mute is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

The ES9020 also features the ability to manually mute specific channels, invert the volume control phase as well as control both channel volumes with the CH1 volume control.

### Volume Control Registers

- Register 31-32 VOLUME\_CHx
- Register 33[3:2] MUTE\_CHx
- Register 33[1:0] VOL\_PHASE\_INV\_CHx
- Register 34[7] MONO\_VOLUME
- Register 35 VOL\_RAMP\_RATE\_UP
- Register 36 VOL\_RAMP\_RATE\_DOWN

## Automute

The ES9020 features an automute that triggers when the signal is below the specified level for longer than the specified time. The automute will disengage when the signal is above the specified off value for the same amount of time.

Note: Automute in DSD mode has additional registers that require configuration.

$$Time[s] = \frac{2^{25}}{AUTOMUTE\_TIME * MCLK\_128FS * 2^{64FS\_MODE}}$$

$$Level[dB] = \frac{20 * \log_{10}(AUTOMUTE\_LEVEL)}{(2^{16} - 1) * 2^7}$$

$$Level_{OFF}[dB] = \frac{20 * \log_{10}(AUTOMUTE\_OFF\_LEVEL)}{(2^{16} - 1) * 2^7}$$

### Automute Registers

- Register 38[1:0] AUTOMUTE\_EN\_CHx
- Register 39-40 [10:0] AUTOMUTE\_TIME
- Register 41-42 AUTOMUTE\_LEVEL
- Register 43-44 AUTOMUTE\_OFF\_LEVEL

### DSD Automute Settings Registers

- Register 39-40[15] DSD\_FAULT\_DETECT\_EN
- Register 39-40[14] DSD\_DC\_AM\_ENB
- Register 39-40[13] DSD\_MUTE\_AM\_ENB

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### Digital Gain

The ES9020 has an additional digital gain that can be added through registers. Settings for +0dB to +42dB in 6dB steps are available.

#### Gain Registers

- Register [6:4] DIGITAL\_GAIN\_CH1
- Register [2:0] DIGITAL\_GAIN\_CH2

### 8x FIR Filter

Selection of the 8x interpolation filter is chosen from 8 pre-programmed filters. The 8x filter can be bypassed by setting BYPASS\_FIR to 2'b11. For more information on filters see the Pre-Programmed Digital Filters section.

#### Pre-Programmed Filters

- Minimum Phase (default)
- Linear Phase Apodizing Fast Roll-Off
- Linear Phase Fast Roll-Off
- Linear Phase Fast Roll-Off Low-Ripple
- Linear Phase Slow Roll-Off
- Minimum Phase Fast Roll-Off
- Minimum Phase Slow Roll-Off
- Minimum Phase Slow Roll-Off Low Dispersion

#### 8x FIR Registers

- Register 30[2:0] FILTER\_SHAPE
- Register 30[4:3] BYPASS\_FIR

### IIR Filter

The IIR filter can be bypassed using Register 30[5] BYPASS\_IIR

### Soft Ramp

The ES9020 ramps the output to ground to save power when a mute condition is met. This ability can be disabled and the time it takes to ramp can be set using SOFT\_RAMP\_TIME and MUTE\_RAMP\_TO\_GROUD.

$$Time[s] = \frac{2^{15+SOFT\_RAMP\_TIME}}{MCLK * 2^{MCLK\_RATE\_SEL}}$$

#### Soft Ramp Registers

- Register 34[5] MUTE\_RAMP\_TO\_GROUND
- Register 34[4:0] SOFT\_RAMP\_TIME
- Register 3[3:2] MCLK\_RATE\_SEL
  - Used for soft ramp time equation

## GPIO Configuration

| GPIO_CONFIG | Function                | I/O Direction |
|-------------|-------------------------|---------------|
| 0           | Analog Outputs Off      | Shutdown      |
| 1           | Output 1'b0             | Output        |
| 2           | Output 1'b1             | Output        |
| 3           | Reserved                | -             |
| 4           | PLL Locked Flag         | Output        |
| 5           | DAC Minimum Volume Flag | Output        |
| 6           | DAC Automute Status     | Output        |
| 7           | DAC Soft Ramp Done Flag | Output        |
| 8           | Mute DAC                | Input         |
| 9           | System Mode Control     | Input         |
| 10          | Reserved                | -             |
| 11          | BCK/WS Monitor          | Output        |
| 12-14       | Reserved                | -             |
| 15          | MCLK_128FS              | Output        |

Table 14 - GPIO Configuration

### GPIOx Default states:

GPIO1: Automute Status  
GPIO2-8: Analog Shutdown

### Analog Outputs Off

The GPIO is shut down and has no functionality.

### Output 1'b0

Outputs a constant 1'b0.

### Output 1'b1

Outputs a constant 1'b1.

## ES9020 Product Datasheet

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### PLL Locked Flag

Outputs HIGH if the PLL is locked.

#### Relevant Readback Register

- Register 224 [0] PLL\_LOCKED

### Minimum Volume Flag

Outputs HIGH when the DAC is muted. This can occur from manually muting, automuting, and setting the volume registers to 0xFF.

The output can be a channel specific flag, the logical AND of all flags (default), or the logical OR of all the flags.

#### Relevant Registers

- Register 28[0] GPIO\_AND\_VOL\_MIN sets the output to be the logical OR of all channels' vol min flags.
- Register 28[3] GPIO\_OR\_VOL\_MIN sets the output to be the logical AND of all channels' vol min flags.
- Register 28[6] FLAG\_CH\_SEL selects which of the individual DAC channel flags to output.
  - Requires both GPIO\_AND\_VOL\_MIN and GPIO\_OR\_VOL\_MIN to be 1'b0

#### Relevant Readback Register

- Register 232 [1][0] VOL\_MIN\_CHx

### Automute Status Flag

Outputs HIGH when the DACs automute condition is met. The output can be a channel specific flag, the logical AND of all flags (default), or the logical OR of all the flags.

#### Relevant Registers

- Register 28[1] GPIO\_AND\_AUTOMUTE sets the output to be the logical AND of all channels' automute flags
- Register 28[4] GPIO\_OR\_AUTOMUTE sets the output to be the logical OR of all channels' automute flags
- Register 28[6] FLAG\_CH\_SEL sets the output to be one of the individual channels' flags
  - Requires both GPIO\_AND\_AUTOMUTE and GPIO\_OR\_AUTOMUTE to be 1'b0

#### Relevant Readback Register

- Register 232 [3][2] AUTOMUTE\_CHx

### Soft Ramp Done Flag

Outputs HIGH when the DAC is not in the process of ramping up or down. The output can be a channel specific flag, the logical AND of all flags (default), or the logical OR of all the flags.

#### Relevant Registers

- Register 28[2] GPIO\_AND\_SS\_RAMP sets the output to be the logical AND of all channels soft ramp flags
- Register 28[5] GPIO\_OR\_SS\_RAMP sets the output to be the logical OR of all channels soft ramp flags
- Register 28[6] FLAG\_CH\_SEL sets the output to be one of the individual channels' flags
  - Requires both GPIO\_AND\_SS\_RAMP and GPIO\_OR\_SS\_RAMP to be 1'b0

#### Relevant Readback Register

- Register 232 [7][6] SS\_RAMP\_DOWN\_CHx
- Register 232 [5][4] SS\_RAMP\_UP\_CHx

**Mute DAC**

Mutes all DAC channels.

**System Mode Control**

Change the system mode (enable/disable datapath) via GPIO. Register 27[4] GPIO\_DAC\_MODE changes whether a 1 on the GPIO will enable or disable the datapath.

When GPIOx input is 1'b0, the system mode will be determined by Register 0[0] DAC\_MODE\_REG.

Relevant Registers

- Register 27[4] GPIO\_DAC\_MODE
  - 1'b0: Disable datapath when GPIOx input is 1'b1
  - 1'b1: Enable datapath when GPIOx input is 1'b1
- Register 0[0] ENABLE\_DAC

**BCK/WS Monitor**

Outputs the status of the BCK and WS monitors. HIGH if either monitor detects an invalid signal.

BCK is considered invalid if the ratio  $MCLK/BCK > 1024$ .

WS is considered invalid if the ratio  $BCK/WS > 1024$ .

Relevant Registers

- Register 6[7] ENABLE\_WS\_MONITOR
- Register 6[6] ENABLE\_BCK\_MONITOR

Relevant Readback Register

- Register 230 [6] BCK\_INVALID
- Register 230 [5] WS\_INVALID

**MCLK\_128FS**

Outputs the MCLK\_128FS clock.

Requires Reg 0[0] ENABLE\_DAC to enable the clock.

## ES9020 Product Datasheet

### Pre-Programmed Digital Filters

The ES9020 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 30[2:0] FILTER\_SHAPE for configuration)

| # | Filter                                     | Description                                                                                                                                                                                       |
|---|--------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | Minimum Phase (default)                    | Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection                                                                                                           |
| 2 | Linear Phase Apodizing Fast Roll-Off       | Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.                                                                                                     |
| 3 | Linear Phase Fast Roll-Off                 | Sabre legacy filter, optimized for image rejection @ 0.55FS                                                                                                                                       |
| 4 | Linear Phase Fast Roll-Off Low-Ripple      | Sabre legacy filter, optimized for in-band ripple                                                                                                                                                 |
| 5 | Linear Phase Slow Roll-Off                 | Sabre legacy filter, optimized for lower latency, but symmetric impulse response                                                                                                                  |
| 6 | Minimum Phase Fast Roll-Off                | Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS                                                                                                                |
| 7 | Minimum Phase Slow Roll-Off                | Lowest latency at the cost of image rejection                                                                                                                                                     |
| 8 | Minimum Phase Slow Roll-Off Low Dispersion | Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band. |

Table 15 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

## PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency will reduce (scale) with sampling rate.

| Digital Filter                             | Delay      |
|--------------------------------------------|------------|
| Minimum Phase (default)                    | 5.31 / FS  |
| Linear Phase Apodizing Fast Roll-Off       | 34.67 / FS |
| Linear Phase Fast Roll-Off                 | 35.30 / FS |
| Linear Phase Fast Roll-Off Low-Ripple      | 33.23 / FS |
| Linear Phase Slow Roll-Off                 | 7.73 / FS  |
| Minimum Phase Fast Roll-Off                | 5.31 / FS  |
| Minimum Phase Slow Roll-Off                | 4.34 / FS  |
| Minimum Phase Slow Roll-Off Low Dispersion | 11.27 / FS |

Table 16 - PCM Filter Latency

## ES9020 Product Datasheet

### PCM Filter Properties

| Minimum Phase     |            |         |     |         |      |
|-------------------|------------|---------|-----|---------|------|
| Parameter         | Conditions | MIN     | TYP | MAX     | UNIT |
| Pass band         |            |         |     | 0.49 FS | Hz   |
| Stop band         | -95.46 dB  | 0.55 FS |     |         | Hz   |
| Group Delay       |            | 2.91/FS |     | 9.01/FS | s    |
| Flatness (ripple) | 0.0013     |         |     |         | dB   |

| Linear Phase Apodizing |            |         |          |         |      |
|------------------------|------------|---------|----------|---------|------|
| Parameter              | Conditions | MIN     | TYP      | MAX     | UNIT |
| Pass band              |            |         |          | 0.44 FS | Hz   |
| Stop band              | -104.2 dB  | 0.50 FS |          |         | Hz   |
| Group Delay            |            |         | 32.81 FS |         | s    |
| Flatness (ripple)      | 0.0028     |         |          |         | dB   |

| Linear Phase Fast Roll-Off |            |         |          |         |      |
|----------------------------|------------|---------|----------|---------|------|
| Parameter                  | Conditions | MIN     | TYP      | MAX     | UNIT |
| Pass band                  |            |         |          | 0.48 FS | Hz   |
| Stop band                  | -108.7 dB  | 0.55 FS |          |         | Hz   |
| Group Delay                |            |         | 33.43/FS |         | s    |
| Flatness (ripple)          | 0.0032     |         |          |         | dB   |

| Linear Phase Fast Roll-Off Low Ripple |            |         |          |         |      |
|---------------------------------------|------------|---------|----------|---------|------|
| Parameter                             | Conditions | MIN     | TYP      | MAX     | UNIT |
| Pass band                             |            |         |          | 0.49 FS | Hz   |
| Stop band                             | -88.9 dB   | 0.55 FS |          |         | Hz   |
| Group Delay                           |            |         | 31.37/FS |         | s    |
| Flatness (ripple)                     | 0.0013     |         |          |         | dB   |

| Linear Phase Slow Roll-Off |            |         |         |         |      |
|----------------------------|------------|---------|---------|---------|------|
| Parameter                  | Conditions | MIN     | TYP     | MAX     | UNIT |
| Pass band                  | -3 dB      |         |         | 0.43 FS | Hz   |
| Stop band                  | -90.6      | 0.75 FS |         |         | Hz   |
| Group Delay                |            |         | 5.87/FS |         | s    |
| Flatness (ripple)          |            |         |         |         | dB   |

| Minimum Phase Fast Roll-Off |            |         |     |         |      |
|-----------------------------|------------|---------|-----|---------|------|
| Parameter                   | Conditions | MIN     | TYP | MAX     | UNIT |
| Pass band                   |            |         |     | 0.48 FS | Hz   |
| Stop band                   | -97.8 dB   | 0.55 FS |     |         | Hz   |
| Group Delay                 |            | 2.91/FS |     | 9.14/FS | s    |
| Flatness (ripple)           | 0.0024     |         |     |         | dB   |

## ES9020 Product Datasheet

| Minimum Phase Slow Roll-Off |            |         |     |         |      |
|-----------------------------|------------|---------|-----|---------|------|
| Parameter                   | Conditions | MIN     | TYP | MAX     | UNIT |
| Pass band                   | -3 dB      |         |     | 0.43 FS | Hz   |
| Stop band                   | -90.8 dB   | 0.80 FS |     |         | Hz   |
| Group Delay                 |            | 2.08/FS |     | 3.56/FS | s    |
| Flatness (ripple)           |            |         |     |         | dB   |

| Minimum Phase Slow Roll-Off Low Dispersion |            |         |     |         |      |
|--------------------------------------------|------------|---------|-----|---------|------|
| Parameter                                  | Conditions | MIN     | TYP | MAX     | UNIT |
| Pass band                                  | -3 dB      |         |     | 0.43 FS | Hz   |
| Stop band                                  | -90.9 dB   | 0.80 FS |     |         | Hz   |
| Group Delay                                |            | 9.23/FS |     | 9.75/FS | s    |
| Flatness (ripple)                          |            |         |     |         | dB   |

Table 17 - PCM Filter Properties



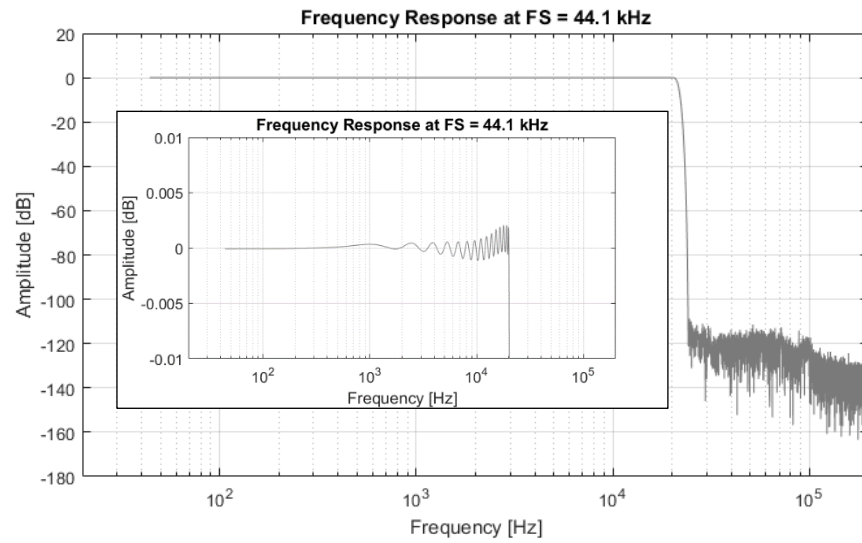
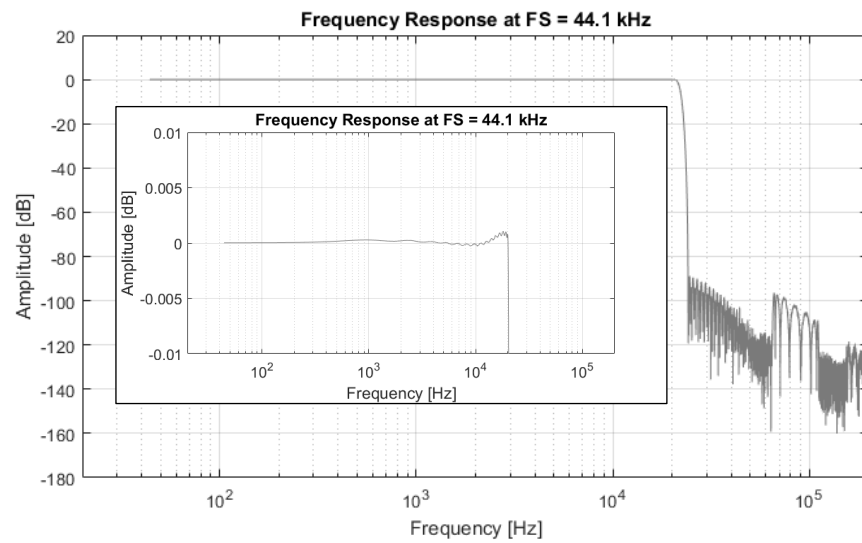
ES9020 Product Datasheet

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

| Filter                 | Frequency Response |
|------------------------|--------------------|
| Minimum Phase          |                    |
| Linear Phase Apodizing |                    |

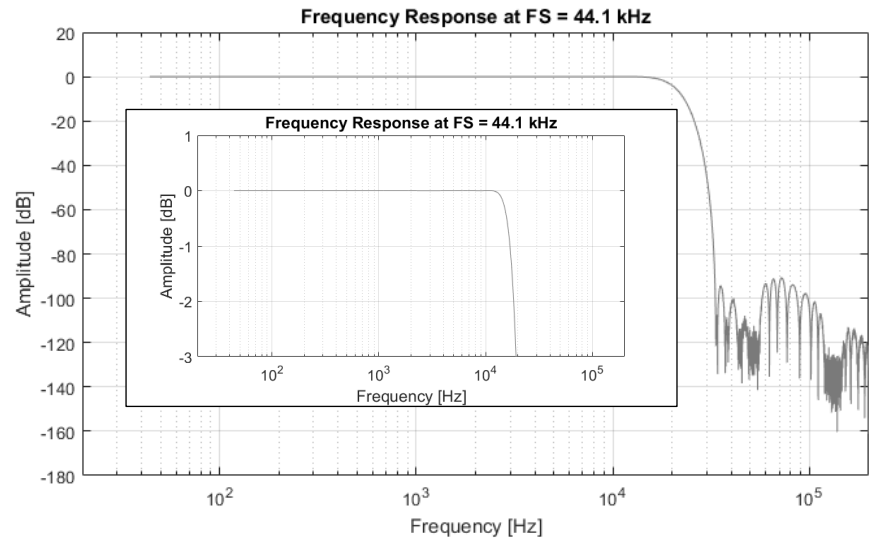
Linear Phase Fast Roll-Off


 Linear Phase Fast Roll-Off  
Low Ripple


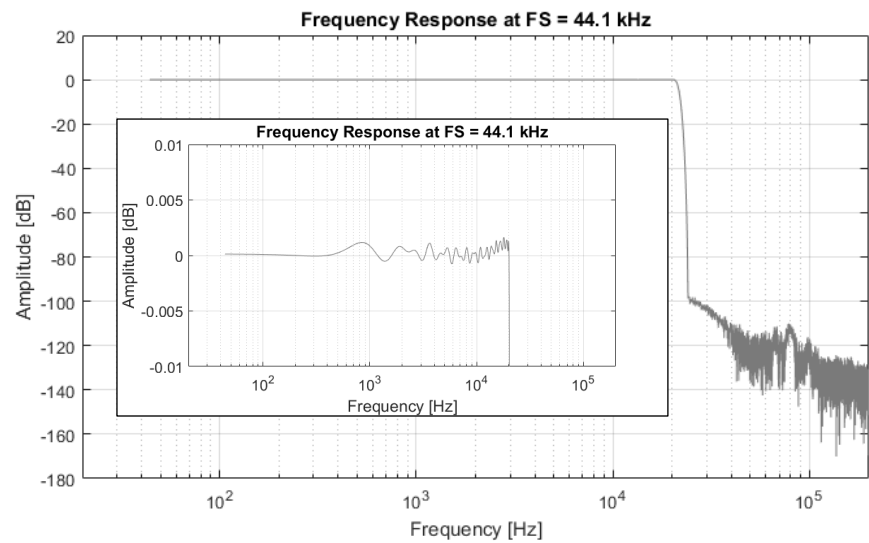


ES9020 Product Datasheet

Linear Phase Slow Roll-Off



Minimum Phase Fast Roll-Off



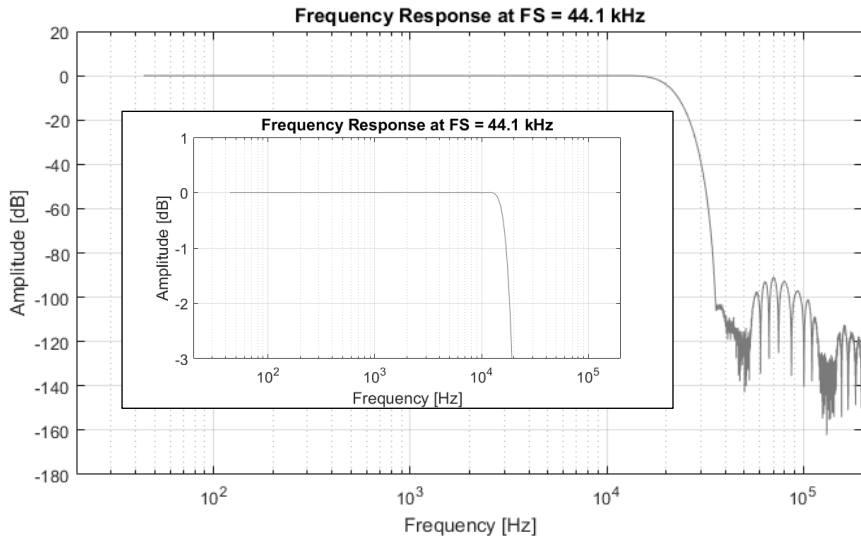
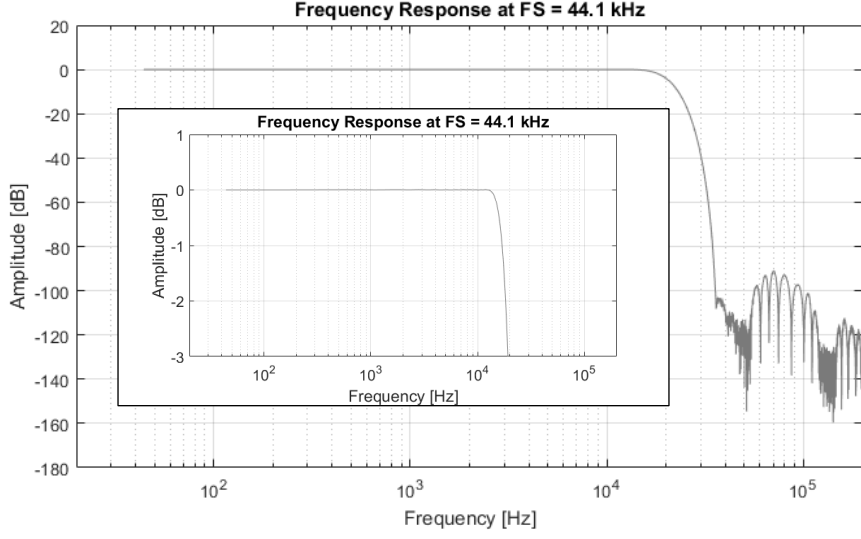
|                                                   |                                                                                      |
|---------------------------------------------------|--------------------------------------------------------------------------------------|
| <p>Minimum Phase Slow Roll-Off</p>                |    |
| <p>Minimum Phase Slow Roll-Off Low Dispersion</p> |  |

Table 18 - PCM Filter Frequency Response



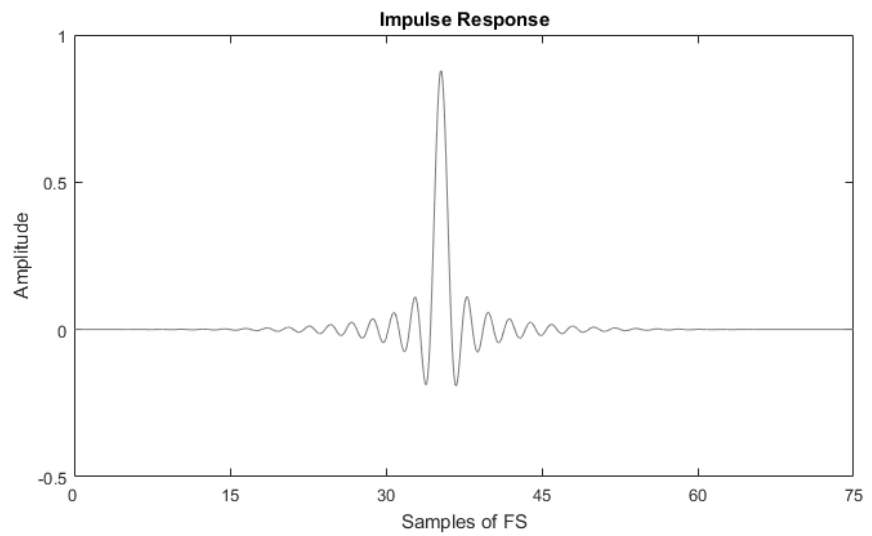
ES9020 Product Datasheet

PCM Filter Impulse Response

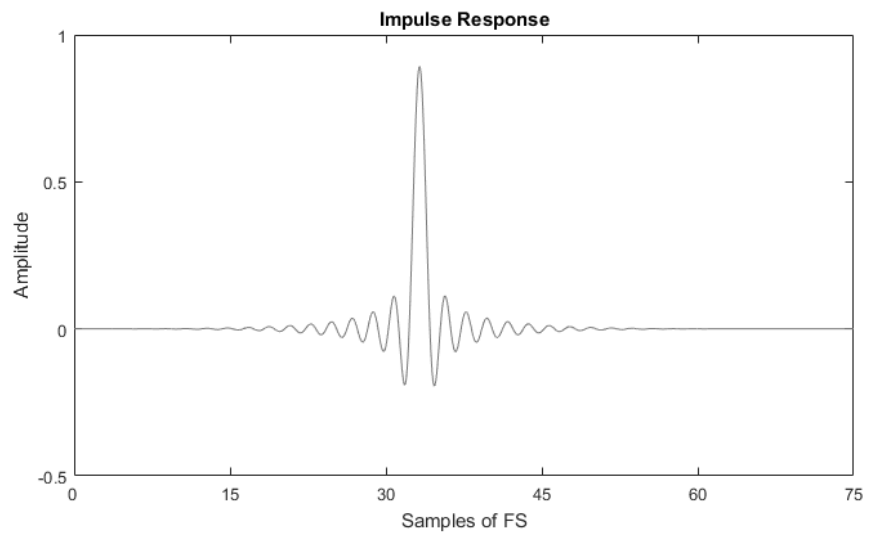
The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

| Filter                 | Impulse Response |
|------------------------|------------------|
| Minimum Phase          |                  |
| Linear Phase Apodizing |                  |

Linear Phase Fast Roll-Off



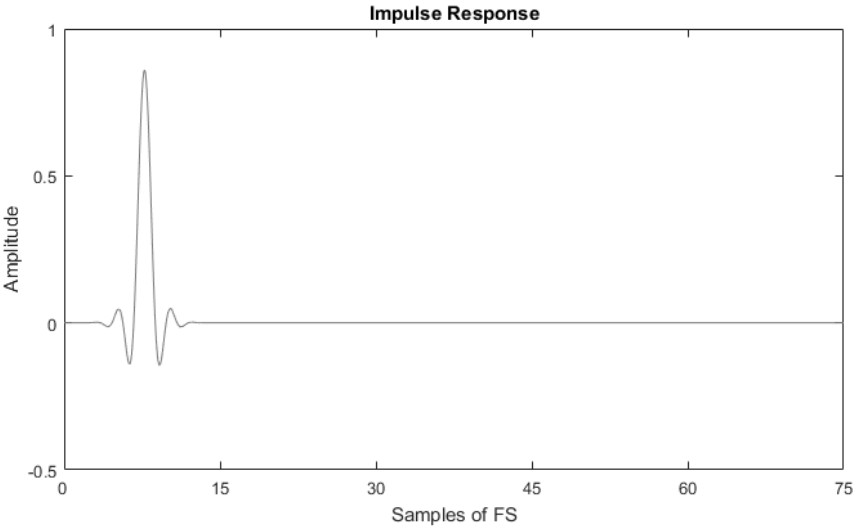
Linear Phase Fast Roll-Off  
Low Ripple



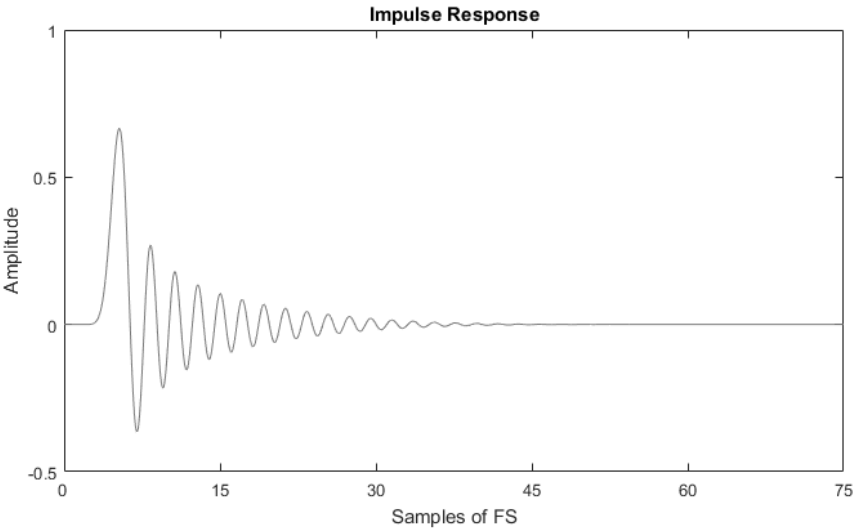


ES9020 Product Datasheet

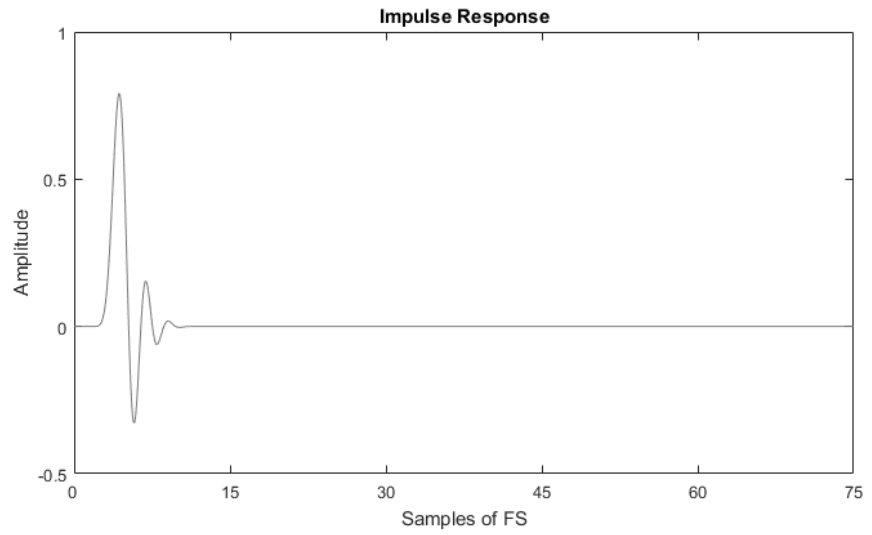
Linear Phase Slow Roll-Off



Minimum Phase Fast Roll-Off



Minimum Phase Slow Roll-Off



Minimum Phase Slow Roll-Off Low Dispersion

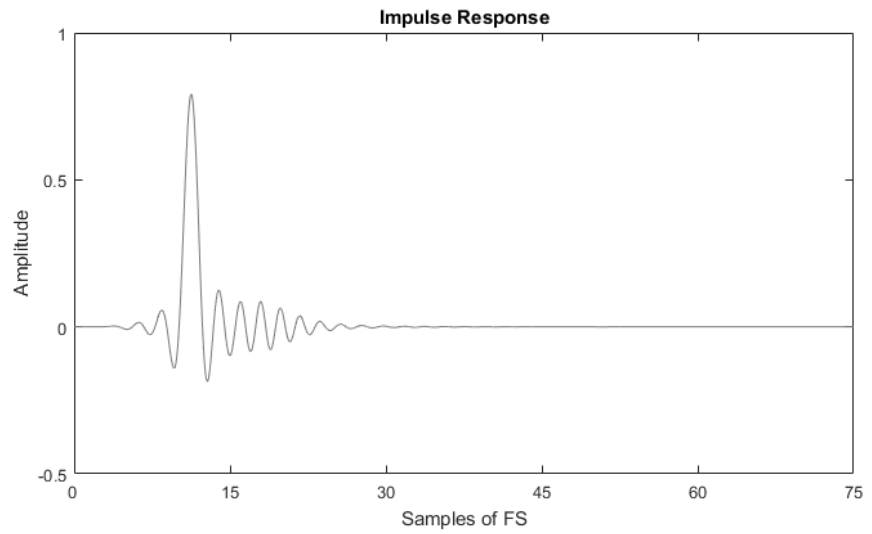


Table 19 - PCM Filter Impulse Response

## ES9020 Product Datasheet

### 64FS Mode

When the MCLK/FS ratio is 64, it is necessary for the ES9020 to be running in 64FS Mode. 64FS Mode can be enabled by setting:

#### Software Register

- Register 0[1] ENABLE\_64FS\_MODE = 1'b1
  - Manually enables 64FS mode
  - Should be used with high sample rates like 705.6kHz & 768kHz
- Register 1[2] AUTO\_FS\_DETECT
  - Sets the MCLK\_128FS divider according to MCLK/FS ratio
  - Automatically enables 64FS mode when MCLK/FS ratio is 64
  - AUTO\_FS\_DETECT can be blocked from entering 64FS mode by setting Register 0[3] AUTO\_FS\_DETECT\_BLOCK\_64FS = 1'b1

### Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

| Digital Filter     | Delay     |
|--------------------|-----------|
| Minimum Phase 64FS | 3.61 / FS |

Table 20 - Minimum Phase 64FS Latency

### Minimum Phase 64FS Properties

| Minimum Phase 64FS Mode |            |         |     |         |      |
|-------------------------|------------|---------|-----|---------|------|
| Parameter               | Conditions | MIN     | TYP | MAX     | UNIT |
| Pass band               | -3 dB      |         |     | 0.45 FS | Hz   |
| Stop band               | -61.3 dB   | 0.68 FS |     |         | Hz   |
| Group Delay             |            | 1.54/FS |     | 2.35/FS | s    |
| Flatness (ripple)       |            |         |     |         | dB   |

Table 21 - Minimum Phase 64FS Properties

## Minimum Phase 64FS Frequency Response

This filter gets selected automatically when  $MCLK/FS = 64$ . The following frequency response was obtained from software simulations with a sample rate of 705.6kHz.

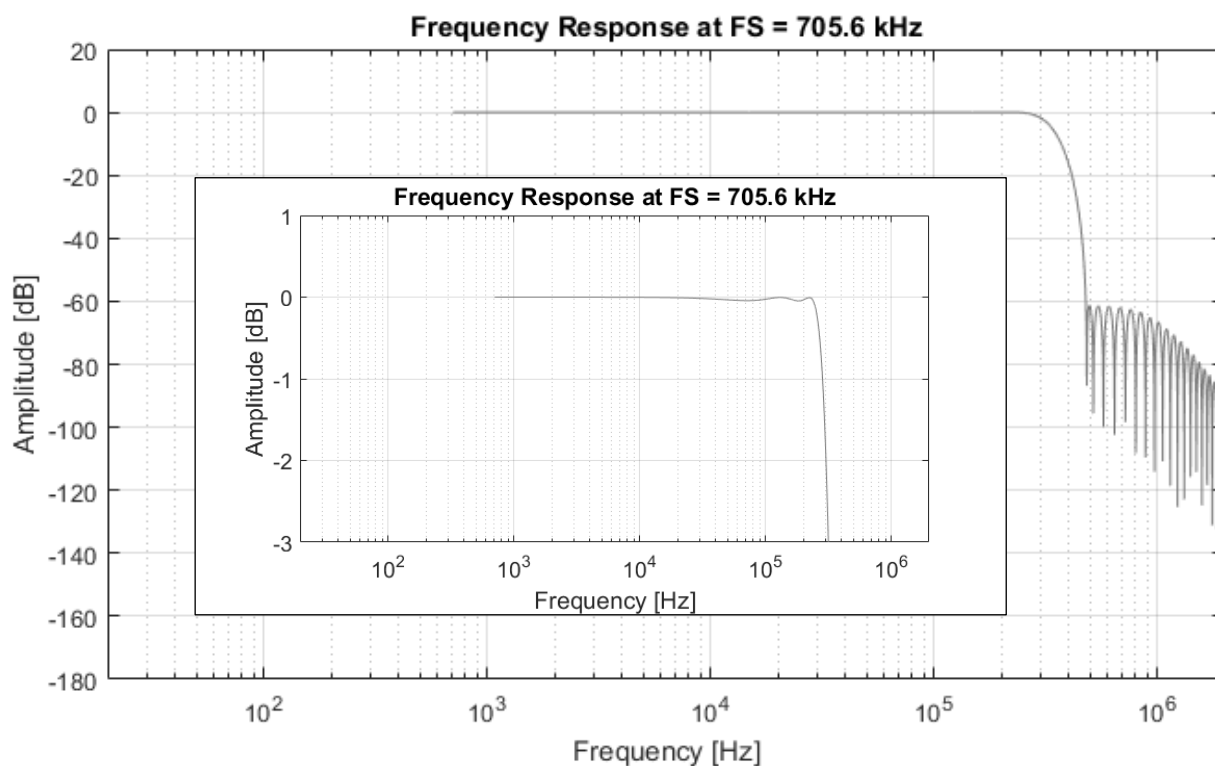


Figure 19 - Minimum Phase 64FS Frequency Response

## ES9020 Product Datasheet

### Minimum Phase 64FS Frequency Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

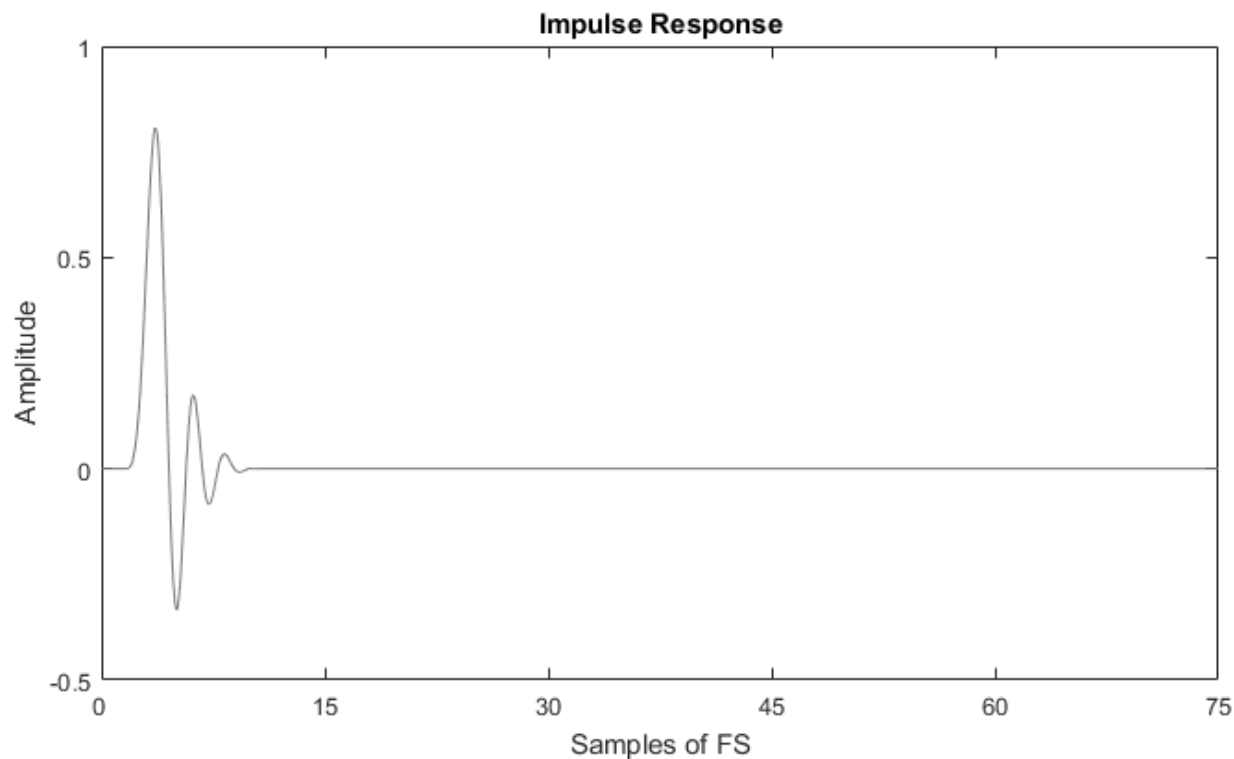


Figure 20 - Minimum Phase 64FS Impulse Response

## Daisy Chain

The ES9020 supports connecting multiple devices together in a daisy chain configuration. Up to 16 devices can be daisy chained together to output data onto any of the 32 channels in a TDM data line. The digital input to Chip#1 through DATA2 is output through GPIO3 for the Chip#2 down the chain. See Application Note for more information.

Note: While operating in 32 or 24bit word widths, TDM must be configured into I<sup>2</sup>S mode.

| DAC RSD | DAC TSD |
|---------|---------|
| DATA2   | GPIO3   |

Table 22 - Daisy Chain Pins

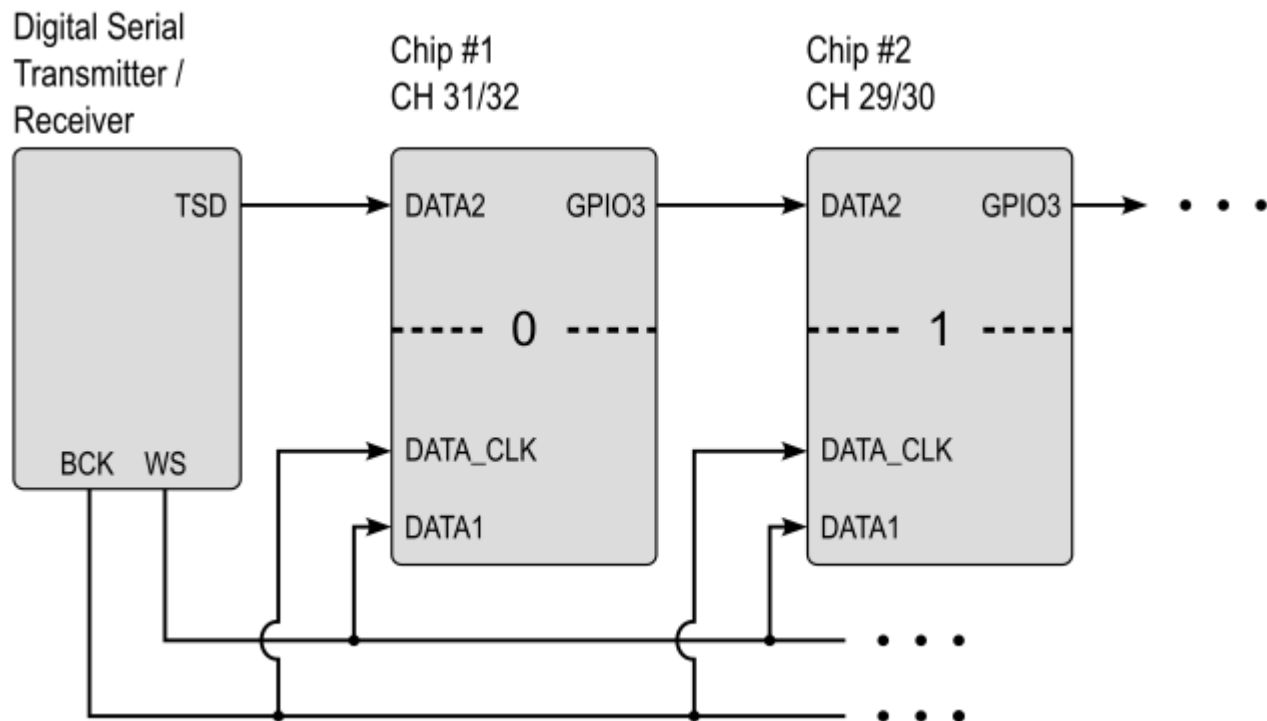


Figure 21 - Daisy Chain Configuration

## ES9020 Product Datasheet

### Sample Rate Readback

The sample rate (FS) of the ES9020 can be acquired using a combination of registers. The sample rate can be calculated using the manually set sample rate registers or the auto fs detect readback registers.

Calculation of the sample rate:

$$FS [Hz] = \frac{Y * MCLK}{(X + 1) * (\frac{128}{2^Z})}$$

| Variable   | Manually Set                      | Auto FS Detect Readback                  |
|------------|-----------------------------------|------------------------------------------|
| X (6 bits) | Register 2[5:0] MCLK_128FS_DIV    | Register 229[5:0] MCLK_128FS_DIV_AUTO    |
| Y (1 bit)  | Register 2[6] MCLK_128FS_HALF_DIV | Register 229[6] MCLK_128FS_HALF_DIV_AUTO |
| Z (1 bit)  | Register 0[1] ENABLE_64FS_MODE    | Register 27[2] ENABLE_64FS_MODE_AUTO     |
| MCLK       |                                   | Master Clock frequency                   |

Table 23 - Sample Rate Readback Variables

## Analog Features

### APLL

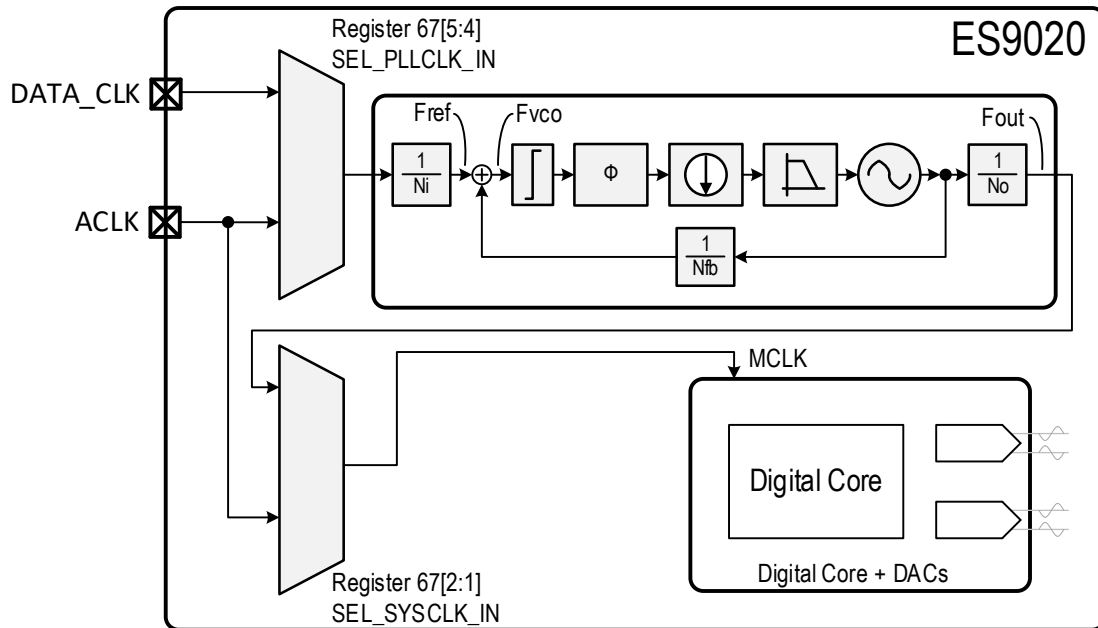


Figure 22 - Functional Block Diagram of ES9020 APLL

The ES9020 features a low jitter Analog PLL (APLL) that can generate high-quality MCLK clocks for the Sabre DACs.

In hardware modes (#9-11 and #13-15), the APLL is used in slave mode with the input from DATA\_CLK (pin 21).

In software mode, the APLL can be used in slave mode with the input from DATA\_CLK (pin 21) or ACLK (pin 2) chosen by Register 67[5:4] SEL\_PLLCLK\_IN. Alternatively, the APLL can be used in master mode with the input from ACLK (pin 2). In master mode, the APLL allows the user to create 44.1kHz and 48kHz clock rates from an asynchronous source, i.e. create 45.1584MHz/49.152MHz MCLKs from a 22MHz source and define the audio rates for the system.

For calculation of the PLL frequency output, use the following formulas:

$$F_{ref} = \left( \frac{F_{in}}{N_i} \right) \quad F_{vco} = \left( \frac{F_{in}}{N_i} \right) * N_{fb} \quad N_{fb} = \frac{2^{25}}{FBDIV} \quad F_{out} = \left( \frac{F_{in}}{N_i} \right) * \frac{N_{fb}}{N_o}$$

Where:

- FBDIV is a 24-bit number
- PLL frequency range requirements:
  - $F_{ref}$ : 1MHz <  $F_{ref}$  < 15 MHz (recommended >3MHz)
  - $F_{vco}$ : 90MHz <  $F_{vco}$  < 110MHz (\* unless otherwise recommended)
  - $F_{out}$ : 22.5792/24.576MHz or 44.1584/49.152MHz (1024\*FS, 512\*FS, 256\*FS, 128\*FS, 64\*FS) or 32.768MHz
- $N_i$  = Reg 73-75[8:0] PLL\_CLK\_IN\_DIV + 1
- $N_o$  = Reg 73-75[15:12] PLL\_CLK\_OUT\_DIV + 1
- $FBDIV = 2^{25} / \text{Reg 70-72 PLL\_CLK\_FB\_DIV}$

## 44.1kHz Base Rates

| 44.1kHz Base Rates (SYNC Slave Mode) |                |    |            |           |            |    |            |
|--------------------------------------|----------------|----|------------|-----------|------------|----|------------|
| FS (kHz)                             | DATA_CLK (MHz) | Ni | Fref (MHz) | FBDIV     | Fvco (MHz) | No | Fout (MHz) |
| 32-Bit Frame                         |                |    |            |           |            |    |            |
| 352.8                                | 22.5792        | 1  | 22.5792    | 8,388,608 | 90.3168    | 4  | 22.5792    |
| 176.4                                | 11.2896        | 1  | 11.2896    | 4,194,304 | 90.3168    | 4  | 22.5792    |
| 88.2                                 | 5.6448         | 1  | 5.6448     | 2,097,152 | 90.3168    | 4  | 22.5792    |
| 44.1                                 | 2.8224         | 1  | 2.8224     | 1,048,576 | 90.3168    | 4  | 22.5792    |
| 16-Bit Frame                         |                |    |            |           |            |    |            |
| 352.8                                | 11.2896        | 1  | 11.2896    | 4,194,304 | 90.3168    | 4  | 22.5792    |
| 176.4                                | 5.6448         | 1  | 5.6448     | 2,097,152 | 90.3168    | 4  | 22.5792    |
| 88.2                                 | 2.8224         | 1  | 2.8224     | 1,048,576 | 90.3168    | 4  | 22.5792    |
| 44.1                                 | 1.4112         | 1  | 1.4112     | 524,288   | 90.3168    | 4  | 22.5792    |

Table 24 - APLL Divider Values for 44.1kHz Base Rates

## 48kHz Base Rates

| 48kHz Base Rates (SYNC Slave Mode) |                |    |            |           |            |    |            |
|------------------------------------|----------------|----|------------|-----------|------------|----|------------|
| FS (kHz)                           | DATA_CLK (MHz) | Ni | Fref (MHz) | FBDIV     | Fvco (MHz) | No | Fout (MHz) |
| 32-Bit Frame                       |                |    |            |           |            |    |            |
| 384                                | 24.576         | 1  | 24.576     | 8,388,608 | 98.304     | 4  | 24.576     |
| 192                                | 12.288         | 1  | 12.288     | 4,194,304 | 98.304     | 4  | 24.576     |
| 96                                 | 6.144          | 1  | 6.144      | 2,097,152 | 98.304     | 4  | 24.576     |
| 48                                 | 3.072          | 1  | 3.072      | 1,048,576 | 98.304     | 4  | 24.576     |
| 16-Bit Frame                       |                |    |            |           |            |    |            |
| 384                                | 12.288         | 1  | 12.288     | 4,194,304 | 98.304     | 4  | 24.576     |
| 192                                | 6.144          | 1  | 6.144      | 2,097,152 | 98.304     | 4  | 24.576     |
| 96                                 | 3.072          | 1  | 3.072      | 1,048,576 | 98.304     | 4  | 24.576     |
| 48                                 | 1.536          | 1  | 1.536      | 524,288   | 98.304     | 4  | 24.576     |

Table 25 - APLL Divider Values for 48kHz Base Rates

## 32kHz Base Rates

In the case of 16kHz or 32kHz sample rates, the VCO operates at a lower frequency and requires Register 76 [7:5]: VCO BAND CTRL to be set to 3'b001 to get the best performance.

| 32kHz base rates (SYNC Slave Mode) |                |    |            |           |            |    |            |
|------------------------------------|----------------|----|------------|-----------|------------|----|------------|
| FS (kHz)                           | DATA_CLK (MHz) | Ni | Fref (MHz) | FBDIV     | Fvco (MHz) | No | Fout (MHz) |
| 32BIT FRAME                        |                |    |            |           |            |    |            |
| 32                                 | 2.048          | 1  | 2.048      | 1,048,576 | 65.536*    | 2  | 32.768     |
| 16                                 | 1.024          | 1  | 1.024      | 524,288   | 65.536*    | 2  | 32.768     |

Table 26 - APLL Divider values for 32kHz Base Rates

For the application note on the APLL, please ask your ESS Technology FAE or distributor.

## Absolute Maximum Ratings

| PARAMETER                                                                                                                                               | RATING                                                                                                                                                                                                                                   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Positive Supply Voltage <ul style="list-style-type: none"> <li>• AVCC</li> <li>• AVDD</li> <li>• VCCA</li> <li>• DVDD (Internally generated)</li> </ul> | <ul style="list-style-type: none"> <li>• -0.3 to +3.7V with respect to ground</li> <li>• -0.3 to +3.7V with respect to ground</li> <li>• -0.3 to +3.7V with respect to ground</li> <li>• -0.3 to +1.4V with respect to ground</li> </ul> |
| Storage Temperature                                                                                                                                     | -65°C to +150°C                                                                                                                                                                                                                          |
| Operating Junction Temperature                                                                                                                          | +125°C                                                                                                                                                                                                                                   |
| Voltage Range for Digital Input Pins                                                                                                                    | -0.3V to AVDD (nom) +0.3V                                                                                                                                                                                                                |

Table 27 - Absolute Maximum Ratings

**WARNING:** Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

## ESD Ratings

| ESD Standard                                      | Rating |
|---------------------------------------------------|--------|
| Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001    | 2kV    |
| Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002 | 500V   |

Table 28 - ESD Ratings

**WARNING:** Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

## IO Electrical Characteristics

| PARAMETER                 | SYMBOL | MINIMUM            | MAXIMUM | UNIT |
|---------------------------|--------|--------------------|---------|------|
| High-level input voltage  | VIH    | $(AVDD / 2) + 0.4$ |         | V    |
| Low-level input voltage   | VIL    |                    | 0.4     | V    |
| High-level output voltage | VOH    | $AVDD - 0.2$       |         | V    |
| Low-level output voltage  | VOL    |                    | 0.2     | V    |

Table 29 - I/O Electrical Characteristics

## ES9020 Product Datasheet

### Switching Characteristics

| Parameter                           | Notes                  | Min.      | Typ.                                  | Max.      | Unit |
|-------------------------------------|------------------------|-----------|---------------------------------------|-----------|------|
| MCLK <sup>1</sup>                   |                        |           |                                       |           |      |
| Frequency                           |                        | 6.144     | -                                     | 49.152    | MHz  |
| Duty Cycle                          |                        | 45        | -                                     | 55        | %    |
|                                     |                        |           |                                       |           |      |
| PCM Mode <sup>2</sup>               |                        |           |                                       |           |      |
| WS Frequency<br>(Word Select Clock) |                        | 8         | -                                     | MCLK/128  | kHz  |
| BCLK Frequency<br>(Bit Clock)       |                        | (16*2*WS) | TDM_BIT_WIDTH)*<br>(TDM_CH_NUM+1)*WS  | MCLK      | MHz  |
| WS Frequency<br>(Word Select Clock) | 64FS Mode <sup>3</sup> | 352.8     | MCLK/64                               | 768       | kHz  |
| BCLK Frequency<br>(Bit Clock)       |                        | 22.5792   | MCLK                                  | 49.152    | MHz  |
|                                     |                        |           |                                       |           |      |
| TDM Mode                            |                        |           |                                       |           |      |
| WS Frequency<br>(Word Select Clock) | TDM4                   | 8kHz      | -                                     | MCLK/128  | kHz  |
|                                     | TDM8                   |           | -                                     | MCLK/256  | kHz  |
|                                     | TDM16                  |           | -                                     | MCLK/512  | kHz  |
|                                     | TDM32                  |           | -                                     | MCLK/1024 | kHz  |
| BCLK Frequency<br>(Bit Clock)       |                        | (16*2*WS) | (TDM_BIT_WIDTH)*<br>(TDM_CH_NUM+1)*WS | MCLK      | MHz  |
|                                     |                        |           |                                       |           |      |
| DSD Mode                            |                        |           |                                       |           |      |
| DSD Clock Frequency                 |                        | 2.8224    | -                                     | MCLK/2    | MHz  |

Table 30 - Switching Characteristics

<sup>1</sup> MCLK must be synchronous to the digital audio clock

<sup>2</sup> In hardware mode, only 32-bit word widths are supported for both PCM and TDM unless otherwise specified.

<sup>3</sup> 64FS mode is for 705.6/768kHz with 45.1584/49.152MHz or 352.8/384kHz with 22.5792/24.576MHz.

## Timing Characteristics

### MCLK Timing

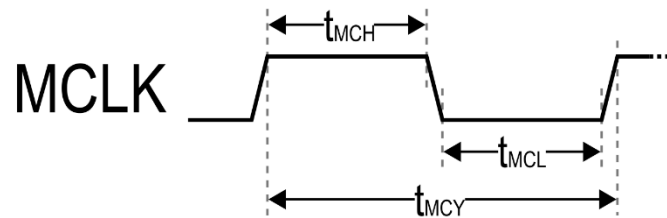


Figure 23 - MCLK Timing

| Parameter             | Symbol    | Min.  | Max.  | Unit |
|-----------------------|-----------|-------|-------|------|
| MCLK Pulse Width High | $t_{MCH}$ | 7     | -     | ns   |
| MCLK Pulse Width Low  | $t_{MCL}$ | 7     | -     | ns   |
| MCLK Cycle Time       | $t_{MCY}$ | 20    | -     | ns   |
| MCLK Duty Cycle       |           | 45:55 | 55:45 | ns   |

Table 31 - MCLK Timing Definitions

### Bit-Clock (BCLK) and Word-Select (WS) Timing

Test Conditions 1 (unless otherwise noted)

$T_A = 25^\circ\text{C}$ , AVCC\_3V3\_L = AVCC\_3V3\_R = AVCC\_CP = AVDD = +3.3V, DVDD= Internal, fs = 48kHz, DAC enabled, 1kHz sine full scale.

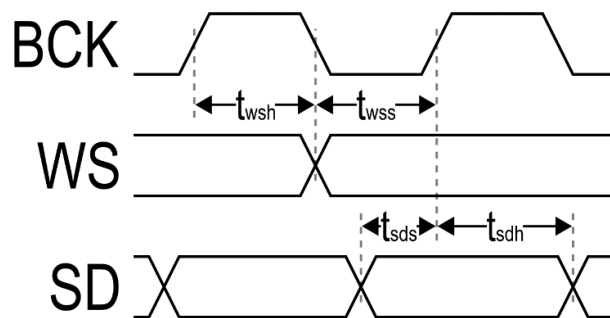
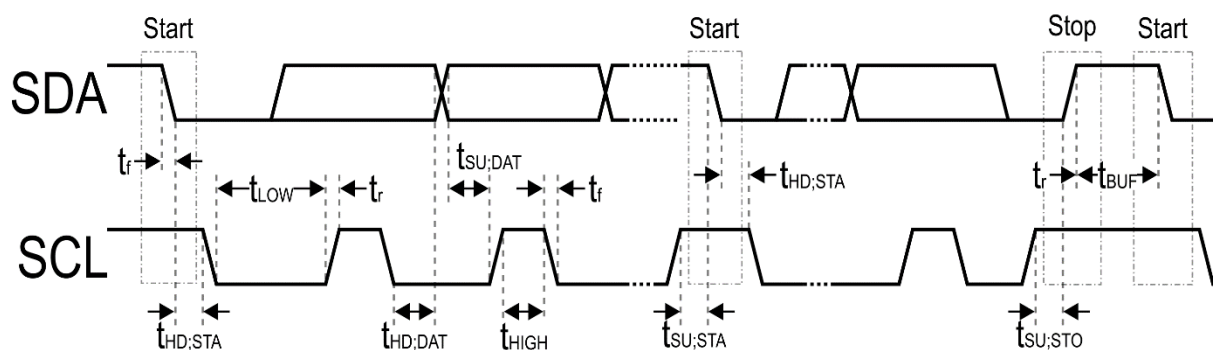


Figure 24 - Bit-Clock and Word-Select Timing

| Parameter     | Symbol    | Min. | Typ. | Max. | Unit |
|---------------|-----------|------|------|------|------|
| WS hold time  | $t_{wsh}$ | 0.5  | -    | -    | ns   |
| WS setup time | $t_{wss}$ | 0    | -    | -    | ns   |
| SD hold time  | $t_{sds}$ | 0.9  | -    | -    | ns   |
| SD setup time | $t_{sdh}$ | 0    | -    | -    | ns   |

Table 32 - Bit-Clock and Word-Select Timing Definitions

## I<sup>2</sup>C Slave Interface Timing

Figure 25 - I<sup>2</sup>C Slave Control Interface Timing

| Parameter                                                                    | Symbol       | CLK Constraint | Standard-Mode |      | Fast-Mode  |     | Unit         |
|------------------------------------------------------------------------------|--------------|----------------|---------------|------|------------|-----|--------------|
|                                                                              |              |                | MIN           | MAX  | MIN        | MAX |              |
| SCL Clock Frequency                                                          | $f_{SCL}$    | $< CLK/20$     | 0             | 100  | 0          | 400 | kHz          |
| START condition hold time                                                    | $t_{HD;STA}$ |                | 4.0           | -    | 0.6        | -   | $\mu s$      |
| LOW period of SCL                                                            | $t_{LOW}$    | $> 10/CLK$     | 4.7           | -    | 1.3        | -   | $\mu s$      |
| HIGH period of SCL ( $> 10/CLK$ )                                            | $t_{HIGH}$   | $> 10/CLK$     | 4.0           | -    | 0.6        | -   | $\mu s$      |
| START condition setup time (repeat)                                          | $t_{SU;STA}$ |                | 4.7           | -    | 0.6        | -   | $\mu s$      |
| SDA hold time from SCL falling<br>- All except NACK read<br>- NACK read only | $t_{HD;DAT}$ |                | 0<br>2/CLK    | -    | 0<br>2/CLK | -   | $\mu s$<br>s |
| SDA setup time from SCL rising                                               | $t_{SU;DAT}$ |                | 250           | -    | 100        | -   | ns           |
| Rise time of SDA and SCL                                                     | $t_r$        |                | -             | 1000 | -          | 300 | ns           |
| Fall time of SDA and SCL                                                     | $t_f$        |                | -             | 300  | -          | 300 | ns           |
| STOP condition setup time                                                    | $t_{SU;STO}$ |                | 4             | -    | 0.6        | -   | $\mu s$      |
| Bus free time between transmissions                                          | $t_{BUF}$    |                | 4.7           | -    | 1.3        | -   | $\mu s$      |
| Capacitive load for each bus line                                            | $C_b$        |                | -             | 400  | -          | 400 | pF           |

Table 33 - I<sup>2</sup>C Slave/Synchronous Slave Interface Timing Definitions

## SPI Slave Interface Timing

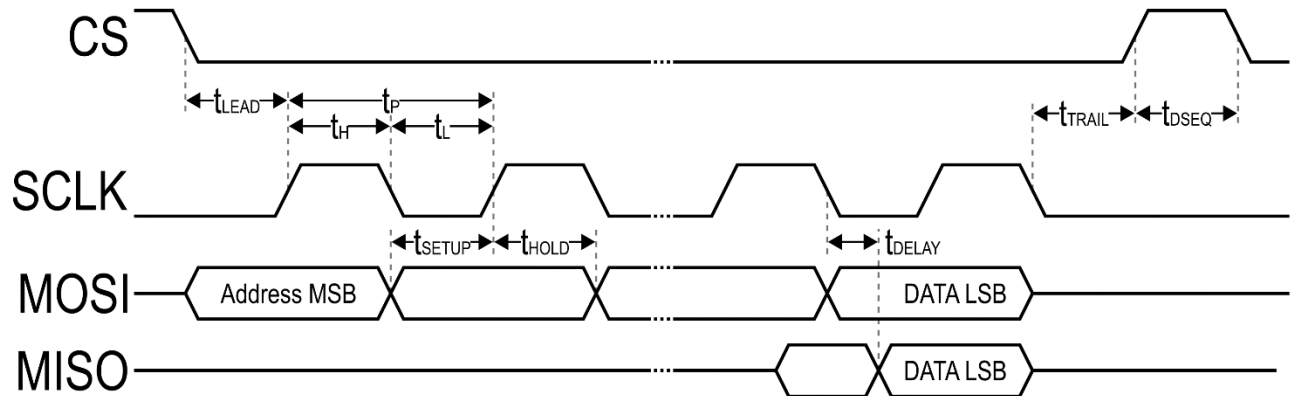


Figure 26 - SPI Slave Interface Timing

| Parameter                         | Symbol            | Min [ns] | Max [ns] |
|-----------------------------------|-------------------|----------|----------|
| CS Lead Time (SCLK rising edge)   | $t_{LEAD}$        | 4        | -        |
| CS Trail Time (SCLK falling edge) | $t_{TRAIL}$       | 4        | -        |
| MOSI Data Setup Time              | $t_{SETUP\_MOSI}$ | -36      | -        |
| MOSI Data Hold Time               | $t_{HOLD\_MOSI}$  | 60       | -        |
| SCLK-MISO Delay Time              | $t_{DELAY\_MISO}$ | -        | 74       |
| SCLK Period                       | $t_{P\_SCLK}$     | 122      | -        |
| SCLK High Pulse Duration          | $t_{H\_SCLK}$     | 94       | -        |
| SCLK Low Pulse Duration           | $t_{L\_SCLK}$     | 60       | -        |
| Sequential Transfer Delay         | $t_{DSEQ}$        | 38       | -        |

Table 34 - SPI Slave Interface Timing

## Recommended Operating Conditions

| PARAMETER             | SYMBOL | CONDITIONS     |
|-----------------------|--------|----------------|
| Operating Temperature | $T_A$  | -20°C to +85°C |
| AVDD                  |        | +3.3V ± 5%     |
| AVCC                  |        | +3.3V ± 5%     |
| VCCA                  |        | +3.3V ± 5%     |
| DVDD                  |        | Internal +1.2V |
| VREF_BUF              |        | Internal +2.8V |
| VREF                  |        | Internal +2.8V |
| PLL_REG               |        | Internal +1.8V |

Table 35 - Recommended Operating Conditions

## ES9020 Product Datasheet

### Recommended Power Up/Down Sequence

The recommended power up sequence for the ES9020, the AVDD supply is enabled ~200us before VCCA. Finally enable AVCC then the chip can be enabled, followed by the MCLK source. There is a ~20ms delay between enabling the DACs and valid analog data output. MCLK must be on before enabling the DACs.

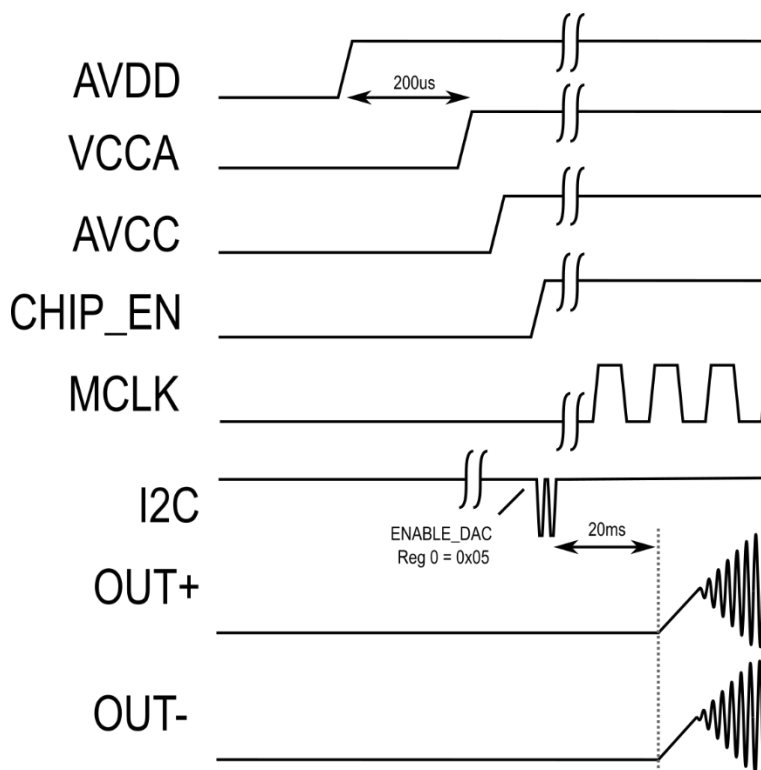


Figure 27 - Recommended Power Up Sequence

On power down, make sure the DAC is muted and set CHIP\_EN low. Then its safe to power down the power supplies.

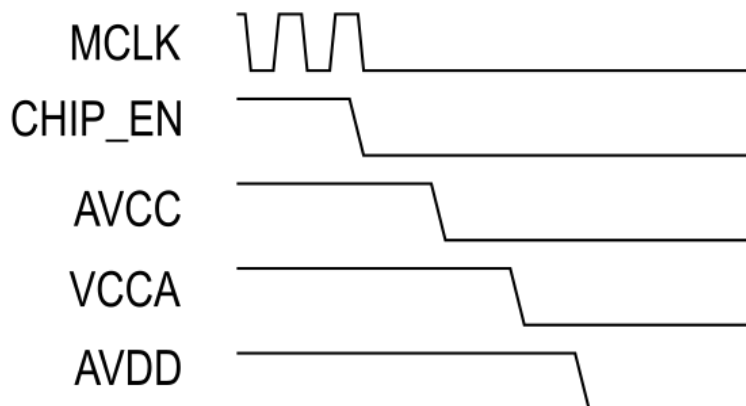


Figure 28 - Recommended Power Down Sequence

## Power Consumption

Test Conditions (unless otherwise noted)

T<sub>A</sub> = 25°C, AVCC = AVDD = VCCA = +3.3V, FS=48kHz, MCLK = 49.152MHz, HW mode #3

AVDD supply includes DVDD current.

| Parameter                                 | Min | Typ. | Max | Unit |
|-------------------------------------------|-----|------|-----|------|
| <b>Standby (CHIP_EN=0)</b>                |     |      |     |      |
| AVCC                                      |     | <0.1 |     | mA   |
| VCCA                                      |     | 0    |     | mA   |
| AVDD                                      |     | <0.1 |     | mA   |
| Total Power Consumption                   |     | <1mW |     | mw   |
| <b>Playback (input level = 0dBFS)</b>     |     |      |     |      |
| AVCC                                      |     | 7.3  |     | mA   |
| VCCA                                      |     | 0.3  |     | mA   |
| AVDD                                      |     | 6.1  |     | mA   |
| Total Power Consumption                   |     | 46   |     | mW   |
| <b>Quiescent (input level = -999dBFS)</b> |     |      |     |      |
| AVCC                                      |     | 1.4  |     | mA   |
| VCCA                                      |     | 0.3  |     | mA   |
| AVDD                                      |     | 2.5  |     | mA   |
| Total Power Consumption                   |     | 14   |     | mW   |

Table 36 - ES9020 Power Consumption

Note: Current consumption can be reduced by externally supplying DVDD with 1.2V to decrease AVDD current or lowering the MCLK frequency.

## ES9020 Product Datasheet

### Performance

Test Conditions 1 (unless otherwise noted)

$T_A = 25^\circ\text{C}$ ,  $AVCC = VCCA = AVDD = +3.3\text{V}$ ,  $f_s = 48\text{kHz}$ , HW mode (I<sup>2</sup>S Master Mode)

| Parameter                                                              |                                                     | Min     | Typ.                                           | Max | Unit            |
|------------------------------------------------------------------------|-----------------------------------------------------|---------|------------------------------------------------|-----|-----------------|
| Resolution                                                             |                                                     |         | 32                                             |     | Bit             |
| Max MCLK frequency                                                     | Note: Synchronous clocks required                   |         | 49.152                                         |     | MHz             |
| THD+N Ratio @ $f_s=48\text{kHz}$ (differential)                        | 0dBFS<br>BW=20Hz-20kHz                              |         | -110                                           |     | dB              |
| THD+N Ratio @ $f_s=96\text{kHz}$ (differential)                        | 0dBFS<br>BW=20Hz-40kHz                              |         | -107                                           |     | dB              |
| THD+N Ratio @ $f_s=192\text{kHz}$ (differential)                       | 0dBFS<br>BW=20Hz-80kHz                              |         | -104                                           |     | dB              |
| THD+N Ratio @ $f_s=384\text{kHz}$ (differential)                       | 0dBFS<br>BW=20Hz-160kHz                             |         | -101                                           |     | dB              |
| DNR (A-weighted) (Stereo mode)                                         | MCLK @ 49.152MHz                                    | -60dBFS | 122                                            |     | dB              |
| DNR (A-weighted) (Mono mode – 2 ch sum diff)                           | MCLK @ 49.152MHz                                    |         | 125                                            |     | dB              |
| Voltage output amplitude                                               | Full-scale out <b>per pin</b>                       |         | $0.837 \times VREF\_BUF$                       |     | V <sub>pp</sub> |
| Voltage output offset                                                  | Bipolar zero out                                    |         | $VREF\_BUF / 2$                                |     | V               |
| Current output amplitude                                               | Full-scale out                                      |         | $1000 \times 0.837 \times VREF\_BUF / R_{DAC}$ |     | mApp            |
| Current output offsets                                                 | Bipolar zero out to virtual ground at voltage $V_G$ |         | $1000 \times (VREF\_BUF/2 - V_G) / R_{DAC}$    |     | mA              |
| Output impedance (Per + or – pin of each differential DAC output pair) | $R_{DAC}$                                           |         | 1.05 +/- 15%                                   |     | k $\Omega$      |

Table 37 - ES9020 Performance

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## Register Overview

A system clock is not required to access registers.

### **Read/Write Register Addresses**

Registers 0-81 (0x00 - 0x51) are read and write registers.

### **Read-Only Register Addresses**

Register 224-232 (0xE0 - 0xE8) are read only registers.

### **Multi-Byte Registers**

Multi-Byte registers must be written from LSB to MSB. Data is latched when MSB is written.

Multi-Byte registers must be read from LSB to MSB. Data is latched when LSB is read.

MSB is always stored in the highest register address.

# ES9020 Product Datasheet

## Register Map

| Addr<br>(Hex) | Addr<br>(Dec) | Register                  | 7                   | 6                   | 5                   | 4                    | 3                         | 2                 | 1                  | 0                  |                 |
|---------------|---------------|---------------------------|---------------------|---------------------|---------------------|----------------------|---------------------------|-------------------|--------------------|--------------------|-----------------|
| 0x00          | 0             | SYS CONFIG                | SOFT_RESET          | RESERVED            |                     |                      | AUTO_FS_DETECT_BLOCK_64FS | AUTO_FS_DETECT    | ENABLE_64FS_MODE   | ENABLE_DAC         |                 |
| 0x01          | 1             | DIGITAL INPUT CONFIG      | ENABLE_PDM_DECODE   | ENABLE_DSD_DECODE   | ENABLE_DOP_DECODE   | ENABLE_TDM_DECODE    | RESERVED                  | INPUT_SEL         |                    | AUTO_INPUT_SEL     |                 |
| 0x02          | 2             | CLOCK CONTROL 1           | RESERVED            | MCLK_128FS_HALF_DIV | MCLK_128FS_DIV      |                      |                           |                   |                    |                    |                 |
| 0x03          | 3             | CLOCK CONTROL 2           | RESERVED            |                     |                     |                      | MCLK_RATE_SEL             |                   | DAC_CLK_INV        | RESERVED           |                 |
| 0x04          | 4             | PCM MASTER CLK CONFIG     | MASTER_BCK_DIV      |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x05          | 5             | MASTER MODE CONFIG        | SLAVE_BCK_INVERT    | RESERVED            |                     | MASTER_WS_PULSE_MODE | MASTER_WS_INVERT          | MASTER_BCK_INVERT | DSD_MASTER_MODE_EN | PCM_MASTER_MODE_EN |                 |
| 0x06          | 6             | TDM CONFIG 1              | TDM_RESYNC          | AUTO_CH_DETECT      | RESERVED            | TDM_CH_NUM           |                           |                   |                    |                    |                 |
| 0x07          | 7             | TDM CONFIG 2              | ENABLE_WS_MONITOR   | ENABLE_BCK_MONITOR  | TDM_WORD_WIDTH      |                      | TDM_BIT_DEPTH             |                   | TDM_VALID_EDGE     | TDM_LJ             |                 |
| 0x08          | 8             | CH1 INPUT CONFIG          | PDM_SAMPLE_EDGE     | PDM_PHASE           | DSD_LINE_SEL_CH1    | TDM_SLOT_SEL_CH1     |                           |                   |                    |                    |                 |
| 0x09          | 9             | CH2 INPUT CONFIG          | PDM_2X_GAIN_EN      | RESERVED            | DSD_LINE_SEL_CH2    | TDM_SLOT_SEL_CH2     |                           |                   |                    |                    |                 |
| 0x0A          | 10            | TDM DAISY CHAIN           | TDM_DAISY_CHAIN     | RESERVED            |                     | TDM_DATA_LATCH_ADJ   |                           |                   |                    |                    |                 |
| 0x0B-0x16     | 11-22         | RESERVED                  | RESERVED            |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x17          | 23            | GPIO1/2 CONFIG            | GPIO2_CFG           |                     |                     |                      | GPIO1_CFG                 |                   |                    |                    |                 |
| 0x18          | 24            | GPIO3/4 CONFIG            | GPIO4_CFG           |                     |                     |                      | GPIO3_CFG                 |                   |                    |                    |                 |
| 0x19          | 25            | GPIO INPUT OUTPUT CONTROL | GPIO4_SDB           | GPIO3_SDB           | GPIO2_SDB           | GPIO1_SDB            | GPIO4_OE                  | GPIO3_OE          | GPIO2_OE           | GPIO1_OE           |                 |
| 0x1A          | 26            | GPIO CONTROL              | GPIO4_INV           | GPIO3_INV           | GPIO2_INV           | GPIO1_INV            | GPIO4_WK_EN               | GPIO3_WK_EN       | GPIO2_WK_EN        | GPIO1_WK_EN        |                 |
| 0x1B          | 27            | GPIO READ CONTROL         | RESERVED            |                     |                     | GPIO_DAC_MODE        | GPIO4_READ                | GPIO3_READ        | GPIO2_READ         | GPIO1_READ         |                 |
| 0x1C          | 28            | GPIO OUTPUT LOGIC         | RESERVED            | FLAG_CH_SEL         | GPIO_OR_SS_RAMP     | GPIO_OR_AUTOMUTE     | GPIO_OR_VOL_MIN           | GPIO_AND_SS_RAMP  | GPIO_AND_AUTOMUTE  | GPIO_AND_VOL_MIN   |                 |
| 0x1D          | 29            | RESERVED                  | RESERVED            |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x1E          | 30            | DAC FILTER CONFIG         | RESERVED            |                     | BYPASS_IIR          | BYPASS_FIR           |                           | FILTER_SHAPE      |                    |                    |                 |
| 0x1F          | 31            | VOLUME CH1                | VOLUME_CH1          |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x20          | 32            | VOLUME CH2                | VOLUME_CH2          |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x21          | 33            | MUTE AND VOL PHASE        | RESERVED            |                     |                     |                      | MUTE_CH2                  | MUTE_CH1          | VOL_PHASE_IN_V_CH2 | VOL_PHASE_IN_V_CH1 |                 |
| 0x22          | 34            | SOFT RAMP CONFIG          | MONO_VOLUME         | RESERVED            | MUTE_RAMP_TO_GROUND | SOFT_RAMP_TIME       |                           |                   |                    |                    |                 |
| 0x23          | 35            | VOLUME UP RAMP RATE       | VOL_RAMP_RATE_UP    |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x24          | 36            | VOLUME DOWN RAMP RATE     | VOL_RAMP_RATE_DOWN  |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x25          | 37            | DIGITAL GAIN              | RESERVED            | DIGITAL_GAIN_CH2    |                     |                      | RESERVED                  | DIGITAL_GAIN_CH1  |                    |                    |                 |
| 0x26          | 38            | AUTOMUTE ENABLE           | RESERVED            |                     |                     |                      |                           |                   |                    | AUTOMUTE_EN_CH2    | AUTOMUTE_EN_CH1 |
| 0x27          | 39            | AUTOMUTE TIME             | AUTOMUTE_TIME       |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x28          | 40            |                           | DSD_FAULT_DETECT_EN | DSD_DC_AM_ENB       | DSD_MUTE_AM_ENB     | RESERVED             |                           | AUTOMUTE_TIME     |                    |                    |                 |
| 0x29          | 41            |                           | AUTOMUTE_LEVEL      |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x2A          | 42            |                           | AUTOMUTE_LEVEL      |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x2B          | 43            |                           | AUTOMUTE_OFF_LEVEL  |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x2C          | 44            | AUTOMUTE OFF LEVEL        | AUTOMUTE_OFF_LEVEL  |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x2D-0x32     | 45-50         | RESERVED                  | RESERVED            |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x33          | 51            | DBQ COEFF SEL             | RESERVED            |                     |                     | DBQ_COEFF_SEL        |                           |                   |                    |                    |                 |
| 0x34          | 52            | PROG DBQ A2 COEFF         | DBQ_A2              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x35          | 53            |                           | DBQ_A2              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x36          | 54            |                           | DBQ_A2              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x37          | 55            | PROG DBQ A1 COEFF         | DBQ_A1              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x38          | 56            |                           | DBQ_A1              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x39          | 57            |                           | DBQ_A1              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x3A          | 58            | PROG DBQ B2 COEFF         | DBQ_B2              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x3B          | 59            |                           | DBQ_B2              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x3C          | 60            |                           | DBQ_B2              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x3D          | 61            | PROG DBQ B1 COEFF         | DBQ_B1              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x3E          | 62            |                           | DBQ_B1              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x3F          | 63            |                           | DBQ_B1              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x40          | 64            | PROG DBQ B0 COEFF         | DBQ_B0              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x41          | 65            |                           | DBQ_B0              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x42          | 66            |                           | DBQ_B0              |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x43          | 67            | PLL CLOCK SELECT          | RESERVED            | PLL_CLK_PHASE_INV   | SEL_PLLCLK_IN       | RESERVED             | EN_PLLCLK_IN              | SEL_SYSCLK_IN     | RESERVED           | EN_SYSCLK_IN       |                 |
| 0x44          | 68            | PLL VCO & CP              | RESERVED            |                     |                     |                      | PLL_CP_EN                 | PLL_VCO_EN        | PLL_CLKSMP_EN      | PLL_DIG_EN         |                 |
| 0x45          | 69            | PLL REGULATOR             | RESERVED            |                     |                     |                      | PLL_REG_EN                | PLL_REG_LN        | RESERVED           |                    |                 |
| 0x46          | 70            | PLL FEEDBACK DIV          | PLL_CLK_FB_DIV      |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x47          | 71            |                           | PLL_CLK_FB_DIV      |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x48          | 72            |                           | PLL_CLK_FB_DIV      |                     |                     |                      |                           |                   |                    |                    |                 |
| 0x49          | 73            |                           | PLL_CLK_IN_DIV      |                     |                     |                      |                           |                   |                    |                    |                 |



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|           |         |                   |                   |                          |                          |                |                    |              |                 |                |
|-----------|---------|-------------------|-------------------|--------------------------|--------------------------|----------------|--------------------|--------------|-----------------|----------------|
| 0x4A      | 74      |                   | PLL_CLK_OUT_DIV   |                          |                          |                | RESERVED           |              | PLL_FB_DIV_LOAD | PLL_CLK_IN_DIV |
| 0x4B      | 75      |                   | RESERVED          |                          | PLL_CLK_OUT_DIV_PHASE_EN |                | RESERVED           |              |                 |                |
| 0x4C      | 76      |                   | VCO_BAND_CTRL     |                          | RESERVED                 |                |                    |              |                 |                |
| 0x4D-0x51 | 77-81   | RESERVED          | RESERVED          |                          |                          |                |                    |              |                 |                |
| 0xE0      | 224     | INPUT FORMAT READ | RESERVED          |                          | DOP_VALID                | DAC_TDM_VALID  | INPUT_SEL_OVERRIDE |              | PLL_LOCKED      |                |
| 0xE1      | 225     | CHIP ID           | CHIP_ID           |                          |                          |                |                    |              |                 |                |
| 0xE2-0xE4 | 226-228 | RESERVED          | RESERVED          |                          |                          |                |                    |              |                 |                |
| 0xE5      | 229     | AUTO FS READ      | EN_64FS_MODE_AUTO | MCLK_128FS_HALF_DIV_AUTO | MCLK_128FS_DIV_AUTO      |                |                    |              |                 |                |
| 0xE6      | 230     | PCM VALIDITY      | RATIO_VALID       | BCK_INVALID              | WS_INVALID               | AUTO_CH_NUM    |                    |              |                 |                |
| 0xE7      | 231     | GPIO READBACK     | RESERVED          |                          |                          |                | GPIO4_R            | GPIO3_R      | GPIO2_R         | GPIO1_R        |
| 0xE8      | 232     | DAC READBACK      | SS_RAMP_DOWN_CH2  | SS_RAMP_DOWN_CH1         | SS_RAMP_UP_CH2           | SS_RAMP_UP_CH1 | AUTOMUTE_CH2       | AUTOMUTE_CH1 | VOL_MIN_CH2     | VOL_MIN_CH1    |

Table 38 - Register Map

## ES9020 Product Datasheet

### Register Listing

#### System Registers

##### Register 0: SYS CONFIG

| Bits    | [7]  | [6:4]  | [3]  | [2]  | [1]  | [0]  |
|---------|------|--------|------|------|------|------|
| Default | 1'b0 | 3'b000 | 1'b0 | 1'b1 | 1'b0 | 1'b0 |

| Bits  | Mnemonic                  | Description                                                                                                                                                                                                                                                   |
|-------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | SOFT_RESET                | Performs soft reset to digital core, resetting all registers to their power-on defaults.                                                                                                                                                                      |
| [6:4] | RESERVED                  | N/A                                                                                                                                                                                                                                                           |
| [3]   | AUTO_FS_DETECT_BLOCK_64FS | Block AUTO_FS_DETECT from transitioning to 64FS mode when the detected MCLK/MCLK_128FS ratio is 64. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                         |
| [2]   | AUTO_FS_DETECT            | Automatically determine optimal (MCLK/MCLK_128FS ratio) according to detected FS. <ul style="list-style-type: none"> <li>1'b0: Disabled, use SELECT_MCLK_128FS_NUM to set ratio.</li> <li>1'b1: Enabled, overrides SELECT_MCLK_128FS_NUM (default)</li> </ul> |
| [1]   | ENABLE_64FS_MODE          | Enables 64FS mode for high sample rates. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                    |
| [0]   | ENABLE_DAC                | Enables the DAC interpolation path. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                         |

**Register 1: DIGITAL INPUT CONFIG**

| Bits    | [7]  | [6]  | [5]  | [4]  | [3]  | [2:1] | [0]  |
|---------|------|------|------|------|------|-------|------|
| Default | 1'b0 | 1'b0 | 1'b0 | 1'b1 | 1'd0 | 2'd0  | 1'b0 |

| Bits  | Mnemonic          | Description                                                                                                                                                                                                                                 |
|-------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | ENABLE_PDM_DECODE | Enables PDM (DSD Double Rate) decoding.<br><ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul> Note: Must be set to 1'b0 when desired input is DSD                                            |
| [6]   | ENABLE_DSD_DECODE | Enables DSD decoding.<br><ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                  |
| [5]   | ENABLE_DOP_DECODE | Enables DoP decoding.<br><ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                  |
| [4]   | ENABLE_TDM_DECODE | Enables I <sup>2</sup> S/TDM decoding.<br><ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul>                                                                                                 |
| [3]   | RESERVED          | N/A                                                                                                                                                                                                                                         |
| [2:1] | INPUT_SEL         | Selects input data format when AUTO_INPUT_SEL is disabled.<br><ul style="list-style-type: none"> <li>2'd0: PCM/TDM (default)</li> <li>2'd1: DSD/PDM</li> <li>2'd2: DoP</li> <li>2'd3: Reserved</li> </ul>                                   |
| [0]   | AUTO_INPUT_SEL    | Automatic input data selection config.<br><ul style="list-style-type: none"> <li>1'b0: Disables auto input select. Input data format is set by INPUT_SEL (default)</li> <li>1'b1: Automatically determine the input data format.</li> </ul> |

**Register 2: CLOCK CONTROL 1**

| Bits    | [7]  | [6]  | [5:0] |
|---------|------|------|-------|
| Default | 1'd0 | 1'b0 | 6'd3  |

| Bits  | Mnemonic            | Description                                                                                                                                                                                                               |
|-------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | RESERVED            | N/A                                                                                                                                                                                                                       |
| [6]   | MCLK_128FS_HALF_DIV | <ul style="list-style-type: none"> <li>1'b0: Divide by MCLK_128FS_DIV + 1 (default)</li> <li>1'b1: Divide by half of MCLK_128FS_DIV + 1</li> </ul> Note: Can only produce half of an odd number divide                    |
| [5:0] | MCLK_128FS_DIV      | Whole number divide value + 1 for MCLK_128FS (MCLK/divide_value).<br><ul style="list-style-type: none"> <li>6'd0: Whole number divide value + 1 = 1</li> <li>6'd3: Whole number divide value + 1 = 4 (default)</li> </ul> |

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### Register 3: CLOCK CONTROL 2

| Bits    | [7:4] | [3:2] | [1]  | [0]  |
|---------|-------|-------|------|------|
| Default | 4'd0  | 2'b11 | 1'b0 | 1'b0 |

| Bits  | Mnemonic      | Description                                                                                                                                                                                                                                                                                           |
|-------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | RESERVED      | N/A                                                                                                                                                                                                                                                                                                   |
| [3:2] | MCLK_RATE_SEL | Sets the frequency of MCLK, allowing controls to automatically scale between MCLK rates. <ul style="list-style-type: none"> <li>2'b00: 5.6448MHz / 6.144MHz</li> <li>2'b01: 11.2896MHz / 12.288MHz</li> <li>2'b10: 22.5792MHz / 24.576MHz</li> <li>2'b11: 45.1584MHz / 49.152MHz (default)</li> </ul> |
| [1]   | DAC_CLK_INV   | Inverts the phase of the analog DAC_CLK. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul>                                                                                                                                                       |
| [0]   | RESERVED      | N/A                                                                                                                                                                                                                                                                                                   |

### Register 4: PCM MASTER CLK CONFIG

| Bits    | [7:0] |
|---------|-------|
| Default | 8'd7  |

| Bits  | Mnemonic       | Description                                                                                                                |
|-------|----------------|----------------------------------------------------------------------------------------------------------------------------|
| [7:0] | MASTER_BCK_DIV | Master mode DCLK and WS generation clock divider.<br>Whole number divide value + 1 for CLK_BCK_WS_GEN (MCLK/divide_value). |

**Register 5: MASTER MODE CONFIG**

| Bits    | [7]  | [6:5] | [4]  | [3]  | [2]  | [1]  | [0]  |
|---------|------|-------|------|------|------|------|------|
| Default | 1'b0 | 2'b01 | 1'b0 | 1'b0 | 1'b1 | 1'b0 | 1'b0 |

| Bits  | Mnemonic             | Description                                                                                                                                                                                                   |
|-------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | SLAVE_BCK_INVERT     | <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Invert BCK input</li> </ul>                                                                                                |
| [6:5] | RESERVED             | N/A                                                                                                                                                                                                           |
| [4]   | MASTER_WS_PULSE_MODE | When enabled, master WS is a 1 BCK pulse signal instead of a 50% duty cycle signal. <ul style="list-style-type: none"> <li>1'b0: 50% duty cycle WS signal (default)</li> <li>1'b1: Pulse WS signal</li> </ul> |
| [3]   | MASTER_WS_INVERT     | Inverts master WS. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul>                                                                                     |
| [2]   | MASTER_BCK_INVERT    | Inverts master BCK. <ul style="list-style-type: none"> <li>1'b0: Non-inverted</li> <li>1'b1: Inverted (default)</li> </ul>                                                                                    |
| [1]   | DSD_MASTER_MODE_EN   | DSD master mode config. <ul style="list-style-type: none"> <li>1'b0: DSD slave mode (default)</li> <li>1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK</li> </ul>                                        |
| [0]   | PCM_MASTER_MODE_EN   | Enables I <sup>2</sup> S/TDM master mode and generates master BCK and master WS. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul>                            |

**Register 6: TDM CONFIG 1**

| Bits    | [7]  | [6]  | [5]  | [4:0] |
|---------|------|------|------|-------|
| Default | 1'b0 | 1'b0 | 1'b0 | 5'd1  |

| Bits  | Mnemonic       | Description                                                                                                                                                                                        |
|-------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | TDM_RESYNC     | Force TDM encoder & decoder to resync. <ul style="list-style-type: none"> <li>1'b0: Enable TDM codec synchronization (default)</li> <li>1'b1: Force TDM codec to desynchronize.</li> </ul>         |
| [6]   | AUTO_CH_DETECT | <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Auto detect BCK/FRAME ratio to determine the number of TDM channels</li> </ul> Note: Only active in TDM slave mode. |
| [5]   | RESERVED       | N/A                                                                                                                                                                                                |
| [4:0] | TDM_CH_NUM     | Sets number of channels in each frame. <ul style="list-style-type: none"> <li>5'd0: 1 channel</li> <li>5'd1: 2 channels (default)</li> <li>5'd31: 32 channels</li> </ul>                           |

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### Register 7: TDM CONFIG 2

| Bits    | [7]  | [6]  | [5:4] | [3:2] | [1]  | [0]  |
|---------|------|------|-------|-------|------|------|
| Default | 1'b1 | 1'b1 | 2'b00 | 2'b00 | 1'b0 | 1'b0 |

| Bits  | Mnemonic           | Description                                                                                                                                                                                                                               |
|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | ENABLE_WS_MONITOR  | Enable WS monitor, used to detect the validity of the WS signal. WS is considered invalid if BCK/WS > 1024. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul>                             |
| [6]   | ENABLE_BCK_MONITOR | Enable BCK monitor, used to detect the validity of the BCK signal. BCK is considered invalid if MCLK/BCK > 256. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul>                         |
| [5:4] | TDM_WORD_WIDTH     | Sets the width, in bits, of one data word / subframe. A subframe is a frame divided by the number of channels. <ul style="list-style-type: none"> <li>2'b00: 32-bits (default)</li> <li>2'b01: 24-bits</li> <li>2'b10: 16-bits</li> </ul> |
| [3:2] | TDM_BIT_DEPTH      | Sets the bit depth, number of data bits, in one data word / subframe. <ul style="list-style-type: none"> <li>2'b00: 32-bit (default)</li> <li>2'b01: 24-bit</li> <li>2'b10: 16-bit</li> </ul>                                             |
| [1]   | TDM_VALID_EDGE     | Sets which WS edge the frame starts on. <ul style="list-style-type: none"> <li>1'b0: Frame starts on negedge of WS (default)</li> <li>1'b1: Frame starts on posedge of WS</li> </ul>                                                      |
| [0]   | TDM_LJ             | Sets left-justified mode. <ul style="list-style-type: none"> <li>1'b0: One BCK period delay (default)</li> <li>1'b1: Left-justified</li> </ul>                                                                                            |

**Register 8: CH1 INPUT CONFIG**

| Bits    | [7]  | [6]  | [5]  | [4:0] |
|---------|------|------|------|-------|
| Default | 1'b1 | 1'b0 | 1'b0 | 5'd0  |

| Bits  | Mnemonic         | Description                                                                                                                                                                                                   |
|-------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | PDM_SAMPLE_EDGE  | Sets the edge of PDM_CLK where the PDM sample increments. <ul style="list-style-type: none"> <li>1'b0: Rising edge</li> <li>1'b1: Falling edge (default)</li> </ul>                                           |
| [6]   | PDM_PHASE        | <ul style="list-style-type: none"> <li>1'b0: CH1 on the rising edge of PDM clock, CH2 on the falling edge (default)</li> <li>1'b1: CH2 on the rising edge of PDM clock, CH1 on the falling edge</li> </ul>    |
| [5]   | DSD_LINE_SEL_CH1 | Selects the source for the CH1 DSD data. <ul style="list-style-type: none"> <li>1'b0: DATA1 (default)</li> <li>1'b1: DATA2</li> </ul>                                                                         |
| [4:0] | TDM_SLOT_SEL_CH1 | Selects which TDM channel slot is latched into CH1. <ul style="list-style-type: none"> <li>5'd0: Slot 1 (default)</li> <li>5'd1: Slot 2</li> <li>5'd2: Slot 3</li> <li>...</li> <li>5'd31: Slot 32</li> </ul> |

**Register 9: CH2 INPUT CONFIG**

| Bits    | [7]  | [6]  | [5]  | [4:0] |
|---------|------|------|------|-------|
| Default | 1'b0 | 1'b0 | 1'b1 | 5'd1  |

| Bits  | Mnemonic         | Description                                                                                                                                                                                                   |
|-------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | PDM_2X_GAIN_EN   | Sets the overall gain of the PDM datapath. <ul style="list-style-type: none"> <li>1'b0: 1x gain (default)</li> <li>1'b1: 2x gain</li> </ul>                                                                   |
| [6]   | RESERVED         | N/A                                                                                                                                                                                                           |
| [5]   | DSD_LINE_SEL_CH2 | Selects the source for the CH2 DSD data. <ul style="list-style-type: none"> <li>1'b0: DATA1</li> <li>1'b1: DATA2 (default)</li> </ul>                                                                         |
| [4:0] | TDM_SLOT_SEL_CH2 | Selects which TDM channel slot is latched into CH2. <ul style="list-style-type: none"> <li>5'd0: Slot 1</li> <li>5'd1: Slot 2 (default)</li> <li>5'd2: Slot 3</li> <li>...</li> <li>5'd31: Slot 32</li> </ul> |

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### Register 10: TDM DAISY CHAIN

| Bits    | [7]  | [6:5] | [4:0] |
|---------|------|-------|-------|
| Default | 1'b0 | 2'd0  | 5'd0  |

| Bits  | Mnemonic           | Description                                                                                                                                                                                                       |
|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | TDM_DAISY_CHAIN    | TDM daisy chain mode. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                           |
| [6:5] | RESERVED           |                                                                                                                                                                                                                   |
| [4:0] | TDM_DATA_LATCH_ADJ | Adjusts the position of the MSB within each TDM slot by TDM_DATA_LATCH_ADJ clock cycles. <ul style="list-style-type: none"> <li>5'd0: Normal position</li> <li>5'd1-31: Number of clock cycles to wait</li> </ul> |

### Register 22-11: RESERVED

## GPIO Registers

### Register 23: GPIO1/2 CONFIG

| Bits    | [7:4] | [3:0] |
|---------|-------|-------|
| Default | 4'd0  | 4'd6  |

| Bits  | Mnemonic  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | GPIO2_CFG | Configure GPIO2 functionality. <ul style="list-style-type: none"> <li>4'd0: Analog outputs off – shutdown (default)</li> <li>4'd1: Output 0 – output</li> <li>4'd2: Output 1 – output</li> <li>4'd3: Reserved</li> <li>4'd4: PLL locked flag – output</li> <li>4'd5: DAC Minimum Volume flag – output</li> <li>4'd6: DAC Automute status – output</li> <li>4'd7: DAC Soft Ramp Done flag – output</li> <li>4'd8: Mute all channels – input</li> <li>4'd9: DAC Mode control – input</li> <li>4'd10: Reserved</li> <li>4'd11: BCK/WS monitor – output</li> <li>4'd12: Reserved</li> <li>4'd13: Reserved</li> <li>4'd14: Reserved</li> <li>4'd15: MCLK_128FS – output</li> </ul> |
| [3:0] | GPIO1_CFG | Configure GPIO1 functionality. <ul style="list-style-type: none"> <li>4'd0: Analog outputs off – shutdown</li> <li>4'd1: Output 0 – output</li> <li>4'd2: Output 1 – output</li> <li>4'd3: Reserved</li> <li>4'd4: PLL locked flag – output</li> <li>4'd5: DAC Minimum Volume flag – output</li> <li>4'd6: DAC Automute status – output (default)</li> <li>4'd7: DAC Soft Ramp Done flag – output</li> <li>4'd8: Mute all channels – input</li> <li>4'd9: DAC Mode control – input</li> <li>4'd10: Reserved</li> <li>4'd11: BCK/WS monitor – output</li> <li>4'd12: Reserved</li> <li>4'd13: Reserved</li> <li>4'd14: Reserved</li> <li>4'd15: MCLK_128FS – output</li> </ul> |

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### Register 24: GPIO3/4 CONFIG

| Bits    | [7:4] | [3:0] |
|---------|-------|-------|
| Default | 4'd0  | 4'd0  |

| Bits  | Mnemonic  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | GPIO4_CFG | Configure GPIO4 functionality. <ul style="list-style-type: none"> <li>• 4'd0: Analog outputs off – shutdown (default)</li> <li>• 4'd1: Output 0 – output</li> <li>• 4'd2: Output 1 – output</li> <li>• 4'd3: Reserved</li> <li>• 4'd4: PLL locked flag – output</li> <li>• 4'd5: DAC Minimum Volume flag – output</li> <li>• 4'd6: DAC Automute status – output</li> <li>• 4'd7: DAC Soft Ramp Done flag – output</li> <li>• 4'd8: Mute all channels – input</li> <li>• 4'd9: DAC Mode control – input</li> <li>• 4'd10: Reserved</li> <li>• 4'd11: BCK/WS monitor – output</li> <li>• 4'd12: Reserved</li> <li>• 4'd13: Reserved</li> <li>• 4'd14: Reserved</li> <li>• 4'd15: MCLK_128FS – output</li> </ul> |
| [3:0] | GPIO3_CFG | Configure GPIO3 functionality. <ul style="list-style-type: none"> <li>• 4'd0: Analog outputs off – shutdown (default)</li> <li>• 4'd1: Output 0 – output</li> <li>• 4'd2: Output 1 – output</li> <li>• 4'd3: Reserved</li> <li>• 4'd4: PLL locked flag – output</li> <li>• 4'd5: DAC Minimum Volume flag – output</li> <li>• 4'd6: DAC Automute status – output</li> <li>• 4'd7: DAC Soft Ramp Done flag – output</li> <li>• 4'd8: Mute all channels – input</li> <li>• 4'd9: DAC Mode control – input</li> <li>• 4'd10: Reserved</li> <li>• 4'd11: BCK/WS monitor – output</li> <li>• 4'd12: Reserved</li> <li>• 4'd13: Reserved</li> <li>• 4'd14: Reserved</li> <li>• 4'd15: MCLK_128FS – output</li> </ul> |

**Register 25: GPIO INPUT OUTPUT CONTROL**

| Bits    | [7]  | [6]  | [5]  | [4]  | [3]  | [2]  | [1]  | [0]  |
|---------|------|------|------|------|------|------|------|------|
| Default | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b1 |

| Bits | Mnemonic  | Description                                                                                                               |
|------|-----------|---------------------------------------------------------------------------------------------------------------------------|
| [7]  | GPIO4_SDB | <ul style="list-style-type: none"> <li>1'b0: Disables GPIO4 input (default)</li> <li>1'b1: Enables GPIO4 input</li> </ul> |
| [6]  | GPIO3_SDB | <ul style="list-style-type: none"> <li>1'b0: Disables GPIO3 input (default)</li> <li>1'b1: Enables GPIO3 input</li> </ul> |
| [5]  | GPIO2_SDB | <ul style="list-style-type: none"> <li>1'b0: Disables GPIO2 input (default)</li> <li>1'b1: Enables GPIO2 input</li> </ul> |
| [4]  | GPIO1_SDB | <ul style="list-style-type: none"> <li>1'b0: Disables GPIO1 input (default)</li> <li>1'b1: Enables GPIO1 input</li> </ul> |
| [3]  | GPIO4_OE  | <ul style="list-style-type: none"> <li>1'b0: Tristate GPIO4 (default)</li> <li>1'b1: GPIO4 Output enabled</li> </ul>      |
| [2]  | GPIO3_OE  | <ul style="list-style-type: none"> <li>1'b0: Tristate GPIO3 (default)</li> <li>1'b1: GPIO3 Output enabled</li> </ul>      |
| [1]  | GPIO2_OE  | <ul style="list-style-type: none"> <li>1'b0: Tristate GPIO2 (default)</li> <li>1'b1: GPIO2 Output enabled</li> </ul>      |
| [0]  | GPIO1_OE  | <ul style="list-style-type: none"> <li>1'b0: Tristate GPIO1 (default)</li> <li>1'b1: GPIO1 Output enabled</li> </ul>      |

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### Register 26: GPIO CONTROL

| Bits    | [7]  | [6]  | [5]  | [4]  | [3]  | [2]  | [1]  | [0]  |
|---------|------|------|------|------|------|------|------|------|
| Default | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

| Bits | Mnemonic    | Description                                                                                                                               |
|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| [7]  | GPIO4_INV   | Invert the GPIO2 input and output. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul> |
| [6]  | GPIO3_INV   | Invert the GPIO1 input and output. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul> |
| [5]  | GPIO2_INV   | Invert the GPIO2 input and output. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul> |
| [4]  | GPIO1_INV   | Invert the GPIO1 input and output. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul> |
| [3]  | GPIO4_WK_EN | <ul style="list-style-type: none"> <li>1'b0: GPIO4 weak keeper disabled (default)</li> <li>1'b1: GPIO4 weak keeper enabled</li> </ul>     |
| [2]  | GPIO3_WK_EN | <ul style="list-style-type: none"> <li>1'b0: GPIO3 weak keeper disabled (default)</li> <li>1'b1: GPIO3 weak keeper enabled</li> </ul>     |
| [1]  | GPIO2_WK_EN | <ul style="list-style-type: none"> <li>1'b0: GPIO2 weak keeper disabled (default)</li> <li>1'b1: GPIO2 weak keeper enabled</li> </ul>     |
| [0]  | GPIO1_WK_EN | <ul style="list-style-type: none"> <li>1'b0: GPIO1 weak keeper disabled (default)</li> <li>1'b1: GPIO1 weak keeper enabled</li> </ul>     |

**Register 27: GPIO READ CONTROL**

| Bits    | [7:5] | [4]  | [3]  | [2]  | [1]  | [0]  |
|---------|-------|------|------|------|------|------|
| Default | 3'd0  | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

| Bits  | Mnemonic      | Description                                                                                                                                                                                                                                                                        |
|-------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:5] | RESERVED      | N/A                                                                                                                                                                                                                                                                                |
| [4]   | GPIO_DAC_MODE | When any GPIO_CFG is "System mode control": <ul style="list-style-type: none"> <li>1'b0: Disable datapath when GPIO input is 1'b1</li> <li>1'b1: Enable datapath when GPIO input is 1'b1</li> </ul> When GPIOx input is 1'b0, system mode is determined by register 0[1] DAC_MODE. |
| [3]   | GPIO4_READ    | Enables readback of the GPIO4 input. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                                             |
| [2]   | GPIO3_READ    | Enables readback of the GPIO3 input. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                                             |
| [1]   | GPIO2_READ    | Enables readback of the GPIO2 input. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                                             |
| [0]   | GPIO1_READ    | Enables readback of the GPIO1 input. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                                             |

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### Register 28: GPIO OUTPUT LOGIC

| Bits    | [7]  | [6]  | [5]  | [4]  | [3]  | [2]  | [1]  | [0]  |
|---------|------|------|------|------|------|------|------|------|
| Default | 1'd0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b1 | 1'b1 | 1'b1 |

| Bits | Mnemonic          | Description                                                                                                                                                                                                                                                                    |
|------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]  | RESERVED          | N/A                                                                                                                                                                                                                                                                            |
| [6]  | FLAG_CH_SEL       | Outputs a specific channel's flag if the corresponding GPIO_AND and GPIO_OR are not set. <ul style="list-style-type: none"> <li>1'b0: Outputs status/flag from CH1</li> <li>1'b1: Outputs status/flag from CH2</li> </ul>                                                      |
| [5]  | GPIO_OR_SS_RAMP   | Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise OR of both channel's flags. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled, GPIO_CFG output is  (ss_full_ramp[CHx])</li> </ul>                                           |
| [4]  | GPIO_OR_AUTOMUTE  | Sets the GPIO_CFG "Automute Status" output as the bitwise OR of both channel's statuses. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled, GPIO_CFG output is  (automute[CHx])</li> </ul>                                                |
| [3]  | GPIO_OR_VOL_MIN   | Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise OR of both channel's flags. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled, GPIO_CFG output is  (vol_min[CHx])</li> </ul>                                                |
| [2]  | GPIO_AND_SS_RAMP  | Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise AND of both channel's flags. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled, GPIO_CFG output is &amp;(ss_full_ramp[CHx]) (default)</li> </ul> Note: Overridden by GPIO_OR_SS_RAMP. |
| [1]  | GPIO_AND_AUTOMUTE | Sets the GPIO_CFG "Automute Status" output as the bitwise AND of both channel's statuses. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled, GPIO_CFG output is &amp;(automute[CHx]) (default)</li> </ul> Note: Overridden by GPIO_OR_AUTOMUTE.     |
| [0]  | GPIO_AND_VOL_MIN  | Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise AND of both channel's flags. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled, GPIO_CFG output is &amp;(vol_min[CHx]) (default)</li> </ul> Note: Overridden by GPIO_OR_VOL_MIN.      |

## DAC Registers

### Register 29: RESERVED

### Register 30: DAC FILTER CONFIG

| Bits    | [7:6] | [5]  | [4:3] | [2:0] |
|---------|-------|------|-------|-------|
| Default | 2'd0  | 1'b0 | 2'b00 | 3'd0  |

| Bits  | Mnemonic     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:6] | RESERVED     | N/A                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| [5]   | BYPASS_IIR   | Bypass the IIR filter. <ul style="list-style-type: none"> <li>1'b0: Non-bypassed (default)</li> <li>1'b1: Bypassed</li> </ul>                                                                                                                                                                                                                                                                                                                                               |
| [4:3] | BYPASS_FIR   | Bypass the 8X FIR filter. <ul style="list-style-type: none"> <li>2'b00: Non-bypassed (default)</li> <li>2'b11: Bypassed</li> <li>Others: Reserved</li> <li>Others: Reserved</li> </ul>                                                                                                                                                                                                                                                                                      |
| [2:0] | FILTER_SHAPE | Selects the 8x interpolation FIR filter shape. <ul style="list-style-type: none"> <li>3'd0: Minimum phase (default)</li> <li>3'd1: Linear phase fast roll-off apodizing</li> <li>3'd2: Linear phase fast roll-off</li> <li>3'd3: Linear phase fast roll-off low ripple</li> <li>3'd4: Linear phase slow roll-off</li> <li>3'd5: Minimum phase fast roll-off</li> <li>3'd6: Minimum phase slow roll-off</li> <li>3'd7: Minimum phase slow roll-off low dispersion</li> </ul> |

### Register 31: VOLUME CH1

| Bits    | [7:0] |
|---------|-------|
| Default | 8'h02 |

| Bits  | Mnemonic   | Description                                                                                                                                                                         |
|-------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | VOLUME_CH1 | DAC CH1 volume. +1dB to -126dB, 0.5dB steps <ul style="list-style-type: none"> <li>8'h00: +1dB</li> <li>8'h02: 0dB (default)</li> <li>8'hFE: -126dB</li> <li>8'hFF: Mute</li> </ul> |

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### Register 32: VOLUME CH2

| Bits    | [7:0] |
|---------|-------|
| Default | 8'h02 |

| Bits  | Mnemonic   | Description                                                                                                                                                                         |
|-------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | VOLUME_CH2 | DAC CH2 volume. +1dB to -126dB, 0.5dB steps <ul style="list-style-type: none"> <li>8'h00: +1dB</li> <li>8'h02: 0dB (default)</li> <li>8'hFE: -126dB</li> <li>8'hFF: Mute</li> </ul> |

### Register 33: MUTE AND VOL PHASE

| Bits    | [7:4] | [3]  | [2]  | [1]  | [0]  |
|---------|-------|------|------|------|------|
| Default | 4'd0  | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

| Bits  | Mnemonic          | Description                                                                                                                                 |
|-------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | RESERVED          | N/A                                                                                                                                         |
| [3]   | MUTE_CH2          | Mutes the CH2 datapath. <ul style="list-style-type: none"> <li>1'b0: Normal CH2 operation (default)</li> <li>1'b1: Mute CH2</li> </ul>      |
| [2]   | MUTE_CH1          | Mutes the CH1 datapath. <ul style="list-style-type: none"> <li>1'b0: Normal CH1 operation (default)</li> <li>1'b1: Mute CH1</li> </ul>      |
| [1]   | VOL_PHASE_INV_CH2 | Inverts the phase of DAC_VOLUME_CH2. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul> |
| [0]   | VOL_PHASE_INV_CH1 | Inverts the phase of DAC_VOLUME_CH1. <ul style="list-style-type: none"> <li>1'b0: Non-inverted (default)</li> <li>1'b1: Inverted</li> </ul> |

**Register 34: SOFT RAMP CONFIG**

| Bits    | [7]  | [6]  | [5]  | [4:0] |
|---------|------|------|------|-------|
| Default | 1'b0 | 1'd0 | 1'b1 | 5'd3  |

| Bits  | Mnemonic            | Description                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | MONO_VOLUME         | All channel volumes controlled by the CH1 volume control. <ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                                                                                                                                                 |
| [6]   | RESERVED            | N/A                                                                                                                                                                                                                                                                                                         |
| [5]   | MUTE_RAMP_TO_GROUND | <ul style="list-style-type: none"> <li>1'b0: When ramped to min volume during normal mute, do not soft ramp to ground</li> <li>1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default)</li> </ul> normal mute includes: automute, mute by register, mute by GPIO |
| [4:0] | SOFT_RAMP_TIME      | Sets the amount of time that it takes to perform a soft start ramp.<br>This time affects both ramp to ground and ramp to AVCC/2.<br>Valid from 0 to 12. $\text{Time [s]} = \frac{2^{15+\text{SOFT\_RAMP\_TIME}}}{\text{MCLK} \cdot 2^{\text{MCLK\_RATE\_SEL}}}$                                             |

**Register 35: VOLUME UP RAMP RATE**

| Bits    | [7:0] |
|---------|-------|
| Default | 8'h04 |

| Bits  | Mnemonic         | Description                                                                                                                                                                                                                                                                                                                                |
|-------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | VOL_RAMP_RATE_UP | Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{ramp\_step [inc/sample]} = \frac{\text{VOL\_RAMP\_RATE\_UP}}{2^{12}}$ <ul style="list-style-type: none"> <li>8'h00: Instant change</li> <li>8'h01: Slowest change</li> <li>8'h04: Default</li> <li>8'hFF: Fastest change</li> </ul> |

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### Register 36: VOLUME DOWN RAMP RATE

| Bits    | [7:0] |
|---------|-------|
| Default | 8'h04 |

| Bits  | Mnemonic           | Description                                                                                                                                                                                                                                                                                                                                         |
|-------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | VOL_RAMP_RATE_DOWN | <p>Linear step size from current volume to target volume, represented as a fraction of full-scale.</p> $\text{ramp\_step [dec/sample]} = \frac{\text{VOL\_RAMP\_RATE\_DOWN}}{2^{12}}$ <ul style="list-style-type: none"> <li>8'h00: Instant change</li> <li>8'h01: Slowest change</li> <li>8'h04: Default</li> <li>8'hFF: Fastest change</li> </ul> |

### Register 37: DIGITAL GAIN

| Bits    | [7]  | [6:4] | [3]  | [2:0] |
|---------|------|-------|------|-------|
| Default | 1'd0 | 3'd0  | 1'd0 | 3'd0  |

| Bits  | Mnemonic         | Description                                                                                                                                       |
|-------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | RESERVED         | N/A                                                                                                                                               |
| [6:4] | DIGITAL_GAIN_CH2 | <p>DAC CH2 gain boost. +0dB to +42dB, +6dB steps.</p> <ul style="list-style-type: none"> <li>3'd0: +0dB (default)</li> <li>3'd7: +42dB</li> </ul> |
| [3]   | RESERVED         | N/A                                                                                                                                               |
| [2:0] | DIGITAL_GAIN_CH1 | <p>DAC CH1 gain boost. +0dB to +42dB, +6dB steps.</p> <ul style="list-style-type: none"> <li>3'd0: +0dB (default)</li> <li>3'd7: +42dB</li> </ul> |

### Register 38: AUTOMUTE ENABLE

| Bits    | [7:2] | [1]  | [0]  |
|---------|-------|------|------|
| Default | 6'd0  | 1'b1 | 1'b1 |

| Bits  | Mnemonic        | Description                                                                                                                    |
|-------|-----------------|--------------------------------------------------------------------------------------------------------------------------------|
| [7:2] | RESERVED        |                                                                                                                                |
| [1]   | AUTOMUTE_EN_CH2 | <p>Enables CH2 automute.</p> <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul> |
| [0]   | AUTOMUTE_EN_CH1 | <p>Enables CH1 automute.</p> <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul> |

**Register 40-39: AUTOMUTE TIME**

| Bits    | [15] | [14] | [13] | [12:11] | [10:0] |
|---------|------|------|------|---------|--------|
| Default | 1'b1 | 1'b0 | 1'b0 | 2'd0    | 11'h0F |

| Bits    | Mnemonic            | Description                                                                                                                                                                                                                                                                                                                                                                                  |
|---------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [15]    | DSD_FAULT_DETECT_EN | Sets a channel to a DSD mute pattern (0x96) if the DSD data has no changes in 64 DATA_CLKs. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul>                                                                                                                                                                                                |
| [14]    | DSD_DC_AM_ENB       | Disables the DSD automute condition, if a DC signal is detected. <ul style="list-style-type: none"> <li>1'b0: Enabled (default)</li> <li>1'b1: Disabled</li> </ul>                                                                                                                                                                                                                           |
| [13]    | DSD_MUTE_AM_ENB     | Disables the DSD automute condition, if a DSD mute pattern is detected. <ul style="list-style-type: none"> <li>1'b0: Enabled (default)</li> <li>1'b1: Disabled</li> </ul>                                                                                                                                                                                                                    |
| [12:11] | RESERVED            | N/A                                                                                                                                                                                                                                                                                                                                                                                          |
| [10:0]  | AUTOMUTE_TIME       | Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. <ul style="list-style-type: none"> <li>11'h000: Disabled</li> <li>11'h001: Slowest</li> <li>11'h00F: Default</li> <li>11'h7FF: Fastest</li> </ul> $\text{Time [s]} = \frac{2^{25}}{\text{AUTOMUTE\_TIME} \cdot \text{MCLK\_128FS} \cdot 2^{64\text{FS\_MODE}}}$ |

**Register 42-41: AUTOMUTE LEVEL**

| Bits    | [15:0]   |
|---------|----------|
| Default | 16'h0008 |

| Bits   | Mnemonic       | Description                                                                                                                                                                                                                                                                                                                        |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [15:0] | AUTOMUTE_LEVEL | The threshold which the audio must be below before an automute condition is flagged. <ul style="list-style-type: none"> <li>16'h0001: -138dB</li> <li>16'h0008: -120dB (default)</li> <li>16'hFFFF: -42dB</li> </ul> $\text{level [dB]} = 20 \cdot \log_{10} \left( \frac{\text{AUTOMUTE\_LEVEL}}{(2^{16} - 1) \cdot 2^7} \right)$ |

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### Register 44-43: AUTOMUTE OFF LEVEL

| Bits    | [15:0]   |
|---------|----------|
| Default | 16'h000A |

| Bits   | Mnemonic           | Description                                                                                                                                                                                                                                                                                                                                                 |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [15:0] | AUTOMUTE_OFF_LEVEL | <p>The threshold which the audio must be above before the automute condition is immediately cleared.</p> <ul style="list-style-type: none"> <li>16'h0001: -138dB</li> <li>16'h000A: -118dB (default)</li> <li>16'hFFFF: -42dB</li> </ul> $\text{level [dB]} = 20 \cdot \log_{10} \left( \frac{\text{AUTOMUTE\_OFF\_LEVEL}}{(2^{16} - 1) \cdot 2^7} \right)$ |

### Register 50-45: RESERVED

### Register 51: DBQ COEFF SEL

| Bits    | [7:5] | [4:0] |
|---------|-------|-------|
| Default | 3'd0  | 5'd1  |

| Bits  | Mnemonic      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:5] | RESERVED      | N/A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| [4:0] | DBQ_COEFF_SEL | <p>Select the filter coefficients used by the DBQ filter.</p> <ul style="list-style-type: none"> <li>5'd0: Use programmable coeffs</li> <li>5'd1: Bypass DBQ Filter (default)</li> <li>5'd2: 48kHz de-emphasis filter</li> <li>5'd3: 44.1kHz de-emphasis filter</li> <li>5'd4: 32kHz de-emphasis filter</li> <li>5'd5: RIAA de-emphasis filter</li> <li>5'd6: RIAA pre-emphasis filter</li> <li>5'd7: DC Blocking filter, FS = 48kHz</li> <li>5'd8: DC Blocking filter, FS = 96kHz</li> <li>5'd9: DC Blocking filter, FS = 192kHz</li> <li>5'd10: DC Blocking filter, FS = 384kHz</li> <li>5'd11: DC Blocking filter, FS = 768kHz</li> <li>5'd12: DC Blocking filter, FS = 44.1kHz</li> <li>5'd13: DC Blocking filter, FS = 88.2kHz</li> <li>5'd14: DC Blocking filter, FS = 176.4kHz</li> <li>5'd15: DC Blocking filter, FS = 352.8kHz</li> <li>5'd16: DC Blocking filter, FS = 705.6kHz</li> <li>Others: Reserved</li> </ul> |

**Register 54-52: PROG DBQ A2 COEFF**

| Bits    | [23:0]     |
|---------|------------|
| Default | 24'h000000 |

| Bits   | Mnemonic | Description                                                                                                        |
|--------|----------|--------------------------------------------------------------------------------------------------------------------|
| [23:0] | DBQ_A2   | A 24-bit signed value for the programmable DBQ filter a2 coefficient.<br>Note: Assign -1*a2 value to the register. |

**Register 57-55: PROG DBQ A1 COEFF**

| Bits    | [23:0]     |
|---------|------------|
| Default | 24'h000000 |

| Bits   | Mnemonic | Description                                                                                                        |
|--------|----------|--------------------------------------------------------------------------------------------------------------------|
| [23:0] | DBQ_A1   | A 24-bit signed value for the programmable DBQ filter a1 coefficient.<br>Note: Assign -1*a1 value to the register. |

**Register 60-58: PROG DBQ B2 COEFF**

| Bits    | [23:0]     |
|---------|------------|
| Default | 24'h000000 |

| Bits   | Mnemonic | Description                                                           |
|--------|----------|-----------------------------------------------------------------------|
| [23:0] | DBQ_B2   | A 24-bit signed value for the programmable DBQ filter b2 coefficient. |

**Register 63-61: PROG DBQ B1 COEFF**

| Bits    | [23:0]     |
|---------|------------|
| Default | 24'h000000 |

| Bits   | Mnemonic | Description                                                           |
|--------|----------|-----------------------------------------------------------------------|
| [23:0] | DBQ_B1   | A 24-bit signed value for the programmable DBQ filter b1 coefficient. |

**Register 66-64: PROG DBQ B0 COEFF**

| Bits    | [23:0]     |
|---------|------------|
| Default | 24'h000000 |

| Bits   | Mnemonic | Description                                                           |
|--------|----------|-----------------------------------------------------------------------|
| [23:0] | DBQ_B0   | A 24-bit signed value for the programmable DBQ filter b0 coefficient. |

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### PLL Registers

#### Register 67: PLL CLOCK SELECT

| Bits    | [7]  | [6]  | [5]  | [4]  | [3]  | [2]  | [1]  | [0]  |
|---------|------|------|------|------|------|------|------|------|
| Default | 1'b0 | 1'b0 | 1'b1 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b1 |

| Bits | Mnemonic          | Description                                                                                                                                                                                                                |
|------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]  | RESERVED          | N/A                                                                                                                                                                                                                        |
| [6]  | PLL_CLK_PHASE_INV | Digital/analog DAC clock invert phase enable. <ul style="list-style-type: none"> <li>1'b0: Digital/analog DAC clocks have inverted phase (default)</li> <li>1'b1: Digital/analog DAC clocks have the same phase</li> </ul> |
| [5]  | SEL_PLLCLK_IN     | Selects PLL input clock source when EN_PLLCLK_IN is set. <ul style="list-style-type: none"> <li>1'b0: ACLK</li> <li>1'b1: BCK (default)</li> </ul>                                                                         |
| [4]  | RESERVED          | N/A                                                                                                                                                                                                                        |
| [3]  | EN_PLLCLK_IN      | Allows SEL_PLLCLK_IN to select PLL input clocks. <ul style="list-style-type: none"> <li>1'b0: Disables SEL_PLLCLK_IN (default)</li> <li>1'b1: Enables SEL_PLLCLK_IN</li> </ul>                                             |
| [2]  | SEL_SYSCLK_IN     | Selects digital core clock source when EN_SYSCLK_IN is set. <ul style="list-style-type: none"> <li>1'b0: ACLK (default)</li> <li>1'b1: PLL_CLK</li> </ul>                                                                  |
| [1]  | RESERVED          | N/A                                                                                                                                                                                                                        |
| [0]  | EN_SYSCLK_IN      | Enables clock inputs to the digital core. <ul style="list-style-type: none"> <li>1'b0: Disabled</li> <li>1'b1: Enabled (default)</li> </ul>                                                                                |

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### Register 68: PLL VCO & CP

| Bits    | [7:4]   | [3]  | [2]  | [1]  | [0]  |
|---------|---------|------|------|------|------|
| Default | 4'b0011 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

| Bits  | Mnemonic      | Description                                                                                                                                                              |
|-------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | RESERVED      | N/A                                                                                                                                                                      |
| [3]   | PLL_CP_EN     | Enables/disables the PLL charge pump.<br><ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>                               |
| [2]   | PLL_VCO_EN    | Enables/disables the PLL voltage-controlled oscillator (VCO).<br><ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> </ul>       |
| [1]   | PLL_CLKSMP_EN | Power on the PLL circuitry.<br><ul style="list-style-type: none"> <li>1'b0: PLL Block disabled (default)</li> <li>1'b1: PLL Block enabled</li> </ul>                     |
| [0]   | PLL_DIG_EN    | Power on the Digital core of the PLL.<br><ul style="list-style-type: none"> <li>1'b0: PLL digital core is off (default)</li> <li>1'b1: PLL digital core is on</li> </ul> |

### Register 69: PLL REGULATOR

| Bits    | [7:4] | [3]  | [2]  | [1:0] |
|---------|-------|------|------|-------|
| Default | 4'd0  | 1'b0 | 1'b0 | 2'b10 |

| Bits  | Mnemonic   | Description                                                                                                                                                              |
|-------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | RESERVED   | N/A                                                                                                                                                                      |
| [3]   | PLL_REG_EN | Power on the PLL regulator.<br><ul style="list-style-type: none"> <li>1'b0: Disable the PLL regulator (default)</li> <li>1'b1: Enable the PLL regulator</li> </ul>       |
| [2]   | PLL_REG_LN | Select low noise reference for HV regulator.<br><ul style="list-style-type: none"> <li>1'b0: Disabled (default)</li> <li>1'b1: Enabled</li> <li>1'b1: Enabled</li> </ul> |
| [1:0] | RESERVED   | N/A                                                                                                                                                                      |

### Register 72-70: PLL FEEDBACK DIV

| Bits    | [23:0]     |
|---------|------------|
| Default | 24'h100000 |

| Bits   | Mnemonic       | Description                                                                                                                                                                                  |
|--------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [23:0] | PLL_CLK_FB_DIV | Sets the PLL clock feedback divider (Nfb).<br><ul style="list-style-type: none"> <li>24'h000000: Reserved</li> <li>24'h100000: Default</li> <li>24'hn: Divide by 2<sup>25/n</sup></li> </ul> |

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### Register 75-73: PLL IN & OUT DIV

| Bits    | [23:21] | [20] | [19:16] | [15:12] | [11:10] | [9]  | [8:0] |
|---------|---------|------|---------|---------|---------|------|-------|
| Default | 3'd0    | 1'b1 | 4'd0    | 4'd3    | 2'd0    | 1'b1 | 9'd0  |

| Bits    | Mnemonic                 | Description                                                                                                                                                                         |
|---------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [23:21] | RESERVED                 | N/A                                                                                                                                                                                 |
| [20]    | PLL_CLK_OUT_DIV_PHASE_EN | Sets the tuning mode for the PLL_CLK_OUT_DIV phase. <ul style="list-style-type: none"> <li>1'b0: Dynamic Tuning of Phase</li> <li>1'b1: Static Tuning of Phase (default)</li> </ul> |
| [19:16] | RESERVED                 | N/A                                                                                                                                                                                 |
| [15:12] | PLL_CLK_OUT_DIV          | Sets the PLL clock output divider (No). <ul style="list-style-type: none"> <li>4'd0: Reserved</li> <li>4'd3: Divide by 4. (default)</li> <li>4'dn: Divide by (n + 1).</li> </ul>    |
| [11:10] | RESERVED                 | N/A                                                                                                                                                                                 |
| [9]     | PLL_FB_DIV_LOAD          | Needs to be toggled whenever CLK_FB_DIV changes. Write 1'b1 then write 1'b0 to load CLK_FB_DIV.                                                                                     |
| [8:0]   | PLL_CLK_IN_DIV           | Sets the PLL clock input divider (Ni). <ul style="list-style-type: none"> <li>9'd0: Reserved (default)</li> <li>9'dn: Divide by (n + 1).</li> </ul>                                 |

### Register 76: PLL VCO CONTROL 1

| Bits    | [7:5]  | [4:0]    |
|---------|--------|----------|
| Default | 3'b010 | 5'b00000 |

| Bits  | Mnemonic      | Description                                                                                                                                |
|-------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| [7:5] | VCO_BAND_CTRL | Selects the frequency band of the VCO. <ul style="list-style-type: none"> <li>3'b001 (Low Speed Mode)</li> <li>3'b010 (default)</li> </ul> |
| [4:0] | RESERVED      | N/A                                                                                                                                        |

### Register 81-77: RESERVED

## Readback Registers

### Register 224: INPUT FORMAT READ

| Bits    | [7:5] | [4] | [3] | [2:1] | [0] |
|---------|-------|-----|-----|-------|-----|
| Default | -     | -   | -   | -     | -   |

| Bits  | Mnemonic           | Description                                                                                                                                                                    |
|-------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:5] | RESERVED           | N/A                                                                                                                                                                            |
| [4]   | DOP_VALID          | DoP Valid flags, per channel pair.                                                                                                                                             |
| [3]   | DAC_TDM_VALID      | TDM decoder valid flag.                                                                                                                                                        |
| [2:1] | INPUT_SEL_OVERRIDE | Readback of the current input data format. <ul style="list-style-type: none"> <li>2'd0: PCM (default)</li> <li>2'd1: DSD</li> <li>2'd2: DoP</li> <li>2'd3: Reserved</li> </ul> |
| [0]   | PLL_LOCKED         | PLL locked flag.                                                                                                                                                               |

### Register 225: CHIP ID

| Bits    | [7:0] |
|---------|-------|
| Default | 8'h00 |

| Bits  | Mnemonic | Description |
|-------|----------|-------------|
| [7:0] | CHIP_ID  |             |

## ES9020 Product Datasheet

### Register 228-226: RESERVED

### Register 229: AUTO FS READ

| Bits    | [7] | [6] | [5:0] |
|---------|-----|-----|-------|
| Default | -   | -   | -     |

| Bits  | Mnemonic                 | Description                                                                                                                                                                                                                                                |
|-------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | EN_64FS_MODE_AUTO        | Result {Z} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic, running the device in 64FS mode. <ul style="list-style-type: none"> <li>1'b0: 64FS disabled</li> <li>1'b1: 64FS enabled</li> </ul>                                          |
| [6]   | MCLK_128FS_HALF_DIV_AUTO | Result {Y} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. <ul style="list-style-type: none"> <li>1'b0: MCLK_128FS is an integer multiple of MCLK, Y = 1.</li> <li>1'b1: MCLK_128FS is a (X+1)*0.5 multiple of MCLK, Y = 2.</li> </ul> |
| [5:0] | MCLK_128FS_DIV_AUTO      | Result {X} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. $FS[Hz] = \frac{Y \cdot MCLK}{(X + 1) \cdot \left(\frac{128^Z}{2}\right)}$                                                                                                  |

### Register 230: PCM VALIDITY

| Bits    | [7] | [6] | [5] | [4:0] |
|---------|-----|-----|-----|-------|
| Default | -   | -   | -   | -     |

| Bits  | Mnemonic    | Description                                                                                                                                                                         |
|-------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | RATIO_VALID | Validity of the MCLK/MCLK_128FS ratio. ((N + 1)/M)*128 MCLK periods in a WS frame. <ul style="list-style-type: none"> <li>1'b0: Invalid ratio</li> <li>1'b1: Valid ratio</li> </ul> |
| [6]   | BCK_INVALID | Validity of the BCK signal, requires BCK_MONITOR to be enabled.                                                                                                                     |
| [5]   | WS_INVALID  | Validity of the WS signal, requires WS_MONITOR to be enabled.                                                                                                                       |
| [4:0] | AUTO_CH_NUM | Automatic TDM channel number tuning result.                                                                                                                                         |

**Register 231: GPIO READBACK**

| Bits    | [7:4] | [3] | [2] | [1] | [0] |
|---------|-------|-----|-----|-----|-----|
| Default | -     | -   | -   | -   | -   |

| Bits  | Mnemonic | Description           |
|-------|----------|-----------------------|
| [7:4] | RESERVED | N/A                   |
| [3]   | GPIO4_R  | GPIO4 input readback. |
| [2]   | GPIO3_R  | GPIO3 input readback. |
| [1]   | GPIO2_R  | GPIO2 input readback. |
| [0]   | GPIO1_R  | GPIO1 input readback. |

**Register 232: DAC READBACK**

| Bits    | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Default | -   | -   | -   | -   | -   | -   | -   | -   |

| Bits | Mnemonic         | Description                |
|------|------------------|----------------------------|
| [7]  | SS_RAMP_DOWN_CH2 | CH2 soft ramped down flag. |
| [6]  | SS_RAMP_DOWN_CH1 | CH1 soft ramped down flag. |
| [5]  | SS_RAMP_UP_CH2   | CH2 soft ramped up flag.   |
| [4]  | SS_RAMP_UP_CH1   | CH1 soft ramped up flag.   |
| [3]  | AUTOMUTE_CH2     | CH2 automute status flag.  |
| [2]  | AUTOMUTE_CH1     | CH1 automute status flag.  |
| [1]  | VOL_MIN_CH2      | CH2 minimum volume flag.   |
| [0]  | VOL_MIN_CH1      | CH1 minimum volume flag.   |

## ES9020 Product Datasheet

### ES9020 Reference Schematic

#### Hardware (HW) Mode

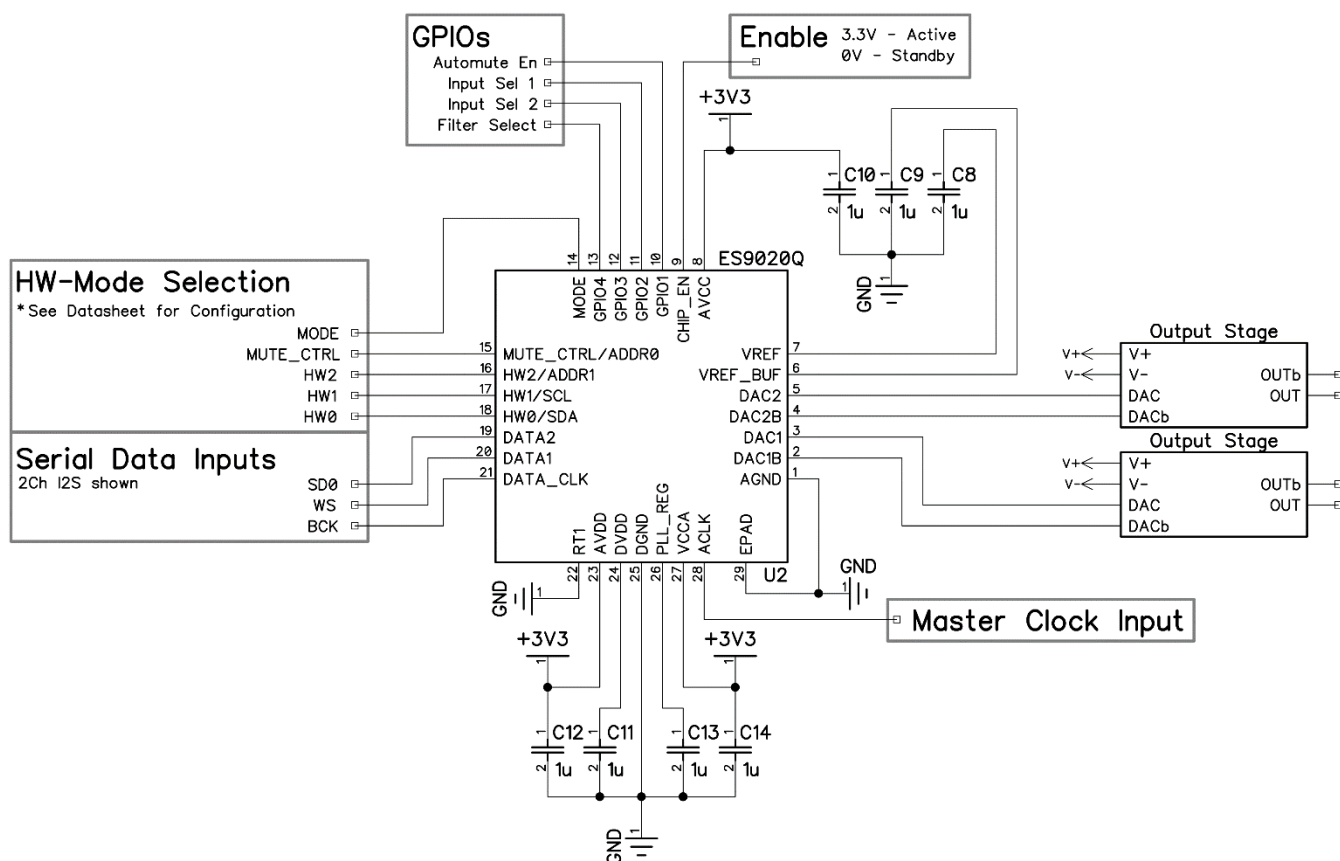


Figure 29 - ES9020 HW Mode Reference Schematic

Note: The ES9020 28QFN package has an exposed pad (Pin 29) that should be connected to ground.

## Software (SW) Mode

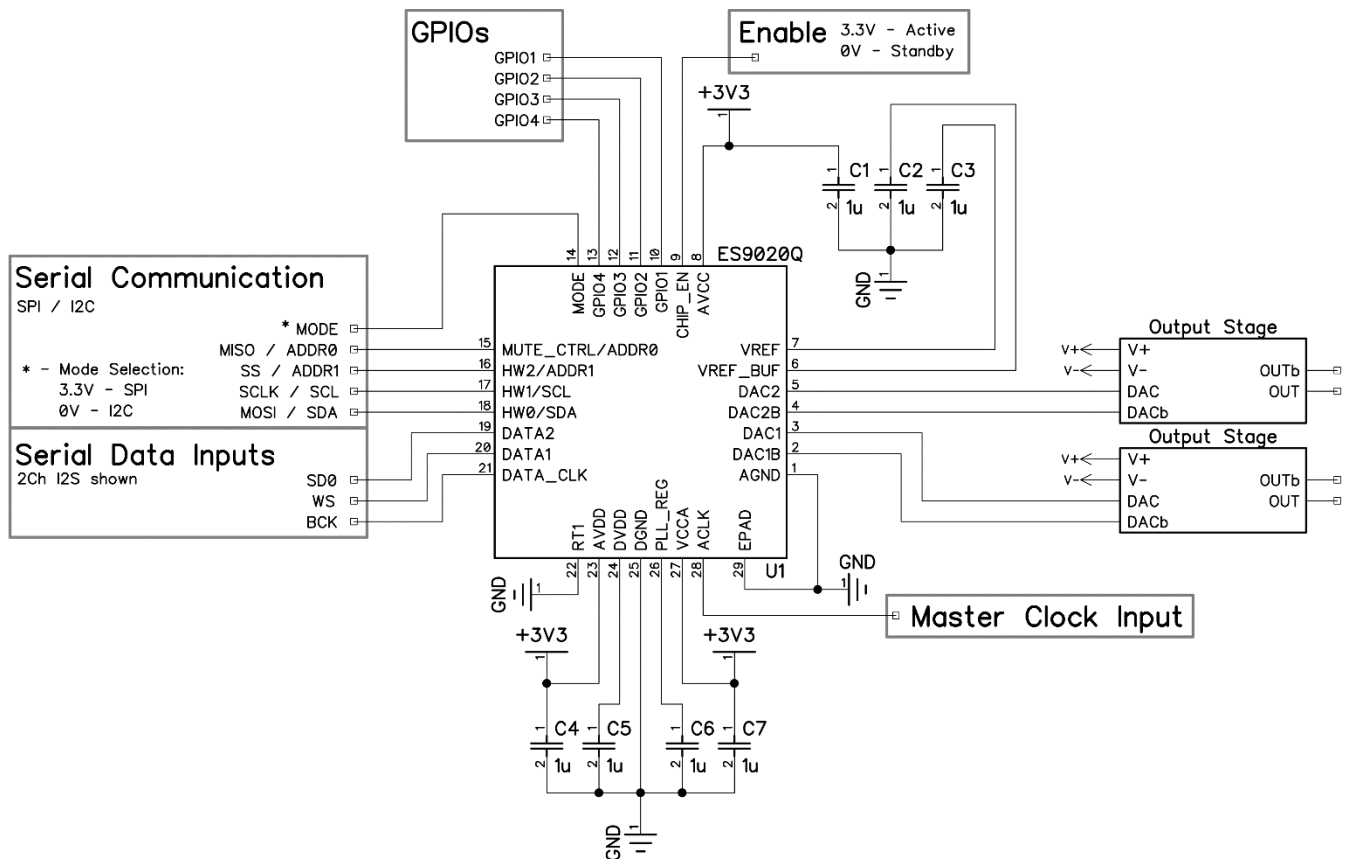


Figure 30 - ES9020 SW Mode Reference Schematic

Note: The ES9020 28QFN package has an exposed pad (Pin 29) that should be connected to ground.

## Reference Output Stage

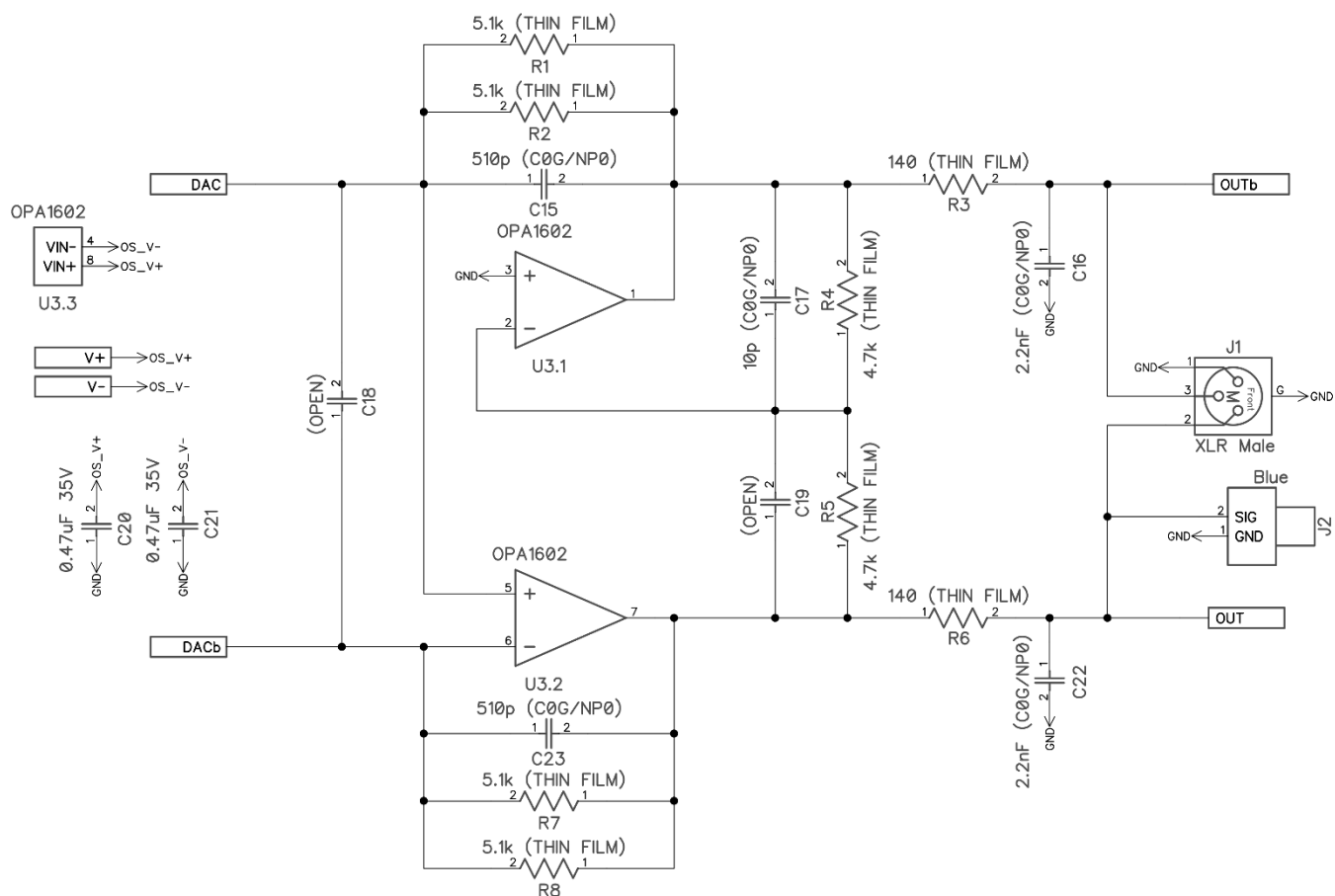


Figure 31 - ES9020 Output Stage Reference Schematic

## Recommended PCB Layout Guidelines

To maximize performance of the ES9020 ESS Technology makes the following PCB Layout recommendations:

1. Use of a 4+ layer PCB with an uninterrupted ground plane immediately beneath the chip. Both analog and digital ground signal can be connected here.
2. All bypass capacitors to be placed as close to the chip as possible while keeping clear ground paths between them and the chip's ground pins.
3. The use of multiple vias for each supply near its bypass capacitor and chip ground pin.
4. Minimize the use of vias for high-speed data and clock lines and avoid routing them near or directly underneath the analog output signals.
5. Ensure the package pad is connected to ground plane on the back side of the PCB with multiple vias for heat dissipation.

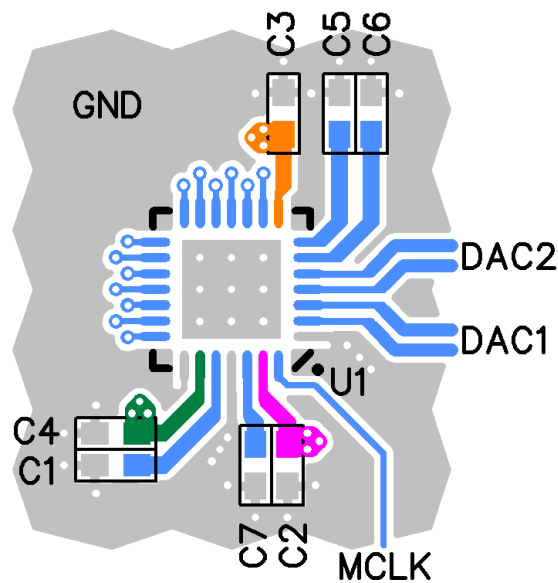
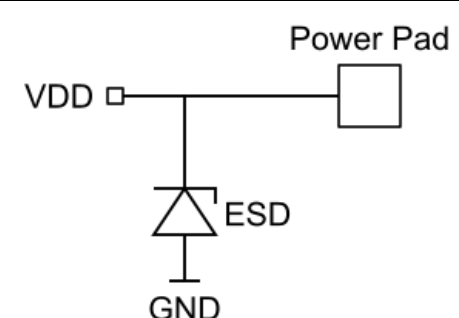
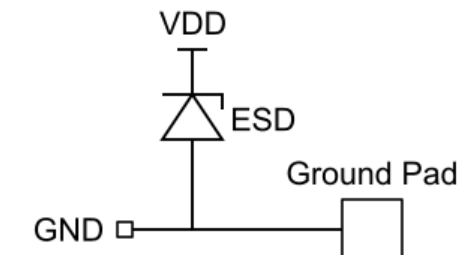
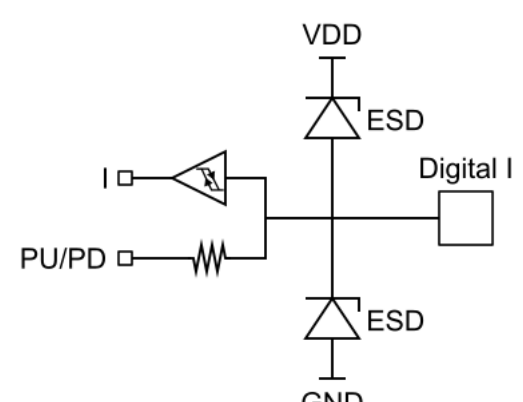
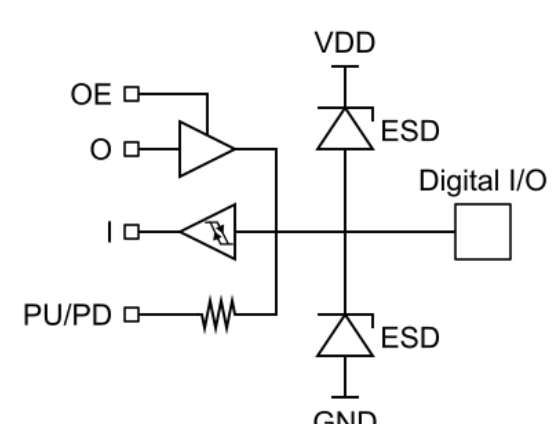


Figure 32 - ES9020 Recommended PCB Layout Guidelines

## Internal Pad Circuitry

| Pin Name                                                                                                                                                   | Pin                                                                        | Type        | Equivalent Circuit                                                                   |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|-------------|--------------------------------------------------------------------------------------|
| AVCC<br>AVDD<br>VCCA                                                                                                                                       | 8<br>23<br>27                                                              | Power       |    |
| AGND<br>DGND                                                                                                                                               | 1<br>25                                                                    | Ground      |    |
| CHIP_EN                                                                                                                                                    | 9                                                                          | Reset       |   |
| GPIO1<br>GPIO2<br>GPIO3<br>GPIO4<br>MODE<br>MISO/ADDR0/MUTE_MCLK_CTRL<br>SS/ADDR1/HW2<br>SCLK/SCL/HW1<br>MOSI/SDA/HW0<br>DATA2<br>DATA1<br>DATA_CLK<br>RT1 | 10<br>11<br>12<br>13<br>14<br>15<br>16<br>17<br>18<br>19<br>20<br>21<br>22 | Digital I/O |  |

# ES9020 Product Datasheet

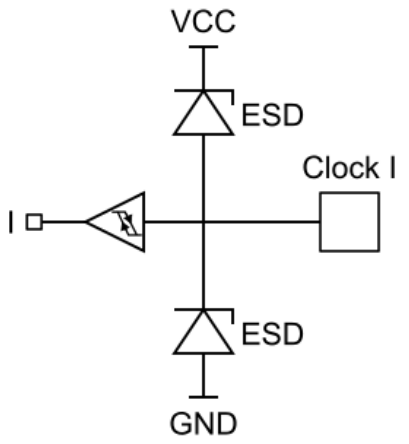
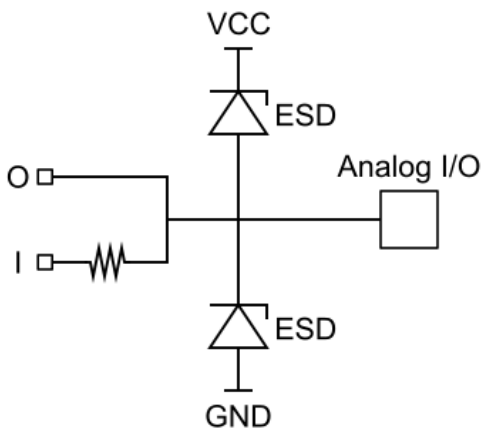
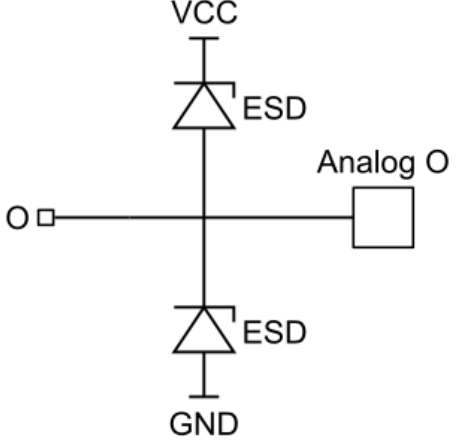
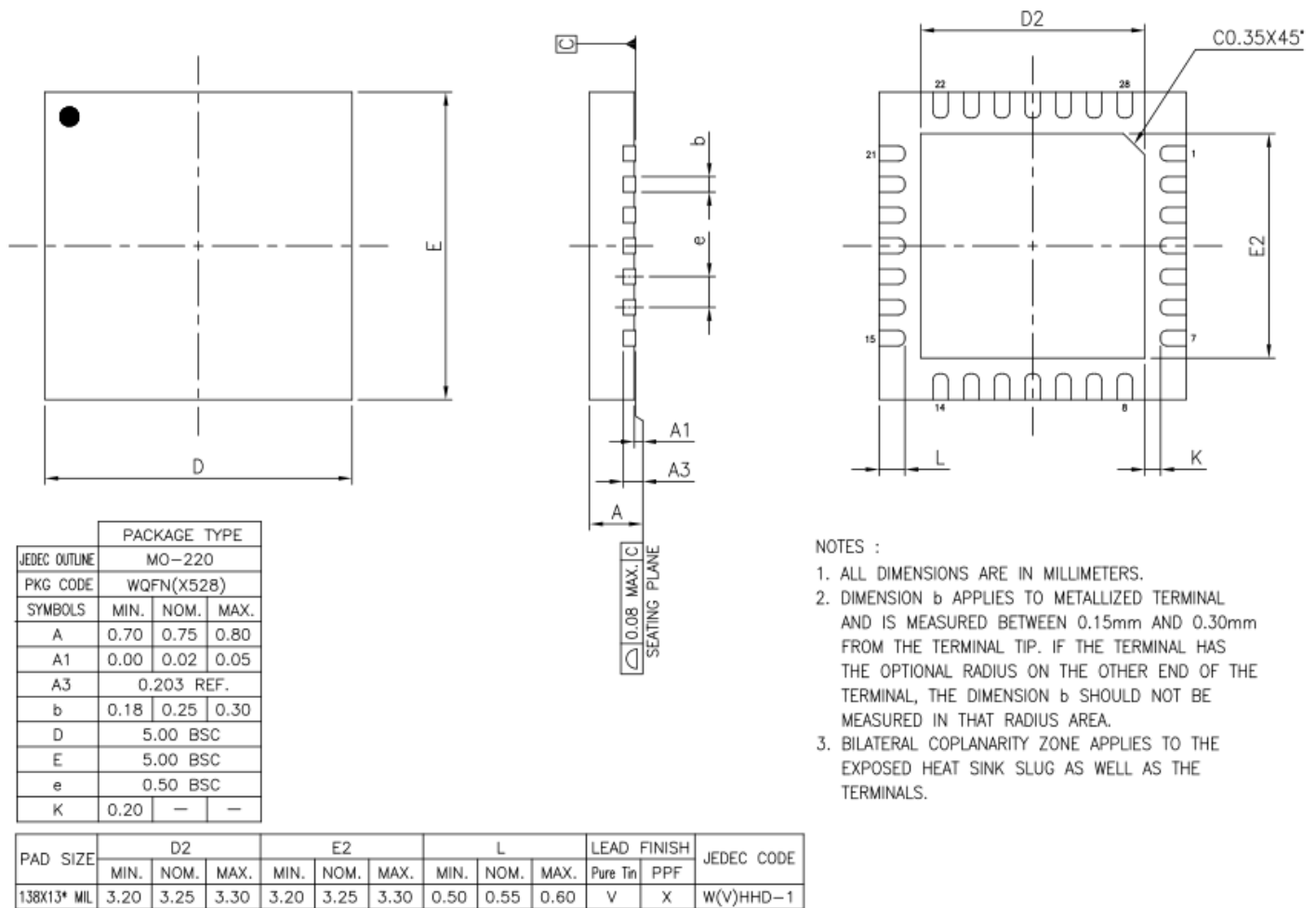
|                                     |                    |            |                                                                                      |
|-------------------------------------|--------------------|------------|--------------------------------------------------------------------------------------|
| ACLK                                | 28                 | Clock I    |   |
| DAC1B<br>DAC1<br>DAC2B<br>DAC2      | 2<br>3<br>4<br>5   | Analog I/O |   |
| VREF_BUF<br>VREF<br>DVDD<br>PLL_REG | 6<br>7<br>24<br>26 | Analog O   |  |

Table 39 - Internal Pad Circuitry

# ES9020 Product Datasheet

## 28 QFN Package Dimensions

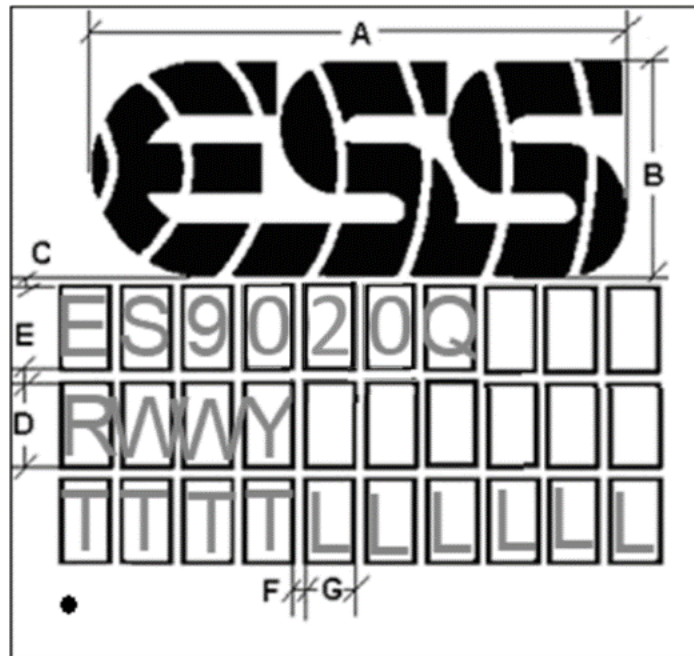


### NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 33 - ES9020 QFN Package Dimensions

## 28 QFN Top View Marking



|               | Dimension in mm |     |     |     |     |     |     |
|---------------|-----------------|-----|-----|-----|-----|-----|-----|
| Package Type  | A               | B   | C   | D   | E   | F   | G   |
| QFN 5mm x 5mm | 4.0             | 1.6 | 0.2 | 0.4 | 0.2 | 0.1 | 0.3 |

|   |                    |
|---|--------------------|
| T | Tracking number    |
| W | Work week          |
| Y | Last digit of year |
| L | Lot number         |
| R | Silicon Revision   |

Marking is subject to change. This drawing is not to scale.

Figure 34 - ES9020 28 QFN Top View Markings

## ES9020 Product Datasheet

### Reflow Process Considerations

#### Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures ( $T_c$ )). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

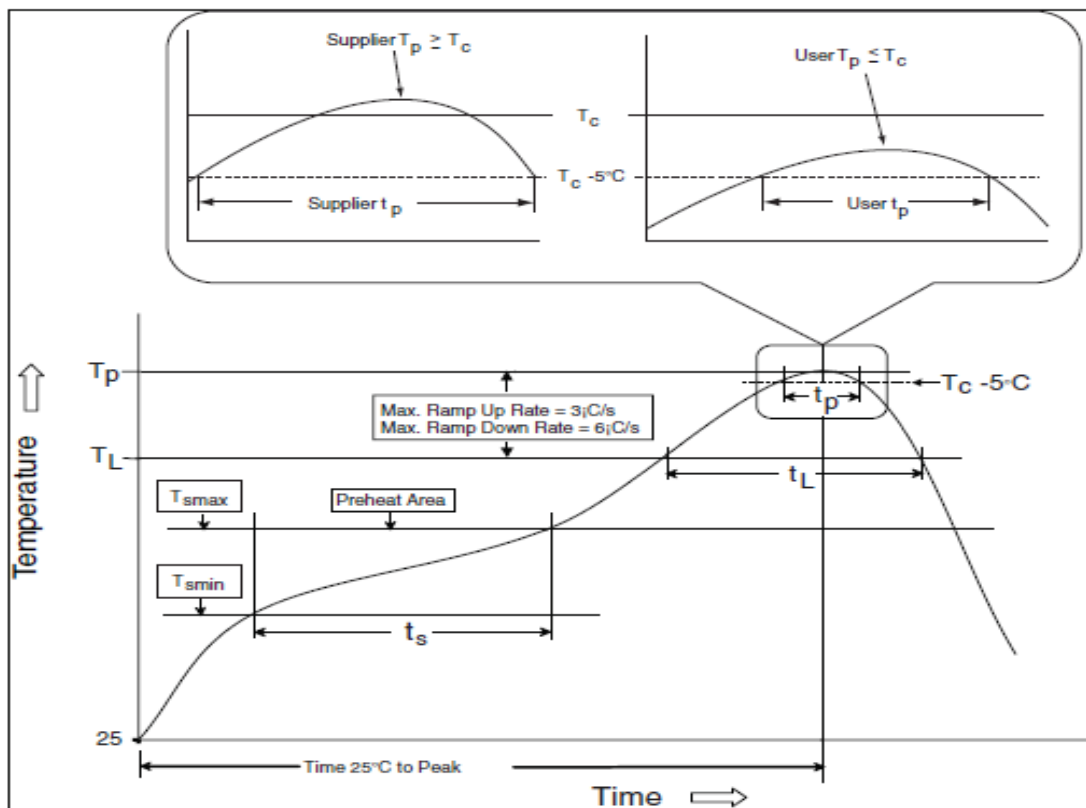


Figure 35 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

## ES9020 Product Datasheet

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time, bake the board according to the moisture sensitivity label instructions.

### Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

### RPC-1 Classification Reflow Profile

| Profile Feature                                                                                    | Pb-Free Assembly                                                                                                                                      |
|----------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Preheat/Soak</b>                                                                                |                                                                                                                                                       |
| Temperature Min (T <sub>smin</sub> )                                                               | 150°C                                                                                                                                                 |
| Temperature Max (T <sub>smax</sub> )                                                               | 200°C                                                                                                                                                 |
| Time (ts) from (T <sub>smin</sub> to T <sub>smax</sub> )                                           | 60-120 seconds                                                                                                                                        |
| Ramp-up rate (TL to Tp)                                                                            | 3°C / second maximum                                                                                                                                  |
| Liquidous temperature (TL)                                                                         | 217°C                                                                                                                                                 |
| Time (tL) maintained above TL                                                                      | 60-150 seconds                                                                                                                                        |
| Peak package body temperature (Tp)                                                                 | For users Tp must not exceed the classification temp in Table RPC-2.<br>For suppliers Tp must equal or exceed the Classification temp in Table RPC-2. |
| Time (tp)* within 5°C of the specified classification temperature (Tc)                             | 30* seconds                                                                                                                                           |
| Ramp-down rate (Tp to TL)                                                                          | 6°C / second maximum                                                                                                                                  |
| Time 25°C to peak temperature                                                                      | 8 minutes maximum                                                                                                                                     |
| * Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum. |                                                                                                                                                       |

Table 40 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within  $\pm 2^\circ\text{C}$  of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

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### RPC-2 Pb-Free Process - Classification Temperatures (Tc)

| Package Thickness | Volume mm <sup>3</sup> , <350 | Volume mm <sup>3</sup> , 350 to 2000 | Volume mm <sup>3</sup> , >2000 |
|-------------------|-------------------------------|--------------------------------------|--------------------------------|
| <1.6 mm           | 260°C                         | 260°C                                | 260°C                          |
| 1.6 mm – 2.5 mm   | 260°C                         | 250°C                                | 245°C                          |
| >2.5 mm           | 250°C                         | 245°C                                | 245°C                          |

Table 41 - RPC-2 Pb Free Classification Temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

## Ordering Information

| Part Number | Description                                 | Package          |
|-------------|---------------------------------------------|------------------|
| ES9020Q     | SABRE 32-bit high performance 2 Channel DAC | 5mm x 5mm 28 QFN |

Table 42 - Ordering Information

## Revision History

Current Version 0.3.1

| Rev.  | Date            | Notes                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0.1   | August, 2024    | Initial release                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 0.2   | June, 2025      | <ul style="list-style-type: none"> <li>Updated reference output stage schematic</li> <li>Added voltage and current output characteristics in performance</li> <li>Reserved Reg 67 [4,1]</li> <li>Unreserved 69[2], 73-75[20], 76[7:5]</li> <li>Added Recommended Power Up/Down Sequence</li> <li>Updated Recommended Operating Conditions and Absolute Maximum Rating</li> </ul>                                                        |
| 0.3   | September, 2025 | <ul style="list-style-type: none"> <li>Added notes for PLL in HW Modes 9-11, 13-15</li> <li>Added Recommended PCB Layout Guidelines</li> <li>Updated note for current output offsets</li> <li>Updated Recommended Power Up/Down Sequence</li> <li>Updated Reg 1[6, 5] Default value</li> <li>Updated Reg 34[4:0], 73-75[20], 76[7:5] Description</li> <li>Added DoP Input format section</li> <li>Updated PDM Format section</li> </ul> |
| 0.3.1 |                 | <ul style="list-style-type: none"> <li>Added MCLK Timing</li> <li>Updated APLL section with 32kHz Base Rates</li> <li>Updated BCLK and Word-Select Timing</li> <li>Updated Recommended Power Up Sequence</li> <li>Renamed Register 68[3:0], 69[3] (PDB -&gt; EN)</li> <li>Updated Register 8[4:0], 9[4:0] Description</li> </ul>                                                                                                        |

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