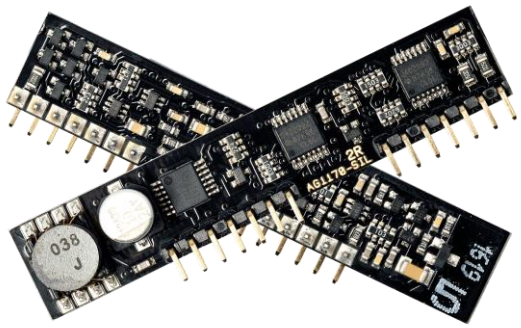
Silvertel

Ag1170

+5V / +3.3V Low Power Ringing SLIC



FEATURES

- A highly featured low power SLIC in a 14 pin SIL or 21 pin DIL format.
- Integral high efficiency DC/DC converter. Single +5V or +3.3V supply voltage.
- Highly integrated with an on-board ringing generator.
- Tip/Ring polarity reversal. On-Hook Transmission for caller line ID.
- Line and balance impedance programmable with external components (on Ag1170-P version)
- Easy to use, with a minimum number of external components.
- Simplified protection in “on-premise” applications.
- Silvertel “design-in” assistance.

DESCRIPTION

The Silvertel Ag1170 is a single Subscriber Line Interface Circuit (SLIC) in a 14 pin single in line (SIL) or 21 pin dual in line (DIL) format. The combination of features and packaging offers extremely efficient use of board area, saving significant system size and cost, minimising time to market for Telephony Systems developers.

The Ag1170 has been designed to work with loop lengths of typically 3.0km (800Ω including telephone). Its performance to regulatory standards (G712) allows use in public and private network applications.

The Ag1170 has integral dc/dc converter and ringing generation thus providing all the line powering requirements from a single supply. The SLIC requires a minimum of external components.

The system interface has been designed for direct connection to popular codecs, for both audio and signalling

The Ag1170 is ideal for low line count, short loop length applications, such as ISDN Terminal Adaptors, Internet Telephony (VoIP), Computer Telephony Integration (CTI), Wireless Local Loops (WLL) and Small Office Home Office (SOHO).

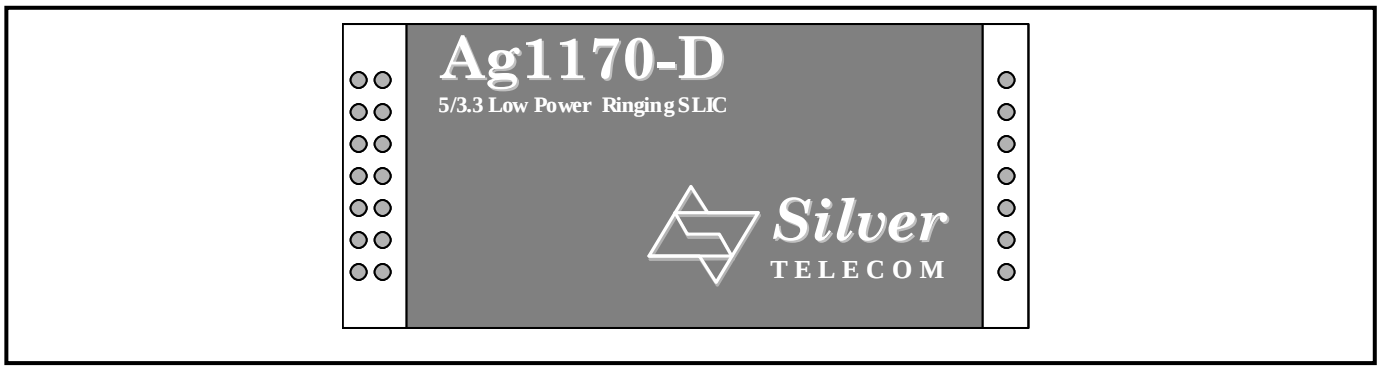


Figure 1: DIL Variant Packaging Format

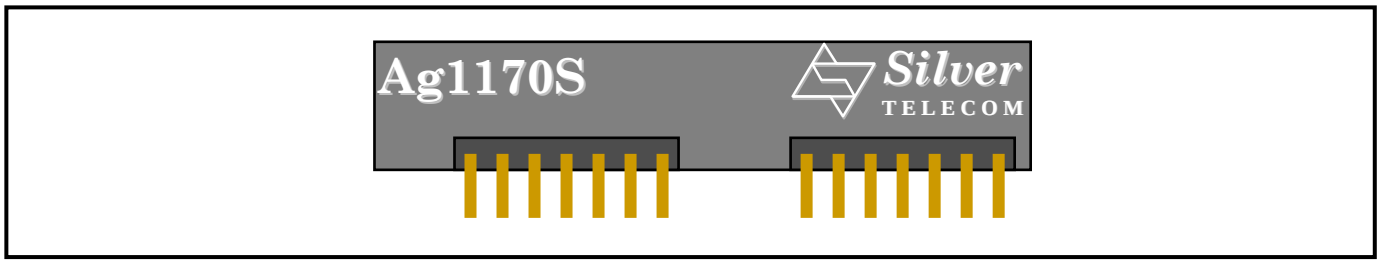


Figure 2: SIL Variant Packaging Format

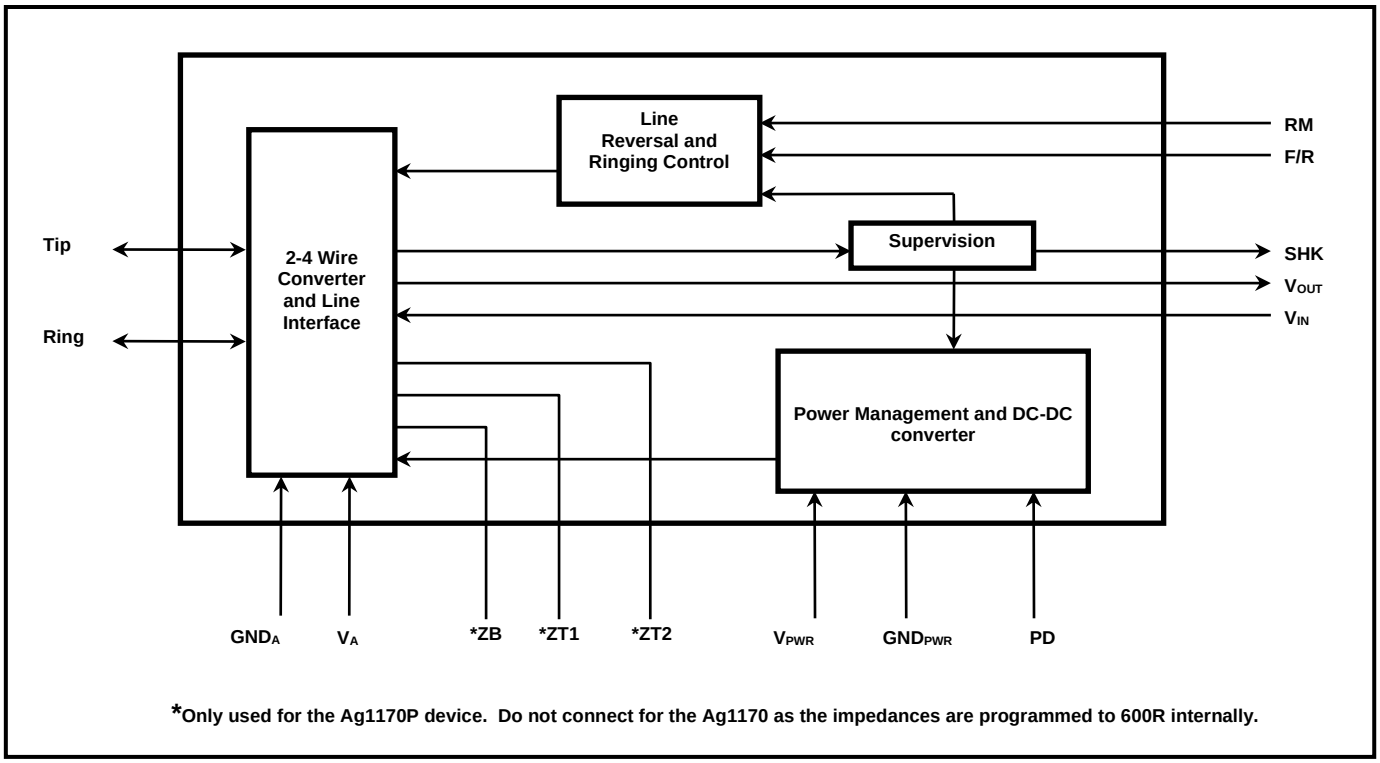
Part Number	Impedance	Package	Supply Voltage	Marking
Ag1170-D5	600 ohm	DIL	5 Volt	5
Ag1170-S5	600 ohm	SIL	5 Volt	5
Ag1170-D3	600 ohm	DIL	3.3 Volt	3
Ag1170-S3	600 ohm	SIL	3.3 Volt	3
Ag1170P-D5	Programmable	DIL	5 Volt	P5
Ag1170P-S5	Programmable	SIL	5 Volt	P5
Ag1170P-D3	Programmable	DIL	3.3 Volt	P3
Ag1170P-S3	Programmable	SIL	3.3 Volt	P3

Table 1: Ordering Information and Device Marking*

* All versions of the Ag1170 are RoHS compliant.

* Industrial temperature range versions of the Ag1170 are available. Contact Silver Telecom for further details.

Figure 3: Functional Block Diagram



*Only used for the Ag1170P device. Do not connect for the Ag1170 as the impedances are programmed to 600R internally.

1.0 Pin Description - DIL Package

Pin #	Name	Description
1	TIP (A)	**Tip.** Connects to the subscriber line Tip.
2	RING (B)	**Ring.** Connects to the subscriber line Ring.
3	IC	**Internal Connection.** Do not connect externally to this pin.
4	PD	**Power Down of DC/DC Converter**. A logic 0 powers off the DC/DC converter. Leave open circuit for free run operation. DO NOT input logic 1 to this pin.
5	NC	**No Connection.** This pin is not connected internally.
6	NC	**No Connection.** This pin is not connected internally.
7	RM	**Ringing Mode.** Sets bias conditions during ringing. Must be set to logic 1 during ringing. Logic 0 for other modes.
8	GND_A	**Analog Ground.** Normally connected to system ground.
9	$+V_A$	**Analog Supply.** Connect to the +5V or +3.3V supply via an RC filter, to supply power to the analog circuits.
10	*ZT2	**Line Impedance.** Connect to ZT1 via impedance programming components.
11	*ZT1	**Line Impedance.** Connect to ZT2 via impedance programming components.
12	*ZB	**Balance Impedance.** Connect to VIN via impedance programming components.
13	V_{IN}	**Audio In.** Analog input signal from the Codec (which is output on Tip and Ring). Connect via a 100nF capacitor.
14	NC	**No Connection.** This pin is not connected internally.
15	V_{OUT}	**Audio Out.** Analog output signal (from Tip and Ring) to the Codec. Connect via a 100nF capacitor.
16	F/R	**Forward/Reverse.** A logic 0 will reverse the Tip and Ring voltage polarities. F/R is toggled to produce the ringing output.
17	SHK	**Switch Hook.** Indicates an off-hook condition when at logic 1.
18	GND_{PWR}	**DC/DC Ground.** Ground input for the DC/DC converter.
19	$+V_{PWR}$	**DC/DC Supply.** +5V or +3.3V input for the DC/DC converter.
20	GND_{PWR}	**DC/DC Ground.** Ground input for the DC/DC converter.
21	$+V_{PWR}$	**DC/DC Supply.** +5V or +3.3V input for the DC/DC converter.

* Only used for the Ag1170P device. Do not connect for Ag1170 as impedance is programmed to 600R internally

1.1 Pin Description – SIL Package

Pin #	Name	Description
1	RING (B)	**Ring.** Connects to the subscriber line Ring.
2	TIP (A)	**Tip.** Connects to the subscriber line Tip.
3	F/R	**Forward/Reverse.** A logic 0 will reverse the Tip and Ring voltage polarities. F/R is toggled to produce the ringing output.
4	RM	**Ringing Mode.** Sets bias conditions during ringing. Must be set to logic 1 during ringing. Logic 0 for other modes.
5	SHK	**Switch Hook.** Indicates an off-hook condition when at logic 1.
6	*ZT1	**Line.** Connect to ZT2 via impedance programming components.
7	*ZT2	**Line Impedance.** Connect to ZT1 via impedance programming components
8	*ZB	**Balance Impedance.** Connect to VIN via impedance programming components
9	V_{IN}	**Audio In.** Analog input signal from the Codec (which is output on Tip and Ring). Connect via a 100nF capacitor
10	V_{OUT}	**Audio Out.** This is the analog output signal (from Tip and Ring) to the Codec. Connect via a 100nF capacitor.
11	$+V_A$	**Analog Supply.** Connected to the +5V or +3.3V supply via an RC filter, to supply power to the analog circuits.
12	GND_{PWR}	**DC/DC Ground.** Ground input for the DC/DC converter.
13	$+V_{PWR}$	**DC/DC Supply.** +5V or +3.3V input for the DC/DC converter.
14	PD	**Power Down of DC/DC Converter**. A logic 0 powers off the DC/DC converter. Leave open circuit for free run operation. DO NOT input logic 1 to this pin.

* Only used for the Ag1170P device. Do not connect for Ag1170 as the impedances are programmed to 600R internally

2.0 Line Interfacing

As well as being used in an electrically demanding environment, the needs of different applications and regulatory standards means that the SLIC must be flexible, and have facilities to ensure robust performance. The Ag1170 SLIC provides a complete and flexible interface to the telephone line.

2.1 Battery Feed

The Ag1170 has an integral DC/DC converter, which generates the battery voltage in the device. This means that only a supply of +5V or 3.3V is needed, unlike conventional SLICs which will also need a battery voltage of anything between -20V and -60V (-75V for ringing). This confers a significant cost, space and time to market benefit on the equipment designer.

The battery feed to the telephone line is generated from the positive supply rail. This provides a -48V battery feed to the line driver, which is adjusted automatically to match line conditions.

Power efficiency is good, because the line is supplied with only as much power as is needed. Little excess heat is generated, even on short lines. The loop current is pre-set to a constant 24mA, under the conditions shown in Section 9.3 of this datasheet, which specifies the 'DC Electrical Characteristics' for the Ag1170.

2.2 Ringing

The ringing signal is generated by switching the SLIC into ringing mode, by setting the RM pin high, and then toggling the F/R pin at the required frequency and cadence. The toggling of the F/R pin produces a balanced signal at Tip and Ring. These signal waveforms and critical timings are shown in Figure 4. Ringing voltage of approximately 65Vrms is applied to a single handset. It is important that the RM pin is only set high during ringing and that this pin is set low at all other times. Applications Note AN1170-14 provides advice on how to implement this requirement.

During ringing the integral DC/DC converter is switched by RM to produce a battery voltage of -72V. This will produce greater than 40Vrms into a REN of 3. The slope of the edges on the ringing waveform is set internally to give the correct waveform with 20Hz to 25Hz ringing frequency.

When an "off-hook" condition occurs during ringing, the ring-trip circuit on the Ag1170 senses the loop current flowing and signals the off-hook condition on the SHK output. The SHK signal must be "de-bounced" (persistence checked by the control processor) for 10ms to remove any spurious pulses. The DC/DC controller limits the power so the Ag1170 will operate continuously with a ring-trip load. The ring-trip function will operate up to a loop resistance of typically 800R (including telephone). It is also guaranteed not give a false ring trip with a load of 3 REN.

2.3 Power Down and Synchronisation

The DC/DC converter can be switched off by applying a logic 0 to the PD input. The SLIC takes 50ms to power up from this powered down state. Logic outputs are not valid during this time. When using the power down function, it is recommended that the SLIC is polled (powered up periodically) to check for SHK (the subscriber has gone off-hook). If not in Power Down mode, the PD pin should be left open circuit. An open-collector gate should be used for applying the PD signal. **Never connect a logic high to the PD pin.** NOTE: This is a sensitive node; keep connections very short.

The DC/DC has an internal oscillator. If desired, the oscillator frequency may be synchronised with an external clock for EMI reasons. To do this, a 128kHz (+5V) or 64kHz (+3.3V) square wave (with 50:50 mark space) should be inputted to the PD pin. See Applications Note: AN1170-12, for further details.

3.0 The 2-4 Wire (hybrid) Conversion.

The Ag1170 SLIC transmits and receives balanced 2-wire analog signals at the Tip and Ring connections. These are converted to a ground referenced output at V_{OUT} and from a ground referenced input at V_{IN}.

The V_{OUT} and V_{IN} pins are normally connected to a Codec for conversion of audio to and from a digital Pulse Code Modulated (PCM) stream.

3.1 Transmit and Receive Gain.

The gain in both the transmit direction (Tip/Ring to V_{OUT}) and the receive direction (V_{IN} to Tip/Ring) is set to 0dB. Normally any gain adjustments required by the user can be made by programming the Codec.

3.2 The 2 Wire Impedance.

The 2 Wire impedance of the Ag1170 at Tip/Ring is set to 600R. It requires no external programming resistors.

The 2 Wire impedance of the Ag1170-P can be programmed to the required value by connecting components across pins ZT1-ZT2.

The impedance ratio for ZT is 100. Resistors should be multiplied by the ratio and capacitor values divided by the ratio to obtain the required programming values. E.g. for 600R impedance, fit 60K resistor (nearest value = 62K).

Further details on the programming of the Ag1170P are contained within Applications Note: AN1170-1.

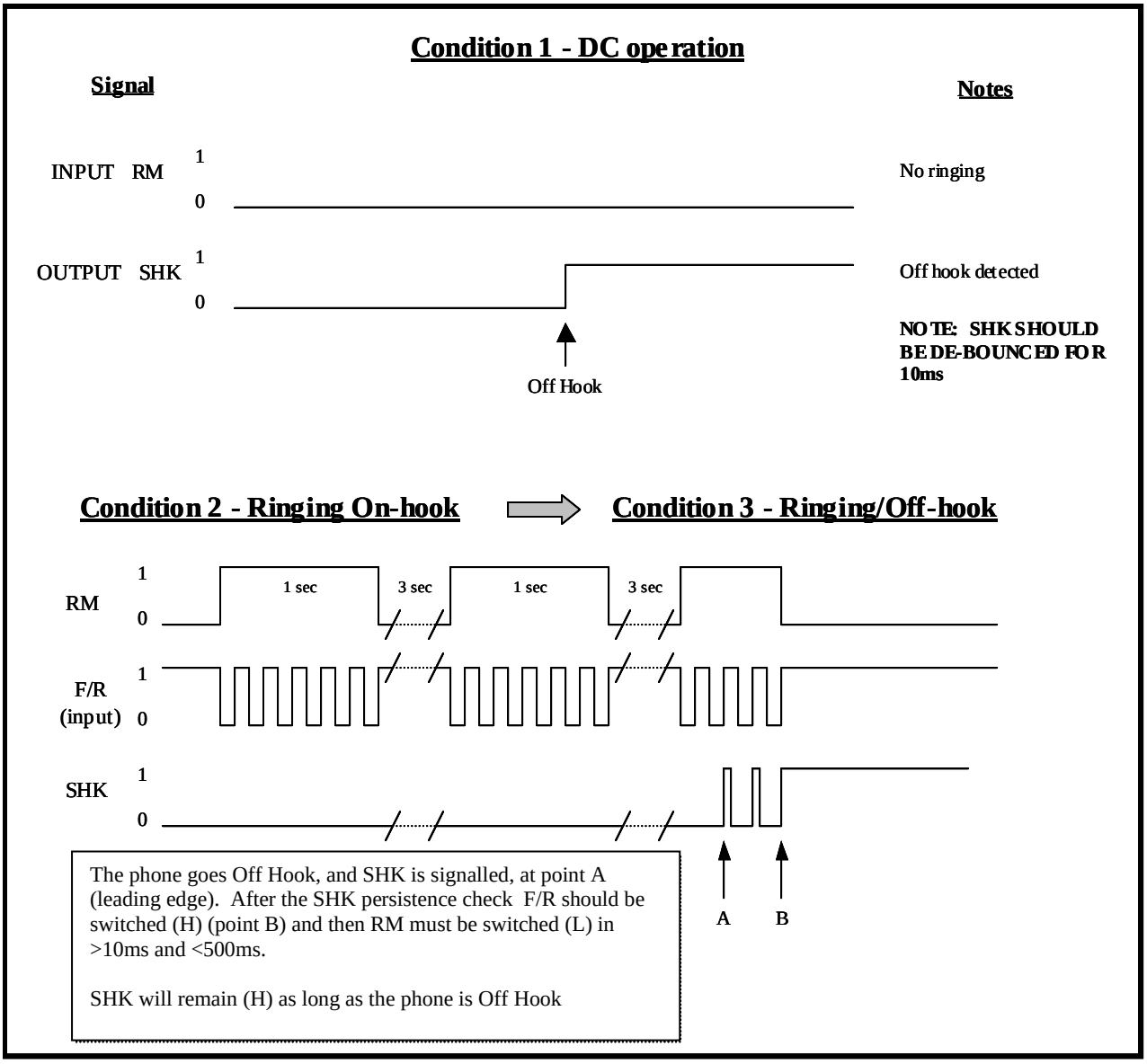


Figure 4: Ringing Signal Waveforms

3.3 Network Balance Impedance.

The network balance impedance ZB of the Ag1170 is set to 600R and it requires no external programming resistors.

To programme the ZB for the Ag1170P components are connected from the V_{IN} pin to the ZB pin. For ZB = ZT use a 100K resistor in series with a 47nF capacitor.

Further details on the programming of the Ag1170P are contained within Applications Note: AN1170-1.

3.4 Tip & Ring Polarity Reversal.

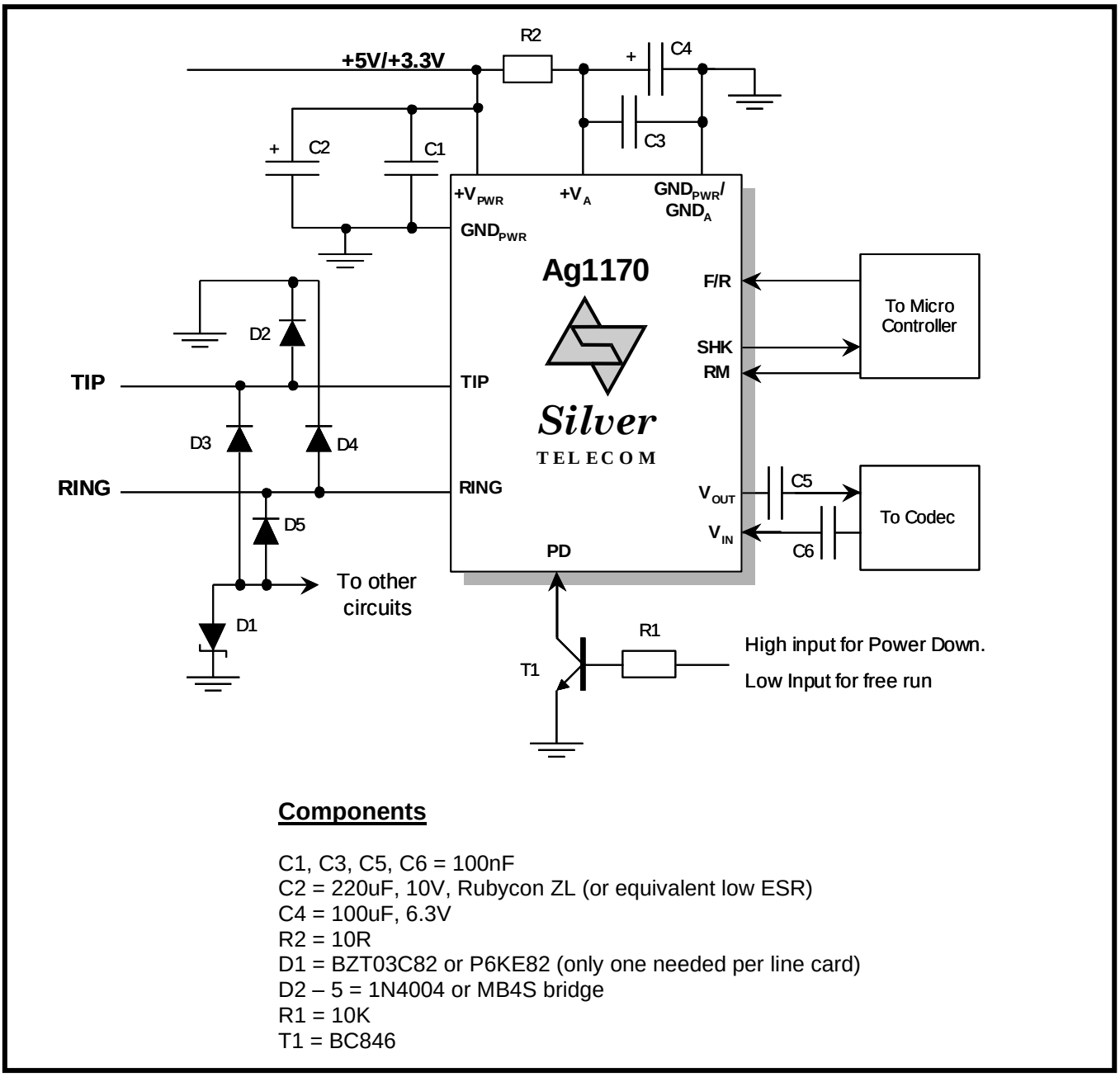
The Ag1170 can reverse the battery voltage polarity at Tip and Ring via the F/R pin.

If F/R is held at logic 1 (forward) the d.c. voltage at Tip is positive with respect to Ring. If F/R is taken to logic 0 the voltage polarity is reversed.

3.5 On Hook Transmission.

The Ag1170 is capable of on-hook transmission. This means analog signals can be transmitted from VIN through Tip and Ring and onto the line even when no loop current is flowing. This can be used when sending Caller Line Identification (CLI) information or for other “no ring” calls.

The Ag1170 will provide on hook transmission with a high impedance on Tip/Ring or with AC loads down to 600R.



Components

C1, C3, C5, C6 = 100nF
C2 = 220uF, 10V, Rubycon ZL (or equivalent low ESR)
C4 = 100uF, 6.3V
R2 = 10R
D1 = BZT03C82 or P6KE82 (only one needed per line card)
D2 – 5 = 1N4004 or MB4S bridge
R1 = 10K
T1 = BC846

Figure 5: Typical Connection Diagram

4.0 Switch Hook Detect Level

When the subscriber goes “off-hook” loop current will begin to flow. If this current is above the detection threshold (10mA) the switch hook output, SHK, will switch to a logic 1. It is recommended that software or hardware de-bouncing of the switch hook signal is used. This is to avoid short pulses which can cause a false switch hook output, triggering the incorrect system response.

During loop disconnect dialling, SHK will pulse between logic 1 and logic 0 to indicate the digits being dialled. Again it is recommended that software de-bouncing is used to avoid false detection of digits.

5.0 Protection of the Ag1170 SLIC

5.1 Thermal Protection

Should the SLIC be operated incorrectly, for example by accidentally shorting Tip and Ring to each other or to ground, the power dissipation is automatically limited by the DC/DC converter

This feature means that the SLIC will always operate within its power limits, without overheating. When operating on very short lines the battery voltage is regulated to a low value. This limits the power dissipation and ensures the Ag1170 operates with a minimum temperature rise.

5.2 Overvoltage Protection.

It is usual for the Ag1170 to be used in “on-premise” applications, such as SOHO, CTI and VoIP. In this case protection from Electrostatic Discharge (ESD) is required.

The Ag1170 has been designed to use low cost over voltage protection components. A typical circuit, for most “on-premise” applications, is shown in Fig. 5.

This circuit is the minimum overvoltage protection that should be used with the Ag1170. Operation with no overvoltage protection or with incorrect components (e.g. Varistors or Gas Discharge tubes) is strongly discouraged and will not be supported by Silvertel.

In ‘off-premise’ applications, a subscriber circuit will be required to withstand over voltage conditions which could be caused by lightning or overhead power cables striking the telephone cables. It is therefore normal in “off-premise” applications to provide additional primary and secondary protection circuits to prevent damage to the SLIC. For further information see application note ANX-Overvolt1. This is available on our website www.silvertel.com.

6.0 Approvals.

It can be seen from the Electrical Characteristics given on subsequent pages that the SLIC has been designed to meet the equipment standards of as many major public telephone authorities as possible.

It is the responsibility of the equipment design authority to ensure that their system meets the requirements of the relevant regulatory bodies. Every effort is made to ensure that Silvertel products are compliant with the latest standards.

7.0 A Typical Application.

The Ag1170 has been designed to interface to any Codec. Applications drawings for many codecs and DSP chips are available. Please contact Silvertel or visit our website www.silvertel.com. An example is shown in figure 5.

The status outputs from the SLIC are passed to the micro-controller. These signals can then be processed as necessary by the system software.

The audio signals which are on the 4 wire side of the connection are coupled by 100nF capacitors to avoid d.c. level problems between the two devices.

The Ag1170 provides for a 2 wire impedance and a network balance impedance of 600Ω. For other impedances the Ag1170-P can be used. This can be programmed using external components (Section 3.2 and 3.3).

7.1 DC Supply Voltage

During operation the DC Supply Voltage MUST be regulated within the limits shown in the Electrical Characteristics – Section 9.0 of this datasheet. Use of a “clean” power supply is extremely important. Should the VCC supply rail go above the Absolute Maximum Rating of 5.5V, for even a short time, then permanent damage to the Ag1170 is likely to result.

We also advise that the designer performs a full system evaluation, under all possible performance conditions, to ensure that the VCC Maximum rating is not exceeded.

In some applications, additional EMI suppression may be needed. In this instance 3 capacitors can be added to filter out the higher frequencies of the DC-DC converter. See figure 6 for details.

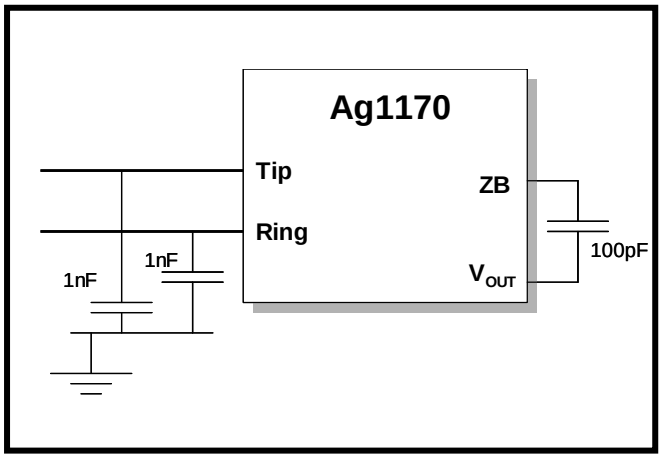


Figure 6: Optional EMI Suppression

8.0 Layout Considerations.

8.1 Power and Ground

Figure 7 gives an example of the tracking needed for the Ag1170. Tracks to the $+V_{PWR}$ and GND_{PWR} should be made as thick as possible. To maximise the performance of the device, signal tracks should be kept as short as possible. A low impedance (ESR) capacitor must be used for C2. To reduce DC/DC noise capacitors up to 10nF may be connected to ground at Tip and Ring.

PD is a sensitive node. Keep the tracking as short as possible. Particularly if connecting a transistor to this pin.

8.2 Impedance

ZT1, ZT2 and ZB are sensitive nodes. Keep the tracks as short as possible.

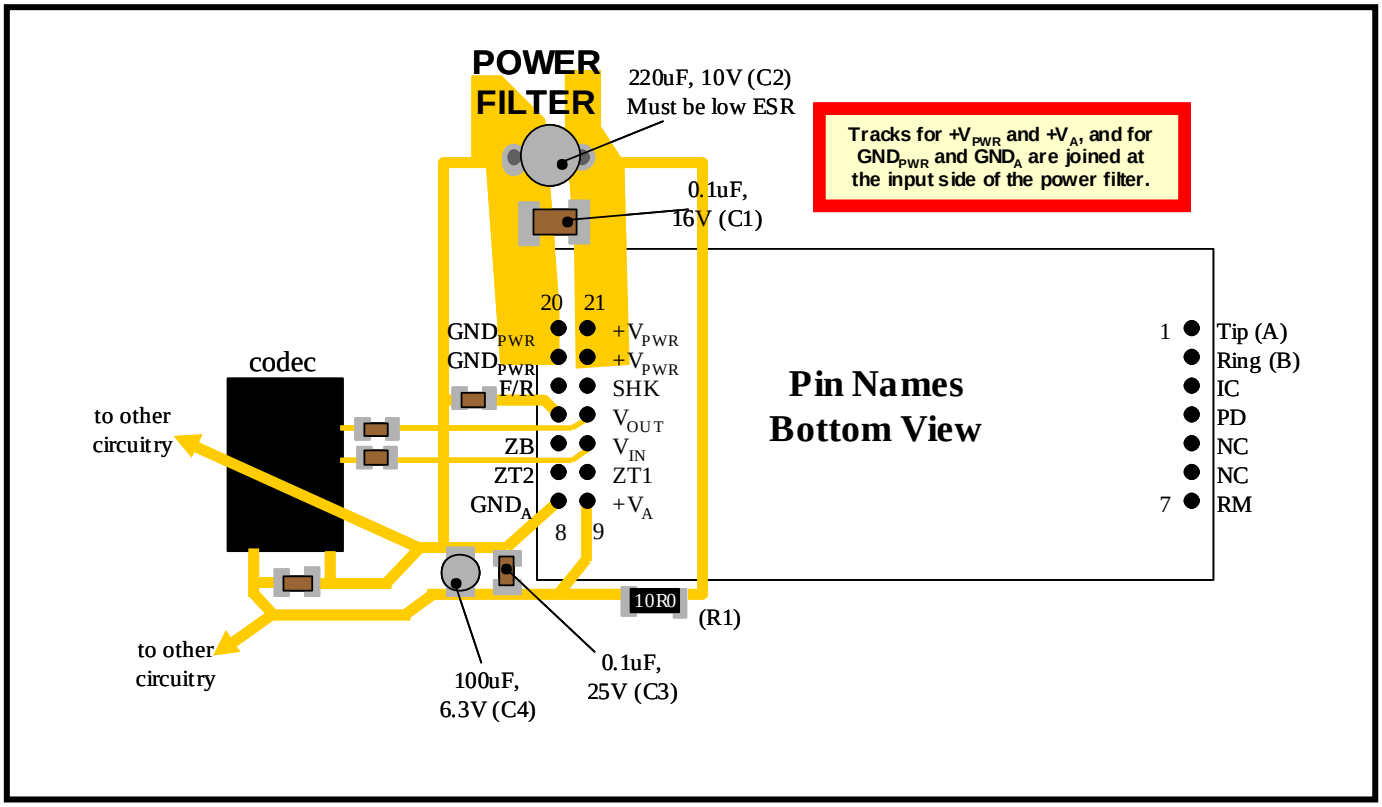


Figure 7: Typical Layout

9.0 Electrical Characteristics.

9.1 Absolute Maximum Ratings*

All Voltages are with respect to ground unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{CC}	-0.3	5.5	V
2	Maximum Power Dissipation, Off Hook @ 25^{o}C	P_{SLIC}		1.2	W
3	Storage Temperature	T_S	-40	+100	^{O}C
4	Duty Cycle for RM(H)			33	%

*Exceeding the above ratings may cause permanent damage to the product. Functional operation under these conditions is not implied. Maximum ratings assume free air flow.

9.2 Recommended Operating Conditions*

All Voltages are with respect to ground unless otherwise stated.

	Parameter	Symbol	Min	Typ	Max	Units
1	DC Supply Voltage (5V Version)	V_{CC}	4.75	5.0	5.25	V
2	DC Supply Voltage (3.3V Version)	V_{CC}	3.10	3.30	3.50	V
3	Operating Temperature	T_{OP}	0	25	70	^{O}C

*Typical figures are at 25°C with nominal +5V/+3.3V supplies and are for design use only. They are not guaranteed

It is important that the user performs a full system evaluation, under all possible performance conditions, to ensure that the VCC Maximum rating is not exceeded.

9.3 DC Electrical Characteristics.

	DC Characteristic	Sym	Min	Typ*	Max	Units	Test Comments
1	Supply Current, on- hook Ag1170-5 Ag1170-3	I_{SUP}		 90 110		 mA mA	
2	Supply current ringing 1 REN Ag1170-5 Ag1170-3	$I_{RINGING}$		 300 500		 mA mA	R_{LOOP} = 0R Load = 1 REN
3	Supply current, off-hook Ag1170-5 Ag1170-3	I_{ACTIVE}		 160 260		 mA mA	R_{LOOP} =0R Load = 300R
4	Supply current during ring trip (<1 sec max) Ag1170-5 Ag1170-3			 420 600		 mA mA	R_{LOOP} =0R Load = 300R
5	Supply current in power down	I_{PD}		5		mA	
6	Wake-up time			50		ms	Logic outputs not valid during wake-up period
7	Constant current feed to line Ag1170-5 Ag1170-3	I_{LOOP}	 21.5 21.5	 24 24	 26.5 26.5	 mA mA	R_{LOOP} =170R (1Km) Load = 300R
8	Tip/Gnd or Ring/Gnd or Tip&Ring/Gnd overcurrent				 35.0 45.0	 mA mA	RM = L RM = H
9	Off-Hook detect; Ag1170 3.3V Output Low Voltage Output High Voltage	 V_{OL} V_{OH}	 2.7		 0.2	 V V	10uA max output (with 62k internal pull-up resistor). Fit external pull-up for higher output current
10	Off-Hook detect; Ag1170 5V Output Low Voltage Output High Voltage	 V_{OL} V_{OH}	 4.4		 0.2	 V V	
11	Control Inputs, F/R, PD, RM Input Low Voltage Input High Voltage	V_{IL} V_{IH}	 2.1		0.9	V V	Ag1170 - 3.3V versions
		V_{IL} V_{IH}	 3.5		1.5	V V	Ag1170 - 5V versions
12	Control Inputs, F/R, PD, RM Input low current Input high current	 I_{IL} I_{IH}	 -0.5 -0.5		 0.5 0.5	 mA mA	
13	Switch Hook Detect Threshold		7.0	10.0	13.0	mA	
14	Load on V_{OUT}		10.0			kohm	100nF coupling

1) All DC Electrical Characteristics are over the Recommended Operating Conditions with V_{CC} at +5.0V ±5%,or +3.3V ±5%, unless otherwise stated.
2) Operating currents are dependent on the users application.
*Typical figures are at 25°C with nominal 5V supply and are for design aid only. Not Guaranteed

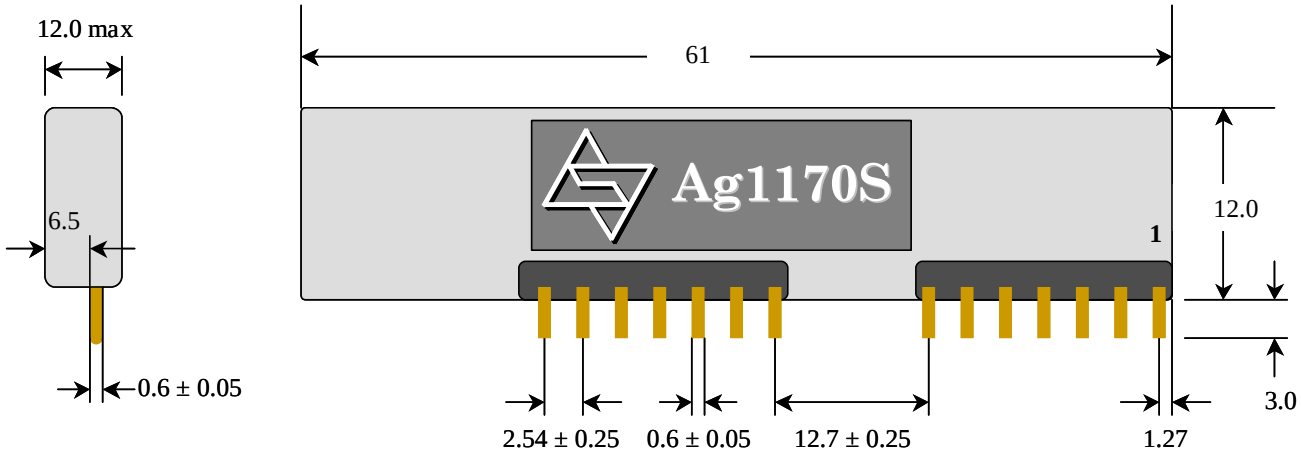
9.4 AC Electrical Characteristics.

	AC Characteristic	Sym	Min	Typ*	Max	Units	Test Comments
1	SHK Detect Time			5.0		ms	No Ringing
2	Ring Trip Capability		500	800		ohm	Includes telephone handset
3	Input Impedance at V_{IN}			100		kohm	
4	Output impedance at V_{OUT}				10	ohm	
5	Ringing Capability $40V_{rms}$ into REN=3		500			ohm	
6	Ringing voltage			65		Vrms	No load
7	Absolute Voltage Gain, 2 Wire to V_{OUT}		-0.5	0	0.5	dB	Off-Hook
8	Absolute Voltage Gain V_{IN} to 2Wire		-0.5	0	0.5	dB	Off-Hook
9	Relative Gain. Referenced to 1kHz. 2Wire - V_{OUT}, V_{IN} - 2Wire		-0.25		0.25	dB	Over frequency range 300 to 3400 Hz
10	Total Harmonic Distortion @ 2Wire and V_{OUT}	THD		0.1	1.0	%	@0dBm, 1kHz
11	Overload Distortion @2 Wire and V_{OUT}	OD		0.5	5.0	%	@+3dBm, 1kHz
12	Common Mode Rejection Ratio	CMRR	40	46		dB	300-3400Hz, at 2 Wire
13	Idle Channel Noise	N_C		2.0	12.0	dBrnC	@2 Wire & V_{OUT}
14	Power Supply Rejection Ratio at 2 Wire and V_{OUT}	PSRR	25	32		dB	Ripple 0.1V, 1kHz on V_{CC}
15	Return Loss	RL	18	35		dB	300-3400Hz
16	Transhybrid Loss	THL	18 21	35 35		dB dB	300-3400Hz 500-2500Hz
17	Load on VOUT		10.0			kohm	Coupling capacitor = 100nF
18	Longitudinal to Metallic Balance		40 46	43 53		dB	300-600Hz 600-3400Hz
19	Tip-Ring Reversal Settling Time				50	ms	To within +20% of set I_{LOOP}

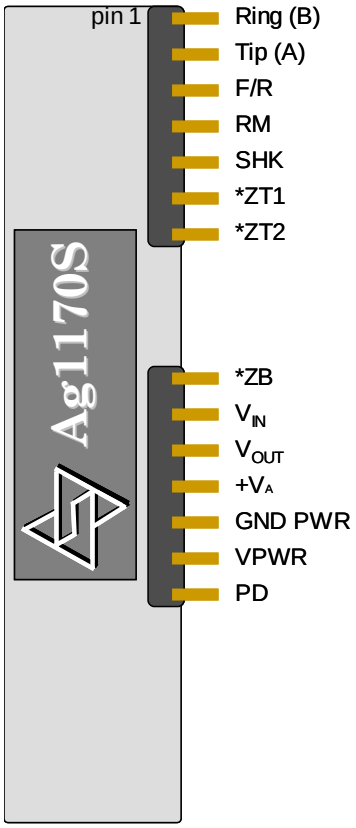
3) All AC Electrical Characteristics are over the Recommended Operating Conditions with V_{CC} at +5.0V ±5%, unless otherwise stated.
4) Gain, Transhybrid Loss and Total Harmonic distortion parameters measured with 600R termination.
*Typical figures are at 25°C with nominal 5V supply and are for design aid only.

10.0 Ag1170-D DIL Package

11.0 Ag1170-S SIL Package



Dimensions (in mm) are nominal unless otherwise stated



*Only used for the Ag1170P device. These pins are "Internal Connect" for the Ag1170 (as the impedances are programmed to 600R internally).

Silvertel Recommends the use of 2.54mm sockets, especially on prototype and pre production boards.

Recommended PCB hole diameter = 1.1 ± 0.05 mm