Toradex
Swiss. Embedded. Computing.

Verdin iMX95

HW Datasheet

Preliminary – Subject to Change

Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
16-Jul-2025	Rev. 0.1	V1.0	Initial release
04-Sep-2025	Rev. 0.2	V1.0	Section 4.1: Clarified default behavior for UART1_TXD and UART2_TXD pins in Table 10
27-Oct-2025	Rev. 0.3	V1.0	Section 1.5: Updated SoC naming convention to include package identifiers in Table 1 Section 1.5: Removed 10GbE reference in Table 3 Section 3.2: Added information for X1 pins 170 to 192 in Table 9
16-Dec-2025	Rev. 0.4	V1.0	Section 2.1: Updated block diagram in Figure 1

Contents

List of Tables

1 Introduction

1.1 Purpose of the Datasheet

This datasheet describes the hardware capabilities of the Verdin iMX95. For details on the features currently supported by software, refer to the corresponding SoM product page on the Toradex Developer Center:

https://developer.toradex.com/hardware/verdin-som-family/modules/verdin-imx95

1.2 Verdin SoM Family

The Verdin System on Module (SoM) family eliminates much of the complexity associated with modern-day electronic design. Complicated circuitry—such as high-speed, impedance-controlled layouts with high component density—is encapsulated on the SoM. This allows customers to design carrier boards focused solely on application-specific electronics, making projects substantially less complex.

The Verdin module goes a step further by implementing an interface pinout that allows direct connection to real-world I/O ports without the need to cross traces or change PCB layers. This feature, known as Direct Breakout™, becomes increasingly valuable as more interfaces adopt high-speed serial technologies that require impedance-controlled differential pairs. Direct Breakout™ allows such interfaces to be routed easily and reliably to common connectors.

The Verdin SoM features a wide input voltage range, allowing it to be powered from a broad range of sources (e.g., a USB power supply or a single lithium cell). Due to increasing transistor density and the need for more power-efficient devices, I/O voltage levels are shifting from 3.3 V to 1.8 V. For this reason, the Verdin SoM family supports a 1.8 V I/O voltage level exclusively. This combination of wide input range and standardized 1.8 V I/O simplifies carrier board power supply design. Together, these features make the Verdin SoM family well suited for battery-powered applications.

1.3 NXP i.MX 95 SoC

The Verdin iMX95 SoM is based on the NXP i.MX 95 family of System on Chips (SoCs). The i.MX 95 family features up to 6 Cortex®-A55 (often shortened to A55) cores as the main processor cluster. These cores provide full 64-bit Arm®v8.2 support while maintaining seamless backward compatibility with 32-bit Arm®v7-A software. The A55 cores run at up to 1.8 GHz and include the following upgrades:

- Faster integer operations
- An enhanced floating-point unit (FPU)
- An L3 cache (in addition to L1 & L2) for improved multicore performance and reduced memory latency.

In addition to the main CPU complex, the i.MX 95 also features the following processors:

- 1x Cortex®-M7 (often shortened to M7), peaking up to 800 MHz.
- 1x Cortex®-M33 (often shortened to M33), peaking up to 333 MHz.

In addition to general-purpose MCUs use, the M33 and M7 cores can be configured as a safety island to support functional safety. This heterogeneous multicore architecture supports running real-time operating systems for time and safety-critical tasks.

The SoC also includes the following specialized processors and accelerators:

- **Mali-G310 GPU** from Arm®: Capable of up to 64 GFLOPs (FP32) and supports OpenCL™ 3.0, OpenGL® ES 3.2, Vulkan®1.3.

- **Neural Processing Unit (NPU)**: Delivers up to 2.0 TOPS to significantly accelerate machine learning tasks.
- **Video Processing Unit (VPU)**: Accelerates video decoding and encoding.
- **Image Signal Processor (ISP)**: Supports both video and still image pipelines with image processing and color space conversion.

The i.MX 95 family features inline ECC (error-correcting code) for LPDDR4 DRAM to improve system reliability and safety.

The SoC even includes a new security enhancement: the EdgeLock® Secure Enclave—a fully isolated subsystem that supports functions such as secure boot, runtime attestation, trust provisioning, key management and other cryptographic operations. This dedicated security unit also simplifies certification for standards such as IEC 62443, US Cyber Trustmark and the Cyber Resilience Act.

1.4 Verdin iMX95 SoM

The Verdin iMX95 is a comprehensive solution, seamlessly combining robust connectivity, advanced interfaces and adaptability for diverse applications.

1.5 Main Features

1.5.1 CPU

Table 1: CPU

Parameter	Verdin iMX95 Hexa 8GB WB IT	Verdin iMX95 Hexa 8GB IT	Verdin iMX95 Quad 4GB WB IT	Verdin iMX95 Quad 4GB IT	Verdin iMX95 Quad 2GB WB IT	Verdin iMX95 Quad 2GB
SoC	MIMX9596CVT	MIMX9596CVT	MIMX9594CVT	MIMX9594CVT	MIMX9594CVT	MIMX9594DVT
A55 Cores	6	6	4	4	4	4
M7 Cores	1	1	1	1	1	1
M33 Cores	1	1	1	1	1	1
L1 Instruction Cache per core	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB
L1 Data Cache per core	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB
L2 Cache per core	A55: 64 kB	A55: 64 kB	A55: 64 kB	A55: 64 kB	A55: 64 kB	A55: 64 kB
L3 Cache shared between cores	A55: 512 kB	A55: 512 kB	A55: 512 kB	A55: 512 kB	A55: 512 kB	A55: 512 kB
Data Tightly Coupled Memory	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB
Instruction Tightly Coupled Memory	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB	M7: 256 kB[1] M33: 256 kB

[1] The sizes of Instruction Tightly Coupled Memory (ITCM) and Data Tightly Coupled Memory (DTCM) are configurable, with default values of 256 kB for ITCM and 256 kB for DTCM. Both memories feature an ECC interface.

1.5.2 GPU

Table 2: GPU

Parameter	Verdin iMX95 Hexa 8GB WB IT	Verdin iMX95 Hexa 8GB IT	Verdin iMX95 Quad 4GB WB IT	Verdin iMX95 Quad 4GB IT	Verdin iMX95 Quad 2GB WB IT	Verdin iMX95 Quad 2GB
GPU Model	Arm Mali-G310	Arm Mali-G310	Arm Mali-G310	Arm Mali-G310	Arm Mali-G310	Arm Mali-G310
2D Acceleration	Yes	Yes	Yes	Yes	Yes	Yes
3D Acceleration	Yes	Yes	Yes	Yes	Yes	Yes
FLOPs	FP32: 64	FP32: 64	FP32: 64	FP32: 64	FP32: 64	FP32: 64
L2 Cache	128 kB	128 kB	128 kB	128 kB	128 kB	128 kB
MSAA anti-aliasing	up to 4x	up to 4x	up to 4x	up to 4x	up to 4x	up to 4x
OpenCL	up to 2.2	up to 2.2	up to 2.2	up to 2.2	up to 2.2	up to 2.2
OpenGL ES	up to 3.2	up to 3.2	up to 3.2	up to 3.2	up to 3.2	up to 3.2
Vulkan	1.2	1.2	1.2	1.2	1.2	1.2

1.5.3 Interfaces

Table 3: SoM interfaces

Parameter	Verdin iMX95 Hexa 8GB WB IT	Verdin iMX95 Hexa 8GB IT	Verdin iMX95 Quad 4GB WB IT	Verdin iMX95 Quad 4GB IT	Verdin iMX95 Quad 2GB WB IT	Verdin iMX95 Quad 2GB
Analog						
Analog Input	6	6	6	6	6	6
Audio						
Digital Audio	2 *I2S or TDM*	2 *I2S or TDM*	2 *I2S or TDM*	2 *I2S or TDM*	2 *I2S or TDM*	2 *I2S or TDM*
Camera						
MIPI-CSI-2	2x Quad Lane	2x Quad Lane	2x Quad Lane	2x Quad Lane	2x Quad Lane	2x Quad Lane
Display						
Display Controllers	Dual	Dual	Dual	Dual	Dual	Dual
LVDS	1x up to 1920x1080	1x up to 1920x1080	1x up to 1920x1080	1x up to 1920x1080	1x up to 1920x1080	1x up to 1920x1080
MIPI DSI	1x Quad Lane up to 4k	1x Quad Lane up to 4k	1x Quad Lane up to 4k	1x Quad Lane up to 4k	1x Quad Lane up to 4k	1x Quad Lane up to 4k
Low Speed						
CAN FD	5	5	5	5	5	5
GPIO	82	82	82	82	82	82
I²C	7	7	7	7	7	7
I3C	1	1	1	1	1	1
JTAG	1	1	1	1	1	1
PWM	21	21	21	21	21	21
QSPI/OSPI	1	1	1	1	1	1
SPI	6	6	6	6	6	6
UART	8	8	8	8	8	8

Continued on next page

Table 3: SoM interfaces (Continued)

Parameter	Verdin iMX95 Hexa 8GB WB IT	Verdin iMX95 Hexa 8GB IT	Verdin iMX95 Quad 4GB WB IT	Verdin iMX95 Quad 4GB IT	Verdin iMX95 Quad 2GB WB IT	Verdin iMX95 Quad 2GB
Network						
Bluetooth	Classic / LE 5.4	–	Classic / LE 5.4	–	Classic / LE 5.4	–
Ethernet	2x 1GbE *all TSN-capable*	2x 1GbE *all TSN-capable*	2x 1GbE *all TSN-capable*	2x 1GbE *all TSN-capable*	2x 1GbE *all TSN-capable*	2x 1GbE *all TSN-capable*
Wi-Fi	Wi-Fi 6 802.11ax	–	Wi-Fi 6 802.11ax	–	Wi-Fi 6 802.11ax	–
Storage						
SDIO/SD/MMC	1	2	1	2	1	2
USB						
USB 2.0 *Host and Client*	1	1	1	1	1	1
USB 3.2 Gen 1 *Host and Client*	1	1	1	1	1	1

1.5.4 Memory

Table 4: Memory features

Parameter	Verdin iMX95 Hexa 8GB WB IT	Verdin iMX95 Hexa 8GB IT	Verdin iMX95 Quad 4GB WB IT	Verdin iMX95 Quad 4GB IT	Verdin iMX95 Quad 2GB WB IT	Verdin iMX95 Quad 2GB
eMMC						
eMMC Configuration	2D MLC[1]	2D MLC[1]	2D MLC[1]	2D MLC[1]	2D MLC[1]	2D MLC[1]
eMMC Capacity	32GB	32GB	32GB	32GB	16GB	16GB
I²C EEPROM						
I²C EEPROM Capacity	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits
RAM						
RAM Capacity	8GB	8GB	4GB	4GB	2GB	2GB
RAM Configuration *ctrl. × ch. × bits*[2]	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16
RAM Type	LPDDR4x	LPDDR4x	LPDDR4x	LPDDR4x	LPDDR4x	LPDDR4x
RAM Speed	4266MT/s	4266MT/s	4266MT/s	4266MT/s	4266MT/s	4266MT/s
Inline ECC	Yes	Yes	Yes	Yes	Yes	Yes

[1] Some eMMC partitions support Enhanced (SLC) mode.
[2] Controllers × channels per controller × bits per channel.

1.5.5 Physical

Table 5: Physical features

Parameter	Verdin iMX95 Hexa 8GB WB IT	Verdin iMX95 Hexa 8GB IT	Verdin iMX95 Quad 4GB WB IT	Verdin iMX95 Quad 4GB IT	Verdin iMX95 Quad 2GB WB IT	Verdin iMX95 Quad 2GB
Module Dimensions	69.6 × 35.0 × 6.0 mm					
Temperature Range	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	0°C to +70°C
Shock / Vibration	EN 60068-2-6/50g 20ms					

1.6 Interface Overview

Features of the Verdin module are split into three distinct categories: **Always Compatible**, **Reserved** and **Module-specific**. The Always Compatible and Reserved pins are also referred to as the **Verdin Standard** pins.

In addition to this definition, the i.MX 95 SoC supports alternate functions. The pins can operate as GPIOs but may be used for other purposes (e.g., UART). **Always Compatible interfaces are features that must be present on every SoM in the Verdin Family**, ensuring upgradability and maximum scalability.

Reserved interfaces are defined features that may be absent on some SoM models due to unavailability. This may occur if a specific SoC does not support a particular interface or if an assembly option omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This ensures that any Verdin SoM can be reliably inserted into any Verdin carrier board without risk of damage due to incompatible Reserved pins.

A **Module-specific feature is not guaranteed to be functionally or electrically compatible across different Verdin modules**. If a carrier board design uses such features, other modules in the Verdin Family might not support them and may instead assign different functions to the same pins. As a result, the number of compatible modules may be limited. An incompatible SoM and carrier board combination could disable functionality or even cause hardware damage. Using Module-specific pins may also prevent future upgrades.

The **Alternate Functions** group refers to interfaces provided as additional functions on Always Compatible, Reserved, or Module-specific pins. These functions can be used only if the primary function of the pin is not in use.

The table below lists the interfaces supported on the Verdin iMX95 module, along with the group in which each feature is provided: Always Compatible, Reserved, Module-specific or Alternate Function.

Table 6: X1 interfaces

Feature	Total	Always Compatible	Reserved	Module-specific or Alternate Function
Analog				
Analog Input *ADC*	6	0	4	2
Audio				
I^2S	2	0	2	0
S/PDIF *RX and TX*	1	0	0	1[1]

Continued on next page

Table 6: X1 interfaces (Continued)

Feature	Total	Always Compatible	Reserved	Module-specific or Alternate Function
PDM Mic Input	4	0	0	4[1]
Camera				
MIPI CSI-2	2	0	1	1[1]
Display				
MIPI DSI	1	0	1	0
LVDS *dual channel*	1	0	0	1
Low Speed				
I^2C	7	1	3	3[1]
I3C	1	0	0	1[1]
SPI	6	1	0	5[1]
UART	8	3	1	4[1]
PWM	21	1	2	18[1]
CAN FD	5	0	2	3[1]
JTAG	1	1	0	0
QSPI	1	0	1	0
OSPI	1	0	0	1[1]
GPIO	82	4	6	72[1]
High-Speed				
PCIe Gen3	1	0	1	0
Network				
Gigabit Ethernet	1	1	0	0
RGMII *for 2nd Gigabit Ethernet*	1	0	1	0
Storage				
SD/SDIO/MMC	2	1	0	1[1]
USB				
USB 2.0 OTG	1	1	0	0
USB 3.2 OTG *SS Signals for USB 2.0 OTG*	1	0	1	0
USB 2.0 Host	1	1	0	0

[1] Not all interfaces are exposed on dedicated SODIMM pins by default. Some features require enabling alternate functions on multiplexed pins via software configuration.

1.7 Reference Documents

1.7.1 Verdin Carrier Board Design Guide

To ensure compatibility with the Verdin module family, custom carrier boards must follow the Verdin Carrier Board Design Guide. Review this document thoroughly before beginning your design.

https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf

1.7.2 Verdin Family Specification

This document outlines the specification that defines the Verdin Computer on Module family. It describes the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also explains the mechanical form factor, including key dimensions and potential thermal solutions.

https://docs.toradex.com/109262-verdin-family-specification.pdf

1.7.3 Layout Design Guide

This document provides guidance on high-speed layout design and other factors that help ensure a correct carrier board layout on the first attempt.

https://docs.toradex.com/102492-layout-design-guide.pdf

1.7.4 Toradex Developer Center

The Toradex Developer Center is regularly updated with the latest product support information. It contains a wealth of additional resources.

Note that the Developer Center is shared across all Toradex products. Always verify that the information is applicable to the Verdin iMX95.

1.7.5 Verdin Carrier Board Schematics

Toradex provides complete schematics and an Altium project file that includes library symbols and IPC-7351–compliant footprints for the Verdin Development Board, as well as other carrier boards, free of charge. This resource is highly useful when designing your own carrier board.

https://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.7.6 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring pin multiplexing on Verdin, Apalis and Colibri modules. It also allows you to compare interfaces across different modules.

https://developer.toradex.com/knowledge-base/pinout-designer

1.7.7 NXP i.MX 95

Additional details about the NXP i.MX 95 SoC are available in the datasheet and reference manual provided by NXP.

https://www.nxp.com/products/i.MX95

1.7.8 EEPROM

The Verdin iMX95 includes an on-module I²C EEPROM: the M24C02-F from STMicroelectronics.

https://www.st.com/en/memories/m24c02-f.html

1.7.9 I/O Expander

The Verdin iMX95 features an on-module I/O expander: the PCAL6416AHF from NXP.

https://www.nxp.com/part/PCAL6416AHF

1.7.10 Ethernet Transceiver

The Verdin iMX95 SoM utilizes the DP83867IR industrial-temperature, robust Gigabit Ethernet PHY transceiver from Texas Instruments.

https://www.ti.com/product/DP83867IR

1.7.11 PCB Temperature Sensor

The Verdin iMX95 can be assembled with an onboard PCB temperature sensor: the TI TMP1075DSGR.

https://www.ti.com/product/TMP1075

1.7.12 RTC

The Verdin iMX95 features the low-power Epson RX8130CE real-time clock.

https://www5.epsondevice.com/en/products/rtc/rx8130ce.html

1.7.13 TPM 2.0 Module

The Verdin iMX95 can be assembled with a Trusted Platform Module (TPM 2.0): the ST33KTPM2I from STMicroelectronics. Complete documentation is available only under an NDA with STMicroelectronics.

https://www.st.com/en/secure-mcus/st33ktpm2i.html

1.7.14 Wi-Fi and Bluetooth Module

The WB versions of the Verdin iMX95 utilize a u-blox MAYA-W260-00B host-based module that supports Wi-Fi 6, Bluetooth 5.4 and IEEE 802.15.4. This module uses two U.FL antenna connectors.

https://www.u-blox.com/en/product/maya-w2-series

Information about pre-certified antennas and cables is available here:

https://developer.toradex.com/hardware/hardware-resources/peripherals/wireless/wi-fi-cables-and-antennas-for-toradex-modules/

1.8 Naming Conventions

This document follows a consistent naming convention. Pay close attention to punctuation and spacing in names. Do not confuse the NXP i.MX 95 SoC with the Toradex Verdin iMX95 SoM.

Table 7: Toradex naming conventions

Name	Description
i.MX 95	NXP i.MX 95 System on Chip family.
Verdin iMX95	Verdin module based on the i.MX 95 SoC. In this document, the term Verdin iMX95 refers to all versions of the module.
Verdin iMX95 Hexa 8GB WB IT	Verdin module based on the i.MX 95 SoC with 6 cores, 8 GB of RAM, Wi-Fi, Bluetooth and support for the industrial temperature range (IT).

1.9 Build-To-Order (BTO) Options

In addition to the configurations above, customized versions of the module are available as Build-To-Order (BTO) options. The following customization options are available for the Verdin iMX95:

Connectivity:

- Addition or removal of the Wi-Fi/Bluetooth module

Memory:

- RAM density
- eMMC capacity
- EEPROM capacity

SoC variants:

- Core count
- Featured IPs
- Contact us for more details, as these variants are subject to NXP's i.MX 95 portfolio options.

Temperature range:

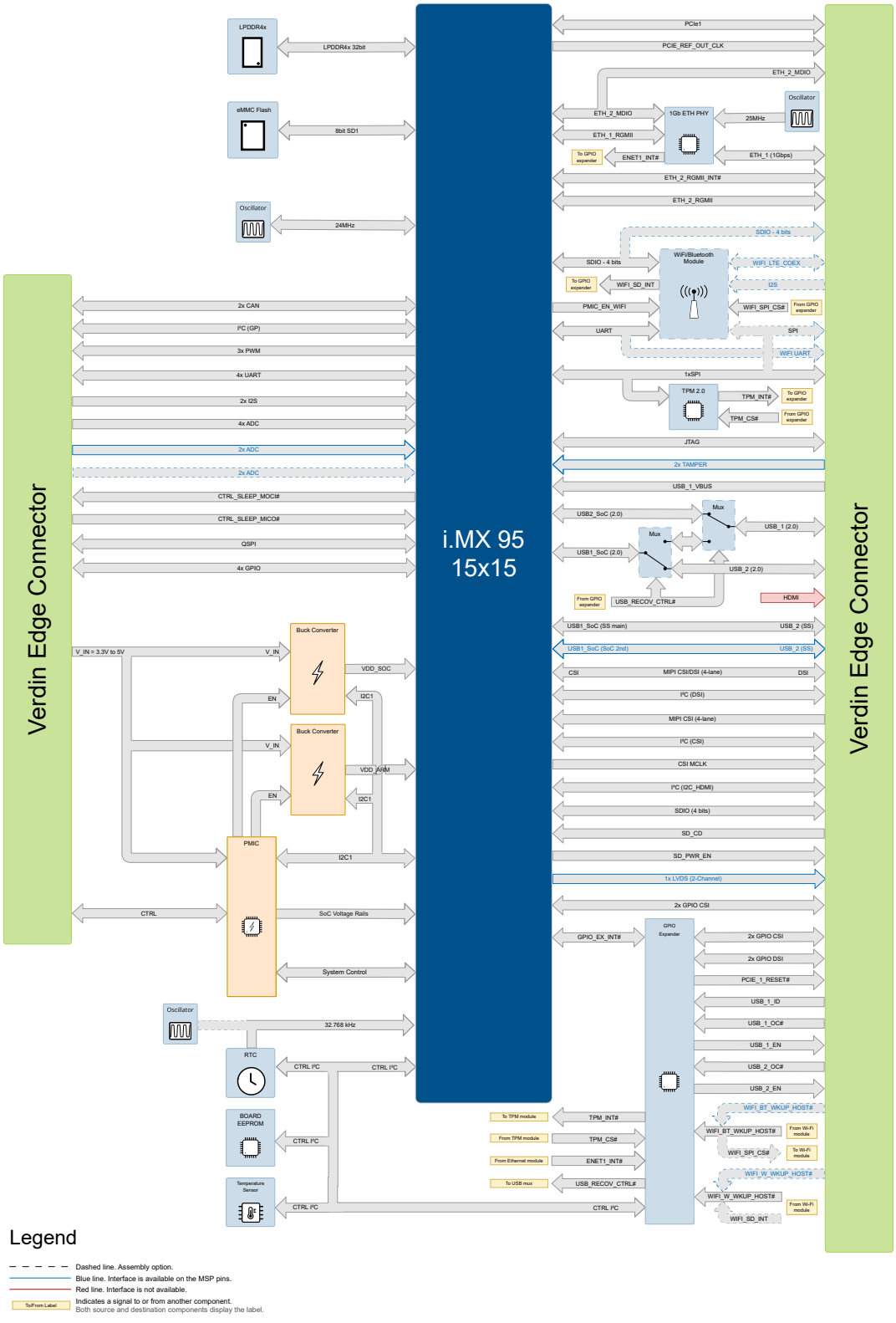
- Commercial: 0 °C - 70 °C
- Wide Temp: -25 °C - 85 °C
- Industrial: -40 °C - 85 °C

TPM 2.0 (on the SPI interface)

2 Architecture Overview

2.1 Block Diagram

Figure 1: Block Diagram



3 Verdin iMX95 Connector

3.1 Pin Numbering

The Verdin module follows the same pin numbering scheme as the DDR4 SODIMM standard. Pins on the top side of the module are odd-numbered, while pins on the bottom side are even-numbered.

Figure 2: Pin numbering (top)

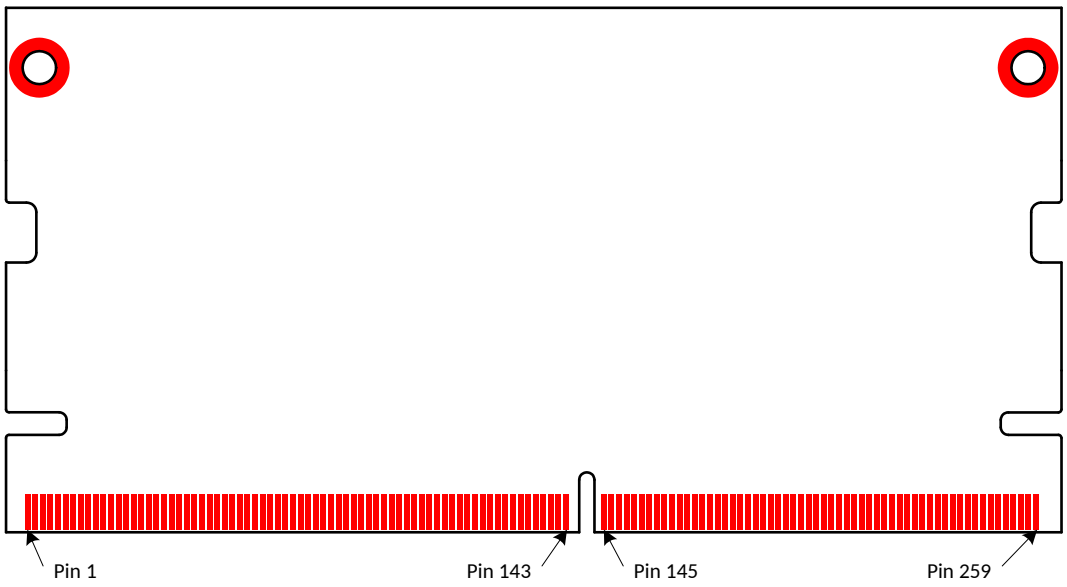
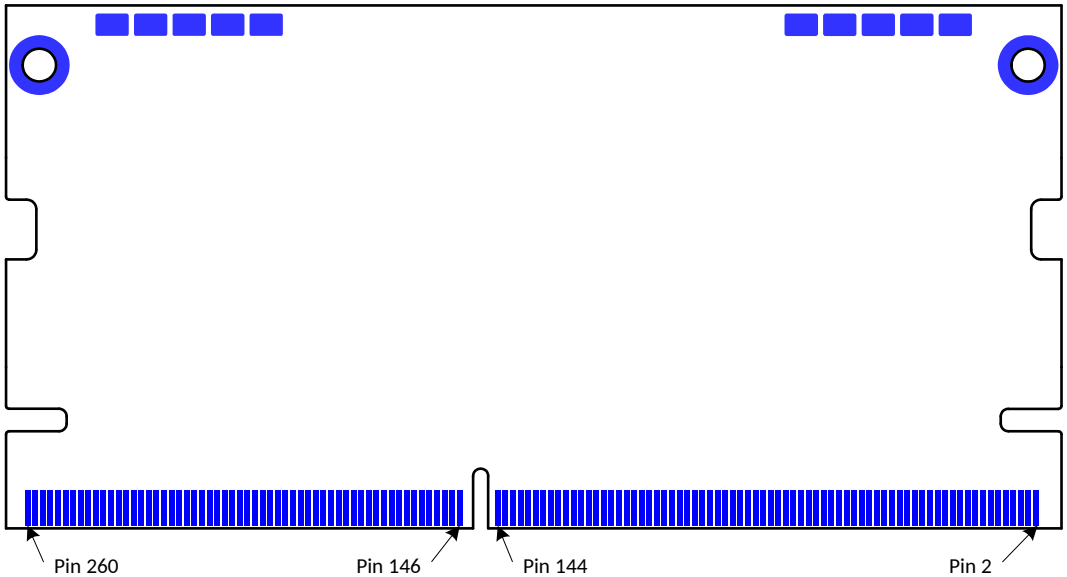


Figure 3: Pin numbering (bottom)



3.2 Pin Assignment

Table 8 and Table 9 describe the main connector (X1) pinout and highlight the compatibility of each pin's function with the Verdin Family Specification. A detailed explanation of the compatibility groups defined in the specification is available in Section 1.6.

Table 8: X1 pin assignment – top side – odd pins even pins – alternate functions

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
1	JTAG_1_TDI	Yes	Reserved	DAP_TDI		Pull-Up	
3	JTAG_1_TRST#	Yes	Reserved			–	Not connected.
5	JTAG_1_TDO	Yes	Reserved	DAP_TDO_TRACESWO		–	
7	JTAG_1_VREF	Yes	Reserved		1.8V	–	
9	JTAG_1_TCK	Yes	Reserved	DAP_TCLK_SWCLK		Pull-Down	
11	GND	Yes	Always Compatible		GND	–	
13	JTAG_1_TMS	Yes	Reserved	DAP_TMS_SWDIO		Pull-Up	
15	PWM_1	Yes	Always Compatible	GPIO_IO05		Pull-Down	
17	GPIO_9_DSI	Yes	Reserved		P0_2 *GPIO expander*	–	
19	PWM_3_DSI	Yes	Reserved	GPIO_IO19		Pull-Down	
21	GPIO_10_DSI	Yes	Reserved		P0_3 *GPIO expander*	–	
23	DSI_1_D3_N	Yes	Reserved	MIPI_DSICSI1_D3_N		–	
25	DSI_1_D3_P	Yes	Reserved	MIPI_DSICSI1_D3_P		–	
27	GND	Yes	Always Compatible		GND	–	
29	DSI_1_D2_N	Yes	Reserved	MIPI_DSICSI1_D2_N		–	
31	DSI_1_D2_P	Yes	Reserved	MIPI_DSICSI1_D2_P		–	
33	GND	Yes	Always Compatible		GND	–	
35	DSI_1_CLK_N	Yes	Reserved	MIPI_DSICSI1_CLK_N		–	
37	DSI_1_CLK_P	Yes	Reserved	MIPI_DSICSI1_CLK_P		–	
39	GND	Yes	Always Compatible		GND	–	
41	DSI_1_D1_N	Yes	Reserved	MIPI_DSICSI1_D1_N		–	
43	DSI_1_D1_P	Yes	Reserved	MIPI_DSICSI1_D1_P		–	

Continued on next page

Table 8: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
45	GND	Yes	Always Compatible		GND	–	
47	DSI_1_D0_N	Yes	Reserved	MIPI_DSICSI1_D0_N		–	
49	DSI_1_D0_P	Yes	Reserved	MIPI_DSICSI1_D0_P		–	
51	GND	Yes	Always Compatible		GND	–	
53	I2C_2_DSI_SDA	Yes	Reserved	GPIO_IO28		Pull-Down	
55	I2C_2_DSI_SCL	Yes	Reserved	GPIO_IO29		Pull-Down	
57	I2C_3_HDMI_SDA	Yes	Reserved	ENET1_MDIO		Pull-Down	
59	I2C_3_HDMI_SCL	Yes	Reserved	ENET1_MDC		Pull-Down	
61	HDMI_1_HPD	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
63	HDMI_1_CEC	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
65	GND	Yes	Always Compatible		GND	–	
67	HDMI_1_TXC_N	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
69	HDMI_1_TXC_P	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
71	GND	Yes	Always Compatible		GND	–	
73	HDMI_1_TXD0_N	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
75	HDMI_1_TXD0_P	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
77	GND	Yes	Always Compatible		GND	–	
79	HDMI_1_TXD1_N	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
81	HDMI_1_TXD1_P	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
83	GND	Yes	Always Compatible		GND	–	
85	HDMI_1_TXD2_N	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
87	HDMI_1_TXD2_P	No	Reserved			–	Not connected. HDMI not supported on Verdin i.MX 95.
89	GND	Yes	Always Compatible		GND	–	

Continued on next page

Table 8: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
91	CSI_1_MCLK	Yes	Reserved	CCM_CLKO1		Output low	
93	I2C_4_CSI_SDA	Yes	Reserved	GPIO_IO22		Pull-Down	
95	I2C_4_CSI_SCL	Yes	Reserved	GPIO_IO23		Pull-Down	
97	GND	Yes	Always Compatible		GND	–	
99	CSI_1_D3_P	Yes	Reserved	MIPI_CSI1_D3_P		–	
101	CSI_1_D3_N	Yes	Reserved	MIPI_CSI1_D3_N		–	
103	GND	Yes	Always Compatible		GND	–	
105	CSI_1_D2_P	Yes	Reserved	MIPI_CSI1_D2_P		–	
107	CSI_1_D2_N	Yes	Reserved	MIPI_CSI1_D2_N		–	
109	GND	Yes	Always Compatible		GND	–	
111	CSI_1_CLK_P	Yes	Reserved	MIPI_CSI1_CLK_P		–	
113	CSI_1_CLK_N	Yes	Reserved	MIPI_CSI1_CLK_N		–	
115	GND	Yes	Always Compatible		GND	–	
117	CSI_1_D1_P	Yes	Reserved	MIPI_CSI1_D1_P		–	
119	CSI_1_D1_N	Yes	Reserved	MIPI_CSI1_D1_N		–	
121	GND	Yes	Always Compatible		GND	–	
123	CSI_1_D0_P	Yes	Reserved	MIPI_CSI1_D0_P		–	
125	CSI_1_D0_N	Yes	Reserved	MIPI_CSI1_D0_N		–	
127	GND	Yes	Always Compatible		GND	–	
129	UART_1_RXD	Yes	Always Compatible	GPIO_IO09		Pull-Down	
131	UART_1_TXD	Yes	Always Compatible	GPIO_IO08		Pull-Down	
133	UART_1_RTS	Yes	Reserved	GPIO_IO11		Pull-Down	
135	UART_1_CTS	Yes	Reserved	GPIO_IO10		Pull-Down	

Continued on next page

Table 8: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
137	UART_2_RXD	Yes	Always Compatible	GPIO_IO13		Pull-Down	
139	UART_2_TXD	Yes	Always Compatible	GPIO_IO12		Pull-Down	
141	UART_2_RTS	Yes	Reserved	GPIO_IO15		Pull-Down	
143	UART_2_CTS	Yes	Reserved	GPIO_IO14		Pull-Down	
145	GND	Yes	Always Compatible	GND	GND	–	
147	UART_3_RXD	Yes	Always Compatible	UART1_RXD		Pull-Down	
149	UART_3_TXD	Yes	Always Compatible	UART1_TXD		Pull-Down	
151	UART_4_RXD	Yes	Reserved	UART2_RXD		Pull-Down	
153	UART_4_TXD	Yes	Reserved	UART2_TXD		Pull-Down	
155	USB_1_EN	Yes	Always Compatible		P0_7 *GPIO expander*	–	
157	USB_1_OC#	Yes	Always Compatible		P0_6 *GPIO expander*	–	
159	USB_1_VBUS	Yes	Always Compatible	USB2_VBUS		–	
161	USB_1_ID	Yes	Always Compatible		P0_5 *GPIO expander*	–	
163	USB_1_D_N	Yes	Always Compatible	USB2_D_N		–	
165	USB_1_D_P	Yes	Always Compatible	USB2_D_P		–	
167	GND	Yes	Always Compatible	_GND	GND	–	
169	USB_2_SSTX_N	Yes	Reserved	USB1_TX0_N		–	
171	USB_2_SSTX_P	Yes	Reserved	USB1_TX0_P		–	
173	GND	Yes	Always Compatible	_GND	GND	–	
175	USB_2_SSRX_N	Yes	Reserved	USB1_RX0_N		–	
177	USB_2_SSRX_P	Yes	Reserved	USB1_RX0_P		–	

Continued on next page

Table 8: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
179	GND	Yes	Always Compatible	_GND	GND	–	
181	USB_2_D_N	Yes	Always Compatible	USB1_D_N		–	
183	USB_2_D_P	Yes	Always Compatible	USB1_D_P		–	
185	USB_2_EN	Yes	Always Compatible		P1_0 *GPIO expander*	–	
187	USB_2_OC#	Yes	Always Compatible		P1_1 *GPIO expander*	–	
189	ETH_2_RGMII_INT#	Yes	Reserved	SAI1_TXC		–	
191	ETH_2_RGMII_MDIO	Yes	Reserved	ENET2_MDIO		–	
193	ETH_2_RGMII_MDC	Yes	Reserved	ENET2_MDC		–	
195	GND	Yes	Always Compatible		GND	–	
197	ETH_2_RGMII_RXC	Yes	Reserved	ENET2_RXC		–	
199	ETH_2_RGMII_RX_CTL	Yes	Reserved	ENET2_RX_CTL		–	
201	ETH_2_RGMII_RXD_0	Yes	Reserved	ENET2_RD0		–	
203	ETH_2_RGMII_RXD_1	Yes	Reserved	ENET2_RD1		–	
205	ETH_2_RGMII_RXD_2	Yes	Reserved	ENET2_RD2		–	
207	ETH_2_RGMII_RXD_3	Yes	Reserved	ENET2_RD3		–	
209	GND	Yes	Always Compatible		GND	–	
211	ETH_2_RGMII_TX_CTL	Yes	Reserved	ENET2_TX_CTL		–	
213	ETH_2_RGMII_TXC	Yes	Reserved	ENET2_TXC		–	
215	ETH_2_RGMII_TXD_3	Yes	Reserved	ENET2_TD3		–	
217	ETH_2_RGMII_TXD_2	Yes	Reserved	ENET2_TD2		–	
219	ETH_2_RGMII_TXD_1	Yes	Reserved	ENET2_TD1		–	
221	ETH_2_RGMII_TXD_0	Yes	Reserved	ENET2_TD0		–	

Continued on next page

Table 8: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
223	GND	Yes	Always Compatible		GND	–	
225	ETH_1_MDI0_P	Yes	Always Compatible		TD_P_A *Ethernet PHY*	–	
227	ETH_1_MDI0_N	Yes	Always Compatible		TD_M_A *Ethernet PHY*	–	
229	GND	Yes	Always Compatible		GND	–	
231	ETH_1_MDI1_N	Yes	Always Compatible		TD_M_B *Ethernet PHY*	–	
233	ETH_1_MDI1_P	Yes	Always Compatible		TD_P_B *Ethernet PHY*	–	
235	ETH_1_LED_1	Yes	Always Compatible		Circuit	–	
237	ETH_1_LED_2	Yes	Always Compatible		Circuit	–	
239	ETH_1_MDI2_P	Yes	Always Compatible		TD_P_C *Ethernet PHY*	–	
241	ETH_1_MDI2_N	Yes	Always Compatible		TD_M_C *Ethernet PHY*	–	
243	GND	Yes	Always Compatible		GND	–	
245	ETH_1_MDI3_N	Yes	Always Compatible		TD_M_D *Ethernet PHY*	–	
247	ETH_1_MDI3_P	Yes	Always Compatible		TD_P_D *Ethernet PHY*	–	
249	VCC_BACKUP	Yes	Always Compatible		VBAT *RTC battery*	–	
251	VCC	Yes	Always Compatible		VCC	–	3.135 to 5.5V input.
253	VCC	Yes	Always Compatible		VCC	–	3.135 to 5.5V input.
255	VCC	Yes	Always Compatible		VCC	–	3.135 to 5.5V input.
257	VCC	Yes	Always Compatible		VCC	–	3.135 to 5.5V input.

Continued on next page

Table 8: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
259	VCC	Yes	Always Compatible		VCC	–	3.135 to 5.5V input.

[1] The available pin functions comply with the definitions specified in the Verdin Family Specification.

Table 9: X1 pin assignment – bottom side – even pins odd pins – alternate functions

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
2	ADC_1	Yes	Reserved	ADC_IN0		–	
4	ADC_2	Yes	Reserved	ADC_IN1		–	
6	ADC_3	Yes	Reserved	ADC_IN2		–	
8	ADC_4	Yes	Reserved	ADC_IN3		–	
10	GND	Yes	Always Compatible		GND	–	
12	I2C_1_SDA	Yes	Always Compatible	GPIO_IO30		Pull-Down	
14	I2C_1_SCL	Yes	Always Compatible	GPIO_IO31		Pull-Down	
16	PWM_2	Yes	Reserved	GPIO_IO06		Pull-Down	
18	GND	Yes	Always Compatible		GND	–	
20	CAN_1_TX	Yes	Reserved	PDM_CLK		Pull-Down	
22	CAN_1_RX	Yes	Reserved	PDM_BIT_STREAM0		Pull-Down	
24	CAN_2_TX	Yes	Reserved	GPIO_IO25		Pull-Down	
26	CAN_2_RX	Yes	Reserved	GPIO_IO27		Pull-Down	
28	GND	Yes	Always Compatible		GND	–	
30	I2S_1_BCLK	Yes	Reserved	GPIO_IO16		Pull-Down	
32	I2S_1_SYNC	Yes	Reserved	GPIO_IO26		Pull-Down	
34	I2S_1_D_OUT	Yes	Reserved	GPIO_IO21		Pull-Down	
36	I2S_1_D_IN	Yes	Reserved	GPIO_IO20		Pull-Down	
38	I2S_1_MCLK	Yes	Reserved	GPIO_IO17		Pull-Down	
40	GND	Yes	Always Compatible		GND	–	
42	I2S_2_BCLK	Yes	Reserved	XSPI1_DATA6		Pull-Down	
44	I2S_2_SYNC	Yes	Reserved	XSPI1_DATA5		Pull-Down	
46	I2S_2_D_OUT	Yes	Reserved	XSPI1_DATA4		Pull-Down	

Continued on next page

Table 9: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
48	I2S_2_D_IN	Yes	Reserved	XSPI1_DATA7		Pull-Down	
50	GND	Yes	Always Compatible		GND	–	
52	QSPI_1_CLK	Yes	Reserved	XSPI1_SCLK		Pull-Down	
54	QSPI_1_CS#	Yes	Reserved	XSPI1_SS0_B		Pull-Down	
56	QSPI_1_IO0	Yes	Reserved	XSPI1_DATA0		Pull-Down	
58	QSPI_1_IO1	Yes	Reserved	XSPI1_DATA1		Pull-Down	
60	QSPI_1_IO2	Yes	Reserved	XSPI1_DATA2		Pull-Down	
62	QSPI_1_IO3	Yes	Reserved	XSPI1_DATA3		Pull-Down	
64	QSPI_1_CS2#	Yes	Reserved	XSPI1_SS1_B		Pull-Down	
66	QSPI_1_DQS	Yes	Reserved	XSPI1_DQS		Pull-Down	
68	GND	Yes	Always Compatible		GND	–	
70	SD_1_D2	Yes	Always Compatible	SD2_DATA2		Pull-Down	
72	SD_1_D3	Yes	Always Compatible	SD2_DATA3		Pull-Down	
74	SD_1_CMD	Yes	Always Compatible	SD2_CMD		Pull-Down	
76	SD_1_PWR_EN	Yes	Always Compatible	SD2_RESET_B		Pull-Down	
78	SD_1_CLK	Yes	Always Compatible	SD2_CLK		Pull-Down	
80	SD_1_D0	Yes	Always Compatible	SD2_DATA0		Pull-Down	
82	SD_1_D1	Yes	Always Compatible	SD2_DATA1		Pull-Down	
84	SD_1_CD#	Yes	Always Compatible	SD2_CD_B		Pull-Down	
86	GND	Yes	Always Compatible		GND	–	
88	MSP_1	–	Module-specific	LVDS0_CLK_N		–	
90	MSP_2	–	Module-specific	LVDS0_CLK_P		–	
92	MSP_3	–	Module-specific	TAMPER0		–	

Continued on next page

Table 9: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
94	MSP_4	–	Module-specific	LVDS0_D0_N		–	
96	MSP_5	–	Module-specific	LVDS0_D0_P		–	
98	GND	Yes	Always Compatible		GND	–	
100	MSP_6	–	Module-specific	LVDS0_D1_N		–	
102	MSP_7	–	Module-specific	LVDS0_D1_P		–	
104	MSP_8	–	Module-specific	TAMPER1		–	
106	MSP_9	–	Module-specific	LVDS0_D2_N		–	
108	MSP_10	–	Module-specific	LVDS0_D2_P		–	
110	GND	Yes	Always Compatible		GND	–	
112	MSP_11	–	Module-specific	LVDS0_D3_N		–	
114	MSP_12	–	Module-specific	LVDS0_D3_P		–	
116	MSP_13	Yes	Module-specific		GND	–	
118	MSP_14	–	Module-specific	LVDS1_CLK_N		–	
120	MSP_15	–	Module-specific	LVDS1_CLK_P		–	
122	GND	Yes	Always Compatible		GND	–	
124	MSP_16	–	Module-specific	LVDS1_D0_N		–	
126	MSP_17	–	Module-specific	LVDS1_D0_P		–	
128	MSP_18	–	Module-specific			–	
130	MSP_19	–	Module-specific	LVDS1_D1_N		–	
132	MSP_20	–	Module-specific	LVDS1_D1_P		–	
134	GND	Yes	Always Compatible		GND	–	
136	MSP_21	–	Module-specific	LVDS1_D2_N		–	
138	MSP_22	–	Module-specific	LVDS1_D2_P		–	

Continued on next page

Table 9: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
140	MSP_23	–	Module-specific		IRQ# *RTC*	–	
142	MSP_24	–	Module-specific	LVDS1_D3_N		–	
144	MSP_25	–	Module-specific	LVDS1_D3_P		–	
146	GND	Yes	Always Compatible		GND	–	
148	MSP_26	–	Module-specific	GPIO_IO34	PCM_CLK *Wi-Fi Module*	Pull-Down	UART assembly option on modules w/o Wi-Fi.
150	MSP_27	–	Module-specific	GPIO_IO33	PCM_DIN *Wi-Fi Module*	Pull-Down	UART assembly option on modules w/o Wi-Fi.
152	MSP_28	–	Module-specific	GPIO_IO04	PCM_DOUT *Wi-Fi Module*	Pull-Down	UART assembly option on modules w/o Wi-Fi.
154	MSP_29	–	Module-specific	GPIO_IO07	PCM_SYNC *Wi-Fi Module*	Pull-Down	UART assembly option on modules w/o Wi-Fi.
156	MSP_30	–	Module-specific	SD3_CLK		Pull-Down	SDIO on Modules w/o Wi-Fi
158	GND	Yes	Always Compatible		GND	–	
160	MSP_31	–	Module-specific	SD3_CMD		Pull-Down	SDIO assembly options on modules w/o Wi-Fi
162	MSP_32	–	Module-specific	SD3_DATA0		Pull-Down	SDIO assembly options on modules w/o Wi-Fi
164	MSP_33	–	Module-specific	SD3_DATA1		Pull-Down	SDIO assembly options on modules w/o Wi-Fi
166	MSP_34	–	Module-specific	SD3_DATA2		Pull-Down	SDIO assembly options on modules w/o Wi-Fi
168	MSP_35	–	Module-specific	SD3_DATA3		Pull-Down	SDIO assembly options on modules w/o Wi-Fi
170	GND	Yes	Always Compatible		GND	–	
172	MSP_36	–	Module-specific		WCI_SIN *Wi-Fi Module*	–	ADC assembly options on modules w/o Wi-Fi
174	MSP_37	–	Module-specific		WCI_SOUT *Wi-Fi Module*	–	ADC assembly options on modules w/o Wi-Fi
176	MSP_38	–	Module-specific		PCM_MCLK *Wi-Fi Module*	–	

Continued on next page

Table 9: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
178	MSP_39	–	Module-specific	USB1_TX1_N		–	
180	MSP_40	–	Module-specific	USB1_TX1_P		–	
182	GND	Yes	Module-specific		GND	–	
184	MSP_41	–	Module-specific	USB1_RX1_N		–	
186	MSP_42	–	Module-specific	USB1_RX1_P		–	
188	MSP_43	–	Module-specific			–	Used for high-frequency noise suppression and ESD protection
190	MSP_44	–	Module-specific	ADC_IN4		–	
192	MSP_45	–	Module-specific	ADC_IN5		–	
194	GND	Yes	Always Compatible		GND	–	
196	SPI_1_CLK	Yes	Always Compatible	GPIO_IO03		Pull-Down	
198	SPI_1_MISO	Yes	Always Compatible	GPIO_IO01		Pull-Down	
200	SPI_1_MOSI	Yes	Always Compatible	GPIO_IO02		Pull-Down	
202	SPI_1_CS	Yes	Always Compatible	CCM_CLKO4		Pull-Down	
204	GND	Yes	Always Compatible		GND	–	
206	GPIO_1	Yes	Always Compatible	GPIO_IO00		Pull-Down	
208	GPIO_2	Yes	Always Compatible	GPIO_IO18		Pull-Down	
210	GPIO_3	Yes	Always Compatible	GPIO_IO24		Pull-Down	
212	GPIO_4	Yes	Always Compatible	GPIO_IO32		Pull-Down	
214	PWR_1V8_MOCI	Yes	Always Compatible		1.8V	–	
216	GPIO_5_CSI	Yes	Always Compatible	CCM_CLKO3		Pull-Down	
218	GPIO_6_CSI	Yes	Always Compatible	CCM_CLKO2		Output Low	
220	GPIO_7_CSI	Yes	Always Compatible		P_0 *GPIO expander*	–	

Continued on next page

Table 9: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible fuction[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
222	GPIO_8_CSI	Yes	Always Compatible		P_1 *GPIO expander*	–	
224	GND	Yes	Always Compatible		GND	–	
226	PCIE_1_CLK_N	Yes	Reserved	PCIE_REF_OUT_CLK_N		–	
228	PCIE_1_CLK_P	Yes	Reserved	PCIE_REF_OUT_CLK_P		–	
230	GND	Yes	Always Compatible			–	
232	PCIE_1_L0_RX_N	Yes	Reserved	PCIE1_RX0_N		–	
234	PCIE_1_L0_RX_P	Yes	Reserved	PCIE1_RX0_P		–	
236	GND	Yes	Always Compatible	_GND		–	
238	PCIE_1_L0_TX_N	Yes	Reserved	PCIE1_TX0_N		–	
240	PCIE_1_L0_TX_P	Yes	Reserved	PCIE1_TX0_P		–	
242	GND	Yes	Always Compatible		GND	–	
244	PCIE_1_RESET#	Yes	Reserved		P0_4 *GPIO expander*	–	
246	CTRL_RECOVERY_MICO#	Yes	Always Compatible	Circuit	Recovery Circuit	–	
248	CTRL_PWR_BTN_MICO#	Yes	Always Compatible	ONOFF		–	
250	CTRL_FORCE_OFF_MOCI#	Yes	Always Compatible		PMIC	–	
252	CTRL_WAKE1_MICO#	Yes	Always Compatible	PDM_BIT_STREAM1		Pull-Down	
254	CTRL_PWR_EN_MOCI	Yes	Always Compatible		PMIC	–	
256	CTRL_SLEEP_MOCI#	Yes	Always Compatible	SAI1_RXD0		Pull-Down	
258	CTRL_RESET_MOCI#	Yes	Always Compatible		PMIC	–	
260	CTRL_RESET_MICO#	Yes	Always Compatible		PMIC	–	

[1] The available pin functions comply with the definitions specified in the Verdin Family Specification.

4 I/O Pins

4.1 Function Multiplexing

Low-speed I/O pins on the NXP i.MX 95 SoC can be configured for up to seven alternate functions. Most of these pins can also be used as GPIOs (general-purpose I/O, sometimes referred to as digital I/O). For example, the i.MX 95 signal connected to SODIMM pin 131 exposes the SoC alternate function UART7_TX, which corresponds to the Verdin standard function UART_1_TXD. In addition to this UART function, the pin can also be configured as:

- GPIO2_IO8 (GPIO)
- SPI3_PCS0 (SPI chip select 0)
- TPM6_CH0 (TPM channel 0)
- I2C7_SDA (I²C data line)
- FLEXIO1_FLEXIO8 (Flexible I/O module)

Whenever possible, **it is strongly recommended to use functions that are compatible across all Verdin modules**. This ensures maximum compatibility with standard software and other modules in the Verdin Family.

Some alternate functions are available on more than one pin. **Care must be taken to avoid assigning the same function to multiple pins simultaneously**, as this can result in system instability or undefined behavior.

Table 10 lists all pins that support alternate functions, along with the alternate functions available for each pin. Alternate functions highlighted in bold indicate the primary interfaces selected for optimal Verdin compatibility.

Table 10: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom)

X1 pin	SoC ball name	SoC ball ID *T package*	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6	ALT 7
1	DAP_TDI	AJ8	**DAP_TDI**	MQS2_LEFT	NETC_TMR_1588_ALARM1	CAN2_TX	FLEXIO2_FLEXIO30	GPIO3_IO28	UART5_RX	
5	DAP_TDO_TRACESW	AE12	**DAP_TDO_TRACESWO**	MQS2_RIGHT	NETC_TMR_1588_ALARM2	CAN2_RX	FLEXIO1_FLEXIO31	GPIO3_IO31	UART5_TX	
9	DAP_TCLK_SWCLK	AJ9	**DAP_TCLK_SWCLK**		CAN4_RX		FLEXIO1_FLEXIO30	GPIO3_IO30	UART5_CTS_B	
13	DAP_TMS_SWDIO	AH8	**DAP_TMS_SWDIO**		CAN4_TX		FLEXIO2_FLEXIO31	GPIO3_IO29	UART5_RTS_B	
15	GPIO_IO05	N25	GPIO2_IO05	**TPM4_CH0**	PDM_BIT_STREAM0	CAN4_RX	SPI7_SIN	UART6_RX	I2C6_SCL	FLEXIO1_FLEXIO5
19	GPIO_IO19	U29	GPIO2_IO19	SAI3_RX_SYNC	PDM_BIT_STREAM3	FLEXIO1_FLEXIO19	SPI5_SIN	SPI4_SIN	**TPM6_CH2**	SAI3_TX_DATA0
53	GPIO_IO28	AA24	GPIO2_IO28	**I2C3_SDA**	CAN3_TX					FLEXIO1_FLEXIO28
55	GPIO_IO29	AA25	GPIO2_IO29	**I2C3_SCL**	CAN3_RX					FLEXIO1_FLEXIO29
57	ENET1_MDIO	AH16	NETC_MDIO	UART3_RIN_B	**I3C2_SDA**	USB1_OTG_PWR	FLEXIO2_FLEXIO1	GPIO4_IO1		
59	ENET1_MDC	AJ17	NETC_MDC	UART3_DCB_B	**I3C2_SCL**	USB1_OTG_ID	FLEXIO2_FLEXIO0	GPIO4_IO0		
91	CCM_CLKO1	AF10	**CCMSRCGPCMIX_CLKO1**	NETC_TMR_1588_TRIG1			FLEXIO1_FLEXIO26	GPIO3_IOIO26		
93	GPIO_IO22	W24	GPIO2_IO22	USDHC3_CLK	SPDIF1_IN	CAN5_TX	TPM5_CH1	TPM6_EXTCLK	**I2C5_SDA**	FLEXIO1_FLEXIO22
95	GPIO_IO23	W25	GPIO2_IO23	USDHC3_CMD	SPDIF1_OUT	CAN5_RX	TPM6_CH1		**I2C5_SCL**	FLEXIO1_FLEXIO23
129	GPIO_IO09	P29	GPIO2_IO9	SPI3_SIN			TPM3_EXTCLK	**UART7_RX**	I2C7_SCL	FLEXIO1_FLEXIO9
131	GPIO_IO08	P28	GPIO2_IO8	SPI3_PCS0			TPM6_CH0	**UART7_TX**	I2C7_SDA	FLEXIO1_FLEXIO8
133	GPIO_IO11	R25	GPIO2_IO11	SPI3_SCK			TPM5_EXTCLK	**UART7_RTS_B**	I2C8_SCL	FLEXIO1_FLEXIO11
135	GPIO_IO10	R24	GPIO2_IO10	SPI3_SOUT			TPM4_EXTCLK	**UART7_CTS_B**	I2C8_SDA	FLEXIO1_FLEXIO10
137	GPIO_IO13	R29	GPIO2_IO13	TPM4_CH2	PDM_BIT_STREAM3		SPI8_SIN	**UART8_RX**	I2C8_SCL	FLEXIO1_FLEXIO13
139	GPIO_IO12	R28	GPIO2_IO12	TPM3_CH2	PDM_BIT_STREAM2	FLEXIO1_FLEXIO12	SPI8_PCS0	**UART8_TX**	I2C8_SDA	SAI3_RX_SYNC
141	GPIO_IO15	T29	GPIO2_IO15	UART3_RX			SPI8_SCK	**UART8_RTS_B**	UART4_RX	FLEXIO1_FLEXIO15
143	GPIO_IO14	T28	GPIO2_IO14	UART3_TX			SPI8_SOUT	**UART8_CTS_B**	UART4_TX	FLEXIO1_FLEXIO14
147	UART1_RXD	G28	**UART1_RX**	SECO_RX	SPI2_SIN	TPM1_CH0	VPU_UART_RX	GPIO1_IO04		
149	UART1_TXD	F29	**UART1_TX**	SECO_TX	SPI2_PCS0	TPM1_CH1	VPU_UART_TX	GPIO1_IO05		

Continued on next page

Table 10: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *T package*	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6	ALT 7
151	UART2_RXD	J25	**UART2_RX**	UART1_CTS_B	SPI2_SOUT	TPM1_CH2	SAI1_MCLK	GPIO1_IO06		
153	UART2_TXD	J26	**UART2_TX**	UART1_RTS_B	SPI2_SCK	TPM1_CH3		GPIO1_IO07		
189	SAI1_TXC	J28	**SAI1_TX_BCLK**	UART2_CTS_B	SPI1_SIN	UART1_DSR_B	CAN1_RX	GPIO1_IO12		
191	ENET2_MDIO	AH12	**NETC_MDIO**	UART4_RIN_B	SAI2_RX_BCLK		FLEXIO2_FLEXIO15	GPIO4_IO15		
193	ENET2_MDC	AJ8	**NETC_MDC**	UART4_DCB_B	SAI2_RX_SYNC		FLEXIO2_FLEXIO14	GPIO4_IO14		
197	ENET2_RXC	AH9	**NETC_ETH1_RGMII_RX_CLK**	NETC_ETH1_RMII_RX_ER	SAI2_TX_DATA1	SAI4_RX_SYNC	FLEXIO2_FLEXIO23	GPIO4_IO23		
199	ENET2_RX_CTL	AJ10	**NETC_ETH1_RGMII_RX_CTL**	UART4_DSR_B	SAI2_TX_DATA0		FLEXIO2_FLEXIO22	GPIO4_IO22	NETC_ETH1_RMII_CRS_DV	
201	ENET2_RD0	AH10	**NETC_ETH1_RGMII_RXD0**	UART4_RX	SAI2_TX_DATA2	SAI4_RX_BCLK	FLEXIO2_FLEXIO24	GPIO4_IO24	NETC_ETH1_RMII_RXD0	
203	ENET2_RD1	AJ11	**NETC_ETH1_RGMII_RXD1**	SPDIF1_IN	SAI2_TX_DATA3	SAI4_RX_DATA0	FLEXIO2_FLEXIO25	GPIO4_IO25	NETC_ETH1_RMII_RXD1	
205	ENET2_RD2	AH11	**NETC_ETH1_RGMII_RXD2**	UART4_CTS_B	SAI2_MCLK	MQS2_RIGHT	FLEXIO2_FLEXIO26	GPIO4_IO26	NETC_ETH1_RMII_RX_ER	
207	ENET2_RD3	AJ12	**NETC_ETH1_RGMII_RXD3**	SPDIF1_OUT	SPDIF1_IN	MQS2_LEFT	FLEXIO2_FLEXIO27	GPIO4_IO27		
211	ENET2_TX_CTL	AC12	**ETH1_RGMII_TX_CTL**	UART4_DTR_B	SAI2_TX_SYNC	ETH1_RMII_TX_EN	FLEXIO2_FLEXIO20	GPIO4_IO20		
213	ENET2_TXC	AD12	**NETC_ETH1_RGMII_TX_CLK**	CCMSRCGPCMIX_ENET_CLK_ROOT	SAI2_TX_BCLK		FLEXIO2_FLEXIO21	GPIO4_IO21		
215	ENET2_TD3	AD16	**NETC_ETH1_RGMII_TXD3**		SAI2_RX_DATA0		FLEXIO2_FLEXIO16	GPIO4_IO16		
217	ENET2_TD2	AC14	**NETC_ETH1_RGMII_TXD2**	INPUT: NETC_ETH1_RMII_REF50_CLK OUTPUT: CCMSRCGPCMIX_ENET_REF_CLK_ROOT[1]	SAI2_RX_DATA1	SAI4_TX_SYNC	FLEXIO2_FLEXIO17	GPIO4_IO17		
219	ENET2_TD1	AD14	**NETC_ETH1_RGMII_TXD1**	UART4_RTS_B	SAI2_RX_DATA2	SAI4_TX_BCLK	FLEXIO2_FLEXIO18	GPIO4_IO18	NETC_ETH1_RMII_TXD1	
221	ENET2_TD0	AE14	**NETC_ETH1_RGMII_TXD0**	UART4_TX	SAI2_RX_DATA3	SAI4_TX_DATA0	FLEXIO2_FLEXIO19	GPIO4_IO19	NETC_ETH1_RMII_TXD0	
12	GPIO_IO30	G25	GPIO2_IO30	**I2C4_SDA**	CAN5_TX					FLEXIO1_FLEXIO30
14	GPIO_IO31	G26	GPIO2_IO31	**I2C4_SCL**	CAN5_RX					FLEXIO1_FLEXIO31
16	GPIO2_IO6	N28	GPIO2_IO6	**TPM5_CH0**	PDM_BIT_STREAM1		SPI7_SOUT	UART6_CTS_B	I2C7_SDA	FLEXIO1_FLEXIO6
20	PDM_CLK	H29	PDM_CLK	MQS1_LEFT			LPTMR1_ALT1	GPIO1_IO08	**CAN1_TX**	
22	PDM_BIT_STREAM0	H28	PDM_BIT_STREAM0	MQS1_RIGHT	SPI1_PCS1	TPM1_EXTCLK	LPTMR1_ALT2	GPIO1_IO09	**CAN1_RX**	
24	GPIO_IO25	W29	GPIO2_IO25	USDHC3_DATA1	**CAN2_TX**		TPM4_CH3	DAP_TCLK_SWCLK	SPI7_PCS1	FLEXIO1_FLEXIO25

Continued on next page

Table 10: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *T package*	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6	ALT 7
26	GPIO_IO27	Y29	GPIO2_IO27	USDHC3_DATA3	**CAN2_RX**		TPM6_CH3	DAP_TMS_SWDIO	SPI5_PCS1	FLEXIO1_FLEXIO27
30	GPIO_IO16	U25	GPIO2_IO16	**SAI3_TX_BCLK**	PDM_BIT_STREAM2		UART3_CTS_B	SPI4_PCS2	UART4_CTS_B	FLEXIO1_FLEXIO16
32	GPIO_IO26	Y28	GPIO2_IO26	USDHC3_DATA2	PDM_BIT_STREAM1	FLEXIO1_FLEXIO26	TPM5_CH3	DAP_TDI	SPI8_PCS1	**SAI3_TX_SYNC**
34	GPIO_IO21	V29	GPIO2_IO21	**SAI3_TX_DATA0**	PDM_CLK	FLEXIO1_FLEXIO21	SPI5_SCK	SPI4_SCK	TPM4_CH1	SAI3_RX_BCLK
36	GPIO_IO20	V28	GPIO2_IO20	**SAI3_RX_DATA0**	PDM_BIT_STREAM0		SPI5_SOUT	SPI4_SOUT	TPM3_CH1	FLEXIO1_FLEXIO20
38	GPIO_IO17	U26	GPIO2_IO17	**SAI3_MCLK**			UART3_RTS_B	SPI4_PCS1	UART4_RTS_B	FLEXIO1_FLEXIO17
42	XSPI1_DATA6	AH22	**FLEXSPI_A_DATA6**	SAI5_TX_BCLK	SAI5_RX_DATA3	SAI2_RX_DATA7	XSPI_SLV_DATA6	GPIO5_IO6		
44	XSPI1_DATA5	AJ22	**FLEXSPI_A_DATA5**	SAI5_TX_SYNC	SAI5_RX_DATA2	SAI2_RX_DATA6	XSPI_SLV_DATA5	GPIO5_IO5		
46	XSPI1_DATA4	AH21	**FLEXSPI_A_DATA4**	SAI5_TX_DATA0	SAI5_RX_DATA1		XSPI_SLV_DATA4	GPIO5_IO4		
48	XSPI1_DATA7	AJ23	**FLEXSPI_A_DATA7**	SAI5_RX_DATA0	SAI5_TX_DATA1		XSPI_SLV_DATA7	GPIO5_IO7		
52	XSPI1_SCLK	AH18	**FLEXSPI_A_SCLK**	SAI2_RX_DATA4	SAI4_RX_SYNC	EARC_HPD	XSPI_SLV_CLK	GPIO5_IO9		
54	XSPI1_SS0_B	AH17	**FLEXSPI_A_SS0_B**	SAI2_RX_DATA5	SAI4_RX_BCLK	EARC_CEC	XSPI_SLV_CS	GPIO5_IO10		
56	XSPI1_DATA0	AH19	**FLEXSPI_A_DATA0**	SAI2_TX_DATA4	SAI4_TX_BCLK	SAI4_RX_DATA1	XSPI_SLV_DATA0	GPIO5_IO0		
58	XSPI1_DATA1	AJ20	**FLEXSPI_A_DATA1**	SAI2_TX_DATA5	SAI4_TX_SYNC	SAI4_TX_DATA1	XSPI_SLV_DATA1	GPIO5_IO1		
60	XSPI1_DATA2	AH20	**FLEXSPI_A_DATA2**	SAI2_TX_DATA6	SAI4_TX_DATA0		XSPI_SLV_DATA2	GPIO5_IO2		
62	XSPI1_DATA3	AJ21	**FLEXSPI_A_DATA3**	SAI2_TX_DATA7	SAI4_RX_DATA0		XSPI_SLV_DATA3	GPIO5_IO3		
64	XSPI1_SS1_B	AJ18	**FLEXSPI_A_SS1_B**	SAI5_RX_BCLK	SAI5_TX_DATA3	SAI2_RX_DATA7		GPIO5_IO11		
66	XSPI1_DQS	AJ19	**FLEXSPI_A_DQS**	SAI5_RX_SYNC	SAI5_TX_DATA2	SAI2_RX_DATA6	XSPI_SLV_DQS	GPIO5_IO8		
70	SD2_DATA2	AD29	**USDHC2_DATA2**	NETC_TMR_1588_PP3	MQS2_RIGHT		FLEXIO1_FLEXIO5	GPIO3_IO5		
72	SD2_DATA3	AD28	**USDHC2_DATA3**	LPTMR2_ALT1	MQS2_LEFT	NETC_TMR_1588_ALARM1	FLEXIO1_FLEXIO6	GPIO3_IO6		
74	SD2_CMD	AE29	**USDHC2_CMD**	NETC_TMR_1588_TRIG2	I3C2_PUR	I3C2_PUR_B	FLEXIO1_FLEXIO2	GPIO3_IO2		
76	SD2_RESET_B	G28	**USDHC2_RESET_B**	LPTMR2_ALT2		NETC_TMR_1588_GCLK	FLEXIO1_FLEXIO7	GPIO3_IO7		
78	SD2_CLK	AE28	**USDHC2_CLK**	NETC_TMR_1588_PP1	I3C2_SDA		FLEXIO1_FLEXIO1	GPIO3_IO1		

Continued on next page

Table 10: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *T package*	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6	ALT 7
80	SD2_DATA0	AF29	**USDHC2_DATA0**	NETC_TMR_1588_PP2	CAN2_TX		FLEXIO1_FLEXIO3	GPIO3_IO3		
82	SD2_DATA1	AF28	**USDHC2_DATA1**	NETC_TMR_1588_CLK	CAN2_RX		FLEXIO1_FLEXIO4	GPIO3_IO4		
84	SD2_CD_B	AG29	**USDHC2_CD_B**	NETC_TMR_1588_TRIG1	I3C2_SCL		FLEXIO1_FLEXIO0	GPIO3_IO0		
148	GPIO_IO34	AC25	GPIO5_IO14		UART6_CTS_B		SPI4_PCS0			
150	GPIO_IO33	AB29	GPIO5_IO13		UART6_RX		SPI4_PCS1			
152	GPIO_IO04	N24	GPIO5_IO14	TPM3_CH0	PDM_CLK	CAN4_TX	SPI7_PCS0	UART6_TX	I2C6_SDA	FLEXIO1_FLEXIO4
154	GPIO_IO07	N29	GPIO2_IO7	SPI3_PCS1			SPI7_SCK	UART6_RTS_B	I2C7_SCL	FLEXIO1_FLEXIO7
156	SD3_CLK	AD22	USDHC3_CLK	FLEXSPI_A_SCLK	SAI5_TX_DATA1	SAI5_RX_DATA0	FLEXIO1_FLEXIO20	GPIO3_IO20	XSPI_SLV_CLK	
160	SD3_CMD	AC22	USDHC3_CMD	FLEXSPI_A_SS0_B	SAI5_TX_DATA2	SAI5_RX_SYNC	FLEXIO1_FLEXIO21	GPIO3_IO21	XSPI_SLV_CS	
162	SD3_DATA0	AE22	USDHC3_DATA0	FLEXSPI_A_DATA0	SAI5_TX_DATA3	SAI5_RX_BCLK	FLEXIO1_FLEXIO22	GPIO3_IO22	XSPI_SLV_DATA0	
164	SD3_DATA1	AC20	USDHC3_DATA1	FLEXSPI_A_DATA1	SAI5_RX_DATA1	SAI5_TX_DATA0	FLEXIO1_FLEXIO23	GPIO3_IO23	XSPI_SLV_DATA1	
166	SD3_DATA2	AD24	USDHC3_DATA2	FLEXSPI_A_DATA2	SAI5_RX_DATA2	SAI5_TX_SYNC	FLEXIO1_FLEXIO24	GPIO3_IO24	XSPI_SLV_DATA2	
168	SD3_DATA3	AE24	USDHC3_DATA3	FLEXSPI_A_DATA3	SAI5_RX_DATA3	SAI5_TX_BCLK	FLEXIO1_FLEXIO25	GPIO3_IO25	XSPI_SLV_DATA3	
196	GPIO_IO03	M29	GPIO2_IO3	I2C4_SCL			**SPI6_SCK**	UART5_RTS_B	I2C6_SCL	FLEXIO1_FLEXIO3
198	GPIO_IO01	L29	GPIO2_IO1	I2C3_SCL			**SPI6_SIN**	UART5_RX	I2C5_SCL	FLEXIO1_FLEXIO1
200	GPIO_IO02	M28	GPIO2_IO2	I2C4_SDA			**SPI6_SOUT**	UART5_CTS_B	I2C6_SDA	FLEXIO1_FLEXIO2
202	CCM_CLKO4	AD10	CCMSRCGPCMIX_CLKO4	NETC_TMR_1588_PP2	CAN3_RX		FLEXIO2_FLEXIO29	**GPIO4_IO29**		
206	GPIO_IO00	L28	**GPIO2_IO0**	I2C3_SDA			SPI6_PCS0	UART5_TX	I2C5_SDA	FLEXIO1_FLEXIO0
208	GPIO_IO18	U28	**GPIO2_IO18**	SAI3_RX_BCLK			SPI5_PCS0	SPI4_PCS0	TPM5_CH2	FLEXIO1_FLEXIO18
210	GPIO_IO24	W28	**GPIO2_IO24**	USDHC3_DATA0			TPM3_CH3	DAP_TDO_TRACESWO	SPI6_PCS1	FLEXIO1_FLEXIO24
212	GPIO_IO32	AB28	**GPIO5_IO12**	PCIE1_CLKREQ_B	UART6_TX		SPI4_PCS2			
216	CCM_CLKO3	AE10	CCMSRCGPCMIX_CLKO3	NETC_TMR_1588_TRIG2	CAN3_TX		FLEXIO2_FLEXIO28	**GPIO4_IO28**		
218	CCM_CLKO2	AF8	CCMSRCGPCMIX_CLKO2	NETC_TMR_1588_PP1			FLEXIO1_FLEXIO27	**GPIO3_IO27**		

Continued on next page

Table 10: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *T package*	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6	ALT 7
252	PDM_BIT_STREAM1	G29	PDM_BIT_STREAM1	M33_NMI	SPI2_PCS1	TPM2_EXTCLK	LPTMR1_ALT3	**GPIO1_IO10**		
256	SAI1_RXD0	J29	SAI1_RX_DATA0	SAI1_MCLK	SPI1_SOUT	UART2_DSR_B	MQS1_RIGHT	**GPIO1_IO14**		

[1] This pin assumes different functions depending on whether it is configured as an input or an output. This selection is controlled by the software pinmux and direction settings.

***Bold** text*: Alternate function that provides maximum compatibility between modules of the Verdin family.

Rows in : Module-specific interface.

Rows in : The highlighted pins are output-only, so they can't be used for boot mode selection or as inputs in standard product configurations. A custom Build-to-Order (BTO) configuration can allow the pins to be used for boot mode selection or as inputs.

4.2 Pin Control

The alternate function of each pin can be configured independently. Each pin has a Pad Mux register where various settings can be defined (note that some settings may not be available for certain pins). The register is named IOMUXC_SW_MUX_CTL_PAD_x, where x corresponds to the name of the i.MX 95 pin.

Table 11: Pad control register

Bit	Field	Description	Remarks
31-5	Reserverd		
4	SION	0 Software Input On Field disabled 1 Software Input On Field enable	Force the selected mux mode input path.
3	Reserved		
2-0	MUX_MODE	000 Select mux mode: ALT0 mux port 001 Select mux mode: ALT1 mux port 010 Select mux mode: ALT2 mux port 011 Select mux mode: ALT3 mux port 100 Select mux mode: ALT4 mux port 101 Select mux mode: ALT5 mux port (GPIO) 110 Select mux mode: ALT6 mux port	Check Section section 4.1 for the available alternate function of the pin.

Each pin also has an associated register that allows configuration of pull-up/pull-down resistors, drive strength, and other electrical settings. This register is named IOMUXC_SW_PAD_CTL_PAD_x, where x corresponds to the name of the i.MX 95 pin. Note that some settings may not be available on all pins.

Input functions available on more than one physical pin require an additional input multiplexer. This multiplexer is configured using a register named IOMUXC_x_SELECT_INPUT, where x corresponds to the name of the input function.

Table 12: Pad mux register

Bit	Field	Description
31-28	APC_LCK	APC lock bits APC_LCK[3:0] are lock bits for APC[3:0], they are one-to-one mapped: APC_LCK[3] locks APC[3] APC_LCK[2] locks APC[2] APC_LCK[1] locks APC[1] APC_LCK[0] locks APC[0] Once an APC_LCK lock bit is set, the corresponding APC data bit cannot be changed. APC_LCK bits are sticky bits, which means that once they are set to 1, they cannot be set to 0 unless reset is performed.
27-24	APC	Domain Access Field The Domain Access bits control whether the corresponding domain can access the IOMUX registers. When set to 1, the corresponding domain cannot access the IOMUX register. When set to 0, the corresponding domain can access the IOMUX register. Select one out of next values for pad: <PAD_NAME> 0000 ... 1111
23-16	Reserved	

Continued on next page

Table 12: Pad mux register (Continued)

Bit	Field	Description
15-13	SMIC	Safe Mode Control Bypasses pin safe-stating: • When SMC is enabled, pin safe-stating is allowed. FCCU fault reaction disables the pin by keeping the OBE field value to 1'b0. • When SMC is disabled, pin safe-stating by FCCU fault reaction is bypassed and does not affect the pin. Pin safe-stating is managed per application domains. Accordingly, SMC manages pin safe-state bypassing by application domains. 000b - Disabled on all four application domains 001b - Enabled safe stating for application domain 1 010b - Enabled safe stating for application domain 2 011b - Enabled safe stating for application domain 1 and application domain 2 100b - Enabled safe stating for application domain 3 101b - Enabled safe stating for application domain 1 and application domain 3 110b - Enabled safe stating for application domain 2 and application domain 3 111b - Enabled safe stating for all application domains
12	HYS	Schmitt trigger Field Select one out of next values for pad: SAI1_TXD0 0b - No Schmitt input 1b - Schmitt input
11	OD	Open Drain Field Select one out of next values for pad: SAI1_TXD0 0b - Open Drain Disable 1b - Open Drain Enable
10	PD	Pull Down Field Select one out of next values for pad: SAI1_TXD0 0b - Not pull down 1b - Pull down
9	PU	Pull Up Field Select one out of next values for pad: SAI1_TXD0 0b - No pull up 1b - Pull up
8-7	FSEL1	Slew Rate Field Select one out of next values for pad: SAI1_TXD0 00b - 01b - 10b - Slight Fast Slew Rate 11b - Fast Slew Rate
6-1	DSE	Drive Strength Field Select one out of next values for pad: SAI1_TXD0 00_0000b - No drive 00_0001b - x1 00_0011b - x2 00_0111b - x3 00_1111b - x4 01_1111b - x5 11_1111b - X6
0	Reserved	

For more information about the available register settings, refer to the i.MX 95 Reference Manual[1].

4.3 Pin Reset Status

After a reset, i.MX 95 pins can be in different modes. Most are pulled low, while some are in a high-impedance state or pulled high. Refer to Section 3.2 for a complete list of the reset states of each pin. Once the bootloader is running, pins and their states can be reconfigured.

Pin reset states are only guaranteed during the release of the reset signal. During the power-up sequence, pin states may be undefined until the corresponding I/O bank voltage is enabled on the module.

[1] https://www.nxp.com/products/i.MX95

5 Interface Description

5.1 ADC – Analog to Digital Converter

Table 13: ADC pins

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function	I/O *SoM perspective*	Description
2	ADC_1	ADC_IN0	ALT0 [1]	I	Analog Input 1
4	ADC_2	ADC_IN1	ALT0 [1]	I	Analog Input 2
6	ADC_3	ADC_IN2	ALT0 [1]	I	Analog Input 3
8	ADC_4	ADC_IN3	ALT0 [1]	I	Analog Input 4

[1] This pin has no alternate functions.

Table 14: ADC assembly options on modules without Wi-Fi

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function	I/O *SoM perspective*	Description
172	MSP_36	ADC_IN6	ALT0 [1]	I	Analog Input 6
174	MSP_37	ADC_IN7	ALT0 [1]	I	Analog Input 7

[1] This pin has no alternate functions.

5.2 CAN – Controller Area Network

The i.MX 95 SoC includes five instances of CAN:

Table 15: CAN pins

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
CAN1						
20	CAN_1_TX	PDM_CLK	ALT6	CAN1_TX	O	CAN port 1 transmit pin
22	CAN_1_RX	PDM_BIT_STREAM0	ALT6	CAN1_RX	I	CAN port 1 receive pin
CAN2						
24	CAN_2_TX	GPIO_IO25	ALT2	CAN2_TX	O	CAN port 2 transmit pin
26	CAN_2_RX	GPIO_IO27	ALT2	CAN2_RX	I	CAN port 2 receive pin

The remaining interfaces are available as alternate functions on other pins. The Toradex Pinout Designer[2] tool can help verify pin multiplexing, especially for alternate functions that are not part of the standard Verdin specification.

5.3 Digital Audio Interfaces

The i.MX 95 SoC features six Synchronous Audio Interfaces (SAIs). These interfaces support I²S, AC'97, TDM and Codec/DSP audio protocols.

SAI_2 supports up to 8 RX and 8 TX lines. However, due to pin multiplexing limitations, not all signal combinations are supported, and some interface pins are not available on the module edge connector.

[2] https://developer.toradex.com/carrier-board-design/pinout-designer/

The remaining interfaces are available as alternate functions on other pins. The Toradex Pinout Designer[3] tool can help verify pin multiplexing, especially for alternate functions that are not part of the standard Verdin specification.

Table 16: I²S pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM in controller mode*	Description
I2S_1						
30	I2S_1_BCLK	GPIO_IO16	ALT1	SAI3_TX_BCLK	O	Transmit bit clock
32	I2S_1_SYNC	GPIO_IO26	ALT7	SAI3_TX_SYNC	O	Transmit frame sync
34	I2S_1_D_OUT	GPIO_IO21	ALT1	SAI3_TX_DATA0	O	Data output
36	I2S_1_D_IN	GPIO_IO20	ALT1	SAI3_RX_DATA0	I	Data input
38	I2S_1_MCLK	GPIO_IO17	ALT1	SAI3_MCLK	O	Audio controller clock
I2S_2						
42	I2S_2_BCLK	XSPI1_DATA6	ALT1	SAI5_TX_BCLK	O	Transmit bit clock
44	I2S_2_SYNC	XSPI1_DATA5	ALT1	SAI5_TX_SYNC	O	Transmit frame sync
46	I2S_2_D_OUT	XSPI1_DATA4	ALT2	SAI5_TX_DATA0	O	Data output
48	I2S_2_D_IN	XSPI1_DATA7	ALT2	SAI5_RX_DATA0	I	Data input

5.3.1 SAI Used as I²S

The SAI interfaces can be used as I²S, which is the default use case in the Verdin standard. The i.MX 95 SoC fully supports both controller and peripheral modes, selectable via control bits in the SAI register map. In the Verdin standard, the master configuration offers the highest compatibility with other modules and is therefore the preferred configuration. The following signals are used for a basic I²S interface:

Table 17: SAI in I²S controller mode

SoC port name	Codec signal name	I/O *SoM perspective*	Description
SAIx.TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 95 to the codec.
SAIx.RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 95 from the codec.
SAIx.TX_SYNC	WS	I/O	Word Select (also known as Field Select or LRCLK).
SAIx.TX_BCLK	SCK	I/O	Bit clock serial continuous clock.

Table 18: SAI in I²S peripheral mode

SoC port name	Codec signal name	I/O *SoM perspective*	Description
SAIx.RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 95 from the codec.
SAIx.TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 95 to the codec.
SAIx.TX_SYNC	WS	I/O	Word Select (also known as Field Select or LRCLK).
SAIx.TX_BCLK	SCK	I/O	Bit clock serial continuous clock.

[3] https://developer.toradex.com/carrier-board-design/pinout-designer/

5.3.2 SAI Used as AC'97

The SAI interface can be configured for AC'97 compatibility. The AC'97 audio interface does not require an additional I²C bus for control communication, as the codec is controlled directly through the AC'97 interface.

The AC'97 codec requires a master reference clock, which can be provided either by one of the SAI master clock outputs or by an external crystal or oscillator.

Note that some codecs use unconventional pin naming: for example, a device may label its data input pin as SDATA_OUT and its data output pin as SDATA_IN. These names refer to the signals they should connect to on the host, not to the actual signal direction.

Table 19: SAI in AC'97 mode

SoC port name	Codec signal name	I/O *SoM perspective*	Description
SAIx.RX_DATA[0]	SDATA_IN	I	Audio Serial Input to i.MX 95 from the codec.
SAIx.TX_DATA[0]	SDATA_OUT	O	Audio Serial Output from i.MX 95 to the codec.
SAIx.TX_SYNC	SYNC	O	Audio Sync
SAIx.TX_BCLK	BIT_CLK	I	Audio Bit Clock
GPIOx	RESET#	O	Master H/W Reset. Any GPIO can be used.

5.3.3 MICFIL – PDM Microphone Interface

The i.MX 95 SoC supports up to four PDM microphone input signals. PDM (Pulse-Density Modulation) is a widely used digital interface for transmitting audio from microphones to the SoC. The PDM bitstream is time-multiplexed and carries audio data for two channels (left and right), allowing up to eight microphones to be connected.

Since PDM is not part of the standard Verdin interface, these signals are available only as alternate functions. As a result, PDM microphone support is not guaranteed to be compatible across different Verdin modules.

Table 20: PDM pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM in controller mode*	Description
15	PWM_1	GPIO_IO05	ALT2	PDM_BIT_STREAM0	I	Microphone data input channel 0
16	PWM_2	GPIO_IO06	ALT2	PDM_BIT_STREAM1	I	Microphone data input channel 1
19	PWM_3_DSI	GPIO_IO19	ALT2	PDM_BIT_STREAM3	I	Microphone data input channel 3
20	CAN_1_TX	PDM_CLK	ALT0	PDM_CLK	O	Serial clock
22	CAN_1_RX	PDM_BIT_STREAM0	ALT0	PDM_BIT_STREAM0	I	Microphone data input channel 0
30	I2S_1_BCLK	GPIO_IO16	ALT2	PDM_BIT_STREAM2	I	Microphone data input channel 2
32	I2S_1_SYNC	GPIO_IO26	ALT2	PDM_BIT_STREAM1	I	Microphone data input channel 1
34	I2S_1_D_OUT	GPIO_IO21	ALT2	PDM_CLK	O	Serial clock

Continued on next page

Table 20: PDM pins (Continued)

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM in controller mode*	Description
36	I2S_1_D_IN	GPIO_IO20	ALT2	PDM_BIT_STREAM0	I	Microphone data input channel 0
137	UART_2_RXD	GPIO_IO13	ALT2	PDM_BIT_STREAM3	I	Microphone data input channel 3
139	UART_2_TXD	GPIO_IO12	ALT2	PDM_BIT_STREAM2	I	Microphone data input channel 2
152	MSP_28	GPIO_IO04	ALT2	PDM_CLK	O	Serial clock
252	CTRL_WAKE1_MICO#	PDM_BIT_STREAM1	ALT0	PDM_BIT_STREAM1	I	Microphone data input channel 1

5.3.4 S/PDIF – Sony-Philips Digital Interface

The S/PDIF interface supports both input and output. The input controller can digitally recover the clock from the incoming stream and conforms to the AES/EBU IEC 60958 standard.

S/PDIF is not part of the Verdin standard, meaning that its signals are only available as alternate functions on other interface pins. As a result, S/PDIF support is not guaranteed to be compatible across different Verdin modules.

Table 21: S/PDIF pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM in controller mode*	Description
93	I2C_4_CSI_SDA	GPIO_IO22	ALT2	SPDIF1_IN	I	Audio input
95	I2C_4_CSI_SCL	GPIO_IO23	ALT2	SPDIF1_OUT	O	Audio output
203	ETH_2_RGMII_RXD_1	ENET2_RD1	ALT1	SPDIF1_IN	I	Audio input
207	ETH_2_RGMII_RXD_3	ENET2_RD3	ALT1	SPDIF1_OUT	O	Audio output
207	ETH_2_RGMII_RXD_3	ENET2_RD3	ALT2	SPDIF1_IN	I	Audio input

5.4 Display

The i.MX 95 SoC features a single display controller capable of driving up to three screens (1× MIPI DSI and 2× LVDS) using two display engines. Both LVDS displays must use the same resolution and timing. The display engines are connected to one DSI and one LVDS interface.

HDMI port is not natively supported on the Verdin iMX95 SoM. However, HDMI can be enabled with a DSI-to-HDMI bridge solution on the carrier board.

5.4.1 DSI

Table 22: DSI pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
DSI clock						
37	DSI_1_CLK_P	MIPI_DSICSI1_CLK_P	–	–	O	Positive differential DSI Interface clock

Continued on next page

Table 22: DSI pins (Continued)

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
35	DSI_1_CLK_N	MIPI_DSICSI1_CLK_N	–	–	O	Negative differential DSI Interface clock
DSI data						
49	DSI_1_D0_P	MIPI_DSICSI1_D0_P	–	–	I/O	Positive differential DSI Interface data lane 0
47	DSI_1_D0_N	MIPI_DSICSI1_D0_N	–	–	I/O	Negative differential DSI Interface data lane 0
43	DSI_1_D1_P	MIPI_DSICSI1_D1_P	–	–	O	Positive differential DSI Interface data lane 1
41	DSI_1_D1_N	MIPI_DSICSI1_D1_N	–	–	O	Negative differential DSI Interface data lane 1
31	DSI_1_D2_P	MIPI_DSICSI1_D2_P	–	–	O	Positive differential DSI Interface data lane 2
29	DSI_1_D2_N	MIPI_DSICSI1_D2_N	–	–	O	Negative differential DSI Interface data lane 2
25	DSI_1_D3_P	MIPI_DSICSI1_D3_P	–	–	O	Positive differential DSI Interface data lane 3
23	DSI_1_D3_N	MIPI_DSICSI1_D3_N	–	–	O	Negative differential DSI Interface data lane 3
Bridge control						
17	GPIO_9_DSI	–[1]	–	–	I	DSI_1_INT# Inpt input, intended to be used as hotplug detect or for interrupt messages from DSI bridges on carrier board.
53	I2C_2_DSI_SCL	GPIO_IO29	ALT1	I2C3_SCL	I/O	I2C interface, intended to be used as DDC or for controlling DSI bridges on carrier board.
55	I2C_2_DSI_SDA	GPIO_IO28	ALT1	I2C3_SDA	I/O	
Backlight control						
19	PWM_3_DSI	GPIO_IO19	ALT0	GPIO2_IO19	O	Display backlight brightness control
21	GPIO_10_DSI	–[1]	–	–	O	DSI_1_BKL_EN ay backlight enable

[1] Available through the on-module GPIO expander.

5.4.2 LVDS

Table 23: LVDS pins

X1 pin	Verdin specification signal name	SoC ball name	I/O *SoM perspective*	Description
Channel 0				
88	LVDS0_CLK_N	LVDS0_CLK_N	O	LVDS clock lane, N polarity signal, channel 0
90	LVDS0_CLK_P	LVDS0_CLK_P	O	LVDS clock lane, P polarity signal, channel 0
94	LVDS0_D0_N	LVDS0_D0_N	O	LVDS data lane 0, N polarity signal, channel 0
96	LVDS0_D0_P	LVDS0_D0_P	O	LVDS data lane 0, P polarity signal, channel 0
100	LVDS0_D1_N	LVDS0_D1_N	O	LVDS data lane 1, N polarity signal, channel 0
102	LVDS0_D1_P	LVDS0_D1_P	O	LVDS data lane 1, P polarity signal, channel 0

Continued on next page

Table 23: LVDS pins (Continued)

X1 pin	Verdin specification signal name	SoC ball name	I/O *SoM perspective*	Description
106	LVDS0_D2_N	LVDS0_D2_N	O	LVDS data lane 2, N polarity signal, channel 0
108	LVDS0_D2_P	LVDS0_D2_P	O	LVDS data lane 2, P polarity signal, channel 0
112	LVDS0_D3_N	LVDS0_D3_N	O	LVDS data lane 3, N polarity signal, channel 0
114	LVDS0_D3_P	LVDS0_D3_P	O	LVDS data lane 3, P polarity signal, channel 0
Channel 1				
118	LVDS1_CLK_N	LVDS1_CLK_N	O	LVDS clock lane, N polarity signal, channel 1
120	LVDS1_CLK_P	LVDS1_CLK_P	O	LVDS clock lane, P polarity signal, channel 1
124	LVDS1_D0_N	LVDS1_D0_N	O	LVDS data lane 0, N polarity signal, channel 1
126	LVDS1_D0_P	LVDS1_D0_P	O	LVDS data lane 0, P polarity signal, channel 1
130	LVDS1_D1_N	LVDS1_D1_N	O	LVDS data lane 1, N polarity signal, channel 1
132	LVDS1_D1_P	LVDS1_D1_P	O	LVDS data lane 1, P polarity signal, channel 1
136	LVDS1_D2_N	LVDS1_D2_N	O	LVDS data lane 2, N polarity signal, channel 1
138	LVDS1_D2_P	LVDS1_D2_P	O	LVDS data lane 2, P polarity signal, channel 1
142	LVDS1_D3_N	LVDS1_D3_N	O	LVDS data lane 3, N polarity signal, channel 1
144	LVDS1_D3_P	LVDS1_D3_P	O	LVDS data lane 3, P polarity signal, channel 1

Table 24: LVDS modes × Active lanes

Signal pair	Single channel 16-bit	Single channel 24-bit	Dual channel 16-bit	Dual channel 24-bit
Channel 0				
Ch. 0 Clock	Yes	Yes	Yes	Yes
Ch. 0 Data 0	Yes	Yes	Yes	Yes
Ch. 0 Data 1	Yes	Yes	Yes	Yes
Ch. 0 Data 2	Yes	Yes	Yes	Yes
Ch. 0 Data 3	No	Yes	No	Yes
Channel 1				
Ch. 1 Clock	No	No	Yes	Yes
Ch. 1 Data 0	No	No	Yes	Yes
Ch. 1 Data 1	No	No	Yes	Yes
Ch. 1 Data 2	No	No	Yes	Yes
Ch. 1 Data 3	No	No	No	Yes

5.5 Ethernet

Table 25: Media-Dependent Interface Ethernet pins

X1 pin	Verdin specification signal name	DP83867 signal name	I/O *SoM perspective*	Description
Lane 0				

Continued on next page

Table 25: Media-Dependent Interface Ethernet pins (Continued)

X1 pin	Verdin specification signal name	DP83867 signal name	I/O *SoM perspective*	Description
225	ETH_1_MDI0_P	TD_P_A	I/O	Positive differential MDI signal
227	ETH_1_MDI0_N	TD_M_A	I/O	Negative differential MDI signal
Lane 1				
231	ETH_1_MDI1_N	TD_M_B	I/O	Negative differential MDI signal
233	ETH_1_MDI1_P	TD_P_B	I/O	Positive differential MDI signal
Lane 2				
239	ETH_1_MDI2_P	TD_P_C	I/O	Positive differential MDI signal
241	ETH_1_MDI2_N	TD_M_C	I/O	Negative differential MDI signal
Lane 3				
245	ETH_1_MDI3_N	TD_M_D	I/O	Negative differential MDI signal
247	ETH_1_MDI3_P	TD_P_D	I/O	Positive differential MDI signal
LED control				
235	ETH_1_LED_1	LED_2	O	Toggles during RX/TX activity.
237	ETH_1_LED_2	LED_0	O	Low when a link (any speed) is established.

Table 26: RGMII pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
Interrupt line						
189	ETH_2_RGMII_INT#	SAI1_TXC	ALT5	GPIO1_IO12	I	Interrupt signal signal from Ethernet PHY configuration and status
Management interface						
191	ETH_2_RGMII_MDIO	ENET2_MDIO	ALT0[1]	NETC_MDIO	I/O	Bidirectional Management Data I/O for PHY configuration and status
193	ETH_2_RGMII_MDC	ENET2_MDC	ALT0[1]	NETC_MDIC	O	Management data clock signal
Receive interface						
197	ETH_2_RGMII_RXC	ENET2_RXC	ALT0[1]	NETC_ETH1_RGMII_RX_CLK	I	Receive clock input
199	ETH_2_RGMII_RX_CTL	ENET2_RX_CTL	ALT0[1]	NETC_ETH1_RGMII_RX_CTL	I	Indicates data validity
201	ETH_2_RGMII_RXD_0	ENET2_RD0	ALT0[1]	NETC_ETH1_RGMII_RXD0	I	Receive data bit 0
203	ETH_2_RGMII_RXD_1	ENET2_RD1	ALT0[1]	NETC_ETH1_RGMII_RXD1	I	Receive data bit 1
205	ETH_2_RGMII_RXD_2	ENET2_RD2	ALT0[1]	NETC_ETH1_RGMII_RXD2	I	Receive data bit 2
207	ETH_2_RGMII_RXD_3	ENET2_RD3	ALT0[1]	NETC_ETH1_RGMII_RXD3	I	Receive data bit 3
Transmit interface						
211	ETH_2_RGMII_TX_CTL	ENET2_TX_CTL	ALT0[1]	NETC_ETH1_RGMII_TX_CTL	O	Transmit control signal
213	ETH_2_RGMII_TXC	ENET2_TXC	ALT0[1]	NETC_ETH1_RGMII_TX_CLK	O	Transmit clock output
215	ETH_2_RGMII_TXD_3	ENET2_TD3	ALT0[1]	NETC_ETH1_RGMII_TXD3	O	Transmit data bit 3
217	ETH_2_RGMII_TXD_2	ENET2_TD2	ALT0[1]	NETC_ETH1_RGMII_TXD2	O	Transmit data bit 2

Continued on next page

Table 26: RGMII pins (Continued)

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
219	ETH_2_RGMII_TXD_1	ENET2_TD1	ALT0[1]	NETC_ETH1_RGMII_TXD1	O	Transmit data bit 1
221	ETH_2_RGMII_TXD_0	ENET2_TD0	ALT0[1]	NETC_ETH1_RGMII_TXD0	O	Transmit data bit 0

[1] This pin has no alternate functions.

5.6 FlexSPI – Flexible Serial Peripheral Interface

The Verdin standard offers one QuadSPI channel with two chip selects for up to two memory devices in the Reserved pin class.

On the Verdin iMX95, additional SPI signals are available via alternate functions, enabling FlexSPI to operate in octal mode. Note that this feature may not be available on other modules in the Verdin family.

Table 27: FlexSPI modes

SoC function	Single mode	Dual mode	Quad mode	Octal mode
XSPI1_DATA0	TX	Bi-dir	Bi-dir	Bi-dir
XSPI1_DATA1	RX	Bi-dir	Bi-dir	Bi-dir
XSPI1_DATA2	–	–	Bi-dir	Bi-dir
XSPI1_DATA3	–	–	Bi-dir	Bi-dir
XSPI1_DATA4	–	–	–	Bi-dir
XSPI1_DATA5	–	–	–	Bi-dir
XSPI1_DATA6	–	–	–	Bi-dir
XSPI1_DATA7	–	–	–	Bi-dir

Table 28: FlexSPI pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
Clock						
52	QSPI_1_CLK	XSPI1_SCLK	ALT0	FLEXSPI_A_SCLK	O	Serial Clock
Chip select						
54	QSPI_1_CS#	XSPI1_SS0_B	ALT0	FLEXSPI_A_SS0_B	O	Chip Select 0
64	QSPI_1_CS2#	XSPI1_SS1_B	ALT0	FLEXSPI_A_SS1_B	O	Chip Select 1
Data strobe						
66	QSPI_1_DQS	XSPI1_DQS	ALT0	FLEXSPI_A_DQS	I	Data Strobe signal, required by some high-speed DDR devices.
Data lines						
56	QSPI_1_IO0	XSPI1_DATA0	ALT0	FLEXSPI_A_DATA0	I/O	Serial data line 1
58	QSPI_1_IO1	XSPI1_DATA1	ALT0	FLEXSPI_A_DATA1	I/O	Serial data line 1
60	QSPI_1_IO2	XSPI1_DATA2	ALT0	FLEXSPI_A_DATA2	I/O	Serial data line 2

Continued on next page

Table 28: FlexSPI pins (Continued)

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
62	QSPI_1_IO3	XSPI1_DATA3	ALT0	FLEXSPI_A_DATA3	I/O	Serial data line 3

5.7 GPIO – General-Purpose Input/Output

The Verdin Standard includes ten dedicated GPIO pins. Four of these are reserved for the MIPI CSI camera interface and two for the MIPI DSI display interface.

In addition to the ten dedicated GPIOs, several other pins can function as GPIOs if their primary functions are not used. For compatibility reasons, it is recommended to use the ten dedicated GPIOs first.

Table 29: GPIO pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*
General-purpose					
206	GPIO_1	GPIO_IO00	ALT0	GPIO2_IO0	I/O
208	GPIO_2	GPIO_IO18	ALT0	GPIO2_IO18	I/O
210	GPIO_3	GPIO_IO24	ALT0	GPIO2_IO24	I/O
212	GPIO_4	GPIO_IO32	ALT0	GPIO5_IO12	I/O
Reserved GPIO for MIPI CSI camera interface					
216	GPIO_5_CSI	CCM_CLKO3	ALT5	GPIO4_IO28	I/O
218	GPIO_6_CSI	CCM_CLKO2	ALT5	GPIO3_IO27	I/O
220	GPIO_7_CSI	–[1]	–	–	I/O
222	GPIO_8_CSI	–[1]	–	–	I/O
Reserved GPIO for MIPI DSI camera interface					
17	GPIO_9_DSI	–[1]	–	–	I/O
21	GPIO_10_DSI	–[1]	–	–	I/O

[1] Available through the on-module GPIO expander.

Note the reset state of the GPIO pins: after a reset, the i.MX 95 pins may be configured in different modes. Most pins are pulled low, while some are high-impedance or pulled high. Once the bootloader is running, the pins and their states can be reconfigured. The reset state is only guaranteed during the release of the reset signal.

5.7.1 GPIO Wakeup

In principle, all GPIOs can be used to wake the Verdin iMX95 module from a suspended state. In the Verdin Standard, pin 252 is the default wake-up source. Only this pin is guaranteed to be wake-up compatible across Verdin modules. If carrier board compatibility with other Verdin modules is required, use only this pin for wake-up functionality.

Table 30: GPIO wakeup pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
251	CTRL_WAKE1_MICO#	PDM_BIT_STREAM1	ALT5	GPIO1_IO10	I/O	Default external wake-up signal.

5.8 MIPI CSI – MIPI Camera Serial Interface

Table 31: MIPI-CSI pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	I/O *SoM perspective*	Description
99	CSI_1_D3_P	MIPI_CSI1_D3_P	–[1]	I	Positive differential CSI interface data signal, lane 3
101	CSI_1_D3_N	MIPI_CSI1_D3_N	–[1]	I	Negative differential CSI interface data signal, lane 3
105	CSI_1_D2_P	MIPI_CSI1_D2_P	–[1]	I	Positive differential CSI interface data signal, lane 2
107	CSI_1_D2_N	MIPI_CSI1_D2_N	–[1]	I	Negative differential CSI interface data signal, lane 2
111	CSI_1_CLK_P	MIPI_CSI1_CLK_P	–[1]	I	Positive differential CSI interface clock signal
113	CSI_1_CLK_N	MIPI_CSI1_CLK_N	–[1]	I	Negative differential CSI interface clock signal
117	CSI_1_D1_P	MIPI_CSI1_D1_P	–[1]	I	Positive differential CSI interface data signal, lane 1
119	CSI_1_D1_N	MIPI_CSI1_D1_N	–[1]	I	Negative differential CSI interface data signal, lane 1
123	CSI_1_D0_P	MIPI_CSI1_D0_P	–[1]	I	Positive differential CSI interface data signal, lane 0
125	CSI_1_D0_N	MIPI_CSI1_D0_N	–[1]	I	Negative differential CSI interface data signal, lane 0

[1] Dedicated to the MIPI-CSI interface and does not support alternate functions.

Four GPIOs are reserved for the MIPI CSI camera interface. Details are available in Table 29.

5.9 I²C Inter-Integrated Circuit

The NXP i.MX 95 SoC features eight I2C controllers, **six of which can be used externally**. The fifth and sixth I²C ports are only available as alternate functions of other pins. Therefore, these interfaces are not compatible with other Verdin modules.

Table 32: I²C pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I²C port	I/O *SoM perspective*	Description
Generic							
12	I2C_1_SDA	GPIO_IO30	ALT1	I2C4_SDA	I2C4	I/O	Generic I²C
14	I2C_1_SCL	GPIO_IO31	ALT1	I2C4_SCL	I2C4	I/O	
MIPI DSI							
53	I2C_2_DSI_SDA	GPIO_IO28	ALT1	I2C3_SDA	I2C3	I/O	I²C port for the DSI interface. Intended to be used as DDC or for controlling DSI bridges on the carrier board.
55	I2C_2_DSI_SCL	GPIO_IO29	ALT1	I2C3_SCL	I2C3	I/O	
HDMI							
57	I2C_3_HDMI_SDA	ENET1_MDIO	ALT2	I3C2_SDA	I3C2[1]	I/O	Dedicated DDC port for HDMI.[2]
59	I2C_3_HDMI_SCL	ENET1_MDC	ALT2	I3C2_SCL	I3C2[1]	I/O	

Continued on next page

Table 32: I²C pins (Continued)

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I²C port	I/O *SoM perspective*	Description
MIPI CSI							
93	I2C_4_CSI_SDA	GPIO_IO22	ALT6	I2C5_SDA	I2C5	I/O	I²C port for the camera interface.
95	I2C_4_CSI_SCL	GPIO_IO23	ALT6	I2C5_SCL	I2C5	I/O	

[1] These signals are available through the I3C interface, which is backward-compatible with I²C.
[2] Although HDMI is not available on the Verdin iMX95, the I²C interface on these pins can be used for other purposes.

5.9.1 RTC

The Verdin iMX95 module features an RTC IC on the module. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for timekeeping. When the main power supply is available, the RTC is powered from that rail. However, to retain RTC functionality when the main power is off, a coin cell must be connected to the VCC_BACKUP supply pin (pin 249).

While the module's main voltage is available, the onboard RTC can recharge a supercapacitor or rechargeable battery via the VCC_BACKUP pin. The available charging current is very low (<500 µA at 3 V). If higher charging current is required, an external charging circuit can be implemented on the carrier board.

When using the RTC's recharging capability, a current-limiting resistor of at least 47 kΩ must be placed between the battery and the VCC_BACKUP pin. **Using a lower resistance may prevent the module from booting**.

5.10 JTAG

The JTAG interface is typically not required for programming the Verdin module. However, it can be useful for debugging the Cortex®-M7 core or performing advanced debugging on the Arm® Cortex®-A cores.

The i.MX 95 SoC **does not feature a JTAG_TRST# reset input**. Instead of using the JTAG port, the module can be reprogrammed via Recovery Mode over USB. To support flashing in recovery mode—and for debugging—**it is strongly recommended that the USB_1 interface remain accessible**, even if it is not used in the final production system. Additionally, **UART_3 (for the Cortex-A53 console) and UART_4 (for debugging the M7 core) should also remain accessible**.

Table 33: JTAG pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
1	JTAG_1_TDI	DAP_TDI	ALT0	DAP_TDI	I	Test Data In
3	JTAG_1_TRST#	–	–	–	–	Not connected.
5	JTAG_1_TDO	DAP_TDO_TRACESWO	ALT0	DAP_TDO_TRACESWO	O	Test Data Out
7	JTAG_1_VREF	–	–	–	O	1.8V output reference for the debugger.
9	JTAG_1_TCK	DAP_TCLK_SWCLK	ALT0	DAP_TCLK_SWCLK	I	Test Clock
13	JTAG_1_TMS	DAP_TMS_SWDIO	ALT0	DAP_TMS_SWDIO	I	Test Mode Select

5.11 PCI Express

The NXP i.MX 95 features a single-lane PCI Express (PCIe) interface. It complies with the PCIe 3.0 base specification and supports data rates of up to 8 Gb/s (Gen 3). The interface is backward-compatible with earlier standards that support 5 Gb/s (Gen 2) and 2.5 Gb/s (Gen 1).

The 100 MHz PCIe reference clock is generated by the SoC and made available to peripherals through the module edge connector pins. All required source terminations for the reference clock are located on the Verdin module.

PCIe is a high-speed interface that requires special layout considerations. Refer to the Verdin Carrier Board Design Guide and the Layout Design Guide for detailed guidance.

Table 34: PCI Express pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	I/O *SoM perspective*	Description
226	PCIE_1_CLK_N	PCIE_REF_OUT_CLK_N	–[3]	O	Negative differential 100MHz reference clock signal. Sourced by a reference clock oscillator.
228	PCIE_1_CLK_P	PCIE_REF_OUT_CLK_P	–[3]	O	Positive differential 100MHz reference clock signal. Sourced by a reference clock oscillator.
232	PCIE_1_L0_RX_N	PCIE1_RX0_N	–[3]	I	Negative differential receive data signal, lane 0.
234	PCIE_1_L0_RX_P	PCIE1_RX0_P	–[3]	I	Positive differential receive data signal, lane 0.
238	PCIE_1_L0_TX_N	PCIE1_TX0_N	–[3]	O	Negative differential receive data signal, lane 0.
240	PCIE_1_L0_TX_P	PCIE1_TX0_P	–[3]	O	Positive differential receive data signal, lane 0.
244	PCIE_1_RESET#	–[2]	–	O	Dedicated reset output for PCIe.
–[1]	–	PCIE1_REF_PAD_CLK_N	–	O	Negative side of the external reference clock input.
–[1]	–	PCIE1_REF_PAD_CLK_P	–	O	Positive side of the external reference clock input.

[1] Not used; connected to GND through 10k Ω resistors.
[2] Available through the on-module GPIO expander, pin P0_4.
[3] Dedicated to the PCI Express interface and does not support alternate functions.

5.12 Power

5.12.1 Digital Supply

Table 35: Power supply pins

X1 pin	Verdin signal name	I/O	Description	Remarks
251, 253, 255, 257, 259	VCC	I	3.135V to 5.5V main power supply.	Use decoupling capacitors on the carrier board.
10, 11, 18, 27, 28, 33, 39, 40, 45, 50, 51, 65, 68, 71, 77, 83, 86, 89, 97, 98, 103, 109, 110, 115, 121, 122, 127, 134, 145, 146, 158, 167, 170, 173, 179, 182, 194, 195, 204, 209, 223, 224, 229, 230, 236, 242, 243	GND	I	Digital Ground	
249	VCC_BACKUP	I	RTC Power supply can be connected to a backup battery.	Can be left unconnected if the internal RTC is not used. VCC, not VCC_BACKUP, powers the SNVS supplies of the SoC.

5.12.2 Analog Supply

The analog power rails of the SoC receive power from the main power rails.

5.12.3 Power Management Signals

Table 36: Power management pins

X1 pin	Verdin signal name	I/O	Type	Remarks
246	CTRL_RECOVERY_MICO#	I	OD 1.8V	Shorting the pin to ground during power-up puts the module into recovery mode. The module includes a 10 kΩ pull-up resistor, so the pin can be left floating on the carrier board.
248	CTRL_PWR_BTN_MICO#	I	OD 1.8V	Pulling the pin low for a long duration shuts down the module, while a short pull-down turns on the module from the off state. The pin is an open-drain input with a 100 kΩ pull-up resistor to the 1.8 V BBSM rail on the module. It can be left floating on the carrier board.
250	CTRL_FORCE_OFF_MOCI#	O	OD 5V	Output used to force shutdown of the main power rail. Must be ignored for the first 400 ms of power-up. The signal is 5 V tolerant and can be pulled up to 1.8 V, 3.3 V, or 5 V by the carrier board. It can be left floating.
252	CTRL_WAKE1_MICO#	I	1.8V	Wake-capable pin that allows the system to resume from sleep mode. There are no pull resistors on the carrier board. The pin can be left floating if the wake feature is disabled in software. It functions as a regular SoC GPIO.
254	CTRL_PWR_EN_MOCI	O	1.8V	Enable signal for the power rails of carrier board peripherals. It remains high during sleep modes.
256	CTRL_SLEEP_MOCI#	O	1.8V	Enable signal for power rails of carrier board peripherals that must be turned off during sleep mode. The signal is high only in running mode. It is a standard GPIO with an on-module 10 kΩ pull-down resistor. The signal is defined during the power-up sequence and can be left floating on the carrier board.
258	CTRL_RESET_MOCI#	O	OD 3.3V	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and after a sleep state, the CTRL_RESET_MOCI# signal is not asserted. The output is open-drain and does not include a pull-up resistor on the module. The signal is 3.3 V tolerant, and the carrier board can pull it up to 1.8 V or 3.3 V. It can be left floating on the carrier board.
260	CTRL_RESET_MICO#	I	OD 1.8V	Open-drain input. It resets the module when pulled low on the carrier board. This module includes a 100 kΩ pull-up resistor to the 1.8 V BBSM rail. It can be left floating on the carrier board.

The **Wi-Fi module** includes a power-down pin, controlled by the SoC's **SAI1_TXFS** pin, which turns off the internal power rails and reduces current consumption to 0.06 mA.

5.13 PWM

Table 37: PWM pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
15	PWM_1	GPIO_IO05	ALT1	TPM4_CH0	I/O	General-purpose PWM signal
16	PWM_2	GPIO_IO06	ALT1	TPM5_CH0	I/O	General-purpose PWM signal
19	PWM_3_DSI	GPIO_IO19	ALT6	TPM6_CH2	O	PWM output dedicated to the DSI output for the display backlight inverter control.

5.14 SPI

The i.MX 95 SoC features a total of eight SPI interfaces. One of these is available on the Verdin module as an Always Compatible interface, while the others are available as alternate functions on different pins.

The LPSPI_1 and LPSPI_2 instances are part of the Always-On domain, meaning they remain powered even in low-power modes. These instances **support only controller mode and cannot operate as peripherals**. The remaining SPI instances belong to the Wakeup domain, which allows them to be reactivated by events during low-power states. These instances **support both controller and peripheral modes**.

Table 38: SPI pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM in controller mode*	Description
196	SPI_1_CLK	GPIO_IO03	ALT4	SPI6_SCK	O	Serial clock
198	SPI_1_MISO	GPIO_IO01	ALT4	SPI6_SIN	I	Controller input, peripheral output
200	SPI_1_MOSI	GPIO_IO02	ALT4	SPI6_SOUT	O	Controller output, peripheral input
202	SPI_1_CS	CCM_CLKO4	ALT5	GPIO4_IO29	O	Peripheral select

5.15 UART

The i.MX 95 SoC features a total of eight UART interfaces. In the Verdin Standard, four of these are available:

- **UART_1** and **UART_2** are **general-purpose** interfaces. Their RX and TX signals are in the Always Compatible section, while the RTS/CTS signals are part of the Reserved section.
- **UART_3** is in the Always Compatible section and is intended to be used for **the main OS terminal (A55 cores) as a debug port**. While it can be repurposed, we recommend reserving this interface for debugging.
- **UART_4** belongs to the Reserved section and is intended for the **real-time operating system (M7 core)**. It may also be used as a general-purpose UART.

Table 39: UART pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
UART_1						
129	UART_1_RXD	GPIO_IO09	ALT5	UART7_RX	I	Receive data line
131	UART_1_TXD	GPIO_IO08	ALT5	UART7_TX	O	Transmit data line
133	UART_1_RTS	GPIO_IO11	ALT5	UART7_RTS_B	O	Request to Send
135	UART_1_CTS	GPIO_IO10	ALT5	UART7_CTS_B	I	Clear to Send
UART_2						
137	UART_2_RXD	GPIO_IO13	ALT5	UART8_RX	I	Receive data line
139	UART_2_TXD	GPIO_IO12	ALT5	UART8_TX	O	Transmit data line
141	UART_2_RTS	GPIO_IO15	ALT5	UART8_RTS_B	O	Request to Send
143	UART_2_CTS	GPIO_IO14	ALT5	UART8_CTS_B	I	Clear to Send
UART_3						
147	UART_3_RXD	UART1_RXD	ALT0	UART1_RX	I	Receive data line
149	UART_3_TXD	UART1_TXD	ALT0	UART1_TX	O	Transmit data line
UART_4						

Continued on next page

Table 39: UART pins (Continued)

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
151	UART_4_RXD	UART2_RXD	ALT0	UART2_RX	I	Receive data line
153	UART_4_TXD	UART2_TXD	ALT0	UART2_TX	O	Transmit data line

On Verdin iMX95 modules without Wi-Fi, the following UART signals are also exposed through the SODIMM (X1) connector:

Table 40: UART pins – Verdin Modules without Wi-Fi

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
148	MSP_26	GPIO_IO34	ALT2	UART6_CTS_B	I	Clear to Send
150	MSP_27	GPIO_IO33	ALT2	UART6_RX	O	Receive data line
152	MSP_28	GPIO_IO04	ALT5	UART6_TX	O	Transmit data line
154	MSP_29	GPIO_IO07	ALT5	UART6_RTS_B	I	Request to Send

5.16 uSDHC – Ultra Secured Digital Host Controller

The i.MX 95 SoC provides three SDIO interfaces:

- **SDIO 1**: Used internally for the eMMC flash.
- **SDIO 2**: Exposed on the module edge connector as the Always Compatible Verdin SD® Memory Card Interface.
- **SDIO 3**: Used by the on-module Wi-Fi and Bluetooth module. It is available on module-specific pins for SoM variants without Wi-Fi/Bluetooth.

Table 41: SDIO interfaces

SoC SDIO interface	Max bus width	Description
USDHC1	8-bit	Connected to the internal eMMC boot device. Not available on the module edge connector.
USDHC2	4-bit	Exposed as the Always Compatible Verdin SD® interface.
USDHC3	4-bit	Used by the on-module Wi-Fi and Bluetooth module.

Features:

- Compatible with SD Memory Card Specification versions 2.0 and 3.0.
- Compatible with SDIO Card Specification versions 2.0 and 3.0.
- Compatible SD UHS-I mode (up to 208 MHz) with a 1.8 V I/O voltage level.
- Supports both 3.3 V and 1.8 V I/O voltage modes.

The SD interface in the Always Compatible class supports both I/O voltage levels. No external pull-up resistors are required on the carrier board, as pull-up resistors are provided on the module.

Table 42: SD Card pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoM perspective*	Description
USDHC2[1]						
70	SD_1_D2	SD2_DATA2	ALT0	USDHC2_DATA2	I/O	Data line 2
72	SD_1_D3	SD2_DATA3	ALT0	USDHC2_DATA3	I/O	Data line 3
74	SD_1_CMD	SD2_CMD	ALT0	USDHC2_CMD	I/O	SDIO command line
76	SD_1_PWR_EN	SD2_RESET_B	ALT0	USDHC2_RESET_B	O	Power enable signal for SD cards
78	SD_1_CLK	SD2_CLK	ALT0	USDHC2_CLK	O	Clock signal
80	SD_1_D0	SD2_DATA0	ALT0	USDHC2_DATA0	I/O	Data line 0
82	SD_1_D1	SD2_DATA1	ALT0	USDHC2_DATA1	I/O	Data line 1
84	SD_1_CD#	SD2_CD_B	ALT0	USDHC2_CD_B	I	Card detect input
USDHC3 *Available on SoM variants without Wi-Fi/Bluetooth*						
156	MSP_30	SD3_CLK	ALT0	USDHC3_CLK	O	Clock signal
160	MSP_31	SD3_CMD	ALT0	USDHC3_CMD	I/O	SDIO command line
162	MSP_32	SD3_DATA0	ALT0	USDHC3_DATA0	I/O	Data line 0
164	MSP_33	SD3_DATA1	ALT0	USDHC3_DATA1	I/O	Data line 1
166	MSP_34	SD3_DATA2	ALT0	USDHC3_DATA2	I/O	Data line 2
168	MSP_35	SD3_DATA3	ALT0	USDHC3_DATA3	I/O	Data line 3

[1] All signals are on the same power domain, and can operate at either 1.8 V or 3.3 V—including SD_1_PWR_EN and SD_1_CD#.

5.17 USB

The i.MX 95 SoC features two USB controllers. In the Verdin standard, only the USB_1 port supports OTG functionality; USB_2 functions solely as a host port. Therefore, USB_1 is the recommended port for host/client (OTG) operation. It is also used for serial mode (recovery mode).

Table 43: USB overview

Verdin USB port	Speed capabilities supported by SoC	Role capabilities supported by SoC	Speed according to Verdin standard	Role according to Verdin standard	Recovery mode
USB_1	USB 2.0	Host and client[1]	USB 2.0	OTG *host and client*	Supported
USB_2	USB 3.2 Gen 1	Host and client[1]	USB 3.0	Host only	Not supported

[1] The i.MX 95 SoC does not support OTG functionality.

In the Verdin standard, only USB_2 supports the SuperSpeed signals required for a USB 3.2 Gen 1–capable interface.

The i.MX 95 USB controller and PHY support USB Type-C's ability to provide two sets of SuperSpeed SerDes lanes. The first set (**RX0 and TX0**) of SuperSpeed SerDes lanes **is guaranteed to be compatible with other Verdin modules** that support USB 3.2 Gen 1. The second set (**RX1 and TX1**) is available on **module-specific pins**; therefore, **compatibility with other Verdin modules is not guaranteed**.

Table 44: USB pins

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	I/O *SoM perspective*	Description
USB_1					
165	USB_1_D_P	USB2_D_P	–[3]	I/O	Positive differential USB Signal.
163	USB_1_D_N	USB2_D_N	–[3]	I/O	Negative differential USB signal.
159	USB_1_VBUS	USB2_VBUS	–[3]	I	Detects whether VBUS is present. This is a 5 V input.
161	USB_1_ID	–[2]	–	I	Detects the ID signal when the port operates in OTG mode. It functions as a regular GPIO.
155	USB_1_EN	–[2]	–	O	Enables the external USB voltage supply.
157	USB_1_OC#	–[2]	–	I	Indicates USB overcurrent. This pin can signal an overcurrent condition on the USB_1 supply
USB_2					
169	USB_2_SSTX_N	USB1_TX0_N	–[3]	O	Negative SuperSpeed USB transmit signal.
171	USB_2_SSTX_P	USB1_TX0_P	–[3]	O	Positive SuperSpeed USB transmit signal.
175	USB_2_SSRX_N	USB1_RX0_N	–[3]	I	Negative SuperSpeed USB receive signal.
177	USB_2_SSRX_P	USB1_RX0_P	–[3]	I	Positive SuperSpeed USB receive signal.
178	MSP_39[1]	USB1_TX1_N	–[3]	O	Negative SuperSpeed USB transmit signal.
180	MSP_40[1]	USB1_TX1_P	–[3]	O	Positive SuperSpeed USB transmit signal.
181	USB_2_D_N	USB1_D_N	–[3]	I/O	Negative differential USB signal.
183	USB_2_D_P	USB1_D_P	–[3]	I/O	Positive differential USB signal.
184	MSP_41[1]	USB1_RX1_N	–[3]	I	Negative SuperSpeed USB receive signal.
185	USB_2_EN	–[2]	–	O	Enables the external USB voltage supply for the USB_2 interface.
186	MSP_42[1]	USB1_RX1_P	–[3]	I	Positive SuperSpeed USB receive signal.
187	USB_2_OC#	–[2]	–	I	Indicates USB overcurrent. This pin can signal an overcurrent condition on the USB_2 supply. This is a regular GPIO.

[1] Available on module-specific pins; compatibility with other Verdin modules is not guaranteed.
[2] Available through the on-module GPIO expander.
[3] Dedicated to the USB interface and does not support alternate functions.

5.18 Wi-Fi and Bluetooth

The Verdin iMX95 is available with optional on-module Wi-Fi and Bluetooth interfaces. These versions use the **u-blox MAYA-W260-00B** dual-band Wi-Fi and Bluetooth module.

Features:

- Wi-Fi 6 (IEEE 802.11a/b/g/n/ac/ax)
- Dual-band 5 GHz and 2.4 GHz
- Data rates up to 600 Mbit/s
- 20/40/80 MHz channel bandwidth
- Supports simultaneous Station, Access Point and P2P modes
- Bluetooth BR/EDR and Bluetooth Low Energy 5.4
- Dual antenna for simultaneous Wi-Fi and Bluetooth/802.15.4 operation

Country certification documents are available on the MAYA-W2 series[4] page.

Table 45: Signal mapping between MAYA-W260-00B and i.MX 95

MAYA-W260-00B Pin Name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoC perspective*	Description
SDIO					
SD_CLK	SD3_CLK	ALT0	USDHC3_CLK	O	4-bit SDIO interface for Wi-Fi
SD_DAT0	SD3_DATA0	ALT0	USDHC3_DATA0	I/O	
SD_DAT1	SD3_DATA1	ALT0	USDHC3_DATA1	I/O	
SD_DAT2	SD3_DATA2	ALT0	USDHC3_DATA2	I/O	
SD_DAT3	SD3_DATA3	ALT0	USDHC3_DATA3	I/O	
UART					
UART_CTSn	GPIO_IO34	ALT2	UART6_CTS_B	I	UART interface for Bluetooth.
PCM_RTSn	GPIO_IO07	ALT5	UART6_RTS_B	O	
UART_RX	GPIO_IO33	ALT2	UART6_RX	I	
UART_TX	GPIO_IO04	ALT5	UART6_TX	O	
Control signals					
PDn	SA1_TXFS	ALT0	GPIO1_IO11	I	Powers down the entire Wi-Fi/Bluetooth module (active low). Firmware needs to be reloaded after power-up.

The following signals are available on the SODIMM (X1) connector:

Table 46: MAYA-W260-00B signals available on X1

MAYA-W260-00B Pin Name	X1 Pin	Verdin specification signal name	SoC ball name function	I/O *SoM perspective*	Description
Wake signals					
WLAN_WAKE_HOST	116	MSP_13	–	I	Wi-Fi Wakeup for the Host.
BT_WAKE_HOST	128	MSP_18	–	I	Bluetooth Wakeup for the Host.
PCM *Bluetooth Audio*					
PCM_CLK	148	MSP_26	–	I	PCM interface for Bluetooth.
PCM_DIN	150	MSP_27	–	I	
PCM_DOUT	152	MSP_28	–	O	
PCM_SYNC	154	MSP_29	–	I	
WCI Coexistence Interface					
WCI_SIN	172	MSP_36	–	I	Multi-functional pin: • GPIO[25] • WCI-2 coexistence serial interface input
WCI_SOUT	174	MSP_37	–	O	Multi-functional pin: • GPIO[26] • WCI-2 coexistence serial interface output

[4] https://developer.toradex.com/hardware/hardware-resources/peripherals/wireless/certification-documents-for-azurewave-aw-cm276nf-wi-fi-bluetooth-module/

6 Technical Specifications

6.1 Absolute Maximum Ratings

Table 47: Absolute maximum ratings

Symbol	Description	Minimum	Maximum	Unit
VCC	Main power supply	-0.3	6	V
VCC_BACKUP	RTC power supply	-0.3	6	V
IO_1.8V	SoC IO pins with 1.8V logic level	-0.3	2.1	V
IO_3.3V	SoC IO pins with 3.3 logic level (SDIO)	-0.3	3.6	V
ADC	ADC analog input	-0.3	2.1	V
USB_1_VBUS	Input voltage at USB_1_VBUS	-0.3	5.5	V

6.2 Recommended Operation Conditions

Table 48: Recommended operation conditions

Symbol	Description	Minimum	Typical	Maximum	Unit
VCC	Main power supply	3.135	3.3 to 5.0	5.5	V
VCC_BACKUP	RTC power supply	1.1	3.0	5.5	V

6.3 Power Consumption

To design and scale power supplies, follow the recommendations provided in the Verdin Family Specification. Adhering to these guidelines ensures that the carrier board under development is compatible with all current and future Verdin modules. For more information, refer to the Verdin Family Specification or the Verdin Carrier Board Design Guide[5].

Detailed information about the Verdin iMX95 power consumption will be available soon on our Developer Website.

6.4 Power Ramp-Up Time Requirements

The carrier board must follow the power supply ramp-up requirements defined by the Verdin module standard. These requirements are specified in the Verdin Carrier Board Design Guide.

[5] https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf

6.5 Mechanical Characteristics

Tolerance for all measures:
±0.1mm, unless otherwise specified.

Figure 4: Module dimensions (top view)

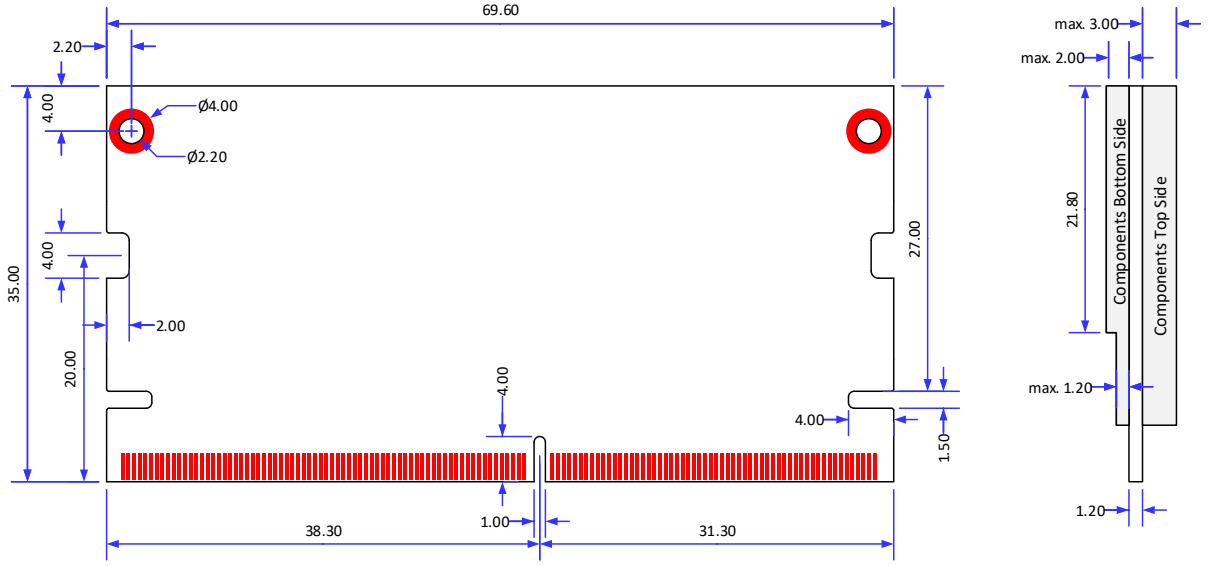
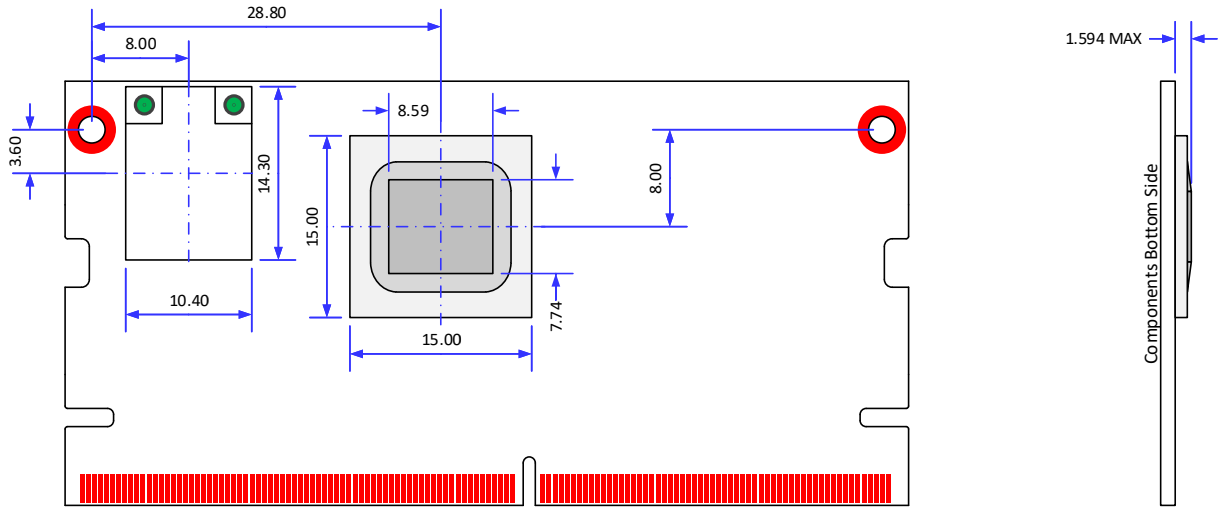


Figure 5: SoC and Wi-Fi/BT dimensions (top view)



6.5.1 Sockets for the Verdin Modules

The Verdin module uses a **260-pin SODIMM DDR4 edge connector**. This connector is available from multiple manufacturers in various stacking heights, ranging from 4 mm to 9.2 mm. Toradex recommends the TE Connectivity 2309409-2 connector, which has a stacking height of 5.2 mm and provides a board-to-board distance of 2.62 mm.

A list of other SODIMM DDR4 connector manufacturers is provided below:

Amphenol:
https://www.amphenol-icc.com/product-series/ddr4-so-dimm.html

TE Connectivity:
https://www.te.com/usa-en/products/connectors/card-socket-connectors/memory-sockets.html

6.6 Thermal Specification

The Verdin iMX95 incorporates **DVFS (Dynamic Voltage and Frequency Scaling) and thermal throttling**, enabling the system to dynamically adjust operating frequency and voltage based on workload and temperature. The i.MX 95 SoC features DVFS for both the CPU cluster and the GPU. This allows the Verdin iMX95 to deliver higher performance with lower average power consumption compared to other solutions.

Verdin iMX95 modules include embedded temperature sensors that monitor die (junction) temperature and determine whether core throttling is required to prevent overheating. If the temperature reaches the maximum permitted threshold, the system automatically shuts down.

General thermal and performance considerations:

- **If peak performance is used only briefly**, heat dissipation is less critical, as advanced power management reduces power consumption when full performance is not needed.
- **Lower die temperatures reduce power consumption**, due to lower leakage currents during idle states. For example, an increase in die temperature from 25 °C to 125 °C can increase leakage by a factor of 10.
- **Effective thermal solutions improve performance**, as better heat dissipation enables the module to operate closer to its peak capability for longer durations.

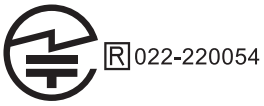
Table 49: Thermal Specification – Verdin iMX95

Description	Minimum	Typical	Maximum	Unit
Operating temperature range.	-40[1]		85[2]	°C
Storage Temperature (eMMC flash memory is the limiting device).	-40		85	°C
Junction temperature SoC.	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 95 only. ($R_{\theta JA}$)[3]		21.1		°C/W
Thermal Resistance Junction-to-Top of i.MX 95 chip case. ($R_{\theta JCtop}$)[3]		0.98		°C/W

[1] The Wi-Fi module is currently validated only from -30 °C to 85 °C. Validation down to -40 °C is pending. All other components are rated for the full -40 °C to 85 °C range.
[2] Depends on the cooling solution.
[3] Tested on a high-K JEDEC four-layer board, as defined by JEDEC Standard JESD51-2A. Board mounted horizontally, natural convection.

6.7 Product Compliance

Up-to-date information about product compliance—such as RoHS, CE, UL 94, Conflict Minerals, REACH, and others—can be found on our website[6].



[6] https://www.toradex.com/support/product-compliance

7 Device and Documentation Support

7.1 Trademarks

NXP is a trademark of NXP B.V. All other product or service names are the property of their respective owners. © 2023 NXP B.V.

Arm®, Cortex®, TrustZone® are registered trademarks or trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. Neon™ is a trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

MIPI® is a registered trademark of MIPI Alliance.

The Bluetooth® word mark is a registered trademark owned by Bluetooth SIG, Inc.

Android™ is a trademark owned by Google LLC.

Intel is a trademark of Intel Corporation or its subsidiaries.

Secure Digital® and SD® are registered trademarks of SD Card Association.

OpenGL is a registered trademark of Hewlett Packard Enterprise in the United States and/or other countries worldwide.

OpenCL is a trademark of Apple Inc. used by permission by Khronos Group Inc.

OpenVG is a trademark of the Khronos Group Inc.

Vivante® is a registered trademark of Vivante Corporation. All other brand and product names may be trademarks of their respective companies.

Vulkan is a registered trademark of the Khronos Group Inc.

DISCLAIMER

Copyright © Toradex AG. All rights are reserved. The information and content in this document are provided “as-is” with no warranties of any kind and are for informational purposes only. Data and information have been carefully checked and are believed to be accurate; however, no liability or responsibility for any errors, omissions or inaccuracies is assumed.

Brand and product names are trademarks or registered trademarks of their respective owners. Specifications are subject to change without notice.