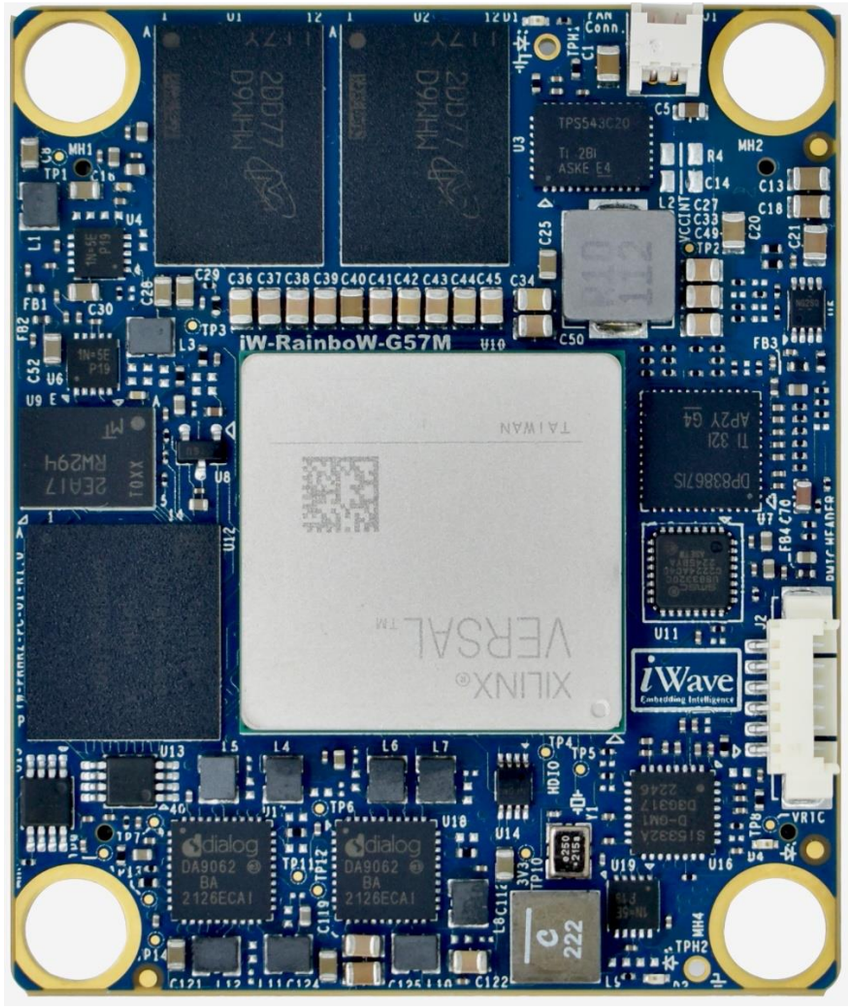
# iW-RainboW-G57M
# Versal AI Edge/Prime SOM
# Hardware User Guide

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# 1. INTRODUCTION

## 1.1 Purpose

This document is the Hardware User Guide for the Versal AI Edge/Prime System on Module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Versal AI Edge/ Prime System on Module from a Hardware Systems perspective.

## 1.2 SOM Overview

Versal AI Edge/Prime SOM has a form factor of 50mm x 60mm and provides the functional requirements for an embedded application with integrated Processing System (PS) and Programable logic (PL). Two High-Speed High-Density connectors provide the carrier board interface to carry all the I/O signals to and from the Versal AI Edge/Prime SOM.

## 1.3 List of Acronyms

The following acronyms will be used throughout this document.

**Table 1: Acronyms & Abbreviations**

| Acronyms | Abbreviations |
|---|---|
| ARM | Advanced RISC Machine |
| BSP | Board Support Package |
| B2B | Board to Board Connector |
| CAN | Controller Area Network |
| CPU | Central Processing Unit |
| LPDDR4 | Low- Power Double Data Rate |
| FPGA | Field Programmable Gate Array |
| eMMC | Embedded Multimedia Card |
| GB | Giga Byte |
| Gbps | Gigabits per sec |
| GEM | Gigabit Ethernet Controller |
| GHz | Giga Hertz |
| GPIO | General Purpose Input Output |
| I2C | Inter-Integrated Circuit |
| IC | Integrated Circuit |
| JTAG | Joint Test Action Group |
| Kbps | Kilobits per second |
| LVDS | Low Voltage Differential Signalling |
| MAC | Media Access Controller |
| MB | Mega Byte |
| Mbps | Megabits per sec |
| MHz | Mega Hertz |

| Acronyms | Abbreviations |
|---|---|
| NPTH | Non-Plated Through hole |
| PCB | Printed Circuit Board |
| PMIC | Power Management Integrated Circuit |
| PTH | Plated Through hole |
| PL | Programmable Logic |
| PS | Processing System |
| QSPI | Quad Serial Peripheral Interface |
| RGMII | Reduced Gigabit Media Independent Interface |
| RTC | Real Time Clock |
| RX | Receiver |
| SD | Secure Digital |
| SDIO | Secure Digital Input Output |
| SoC | System On Chip |
| SPI | Serial Peripheral Interface |
| SOM | System On Module |
| TX | Transmitter |
| UART | Universal Asynchronous Receiver/Transmitter |
| ULPI | UTMI+ Low Pin Interface |
| USB | Universal Serial Bus |
| USB OTG | USB On The Go |

### 1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

**Table 2: Terminology**

| Terminology | Description |
|---|---|
| I | Input Signal |
| O | Output Signal |
| IO | Bidirectional Input/output Signal |
| CMOS | Complementary Metal Oxide Semiconductor Signal |
| DIFF | Differential Signal |
| LVDS | Low Voltage Differential Signal |
| GBE | Gigabit Ethernet Media Dependent Interface differential pair signals |
| USB | Universal Serial Bus differential pair signals |
| OD | Open Drain Signal |
| OC | Open Collector Signal |
| Power | Power Pin |
| PU | Pull Up |
| PD | Pull Down |
| NA | Not Applicable |
| NC | Not Connected |

*Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.*

### 1.5 References

- Versal AI Edge/Prime Technical Reference Manual
- Versal AI Edge/Prime Device Overview
- Versal AI Edge/Prime AC and DC characteristics

# 2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Versal AI Edge/Prime SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

## 2.1 Versal AI Edge/Prime SOM Block Diagram

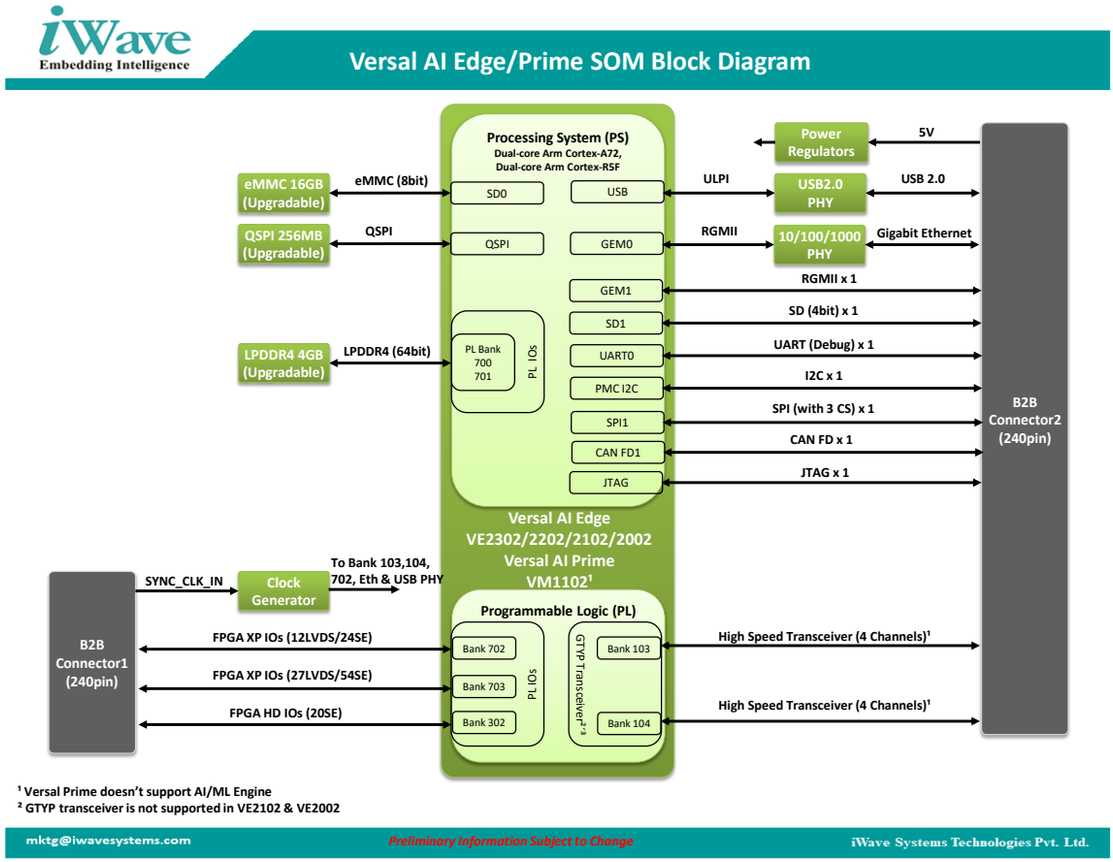


**Figure 1: Versal AI Edge/Prime SOM Block Diagram**

### 2.2 Versal AI Edge SOM Features

The Versal AI Edge/Prime SOM supports the following features.

**SoC**

- Xilinx Versal AI Edge/Prime
  - Pin Compatible Devices: VE2302/VE2202/VE2102/VE2002 & VM1102
  - System Logic cells up to 328.72K Logic cells and up to 300.544K Configurable Logic Blocks and 150.227K LUTs .
  - Processing System with integrated Dual-core Cortex-A72 Cores application processor and Dual-core Cortex-R5F Cores real-time processing and control.
  - Programmable Network on Chip (NoC)
  - 40G Multi-rate Ethernet MAC
  - AIE-ML Data & Shared memory

**PMIC**

- Dialog's DA9062 PMIC Regulator 1 & 2

**Memory**

- 256MB QSPI Flash (Expandable)
- 16GB eMMC Flash (Expandable)
- 4GB LPDDR4 (Expandable)

**Clock Generator**

- 6-bit Clock synthesizer

**Other On-SOM Features**

- 10/100/1000 Ethernet PHY Transceiver
- USB2.0 PHY Transceiver
- FAN Header

**Board to Board Connector1 Interfaces (240pin)**

**From PL Block**

- 12 LVDS/24 Single ended signals from XP Bank 702[2]
- 27 LVDS/54 Single ended signals from XP Bank 703[2]
- 20 Single ended signals from HD Bank 302[2]
- Synchronous Clock In/Out
- 10MHz Reference Clock Input

**Board to Board Connector2 Interfaces (240pin)**

**From PS Block**

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- USB2.0 OTG x 1 Port (through ON-SOM USB2.0 PHY Transceiver)
- RGMII Interface x1
- SD1 (4bit) x1 Port
- UART x1 Port
- PMC I2C x1 Port
- SPI(3CS) x1 Port
- CAN FD x1 Port
- PS JTAG x1 Port

**From PL Block**

- PL-GTYP High Speed Transceivers (up to 32 Gbps) x 8[1]
- 1PPS Clock Input

**General Specification**

- Power Supply : 5V (from Board-to-Board Connector2)
- Form Factor : 50mm x 60mm

*Note:*

*[1] GTYP Transceiver's are not supported in VE2002 & VE2102 devices.*

*[2] In Versal AI Edge/Prime SOM, PL XP & HD IO BANKs supports variable IO voltage setting which configurable through software.*

### 2.3 Versal AI Edge

As an adaptive compute acceleration platform (ACAP), the Versal AI Edge series allows developers to rapidly evolve their sensor fusion and AI algorithms while leveraging the world's most scalable device portfolio for diverse performance and power profiles from edge to endpoint. This is a composition of Scalar Engines, Adaptable Engines, and Intelligent Engines with leading-edge memory and interfacing technologies. As an adaptive compute acceleration platform (ACAP), the Versal AI Edge series allows developers to rapidly evolve their sensor fusion and AI algorithms while leveraging the world's most scalable device portfolio for diverse performance and power profiles from edge to endpoint. It also supports a such as 32 Gbps high-speed transceiver blocks to support all necessary protocols in edge applications, 40G multi-rate Ethernet, PCIe, and native MIPI support for vision sensors which are a must for advanced AI applications. The Versal AI Edge integrated with Processing system (PS) and programmable logic (PL) in a single device. Versal's Processing system includes dual-core Arm Cortex™-A53 and dual-core Arm Cortex-R5F based processing system.

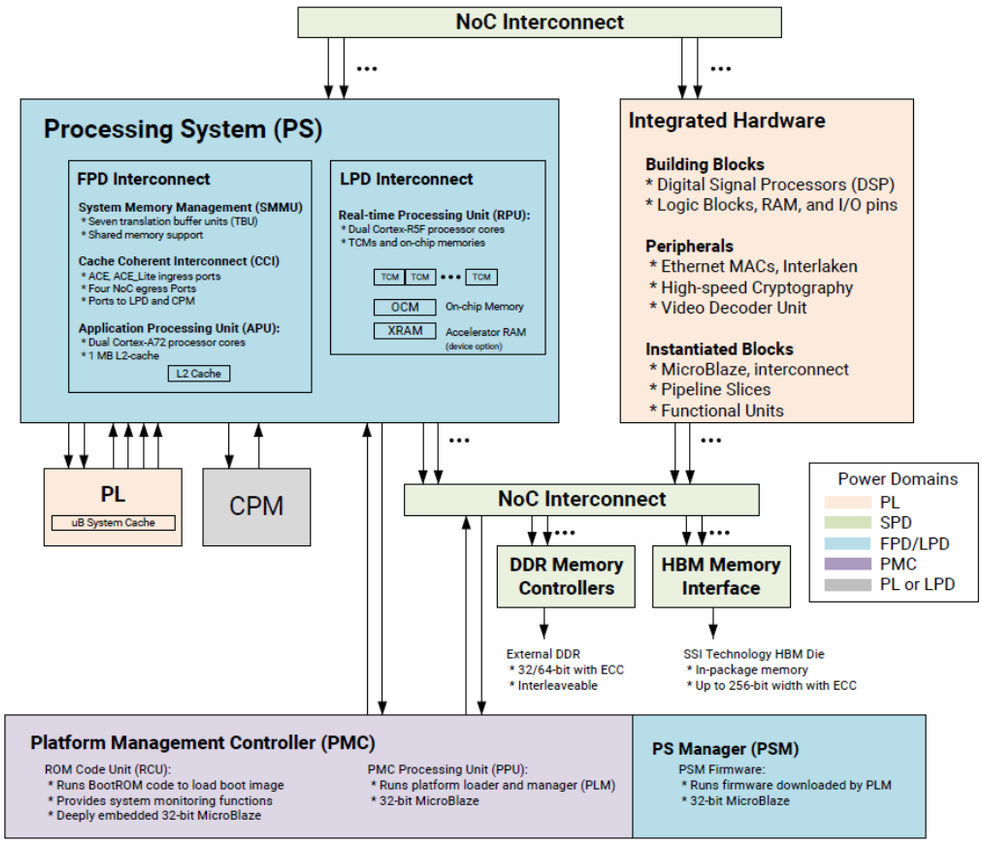


**Figure 1: Versal AI Edge Simplified Block Diagram**

*Note: Please refer the latest Versal AI Edge Datasheet & Technical Reference Manual for more details which may be revised from time to time.*

The Versal AI Edge/Prime SOM is compatible for VE2302/VE2202/VE2102/VE2002 & VM1102 with SFVA784 Pin package of Versal AI Edge devices. This SFVA784 pin package is a 784 pin 23 mm x 23mm with 0.8mm ball pitch. The Versal AI Edge SOM is compatible to VE2302, VE2202, VE2102, VE2002 & VM1102 devices and feature comparison between these devices are shown below.

| Features | VE2002 | VE2102 | VE2202 | VE2302 | VM1102 |
|---|---|---|---|---|---|
| APU | Dual-core Arm Cortex-A72; 48KB/32KB L1 Cache w/ parity and ECC; 1MB L2 Cache w/ ECC | | | | |
| RPU | Dual-core Arm Cortex-R5F; 32KB/32KB L1 Cache, and TCM w/ECC | | | | |
| Memory | 256KB On-Chip Memory w/ECC | | | | |
| Connectivity | Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2) | | | | |
| DDR Memory Controllers | 1 | 1 | 1 | 1 | 1 |
| PCIe-GEN4 | 0 | 0 | 1 | 1 | 0 |
| 40G Multirate Ethernet MAC | 0 | 0 | 1 | 1 | 0 |
| 100G Multirate Ethernet MAC | 0 | 0 | 0 | 0 | 1 |
| AI Engines-ML | 8 | 12 | 24 | 32 | 0 |
| AIE/AIE-ML Data Memory (Mb) | 4 | 6 | 12 | 17 | 0 |
| AIE-ML Shared Memory (Mb) | 48 | 48 | 68 | 68 | 0 |
| AIE to NoC Interface Tiles | 2 | 2 | 6 | 6 | 0 |
| AIE to PL Interface Tiles | 7 | 7 | 12 | 12 | 0 |
| DSP Engines | 90 | 176 | 324 | 464 | 464 |
| System Logic Cells | 43,750 | 80,080 | 229,688 | 328,720 | 328,720 |
| CLB Flip-Flops | 40,000 | 73,216 | 210,000 | 300,544 | 300,544 |
| LUTs | 20,000 | 36,608 | 105,000 | 150,272 | 150,272 |
| Distributed RAM (Mb) | 0.6 | 1.1 | 3.2 | 4.6 | 4.6 |
| Block RAM Blocks | 24 | 47 | 108 | 155 | 155 |
| Block RAM (Mb) | 0.8 | 1.7 | 3.8 | 5.4 | 5.4 |
| UltraRAM Blocks | 24 | 47 | 108 | 155 | 155 |
| UltraRAM (Mb) | 6.8 | 13.2 | 30.4 | 43.6 | 43.6 |
| Accelerator RAM (Mb) | 32 | 32 | 32 | 32 | 32 |
| XPIO | 96 | 96 | 96 | 96 | 96 |
| HDIO | 20 | 20 | 20 | 20 | 20 |
| GTYP Transceivers | 0 | 0 | 8 | 8 | 8 |

The Versal AI Edge, Processing System (PS) supports a total 78 dedicated I/O pins referred as MIO (Multiplexed I/O) for peripheral interfaces. These 78 MIO pins are divided as Platform Management Controller (PMC) and Low Power Domain (LPD). The PMC supports total 52 MIO with BANK 500 & 501 and each bank includes 26 device pins. The LPD supports a 26 MIO with Bank 502 and this bank also includes a 26 MIO pins. 78 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in Versal to route IO peripheral interfaces to PL Bank I/O pins referred as EMIO (Extended MIO). Versal AI Edge PS Peripheral Pin mapping options between MIO & EMIO is shown below.

**Table 3: MIO and EMIO Pin Mapping Table**

| Peripheral Interface | Controller Location | PMC MIO | LPD MIO | EMIO | Notes |
|---|---|---|---|---|---|
| CAN_FD 0,1 | LPD | Yes | Yes | Yes | - |
| GEM 0,1 | LPD | Yes | Yes | - | RGMII |
| | | - | - | Yes | GMII/MII, TSU, and external FIFO |
| | | Yes | Yes | Yes | MDIO |
| LPD DMA | LPD | - | - | YES | Flow control |
| PMC_GPIO | PMC | Yes | - | - | Bank 0,1 (no Bank 2) |
| | | - | - | Yes | BANK 3,4 |
| LPD_GPIO | LPD | - | Yes | - | LPD GPIO BANK 0 (no Bank 1,2) |
| | | - | - | Yes | LPD GPIO Bank 3 |
| LPD_I2C 0,1 | LPD | Yes | Yes | Yes | - |
| PMC_I2C | PMC | Yes | - | Yes | - |
| Octal SPI | PMC | Yes | - | | - |
| SD/eMMC 0, 1 | PMC | Yes | - | Yes | - |
| Select MAP | PMC | Yes | - | | - |
| SPI 0, 1 | LPD | Yes | Yes | Yes | - |
| Quad SPI | PMC | Yes | | | - |
| UART 0, 1 | LPD | Yes | Yes | Yes | MIO only includes RX, TX, CTS, and RTS |
| USB_2.0 | LPD | Yes | | | ULPI |
| LPD_SWDT | LPD | Yes | Yes | Yes | - |

The Versal AI Edge PL Banks are classified as Xtreme Performance (XP) banks or high-density (HD) banks. The XP Bank IO's are optimized for highest performance operation organized in a banks of 700, 701, 702 & 703. Each XPIO bank contains a 54 SE / 27 LVDS pins. The HD Bank I/O's are reduced-feature I/O's organized in a bank of 302 with 20 SE pins.

In Versal AI Edge, each XPIO bank supports four Global Clock (GC) input pin pairs. GC pins have direct access to the global clock buffers, MMCMs and DPLLs of the same Bank. The HD bank supports a two High Density Global Clock (HDGC) input pin pair and have direct access only to the DPLL.

Also, Versal AI Edge supports 8 high-speed transceiver GTYP from Programmable Logic (PL). These transceivers are arranged in groups of four known as a transceiver Quad with Bank 103 & Bank 104 and supported line rate of 32 Gb/s.

#### 2.3.1.1 SoC Power

The Versal AI Edge/ Prime SOM uses discrete power regulators along with two DA9062 PMIC from Dialog Semiconductor for SoC power management. The Versal SOM supports a -2 & -1 speed grade. The -2 devices can operate at a VCCINT voltage of 0.88V (H), 0.80V (M), or 0.70V (L), and the -1 devices can operate at a VCCINT voltage of 0.80V (M) or 0.70V (L). Primary supply operating voltages typically scale with VCCINT, except for supported overdrive of the VCC_PMC, VCC_PSFP, VCC_PSLP, and VCC_CPM5 at 0.88V (H) when VCCINT and other primary supplies operate at 0.70V (L). Also, all PS Bank I/O voltage is fixed to 1.8V.

The I/O voltage of PL XP Banks 700 & 701 are connected to LPDDR4 and generated from On SOM buck regulator with 1.1V. The other two XP Banks 702 & 703 voltages which are connected to Board-to-Board Connectors 1 are generated from PMIC Regulator 1 of LDO2 and LDO3 respectively with 1.0V and 1.8V. The Voltage of XP and HD bank on Versal SOM can be configurable through software after bootup.

#### 2.3.1.2 SoC Reset

The Versal AI Edge Prime SOM uses PMIC Regulator2's Reset output (nRESET) for PS Power On Reset and connected to POR_B_503 pin of SoC.

#### 2.3.1.3 Versal System Monitor

The System Monitor (SYSMON) resides in the PMC and monitors operating conditions on the device. The SYSMON can access internal sensors for monitoring internal power supplies and temperature. The results captured by the SYSMON are stored in a register map that is accessible through platform management controller resources. MIO or high-density I/O (HDIO) pins can be used by the SYSMON for measuring voltage levels external to the device.

#### 2.3.1.4 Versal Configuration Power & Status LEDs

The Platform management controller (PMC) is responsible for booting the Versal from the primary boot source in a multi-stage boot process that supports both a non-secure and a secure boot. Upon reset, device executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip RAM.

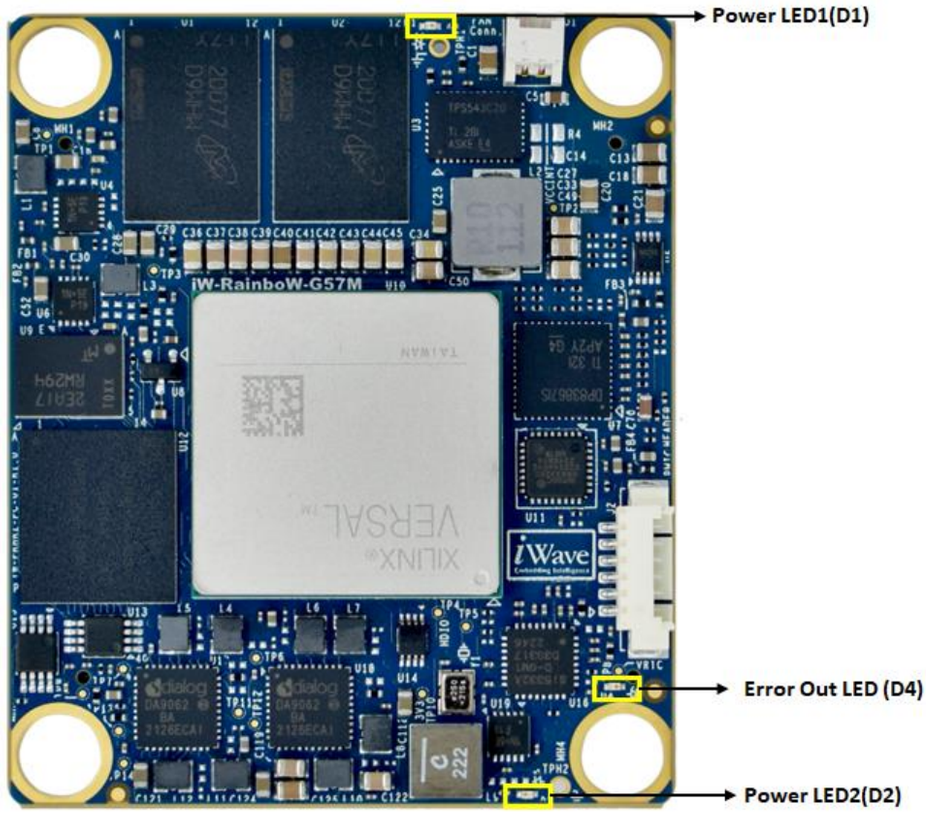


**Figure 2:Indication LEDs**

The Versal AI Edge/Prime SOM supports two LEDs for the Power LED indication and error Out indication. LED D1 & D2 is for Power Status LEDs. D2 LED is connected to PMIC 2 last power rail of the SOM in power sequence to make all the powers are stable. LED D4 is for Error Out indication it is asserted for accidental loss of power, a hardware error and not booting etc..

The Versal AI Edge/Prime SOM supports one dedicated input and output configuration pins. PUDC_B pin is an input and is used to select the behaviour of the XPIO or HDIO during configuration and this pin is connected pullup of VCC_1V8 through 4.7K by default. If the pins is high PL IOs are in tri-stated and if this pin is low PL IOs internal pullups are enabled.

DONE_503 is output and its in open drain pin with weak internal pullup. This pin will become high when the boot sequence is complete. By default this pin is connected to VCC_1V8 through 4.7K.

#### 2.3.1.5 Versal Boot Mode Configuration

In Versal AI Edge/Prime SOM, Boot modes are categorized into master and slave mode. The master boot modes automatically load the programmable device image from a memory source and the slave boot modes require an external processor or controller to load the programmable device image with a command set (JTAG or SelectMAP). Versal SOM can support Quad SPI, SD1, & JTAG as boot device and configurable through boot mode pins. These boot mode pins can be controlled from the D12,D13 & D14 pin of board to board connector2. Upon reset, the mode pins are read to determine the primary boot device. By default PS Mode 0,1,2 signals are directly connected to VCC_1V8 through 200Kilo Ohm and PS Mode 3 signal is connected to ground 10Kilo ohm

**Table 4: Boot Mode Switch Truth Table**

| Versal AI Edge Boot Mode | SW4 (4 Position Switch) | | | |
|---|---|---|---|---|
| | PS Mode 0 (Boot SEL0) SW4.1 | PS Mode 1 (Boot SEL1) SW4.2 | PS Mode 2 (Boot SEL2) SW4.3 | Switch Position Image |
| **PS JTAG** | OFF | OFF | OFF |  |
| **SD1** | ON | OFF | ON |  |
| **QSPI** | OFF | ON | OFF |  |

*Note: SW4 boot media switch is assembled in the Carrier board to control SOM Boot media and SOM boot mode signals are connected to SW4 through Board-to-Board connector2.*

### 2.3.2 Clock Design

#### 2.3.2.1 Clock Synthesizer

The Versal AI Edge/Prime SOM supports on-Board 6-Bit Clock Synthesizer “SI5332A-D-GM1” from Skyworks Solution. This clock synthesizer provides all clock source for whole SOM & other peripheral to make the system completely synchronized. Also Versal AI Edge SOM one dedicated on board oscillator for PS reference clock.

**Table 5: Clock Synthesizer Input & Output**

| Sl. No | Clock Synthesizer In/Out | Frequency | Versal AI Edge Pin Name / Net Name | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| **Input Reference Clock Options to Clock Synthesizer** | | | | | | |
| **1** | CLKIN_2/ CLKIN_2b | 100 MHz | MSIO/SYS_SYNC_CLK_INP/MSIO/SYS_SYNC_CLK_INN | NA | 1.8V, LVDS | External clock input from A15, A16th pin of B2B1 |
| **2** | CLKIN_2 | 10 Mhz | MSIO/SYS_SYNC_CLK_INP | NA | 1.8V, LVCMOS | External clock input from A47th pin of B2B1 (Optional) |
| **3** | XA/XB | 25 MHz | CLK_XA/CLK_XB | NA | - | External Crystal input |
| **Output Clock from Clock Synthesizer** | | | | | | |
| **1** | OUT0/ OUT0b | 156.25MHz | GTYP_REFCLK1P_103/ GTYP_REFCLK1P_103 | K7, K6 | LVDS | Reference clock1 for GTYP Bank 103 |
| **2** | OUT1/ OUT1b | 156.25MHz | GTYP_REFCLK1P_104/GTYP_REFCLK1N_104 | F7, F6 | LVDS | Reference clock1 for GTYP Bank 104 |
| **3** | OUT2/ OUT2b | 200MHz | XP_N23_LVDS702_L24P_GC/ XP_N24_LVDS702_L24N_GC | N23, N24 | LVDS | LPDDR4 Bank reference clock |
| **4** | OUT3 | 25MHz | GEM0_XI_CLK | NA | 1.8V, LVCMOS | GEM0 Ethernet PHY REF Clock |
| **5** | OUT4 | 24MHz | USB0_XI_CLK | NA | 1.8V, LVCMOS | USB 2.0 Transceiver PHY Clock |
| **6** | OUT5/ OUT5b | 100MHz | MSIO/SYS_SYNC_CLK_OUTp/ MSIO/SYS_SYNC_CLK_OUTn | NA | 3.3V, LVDS | Clock input to A31 & A32 pin of B2B1. |

| | | | | | | |
|---|---|---|---|---|---|---|
| **PS Dedicated Input Oscillator** | | | | | | |
| **1** | OUT | 33.3333MHz | MSIO/SYS_SYNC_CLK_INP /MSIO/SYS_SYNC_CLK_IN N | U14 | 1.8V, LVCMOS | Single ended reference clock for PS. |

### 2.3.3 Versal AI Edge/Prime SOM PMIC's

The Versal AI Edge SOM supports two Dialog semiconductor DA9062 PMIC. The PMC I2C module of Versal AI Edge PS is used for PMIC interface through MIO pins.

#### 2.3.3.1 PMIC Regulator 1 with RTC

The PMC I2C module of Versal AI Edge/Prime SOM is used for PMIC 1 chip through Versal AI Edge pins with I2C address 0x48/0x49.

PMIC's BUCK 3 is connected to I/O voltage of PS MIO Banks (MIO Bank 500, 501, 502 & 503). The I/O voltage is configured to fixed 1.8V by PMIC's internal OTP during power up.

PMIC's LDO2 & LDO3 are connected to I/O voltage of PL XPIO Banks (PL Bank 702, & 703). The I/O voltage is configured to 1.0 by PMIC's internal OTP during power up. The I/O voltage is configurable through software to 1.5V after bootup.

PMIC's LDO4 are connected to I/O voltage of PL HD Banks (PL Bank 302). The I/O voltage is configured to 1.8V by PMIC's internal OTP during power up. The I/O voltage is configurable through software to 1.8V after bootup.

The Other PMIC's Buck and LDO regulator is used for on board SOM peripherals. The PMIC supports Real Time Clock functionality. It uses the Coin cell battery power from D9th pin of Board-to-Board Connector2 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

#### 2.3.3.2 PMIC Regulator 2 without RTC

The I2C module of Versal AI Edge/Prime SOM is used for PMIC 2 interface through Versal AI Edge pins with I2C address 0x58/0x59. The 2nd PMIC's Buck and LDO regulator is used for on SOM peripherals. Also, PMIC supports reset output and connected to Versal AI Edge (POR_B_503) for power on reset.

*Important Note: Every Power Off and On, The DA9062 PMIC work as initial OTP Setting*

### 2.3.4 SOM Memory

#### 2.3.4.1 LPDDR4 SDRAM

The Versal AI Edge SOM supports 64bit, 4GB LPDDR4 RAM memory. Two 32 bit, 2GB LPDDR4 SDRAM ICs are used to support a total on board RAM memory of 4GB. These LPDDR4 devices operates at 3733MT/s data rate. Versal AI Edge SOM, PL XPIO bank of 700 & 701 are used for LPDDR4 interface.Also the integrated DDR memory controller(DDRMC) is attached to the NoC interconnect.

The Versal AI Edge SOM supports 300MHz LVDS clock from Clock synthesizer to PL XPIO bank of 702 for LPDDR4 bank reference clock and it is connected to N23 & N24 clock input pins through AC Coupling capacitors.

#### 2.3.4.2 QSPI Flash

The Versal AI Edge/Prime SOM supports 256MB of Quad SPI through QSPI interface. The QSPI controller use an interface through MIO pins of Versal SOM with 1.8V voltage level. The SOM supports 8-bit QSPI Flash. By default, mode bit is configured for QSPI Flash as configuration device.

#### 2.3.4.3 eMMC Flash

The Versal AI Edge/Prime SOM supports 8-bit, 16GB of eMMC Flash memory for Storage of Versal AI Edge PS. This eMMC Flash memory is directly connected to the SD0 controller of the Versal's PS through MIO pins and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC 5.1 standard with up to 8bit HS400 mode. The eMMC Flash size can be expandable based on the availability of higher density eMMC Flash device.

## 2.4 On SOM Features

### 2.4.1 Fan Header

The Versal AI Edge/Prime SOM supports a Fan Header (J1) to connect cooling Fan if required. The Fan Header (J1) is physically located on top side of the SOM as shown below.

Number of Pins - 2

Connector Part - 0530480210 from Molex

Mating Connector - 51021-0200 from Molex

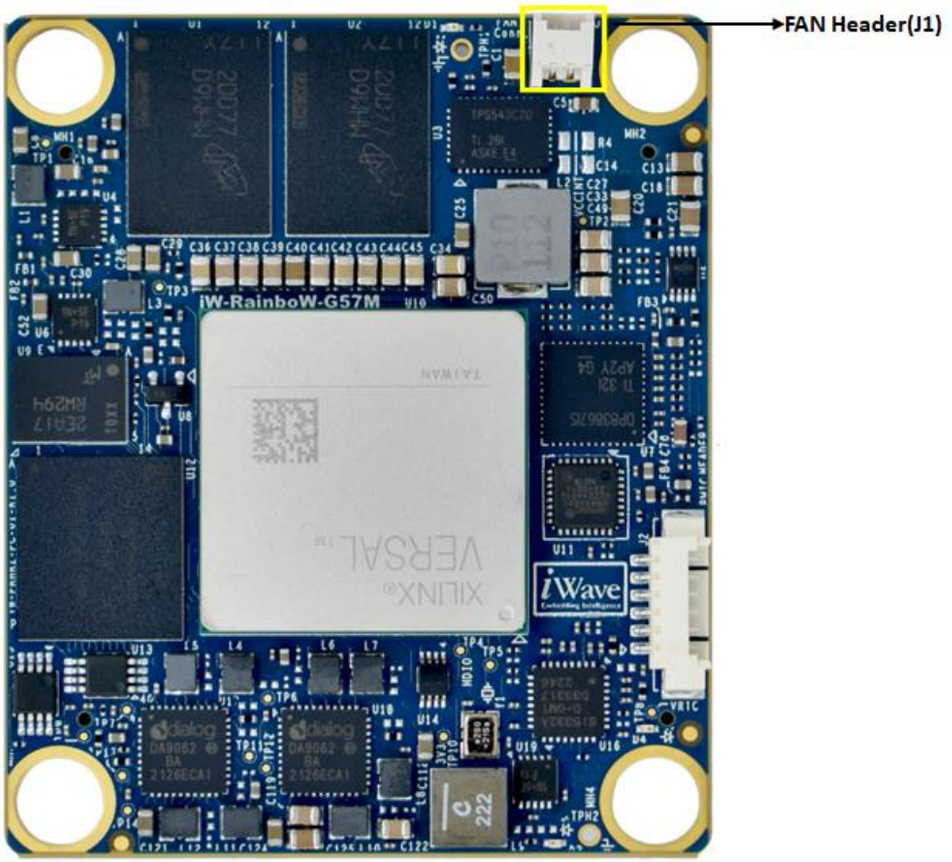


**Figure 3: Fan Header**

**Table 6: Fan Header Pinout**

| Pin No | Signal Name | Versal Pin Name | Versal Bank | Versal Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| **1** | VCC_5V | - | - | - | O, 5V Power | Supply Voltage. |
| **2** | GND | - | - | - | Power | Ground. |

### 2.5 Board to Board Connector1

The Versal AI Edge/Prime SOM supports two 240 pin high speed ruggedized terminal strip connectors for interfaces expansion. All the effort is made in Versal AI Edge SOM design to provide the maximum interfaces of Versal AI Edge to the carrier board by adding these two Board to Board Connectors.

The Versal AI Edge/Prime SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1 (J4) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240
Connector Part Number - ADM6-60-01.5-L-4-2-A-TR from Samtech
Mating Connector - ADF6-60-03.5-L-4-2-A-TR from Samtech
Staking Height - 5mm

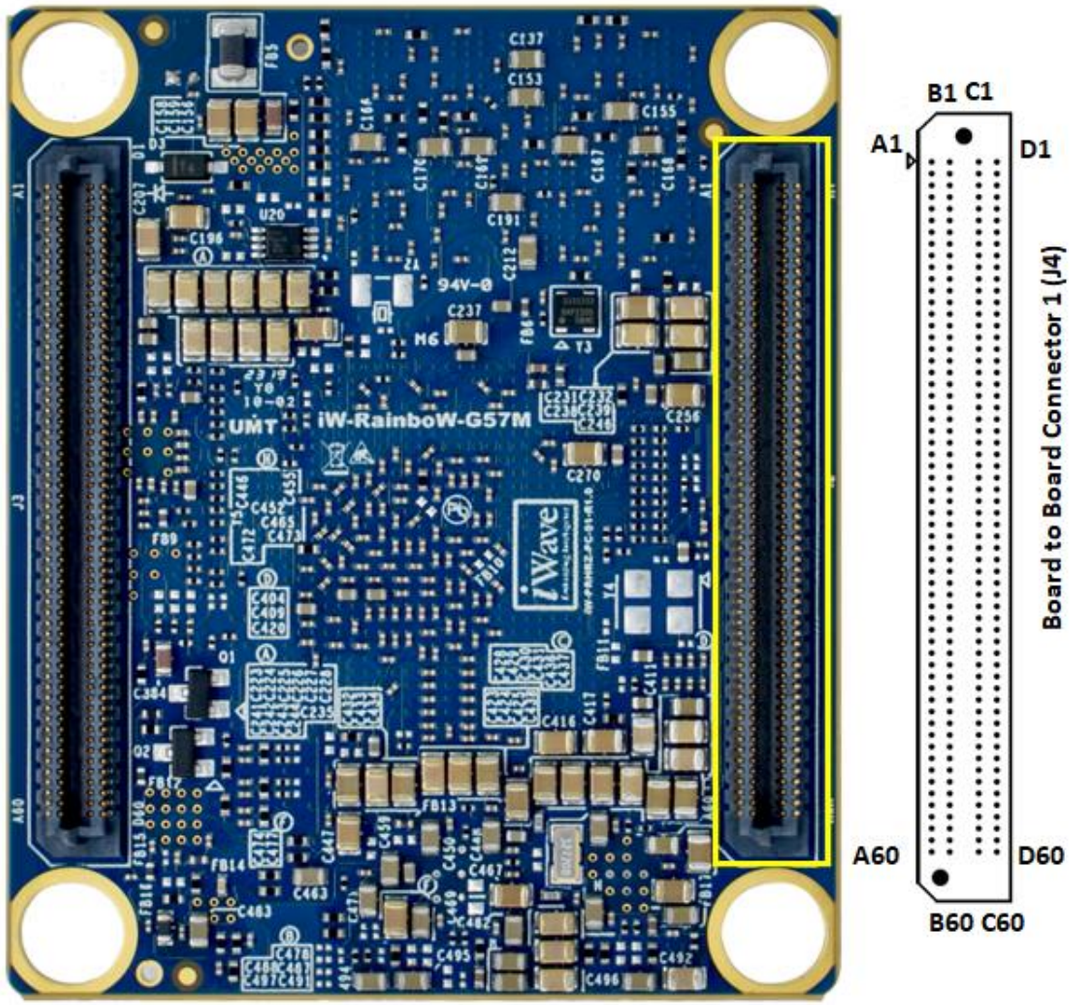


**Figure 4: Board to Board Connector 1**

**Table 7: : Board to Board Connector1 Pinout**

| B2B-1 Pin | Signal Name | B2B-1 Pin | Signal Name | B2B-1 Pin | Signal Name | B2B-1 Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| **A1** | NC | **B1** | VCCO_HDIO | **C1** | VCCO_XPIO_702 | **D1** | VCCO_XPIO_703 |
| **A2** | XP_G25_LVDS703_L7P | **B2** | XP_J27_LVDS703_L0P | **C2** | XP_C27_LVDS703_L5P | **D2** | XP_G21_LVDS703_L18P |
| **A3** | XP_G26_LVDS703_L7N | **B3** | XP_H28_LVDS703_L0N | **C3** | XP_B28_LVDS703_L5N | **D3** | XP_H22_LVDS703_L18N |
| **A4** | XP_F26_LVDS703_L8P | **B4** | XP_H27_LVDS703_L1P | **C4** | XP_D27_LVDS703_L4P | **D4** | XP_E20_LVDS703_L19P |
| **A5** | XP_E26_LVDS703_L8N | **B5** | XP_G28_LVDS703_L1N | **C5** | XP_C28_LVDS703_L4N | **D5** | XP_F21_LVDS703_L19N |
| **A6** | XP_H25_LVDS703_L6P_GC | **B6** | XP_G27_LVDS703_L2P | **C6** | XP_E27_LVDS703_L3P | **D6** | XP_D20_LVDS703_L20P |
| **A7** | XP_J26_LVDS703_L6N_GC | **B7** | XP_F28_LVDS703_L2N | **C7** | XP_E28_LVDS703_L3N | **D7** | XP_D21_LVDS703_L20N |
| **A8** | GND | **B8** | GND | **C8** | GND | **D8** | GND |
| **A9** | XP_B20_LVDS703_L21P | **B9** | XP_C25_LVDS703_L9P_GC | **C9** | XP_F23_LVDS703_L24P_GC | **D9** | XP_H23_LVDS703_L12P_GC |
| **A10** | XP_C21_LVDS703_L21N | **B10** | XP_B25_LVDS703_L9N_GC | **C10** | XP_F24_LVDS703_L24N_GC | **D10** | XP_H24_LVDS703_L12N_GC |
| **A11** | XP_A20_LVDS703_L22P | **B11** | XP_A25_LVDS703_L10P | **C11** | XP_E24_LVDS703_L25P | **D11** | XP_F22_LVDS703_L13P |
| **A12** | XP_A21_LVDS703_L22N | **B12** | XP_A26_LVDS703_L10N | **C12** | XP_F25_LVDS703_L25N | **D12** | XP_G23_LVDS703_L13N |
| **A13** | XP_C22_LVDS703_L23P | **B13** | XP_B26_LVDS703_L11P | **C13** | XP_D25_LVDS703_L26P | **D13** | XP_E22_LVDS703_L14P |
| **A14** | XP_B22_LVDS703_L23N | **B14** | XP_B27_LVDS703_L11N | **C14** | XP_D26_LVDS703_L26N | **D14** | XP_E23_LVDS703_L14N |
| **A15** | MSIO/SYS_SYNC_CLK_INp | **B15** | XP_D24_LVDS703_L15P | **C15** | XP_A23_LVDS703_L17P | **D15** | XP_C23_LVDS703_L16P |
| **A16** | MSIO/SYS_SYNC_CLK_INN | **B16** | XP_C24_LVDS703_L15N | **C16** | XP_A24_LVDS703_L17N | **D16** | XP_B23_LVDS703_L16N |
| **A17** | GND | **B17** | GND | **C17** | GND | **D17** | GND |
| **A18** | XP_T23_LVDS702_L13P | **B18** | NC | **C18** | NC | **D18** | XP_M22_LVDS702_L15P |
| **A19** | XP_R24_LVDS702_L13N | **B19** | NC | **C19** | NC | **D19** | XP_M23_LVDS702_L15N |
| **A20** | XP_R23_LVDS702_L14P | **B20** | NC | **C20** | NC | **D20** | XP_L23_LVDS702_L16P |
| **A21** | XP_P24_LVDS702_L14N | **B21** | NC | **C21** | NC | **D21** | XP_K24_LVDS702_L16N |
| **A22** | XP_U23_LVDS702_L12P_GC | **B22** | NC | **C22** | NC | **D22** | XP_K23_LVDS702_L17P |
| **A23** | XP_T24_LVDS702_L12N_GC | **B23** | NC | **C23** | NC | **D23** | XP_J24_LVDS702_L17N |
| **A24** | GND | **B24** | GND | **C24** | GND | **D24** | GND |
| **A25** | XP_T21_LVDS702_L19P | **B25** | XP_N21_LVDS702_L21P | **C25** | NC | **D25** | NC |
| **A26** | XP_R22_LVDS702_L19N | **B26** | XP_M21_LVDS702_L21N | **C26** | NC | **D26** | NC |
| **A27** | XP_R21_LVDS702_L20P | **B27** | XP_K21_LVDS702_L22P | **C27** | NC | **D27** | NC |
| **A28** | XP_P22_LVDS702_L20N | **B28** | XP_L22_LVDS702_L22N | **C28** | NC | **D28** | NC |
| **A29** | XP_V21_LVDS702_L18P | **B29** | XP_J21_LVDS702_L23P | **C29** | NC | **D29** | NC |
| **A30** | XP_U22_LVDS702_L18N | **B30** | XP_J22_LVDS702_L23N | **C30** | NC | **D30** | NC |
| **A31** | MSIO/SYS_SYNC_CLK_OUTp | **B31** | NC | **C31** | NC | **D31** | NC |

| B2B-1 Pin | Signal Name | B2B-1 Pin | Signal Name | B2B-1 Pin | Signal Name | B2B-1 Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| **A32** | MSIO/SYS_SYNC_CLK_OUTn | **B32** | NC | **C32** | NC | **D32** | NC |
| **A33** | GND | **B33** | GND | **C33** | GND | **D33** | GND |
| **A34** | NC | **B34** | HD_B11_SE302_L8P | **C34** | HD_E12_SE302_L3P | **D34** | HD_F14_SE302_L0P |
| **A35** | NC | **B35** | HD_A11_SE302_L8N | **C35** | HD_D12_SE302_L3N | **D35** | HD_E14_SE302_L0N |
| **A36** | HD_D10_SE302_HDGC_L6P | **B36** | HD_B12_SE302_L9P | **C36** | HD_F11_SE302_L4P | **D36** | HD_C14_SE302_L1P |
| **A37** | HD_C10_SE302_HDGC_L6N | **B37** | HD_A13_SE302_L9N | **C37** | HD_E11_SE302_L4N | **D37** | HD_C13_SE302_L1N |
| **A38** | HD_D11_SE302_HDGC_L5P | **B38** | NC | **C38** | HD_B10_SE302_L7P | **D38** | HD_E13_SE302_L2P |
| **A39** | HD_C12_SE302_HDGC_L5N | **B39** | NC | **C39** | HD_A10_SE302_L7N | **D39** | HD_D14_SE302_L2N |
| **A40** | GND | **B40** | GND | **C40** | GND | **D40** | GND |
| **A41** | NC | **B41** | NC | **C41** | NC | **D41** | NC |
| **A42** | NC | **B42** | NC | **C42** | NC | **D42** | NC |
| **A43** | NC | **B43** | NC | **C43** | NC | **D43** | NC |
| **A44** | NC | **B44** | NC | **C44** | NC | **D44** | NC |
| **A45** | NC | **B45** | NC | **C45** | NC | **D45** | NC |
| **A46** | NC | **B46** | NC | **C46** | NC | **D46** | NC |
| **A47** | MSIO/10MHZ_REFCLK_IN | **B47** | NC | **C47** | NC | **D47** | NC |
| **A48** | GND | **B48** | NC | **C48** | NC | **D48** | NC |
| **A49** | NC | **B49** | GND | **C49** | NC | **D49** | GND |
| **A50** | NC | **B50** | GND | **C50** | NC | **D50** | GND |
| **A51** | GND | **B51** | NC | **C51** | GND | **D51** | NC |
| **A52** | GND | **B52** | NC | **C52** | GND | **D52** | NC |
| **A53** | NC | **B53** | GND | **C53** | NC | **D53** | GND |
| **A54** | NC | **B54** | GND | **C54** | NC | **D54** | GND |
| **A55** | GND | **B55** | NC | **C55** | GND | **D55** | NC |
| **A56** | GND | **B56** | NC | **C56** | GND | **D56** | NC |
| **A57** | NC | **B57** | GND | **C57** | NC | **D57** | GND |
| **A58** | NC | **B58** | GND | **C58** | NC | **D58** | GND |
| **A59** | GND | **B59** | NC | **C59** | GND | **D59** | NC |
| **A60** | GND | **B60** | NC | **C60** | GND | **D60** | NC |

**Power rails are highlighted in RED and Clock signals are highlighted in purple.*

### 2.5.1 PL Interfaces

The interfaces which are supported in Board-to-Board Connector1 from Versal AI Edge/Prime SOM, PL is explained in the following section.

### 2.5.2 PL IOs – XPIO BANK 703

The Versal AI Edge/Prime SOM supports 27 LVDS IOs/54 Single Ended (SE) IOs on Board-to-Board Connector1 from Versal XPIO Bank 703. Upon these 27 LVDS IOs/54 SE IOs, up to 4 GC Global Clock Inputs.

The IO voltage of PL Bank 703 is connected from LDO3 output of PMIC Regulator 1 and it supports variable IO voltage setting. IO voltage is set as 1.0V during power up. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO3 output to appropriate IO voltage for Bank 703. By default, IO voltage of PL Bank 703 is set as 1V and after U-boot bootup configurable to 1.5V. For more details about supported IO standard, refer the Versal AI Edge datasheet.

In Versal AI Edge/Prime SOM, PL Bank 703 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though PL Bank 703 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins A6, A7, B9, B10, C9, C10 D9, and D10, are GC Global Clock Input capable pins of PL Bank 703.

For more details on PL XPIO Bank 703 pinouts on Board-to-Board Connector1, refer the below table.

**Table 8: PL XPIO Bank 703**

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| A2 | XP_G25_LVDS703_L7P | IO_L7P_N2P2_703 | 703 | G25 | IO, 1.5V | XP Bank703 IO7 differential positive or single ended I/O. |
| A3 | XP_G26_LVDS703_L7N | IO_L7N_N2P3_703 | 703 | G26 | IO, 1.5V | XP Bank703 IO7 differential negative or single ended I/O. |
| A4 | XP_F26_LVDS703_L8P | IO_L8P_N2P4_703 | 703 | F26 | IO, 1.5V | XP Bank703 IO8 differential positive or single ended I/O. |
| A5 | XP_E26_LVDS703_L8N | IO_L8N_N2P5_703 | 703 | E26 | IO, 1.5V | XP Bank703 IO8 differential negative or single ended I/O. |
| A6 | XP_H25_LVDS703_L6P_GC | IO_L6P_GC_XCC_N2P0_703 | 703 | H25 | IO, 1.5V | XP Bank703 IO6 differential positive or single ended I/O. Same pin can be used as Global Clock input. |
| A7 | XP_J26_LVDS703_L6N_GC | IO_L6N_GC_XCC_N2P1_703 | 703 | J26 | IO, 1.5V | XP Bank703 IO6 differential negative or single ended I/O. Same pin can be used as Global Clock input. |
| A9 | XP_B20_LVDS703_L21P | IO_L21P_XCC_N7P0_703 | 703 | B20 | IO, 1.5V | XP Bank703 IO21 differential positive or single ended I/O. |
| A10 | XP_C21_LVDS703_L21N | IO_L21N_XCC_N7P1_703 | 703 | C21 | IO, 1.5V | XP Bank703 IO21 differential negative or single ended I/O. |

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| A11 | XP_A20_LVDS703_L22P | IO_L22P_N7P2_703 | 703 | A20 | IO, 1.5V | XP Bank703 IO22 differential positive or single ended I/O. |
| A12 | XP_A21_LVDS703_L22N | IO_L22N_N7P3_703 | 703 | A21 | IO, 1.5V | XP Bank703 IO22 differential negative or single ended I/O. |
| A13 | XP_C22_LVDS703_L23P | IO_L23P_N7P4_703 | 703 | C22 | IO, 1.5V | XP Bank703 IO23 differential positive or single ended I/O. |
| A14 | XP_B22_LVDS703_L23N | IO_L23N_N7P5_703 | 703 | B22 | IO, 1.5V | XP Bank703 IO23 differential negative or single ended I/O. |
| B2 | XP_J27_LVDS703_L0P | IO_L0P_XCC_N0P0_703 | 703 | J27 | IO, 1.5V | XP Bank703 IO0 differential positive or single ended I/O. |
| B3 | XP_H28_LVDS703_L0N | IO_L0N_XCC_N0P1_703 | 703 | H28 | IO, 1.5V | XP Bank703 IO0 differential negative or single ended I/O. |
| B4 | XP_H27_LVDS703_L1P | IO_L1P_N0P2_703 | 703 | H27 | IO, 1.5V | XP Bank703 IO1 differential positive or single ended I/O. |
| B5 | XP_G28_LVDS703_L1N | IO_L1N_N0P3_703 | 703 | G28 | IO, 1.5V | XP Bank703 IO1 differential negative or single ended I/O |
| B6 | XP_G27_LVDS703_L2P | IO_L2P_N0P4_703 | 703 | G27 | IO, 1.5V | XP Bank703 IO2 differential positive or single ended I/O. |
| B7 | XP_F28_LVDS703_L2N | IO_L2N_N0P5_703 | 703 | F28 | IO, 1.5V | XP Bank703 IO2 differential negative or single ended I/O. |
| B9 | XP_C25_LVDS703_L9P_GC | IO_L9P_GC_XCC_N3P0_703 | 703 | C25 | IO, 1.5V | XP Bank703 IO9 differential positive or single ended I/O. Same pin can be used as Global Clock input. |
| B10 | XP_B25_LVDS703_L9N_GC | IO_L9N_GC_XCC_N3P1_703 | 703 | B25 | IO, 1.5V | XP Bank703 IO9 differential negative or single ended I/O. Same pin can be used as Global Clock input. |
| B11 | XP_A25_LVDS703_L10P | IO_L10P_N3P2_703 | 703 | A25 | IO, 1.5V | XP Bank IO10 differential positive or single ended I/O. |
| B12 | XP_A26_LVDS703_L10N | IO_L10N_N3P3_703 | 703 | A26 | IO, 1.5V | XP Bank IO10 differential negative or single ended I/O. |
| B13 | XP_B26_LVDS703_L11P | IO_L11P_N3P4_703 | 703 | B26 | IO, 1.5V | XP Bank703 IO11 differential positive or single ended I/O. |
| B14 | XP_B27_LVDS703_L11N | IO_L11N_N3P5_703 | 703 | B27 | IO, 1.5V | XP Bank703 IO11 differential negative or single ended I/O. |
| B15 | XP_D24_LVDS703_L15P | IO_L15P_XCC_N5P0_703 | 703 | D24 | IO, 1.5V | XP Bank703 IO15 differential positive or single ended I/O. |
| B16 | XP_C24_LVDS703_L15N | IO_L15N_XCC_N5P1_703 | 703 | C24 | IO, 1.5V | XP Bank703 IO15 differential negative or single ended I/O. |
| C2 | XP_C27_LVDS703_L5P | IO_L5P_N1P4_703 | 703 | C27 | IO, 1.5V | XP Bank703 IO5 differential positive or single ended I/O. |
| C3 | XP_B28_LVDS703_L5N | IO_L5N_N1P5_703 | 703 | B28 | IO, 1.5V | XP Bank703 IO5 differential negative or single ended I/O. |

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| C4 | XP_D27_LVDS703_L4P | IO_L4P_N1P2_703 | 703 | D27 | IO, 1.5V | XP Bank703 IO4 differential positive or single ended I/O. |
| C5 | XP_C28_LVDS703_L4N | IO_L4N_N1P3_703 | 703 | C28 | IO, 1.5V | XP Bank703 IO4 differential negative or single ended I/O. |
| C6 | XP_E27_LVDS703_L3P | IO_L3P_XCC_N1P0_703 | 703 | E27 | IO, 1.5V | XP Bank703 IO3 differential positive or single ended I/O. |
| C7 | XP_E28_LVDS703_L3N | IO_L3N_XCC_N1P1_703 | 703 | E28 | IO, 1.5V | XP Bank703 IO3 differential negative or single ended I/O. |
| C9 | XP_F23_LVDS703_L24P_GC | IO_L24P_GC_XCC_N8P0_703 | 703 | F23 | IO, 1.5V | XP Bank703 IO24 differential positive or single ended I/O. Same pin can be used as Global Clock input. |
| C10 | XP_F24_LVDS703_L24N_GC | IO_L24N_GC_XCC_N8P1_703 | 703 | F24 | IO, 1.5V | XP Bank703 IO24 differential negative or single ended I/O. Same pin can be used as Global Clock input. |
| C11 | XP_E24_LVDS703_L25P | IO_L25P_N8P2_703 | 703 | E24 | IO, 1.5V | XP Bank703 IO25 differential positive or single ended I/O. |
| C12 | XP_F25_LVDS703_L25N | IO_L25N_N8P3_703 | 703 | F25 | IO, 1.5V | XP Bank703 IO25 differential negative or single ended I/O. |
| C13 | XP_D25_LVDS703_L26P | IO_L26P_N8P4_703 | 703 | D25 | IO, 1.5V | XP Bank703 IO26 differential positive or single ended I/O. |
| C14 | XP_D26_LVDS703_L26N | IO_L26N_N8P5_703 | 703 | D26 | IO, 1.5V | XP Bank703 IO26 differential negative or single ended I/O. |
| C15 | XP_A23_LVDS703_L17P | IO_L17P_N5P4_703 | 703 | A23 | IO, 1.5V | XP Bank703 IO17 differential positive or single ended I/O. |
| C16 | XP_A24_LVDS703_L17N | IO_L17N_N5P5_703 | 703 | A24 | IO, 1.5V | XP Bank703 IO17 differential negative or single ended I/O. |
| D2 | XP_G21_LVDS703_L18P | IO_L18P_XCC_N6P0_703 | 703 | G21 | IO, 1.5V | XP Bank703 IO18 differential positive or single ended I/O. |
| D3 | XP_H22_LVDS703_L18N | IO_L18N_XCC_N6P1_703 | 703 | H22 | IO, 1.5V | XP Bank703 IO18 differential negative or single ended I/O. |
| D4 | XP_E20_LVDS703_L19P | IO_L19P_N6P2_703 | 703 | E20 | IO, 1.5V | XP Bank703 IO19 differential positive or single ended I/O. |
| D5 | XP_F21_LVDS703_L19N | IO_L19N_N6P3_703 | 703 | F21 | IO, 1.5V | XP Bank703 IO19 differential negative or single ended I/O. |
| D6 | XP_D20_LVDS703_L20P | IO_L20P_N6P4_703 | 703 | D20 | IO, 1.5V | XP Bank703 IO20 differential positive or single ended I/O. |
| D7 | XP_D21_LVDS703_L20N | IO_L20N_N6P5_703 | 703 | D21 | IO, 1.5V | XP Bank703 IO20 differential negative or single ended I/O. |
| D9 | XP_H23_LVDS703_L12P_GC | IO_L12P_GC_XCC_N4P0_703 | 703 | H23 | IO, 1.5V | XP Bank703 IO12 differential positive or single ended I/O. Same pin can be used as Global Clock input. |

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| D10 | XP_H24_LVDS703_L12N_GC | IO_L12N_GC_XCC_N4P1_703 | 703 | H24 | IO, 1.5V | XP Bank703 IO12 differential negative or single ended I/O. Same pin can be used as Global Clock input. |
| D11 | XP_F22_LVDS703_L13P | IO_L13P_N4P2_703 | 703 | F22 | IO, 1.5V | XP Bank703 IO13 differential positive or single ended I/O. |
| D12 | XP_G23_LVDS703_L13N | IO_L13N_N4P3_703 | 703 | G23 | IO, 1.5V | XP Bank703 IO13 differential negative or single ended I/O. |
| D13 | XP_E22_LVDS703_L14P | IO_L14P_N4P4_703 | 703 | E22 | IO, 1.5V | XP Bank703 IO14 differential positive or single ended I/O. |
| D14 | XP_E23_LVDS703_L14N | IO_L14N_N4P5_703 | 703 | E23 | IO, 1.5V | XP Bank703 IO14 differential negative or single ended I/O. |
| D15 | XP_C23_LVDS703_L16P | IO_L16P_N5P2_703 | 703 | C23 | IO, 1.5V | XP Bank703 IO16 differential positive or single ended I/O. |
| D16 | XP_B23_LVDS703_L16N | IO_L16N_N5P3_703 | 703 | B23 | IO, 1.5V | XP Bank703 IO16 differential negative or single ended I/O. |

**IO Type of IOs originating from Versal AI Edge SoC is configurable. Hence for exact IO type configuration options, refer Xilinx Versal AI Edge datasheet.*

### 2.5.3 PL IOs – XPIO BANK 702

The Versal AI Edge/Prime SOM supports 12 LVDS IOs/24 Single Ended (SE) IOs on Board-to-Board Connector1 from Versal XPIO Bank 702. Upon these 12 LVDS IOs/24 SE IOs, up to 2 GC Global Clock. In that 1 GC Global Clock is directly connected to Board-to-Board Connector1 and one more GC Global Clock is connected to LPDDR4 reference Clock .

The IO voltage of PL Bank 702 is connected from LDO2 output of PMIC Regulator 1 and it supports variable IO voltage setting. IO voltage is configurable to 1.0V during power up. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO2 output to appropriate IO voltage for Bank 702. By default, IO voltage of PL Bank 702 is set as 1V and after U-boot bootup configurable to 1.5V. For more details about supported IO standard, refer the Versal AI Edge datasheet.

In the Versal AI Edge/Prime SOM, PL Bank 702 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though PL Bank 702 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins A22 and A23, are GC Global Clock Input capable pins of PL Bank 702.

For more details on PL XPIO Bank 702 pinouts on Board-to-Board Connector1, refer the below table.

**Table 9: PL XPIO Bank 702 Pinouts**

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| A18 | XP_T23_LVDS702_L13P | IO_L13P_N4P2_M0P134_702 | 702 | T23 | IO, 1.5V | XP Bank702 IO13 differential positive or single ended I/O. |
| A19 | XP_R24_LVDS702_L13N | IO_L13N_N4P3_M0P135_702 | 702 | R24 | IO, 1.5V | XP Bank702 IO13 differential negative or single ended I/O. |
| A20 | XP_R23_LVDS702_L14P | IO_L14P_N4P4_M0P136_702 | 702 | R23 | IO, 1.5V | XP Bank702 IO14 differential positive or single ended I/O. |
| A21 | XP_P24_LVDS702_L14N | IO_L14N_N4P5_M0P137_702 | 702 | P24 | IO, 1.5V | XP Bank702 IO14 differential negative or single ended I/O. |
| A22 | XP_U23_LVDS702_L12P_GC | IO_L12P_GC_XCC_N4P0_M0P132_702 | 702 | U23 | IO, 1.5V | XP Bank702 IO12 differential positive or single ended I/O. Same pin can be used as Global Clock input. |
| A23 | XP_T24_LVDS702_L12N_GC | IO_L12N_GC_XCC_N4P1_M0P133_702 | 702 | T24 | IO, 1.5V | XP Bank702 IO12 differential negative or single ended I/O. Same pin can be used as Global Clock input. |
| A25 | XP_T21_LVDS702_L19P | IO_L19P_N6P2_M0P146_702 | 702 | T21 | IO, 1.5V | XP Bank702 IO19 differential positive or single ended I/O. |
| A26 | XP_R22_LVDS702_L19N | IO_L19N_N6P3_M0P147_702 | 702 | R22 | IO, 1.5V | XP Bank702 IO19 differential negative or single ended I/O. |
| A27 | XP_R21_LVDS702_L20P | IO_L20P_N6P4_M0P148_702 | 702 | R21 | IO, 1.5V | XP Bank702 IO20 differential positive or single ended I/O. |

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| A28 | XP_P22_LVDS702_L20N | IO_L20N_N6P5_M0P149_702 | 702 | P22 | IO, 1.5V | XP Bank702 IO20 differential negative or single ended I/O. |
| A29 | XP_V21_LVDS702_L18P | IO_L18P_XCC_N6P0_M0P144_702 | 702 | V21 | IO, 1.5V | XP Bank702 IO18 differential positive or single ended I/O. |
| A30 | XP_U22_LVDS702_L18N | IO_L18N_XCC_N6P1_M0P145_702 | 702 | U22 | IO, 1.5V | XP Bank702 IO18 differential negative or single ended I/O. |
| B18 | NA | NA | NA | NA | NA | NC. |
| B19 | NA | NA | NA | NA | NA | NC. |
| B20 | NA | NA | NA | NA | NA | NC. |
| B21 | NA | NA | NA | NA | NA | NC. |
| B22 | NA | NA | NA | NA | NA | NC. |
| B23 | NA | NA | NA | NA | NA | NC. |
| B25 | XP_N21_LVDS702_L21P | IO_L21P_XCC_N7P0_M0P150_702 | 702 | N21 | IO, 1.5V | XP Bank702 IO21 differential positive or single ended I/O |
| B26 | XP_M21_LVDS702_L21N | IO_L21N_XCC_N7P1_M0P151_702 | 702 | M21 | IO, 1.5V | XP Bank702 IO21 differential negative or single ended I/O |
| B27 | XP_K21_LVDS702_L22P | IO_L22P_N7P2_M0P152_702 | 702 | K21 | IO, 1.5V | XP Bank702 IO22 differential positive or single ended I/O |
| B28 | XP_L22_LVDS702_L22N | IO_L22N_N7P3_M0P153_702 | 702 | L22 | IO, 1.5V | XP Bank702 IO22 differential negative or single ended I/O |
| B29 | XP_J21_LVDS702_L23P | IO_L23P_N7P4_M0P154_702 | 702 | J21 | IO, 1.5V | XP Bank702 IO23 differential positive or single ended I/O. |
| B30 | XP_J22_LVDS702_L23N | IO_L23N_N7P5_M0P155_702 | 702 | J22 | IO, 1.5V | XP Bank702 IO23 differential negative or single ended I/O |
| C18 | NA | NA | NA | NA | NA | NC. |
| C19 | NA | NA | NA | NA | NA | NC. |
| C20 | NA | NA | NA | NA | NA | NC. |
| C21 | NA | NA | NA | NA | NA | NC. |
| C22 | NA | NA | NA | NA | NA | NC. |
| C23 | NA | NA | NA | NA | NA | NC. |
| C25 | NA | NA | NA | NA | NA | NC. |
| C26 | NA | NA | NA | NA | NA | NC. |
| C27 | NA | NA | NA | NA | NA | NC. |
| C28 | NA | NA | NA | NA | NA | NC. |
| C29 | NA | NA | NA | NA | NA | NC. |
| C30 | NA | NA | NA | NA | NA | NC. |
| D18 | XP_M22_LVDS702_L15P | IO_L15P_XCC_N5P0_M0P138_702 | 702 | M22 | IO, 1.5V | XP Bank702 IO15 differential positive or single ended I/O. |
| D19 | XP_M23_LVDS702_L15N | IO_L15N_XCC_N5P1_M0P139_702 | 702 | M23 | IO, 1.5V | XP Bank702 IO15 differential negative or single ended I/O |
| D20 | XP_L23_LVDS702_L16P | IO_L16P_N5P2_M0P140_702 | 702 | L23 | IO, 1.5V | XP Bank702 IO16 differential positive or single ended I/O. |
| D21 | XP_K24_LVDS702_L16N | IO_L16N_N5P3_M0P141_702 | 702 | K24 | IO, 1.5V | XP Bank702 IO16 differential negative or single ended I/O |

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| D22 | XP_K23_LVDS702_L17P | IO_L17P_N5P4_M0P142_702 | 702 | K23 | IO, 1.5V | XP Bank702 IO17 differential positive or single ended I/O |
| D23 | XP_J24_LVDS702_L17N | IO_L17N_N5P5_M0P143_702 | 702 | J24 | IO, 1.5V | XP Bank702 IO17 differential negative or single ended I/O. |
| D25 | NA | NA | NA | NA | NA | NC. |
| D26 | NA | NA | NA | NA | NA | NC. |
| D27 | NA | NA | NA | NA | NA | NC. |
| D28 | NA | NA | NA | NA | NA | NC. |
| D29 | NA | NA | NA | NA | NA | NC. |
| D30 | NA | NA | NA | NA | NA | NC. |

**IO Type of IOs originating from Versal AI Edge SoC is configurable. Hence for exact IO type configuration options, refer Xilinx Versal AI Edge datasheet.*

### 2.5.4 PL IOs – HD BANK 302

The Versal AI Edge/Prime SOM supports 20 Single Ended (SE) IOs on Board-to-Board Connector1 from Versal's PL High-Density (HD) Bank 302. Upon these 20 SE IOs, up to 2 HDGC Global Clock Inputs.

The IO voltage of PL Bank 302 is connected from LDO4 output of the PMIC 1 Regulator, and it supports variable IO voltage setting. IO voltage is configurable to 1.8V during bootup. While using Single Ended IOs, make sure to set the PMIC LDO4 output to appropriate IO voltage for PL Bank 302. By default, IO voltage of PL Bank 302 is set as 1.8V after U-boot bootup. For more details about supported IO standard, refer the Versal AI Edge datasheet.

In the Versal AI Edge/Prime SOM, PL HD Bank 302 signals are routed as Single Ended(SE) IOs to Board-to-Board Connector1. The Board-to-Board Connector1 pins A38, A39, A36, and A37 are HDGC Global Clock Input capable pins of PL Bank 302.

**Table 10: PL HD Bank 302 Pinouts**

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| A36 | HD_D10_SE302_HDGC_L6P | IO_L6P_HDGC_302 | 302 | D10 | IO, 1.8V | HD Bank302 IO6 single ended I/O. Same pin can be configured as HDGC Global Clock Input. |
| A37 | HD_C10_SE302_HDGC_L6N | IO_L6N_HDGC_302 | 302 | C10 | IO, 1.8V | HD Bank302 IO6 single ended I/O. Same pin can be configured as HDGC Global Clock Input. |
| A38 | HD_D11_SE302_HDGC_L5P | IO_L5P_HDGC_302 | 302 | D11 | IO, 1.8V | HD Bank302 IO5 single ended I/O. Same pin can be configured as HDGC Global Clock Input. |
| A39 | HD_C12_SE302_HDGC_L5N | IO_L5N_HDGC_302 | 302 | C12 | IO, 1.8V | HD Bank302 IO5 single ended I/O. Same pin can be configured as HDGC Global Clock Input. |
| B34 | HD_B11_SE302_L8P | IO_L8P_302 | 302 | B11 | IO, 1.8V | HD Bank302 IO8 single ended I/O. |
| B35 | HD_A11_SE302_L8N | IO_L8N_302 | 302 | A11 | IO, 1.8V | HD Bank302 IO8 single ended I/O. |
| B36 | HD_B12_SE302_L9P | IO_L9P_302 | 302 | B12 | IO, 1.8V | HD Bank302 IO9 single ended I/O. |
| B37 | HD_A13_SE302_L9N | IO_L9N_302 | 302 | A13 | IO, 1.8V | HD Bank302 IO9 single ended I/O. |
| C34 | HD_E12_SE302_L3P | IO_L3P_302 | 302 | E12 | IO, 1.8V | HD Bank302 IO3 single ended I/O. |
| C35 | HD_D12_SE302_L3N | IO_L3N_302 | 302 | D12 | IO, 1.8V | HD Bank302 IO3 single ended I/O. |
| C36 | HD_F11_SE302_L4P | IO_L4P_302 | 302 | F11 | IO, 1.8V | HD Bank302 IO4 single ended I/O.. |
| C37 | HD_E11_SE302_L4N | IO_L4N_302 | 302 | E11 | IO, 1.8V | HD Bank302 IO4 single ended I/O.. |
| C38 | HD_B10_SE302_L7P | IO_L7P_302 | 302 | B10 | IO, 1.8V | HD Bank302 IO7 single ended I/O. |
| C39 | HD_A10_SE302_L7N | IO_L7N_302 | 302 | A10 | IO, 1.8V | HD Bank302 IO7 single ended I/O. |
| D34 | HD_F14_SE302_L0P | IO_L0P_302 | 302 | F14 | IO, 1.8V | HD Bank302 IO0 single ended I/O. |
| D35 | HD_E14_SE302_L0N | IO_L0N_302 | 302 | E14 | IO, 1.8V | HD Bank302 IO0 single ended I/O. |
| D36 | HD_C14_SE302_L1P | IO_L1P_302 | 302 | C14 | IO, 1.8V | HD Bank302 IO1 single ended I/O. |
| D37 | HD_C13_SE302_L1N | IO_L1N_302 | 302 | C13 | IO, 1.8V | HD Bank302 IO1 single ended I/O. |
| D38 | HD_E13_SE302_L2P | IO_L2P_302 | 302 | E13 | IO, 1.8V | HD Bank302 IO2 single ended I/O. |

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination* | Description |
|---|---|---|---|---|---|---|
| D39 | HD_D14_SE302_L2N | IO_L2N_302 | 302 | D14 | IO, 1.8V | HD Bank302 IO2 single ended I/O. |

**IO Type of IOs originating from Versal AI Edge SoC is configurable. Hence for exact IO type configuration options, refer Xilinx Versal AI Edge datasheet.*

### 2.5.5 Power Control Output

The Versal AI Edge/Prime SOM, Board to Board Connector1 is assigned with XP IO and HD IO voltage for XP IO and HD Bank IOs connected to the connector. Also, in Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance. For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

**Table 11: Board to Board Connector Power Pins**

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| B1 | VCCO_HDIO | NA | NA | NA | 1.8V | HD Bank 302 IO Voltage |
| C1 | VCCO_XPIO_702 | NA | NA | NA | 1.5V | XPIO Bank 702 IO Voltage |
| D1 | VCCO_XPIO_703 | NA | NA | NA | 1.5V | XPIO Bank 703 IO Voltage |
| A8, A17, A24, A33, A40, A48, A51, A52, A55, A56, A59, A60, B8, B17, B24, B33, B40, B49, B50, B53, B54, B57, B58, C8, C17, C24, C33, C40, C51, C52, C55, C56, C59, C60, D8, D17, D24, D33, D40, D49, D50, D53, D54, D57, D58 | GND | NA | NA | NA | Power | Ground. |

### 2.6 Board to Board Connector2

The Versal AI Edge/Prime SOM Board to Board connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector2 are explained in the following sections. The Board-to-Board Connector2 (J3) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - ADM6-60-01.5-L-4-2-A-TR from Samtech

Mating Connector - ADF6-60-03.5-L-4-2-A-TR from Samtech

Staking Height - 5mm

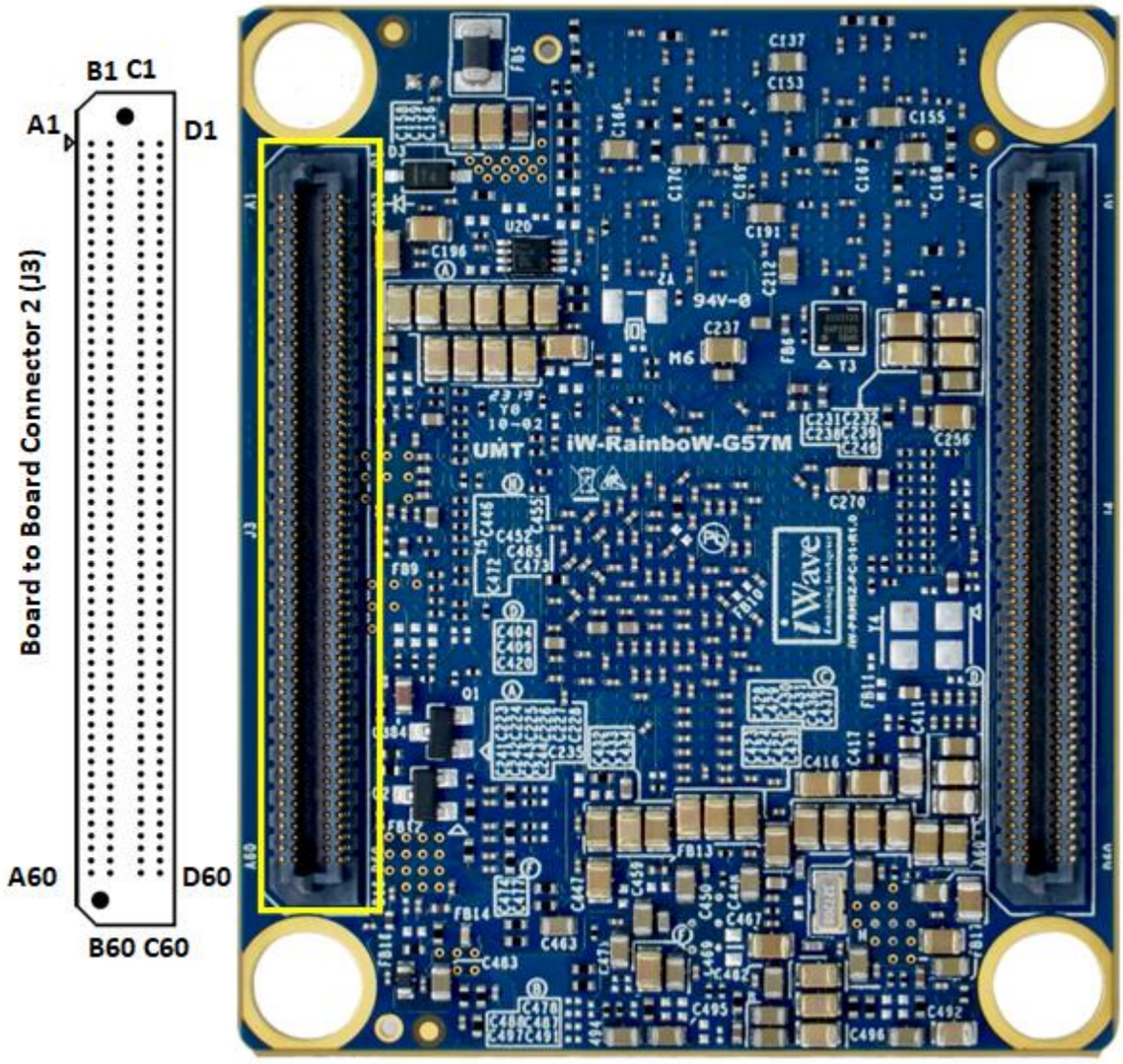


**Figure 5: Board to Board Connector 2**

**Table 12: Board to Board Connector2 Pinout**

| B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| **A1** | VCC_5V | **B1** | VCC_5V | **C1** | VCC_5V | **D1** | VCC_5V |
| **A2** | VCC_5V | **B2** | VCC_5V | **C2** | VCC_5V | **D2** | VCC_5V |
| **A3** | VCC_5V | **B3** | VCC_5V | **C3** | VCC_5V | **D3** | VCC_5V |
| **A4** | VCC_5V | **B4** | VCC_5V | **C4** | VCC_5V | **D4** | VCC_5V |
| **A5** | VCC_5V | **B5** | VCC_5V | **C5** | VCC_5V | **D5** | VCC_5V |
| **A6** | GND | **B6** | GND | **C6** | GND | **D6** | GND |
| **A7** | GND | **B7** | GND | **C7** | GND | **D7** | GND |
| **A8** | NC | **B8** | SOM_PWR_EN | **C8** | I2C_SCL(PMC_MIO50_501) | **D8** | NC |
| **A9** | JTAG_TCK | **B9** | NC | **C9** | I2C_SDA(PMC_MIO51_501) | **D9** | VRTC_3V0 |
| **A10** | JTAG_TMS | **B10** | PMIC2_GEM0_B2B_RST | **C10** | NC | **D10** | SYSMON_D_VP |
| **A11** | JTAG_TDO | **B11** | RESET_SW_IN | **C11** | NC | **D11** | SYSMON_D_VN |
| **A12** | JTAG_TDI | **B12** | CONFIG_DONE | **C12** | GEM1_MDC (LPD_MIO24_502) | **D12** | PS_MODE0 |
| **A13** | UART_TXD (PMC_MIO35_501) | **B13** | MSIO_PWRBTN# | **C13** | GEM1_MDIO(LPD_MIO25_502) | **D13** | PS_MODE1 |
| **A14** | UART_RXD (PMC_MIO34_501) | **B14** | MSIO_1PPS_IN | **C14** | ETH2_INT(PMC_MIO12_500) | **D14** | PS_MODE2 |
| **A15** | GND | **B15** | GND | **C15** | GND | **D15** | GND |
| **A16** | USB_OTG_DM | **B16** | USB_PWR_EN | **C16** | GEM1_TX_CLK (LPD_MIO12_502) | **D16** | SPI1_CLK(PMC_MIO6_500) |
| **A17** | USB_OTG_DP | **B17** | USB_OTG_ID | **C17** | GEM1_TXD0(LPD_MIO13_502) | **D17** | SPI1_SI(PMC_MIO11_500) |
| **A18** | GND | **B18** | VBUS_USB | **C18** | GEM1_TXD1(LPD_MIO14_502) | **D18** | SPI1_S0(PMC_MIO10_500) |
| **A19** | GPHY_ATXRXM | **B19** | GPHY_ACTIVITY_LED1 | **C19** | GEM1_TXD2(LPD_MIO15_502) | **D19** | SPI1_CS2(PMC_MIO7_500) |
| **A20** | GPHY_ATXRXP | **B20** | GPHY_LINK_LED2 | **C20** | GEM1_TXD3(LPD_MIO16_502) | **D20** | SPI1_CS1(PMC_MIO8_500) |
| **A21** | GND | **B21** | GPIO(PMC_MIO27_501) | **C21** | GEM1_TX_CTL(LPD_MIO17_502) | **D21** | SPI1_CS0(PMC_MIO9_500) |
| **A22** | GPHY_BTXRXM | **B22** | GND | **C22** | GND | **D22** | GND |
| **A23** | GPHY_BTXRXP | **B23** | SD1_CLK (PMC_MIO26_501) | **C23** | GEM1_RX_CLK(LPD_MIO18_502) | **D23** | NC |

| B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| **A24** | GND | **B24** | SD1_CMD (PMC_MIO29_501) | **C24** | GEM1_RXD0 (LPD_MIO19_502) | **D24** | NC |
| **A25** | GPHY_CTXRXM | **B25** | SD1_DATA0 (PMC_MIO30_501) | **C25** | GEM1_RXD1 (LPD_MIO20_502) | **D25** | NC |
| **A26** | GPHY_CTXRXP | **B26** | SD1_DATA1 (PMC_MIO31_501) | **C26** | GEM1_RXD2 (LPD_MIO21_502) | **D26** | NC |
| **A27** | GND | **B27** | SD1_DATA2 (PMC_MIO32_501) | **C27** | GEM1_RXD3 (LPD_MIO22_502) | **D27** | CANFD1_RX (PMC_MIO37_501) |
| **A28** | GPHY_DTXRXM | **B28** | SD1_DATA3 (PMC_MIO33_501) | **C28** | GEM1_RX_CTL (LPD_MIO23_502) | **D28** | CANFD1_TX (PMC_MIO36_501) |
| **A29** | GPHY_DTXRXP | **B29** | SD1_CD (PMC_MIO28_501) | **C29** | NC | **D29** | NC |
| **A30** | GND | **B30** | HS_PCIe_RSTN | **C30** | GND | **D30** | NC |
| **A31** | GTYP_REFCLK0P_103 | **B31** | GND | **C31** | B2B_GTYP_REFCLK1P_103 | **D31** | GND |
| **A32** | GTYP_REFCLK0N_103 | **B32** | GND | **C32** | B2B_GTYP_REFCLK1N_103 | **D32** | GND |
| **A33** | GND | **B33** | GTYP_RXP1_103 | **C33** | GND | **D33** | GTYP_RXP3_103 |
| **A34** | GND | **B34** | GTYP_RXN1_103 | **C34** | GND | **D34** | GTYP_RXP3_103 |
| **A35** | GTYP_RXP0_103 | **B35** | GND | **C35** | GTYP_RXP2_103 | **D35** | GND |
| **A36** | GTYP_RXN0_103 | **B36** | GND | **C36** | GTYP_RXN2_103 | **D36** | GND |
| **A37** | GND | **B37** | GTYP_TXP1_103 | **C37** | GND | **D37** | GTYP_TXP3_103 |
| **A38** | GND | **B38** | GTYP_TXN1_103 | **C38** | GND | **D38** | GTYP_TXN3_103 |
| **A39** | GTYP_TXP0_103 | **B39** | GND | **C39** | GTYP_TXP2_103 | **D39** | GND |
| **A40** | GTYP_TXN0_103 | **B40** | GND | **C40** | GTYP_TXN2_103 | **D40** | GND |
| **A41** | GND | **B41** | GTYP_REFCLK0P_104 | **C41** | GND | **D41** | B2B_GTYP_REFCLK1P_104 |
| **A42** | GND | **B42** | GTYP_REFCLK0N_104 | **C42** | GND | **D42** | B2B_GTYP_REFCLK1N_104 |
| **A43** | GTYP_RXP0_104 | **B43** | GND | **C43** | GTYP_RXP2_104 | **D43** | GND |
| **A44** | GTYP_RXN0_104 | **B44** | GND | **C44** | GTYP_RXN2_104 | **D44** | GND |
| **A45** | GND | **B45** | GTYP_RXP1_104 | **C45** | GND | **D45** | GTYP_RXP3_104 |
| **A46** | GND | **B46** | GTYP_RXN1_104 | **C46** | GND | **D46** | GTYP_RXN3_104 |
| **A47** | GTYP_TXP0_104 | **B47** | GND | **C47** | GTYP_TXP2_104 | **D47** | GND |
| **A48** | GTYP_TXN0_104 | **B48** | GND | **C48** | GTYP_TXN2_104 | **D48** | GND |
| **A49** | GND | **B49** | GTYP_TXP1_104 | **C49** | GND | **D49** | GTYP_TXP3_104 |
| **A50** | GND | **B50** | GTYP_TXN1_104 | **C50** | GND | **D50** | GTYP_TXN3_104 |
| **A51** | NC | **B51** | GND | **C51** | NC | **D51** | GND |
| **A52** | NC | **B52** | GND | **C52** | NC | **D52** | GND |

| B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name | B2B-2 Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| **A53** | GND | **B53** | NC | **C53** | GND | **D53** | NC |
| **A54** | GND | **B54** | NC | **C54** | GND | **D54** | NC |
| **A55** | NC | **B55** | GND | **C55** | NC | **D55** | GND |
| **A56** | NC | **B56** | GND | **C56** | NC | **D56** | GND |
| **A57** | GND | **B57** | NC | **C57** | GND | **D57** | NC |
| **A58** | GND | **B58** | NC | **C58** | GND | **D58** | NC |
| **A59** | NC | **B59** | GND | **C59** | NC | **D59** | GND |
| **A60** | NC | **B60** | GND | **C60** | NC | **D60** | GND |

**Power rails are highlighted in RED and Clock signals are highlighted in purple.*

### 2.6.1 PS Interfaces

The interfaces which are supported in Board-to-Board Conenector2 from Versal AI Edge PS is explained in the following section.

### 2.6.2 USB2.0 OTG Interface

The Versal AI Edge/Prime SOM supports one USB2.0 OTG interface on Board-to-Board Connector2. USB0 OTG controller of Versal AI Edge PS is used for USB2.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the PMC MIO pins. The Versal AI Edge SOM supports “USB3320” ULPI transceiver from Microchip and works at 1.8V IO voltage level. In Versal AI Edge SOM, GPIO “PMC_MIO13_500” is used for USB ULPI PHY reset. It supports active high power enable signal on Board-to-Board Connector2 from USB PHY for external VBUS power control.

Also, Versal AI Edge/Prime SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

**Table 13: USB 2.0 Board to Board Connector2 Pinouts**

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| A17 | USB_OTG_DP | NA | NA | NA | IO, USB | USB OTG data Positive. |
| A16 | USB_OTG_DM | NA | NA | NA | IO, USB | USB OTG data negative. |
| B17 | USB_OTG_ID | NA | NA | NA | I,3.3V CMOS | USB OTG ID input for USB host or device detection. |
| B16 | USB_PWR_EN | NA | NA | NA | O, 3.3V CMOS | USB active high power enable output to control external USB Vbus. |
| B18 | VBUS_USB | NA | NA | NA | I, 5V Power | USB VBUS for VBUS monitoring. |

### 2.6.3 Gigabit Ethernet Interface

The Versal AI Edge/Prime SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector2.The MAC is integrated in the Versal AI Edge LPD and connected to the external Gigabit Ethernet PHY "DP83867ISRGZ" on SOM. This Gigabit Ethernet PHY is interfaced with GEM0 interface of Versal through LPD MIO pins and works at 1.8V IO voltage level. Also this MAC supports Time Sensitive Network(TSN).

In Versal AI Edge SOM/Prime, PMIC 2 GPIO "GPIO2/PWR_EN" is used for Ethernet PHY reset and also shared with Board to Board connector 2. Also, SOM supports Ethernet PHY interrupt through PS GPIO "PMC_MIO39_501". This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magnetics is required on the carrier board.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector2, refer the below table.

**Table 14: GEM0 Board to Board Connector2 Pinouts**

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| A20 | GPHY_ATXRXP | NA | NA | NA | IO, GBE | Gigabit Ethernet differential pair 1 positive. |
| A19 | GPHY_ATXRXM | NA | NA | NA | IO, GBE | Gigabit Ethernet differential pair 1 negative. |
| A23 | GPHY_BTXRXP | NA | NA | NA | IO, GBE | Gigabit Ethernet differential pair 2 positive. |
| A22 | GPHY_BTXRXM | NA | NA | NA | IO, GBE | Gigabit Ethernet differential pair 2 negative. |
| A26 | GPHY_CTXRXP | NA | NA | NA | IO, GBE | Gigabit Ethernet differential pair 3 positive. |
| A25 | GPHY_CTXRXM | NA | NA | NA | IO, GBE | Gigabit Ethernet differential pair 3 negative. |
| A29 | GPHY_DTXRXP | NA | NA | NA | IO, GBE | Gigabit Ethernet differential pair 4 positive. |
| A28 | GPHY_DTXRXM | NA | NA | NA | IO, GBE | Gigabit Ethernet differential pair 4 negative. |
| B19 | GPHY_ACTIVITY_LED1 | NA | NA | NA | O, GBE | Gigabit Ethernet Activity LED (Active High). |
| B20 | GPHY_LINK_LED2 | NA | NA | NA | O, GBE | Gigabit Ethernet 1000Mbps Link status LED (Active High). |

### 2.6.4 RGMII/ULPI Interface

The Versal AI Edge/Prime SOM supports RGMII interface on Board-to-Board Connector2. This RGMII is interface with GEM1 interface of Versal's LPD through MIO pins and works at 1.8V IO voltage level. Those LPD MIO pins are directly connected from Versal SoC to Board-to-Board conenctor2.

The Versal AI Edge, Gigabit Ethernet controller (GEM1) implements a 10/100/1000 Mb/s Ethernet MAC that is compatible with the IEEE Standard for Ethernet (IEEE Std 802.3-2008). GEM controller supports MDIO interface for external PHY Management and it can be used through LPD Bank IOs through MIO interface in SOM.

For more details on RGMII/ULPI Interface pinouts on Board-to-Board Connector2, refer the below table.

**Table 15: GEM1 Board to Board Connector2 Pinouts**

| B2B-1 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| C16 | GEM1_TX_CLK(LPD_MIO12_502) | LPD_MIO12_502 | 502 | W4 | O, 1.8V LVCMOS | GEM1 RGMII Transmit Clock. |
| C17 | GEM1_TXD0(LPD_MIO13_502) | LPD_MIO13_502 | 502 | V4 | O, 1.8V LVCMOS | GEM1 RGMII Transmit DATA0. |
| C18 | GEM1_TXD1(LPD_MIO14_502) | LPD_MIO14_502 | 502 | T4 | O, 1.8V LVCMOS | GEM1 RGMII Transmit DATA1. |
| C19 | GEM1_TXD2(LPD_MIO15_502) | LPD_MIO15_502 | 502 | T5 | O, 1.8V LVCMOS | GEM1 RGMII Transmit DATA2. |
| C20 | GEM1_TXD3(LPD_MIO16_502) | LPD_MIO16_502 | 502 | U5 | O, 1.8V LVCMOS | GEM1 RGMII Transmit DATA3. |
| C21 | GEM1_TX_CTL(LPD_MIO17_502) | LPD_MIO17_502 | 502 | V5 | O, 1.8V LVCMOS | GEM1 RGMII Transmit Control. |
| C23 | GEM1_RX_CLK(LPD_MIO18_502) | LPD_MIO18_502 | 502 | W5 | I, 1.8V LVCMOS | GEM1 RGMII Receive Clock. |
| C24 | GEM1_RXD0(LPD_MIO19_502) | LPD_MIO19_502 | 502 | Y6 | I, 1.8V LVCMOS | GEM1 RGMII Receive DATA0 |
| C25 | GEM1_RXD1(LPD_MIO20_502) | LPD_MIO20_502 | 502 | W6 | I, 1.8V LVCMOS | GEM1 RGMII Receive DATA1. |
| C26 | GEM1_RXD2(LPD_MIO21_502) | LPD_MIO21_502 | 502 | U6 | I, 1.8V LVCMOS | GEM1 RGMII Receive DATA2. |
| C27 | GEM1_RXD3(LPD_MIO22_502) | LPD_MIO22_502 | 502 | T6 | I, 1.8V LVCMOS | GEM1 RGMII Receive DATA2. |
| C28 | GEM1_RX_CTL(LPD_MIO23_502) | LPD_MIO23_502 | 502 | Y7 | I, 1.8V LVCMOS | GEM1 RGMII Receive control. |
| C12 | GEM1_MDC(LPD_MIO24_502) | LPD_MIO24_502 | 502 | Y8 | O, 1.8V LVCMOS | MDC Clock Output |
| C13 | GEM1_MDIO(LPD_MIO25_502) | LPD_MIO25_502 | 502 | Y9 | IO, 1.8V LVCMOS | MDIO Data In/Out |

### 2.6.5 SD/SDIO Interface

The Versal AI Edge/Prime SOM supports SD/SDIO interface on Board-to-Board Connector2. The SD1 controller of Versal's PMC is used for SD/SDIO interface through MIO pins. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 3.0. It supports different speed mode like Standard mode (25MHz), High Speed mode (50MHz), SDR12 (25MHz), SDR25 (50MHz), SDR50 (100MHz), SDR104 (200MHz) & DDR50 mode (50MHz). Also in SD mode, data transfers in 1-bit and 4-bit modes. The Versal AI Edge SOM supports Card Detect & Power Enable/Voltage Select pins through MIO pins.

For more details on SD/SDIO Interface pinouts on Board-to-Board Connector2, refer the below table.

**Table 16: SD/SDIO Interface Board to Board Connector2 Pinouts**

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| B23 | SD1_CLK(PMC_MIO26_501) | PMC_MIO26_501 | 501 | AA5 | O, 1.8V LVCMOS/ 10K PU | SD1 Clock. |
| B21 | GPIO(PMC_MIO27_501) | PMC_MIO27_501 | 501 | AB5 | O, 1.8V LVCMOS | SD1 Power Enable/Voltage select through PS GPIO. |
| B29 | SD1_CD(PMC_MIO28_501) | PMC_MIO28_501 | 501 | AC5 | I, 1.8V LVCMOS/ 4.7K PU | SD1 Card Detect. |
| B24 | SD1_CMD(PMC_MIO29_501) | PMC_MIO29_501 | 501 | AD5 | IO, 1.8V LVCMOS/ 10K PU | SD1 Command. |
| B25 | SD1_DATA0(PMC_MIO30_501) | PMC_MIO30_501 | 501 | AE6 | IO, 1.8V LVCMOS/ 10K PU | SD1 DATA0. |
| B26 | SD1_DATA1(PMC_MIO31_501) | PMC_MIO31_501 | 501 | AD6 | IO, 1.8V LVCMOS/ 10K PU | SD1 DATA1. |
| B27 | SD1_DATA2(PMC_MIO32_501) | PMC_MIO32_501 | 501 | AB6 | IO, 1.8V LVCMOS/ 10K PU | SD1 DATA2. |
| B28 | SD1_DATA3(PMC_MIO33_501) | PMC_MIO33_501 | 501 | AA6 | IO, 1.8V LVCMOS/ 10K PU | SD1 DATA3. |

### 2.6.6 Debug UART Interface

The Versal AI Edge/Prime SOM supports one Debug UART interface on Board-to-Board Connector2. The UART0 controller of Versal's PMC is used for Debug UART interface through MIO pins. This controller supports full-duplex asynchronous receiver and transmitter that support a wide range of programmable baud rates.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

**Table 17:Debug UART Board to Board Connector2 Pinouts**

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| A14 | UART_RXD(PMC_MIO34_501) | PMC_MIO34_501 | 501 | AB7 | I, 1.8V LVCMOS | UART0 Receive data line for Debug. |
| A13 | UART_TXD(PMC_MIO35_501) | PMC_MIO35_501 | 501 | AC7 | O, 1.8V LVCMOS | UART0 Transmit data line for Debug. |

### 2.6.7 I2C Interface

The Versal AI Edge/Prime SOM supports one I2C interface on Board-to-Board Connector2. The I2C0 module of Versal's PS is used for I2C interface through PMC MIO pins. The controller supports multi-master mode for 7-bit and extended 10-bit addressing and also supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C interface is also connected to On-SOM PMIC 1 with I2C address 0x58/0x59 and PMIC 2 with I2C address of 0x48/0x49 and also connected with Clock Synthesizer with I2C address of 0x6A in the Versal AI Edge SOM.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

**Table 18: I2C Interface Board to Board Connector2 Pinouts**

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| C8 | I2C_SCL(PMC_MIO50_501) | PMC_MIO50_501 | 501 | AB10 | O, 1.8V OD/ 4.7K PU | I2C Serial Clock. |
| C9 | I2C_SDA(PMC_MIO51_501) | PMC_MIO51_501 | 501 | AA10 | IO, 1.8V OD/ 4.7K PU | I2C Serial Data. |

### 2.6.8 SPI Interface

The Versal AI Edge/Prime SOM supports one SPI interface with on Board-to-Board Connector2. The SPI1 controller of Versal's PS is used for SPI interface through PMC MIO pins. It can function in master mode with multi-master feature, slave mode, or loop-back test mode. The SOM SPI support a 3 Slave select/ Chip select pins.

For more details on SPI Interface pinouts on Board-to-Board Connector2, refer the below table.

**Table 19: SPI Interface Board to Board Connector2 Pinouts**

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| D16 | SPI1_CLK(PMC_MIO6_500) | PMC_MIO6_500 | 500 | AH2 | O, 1.8V LVCMOS | SPI clock. |
| D17 | SPI1_SI(PMC_MIO11_500) | PMC_MIO11_500 | 500 | AB2 | O, 1.8V LVCMOS | SPI Master output Slave input. |
| D18 | SPI1_S0(PMC_MIO10_500) | PMC_MIO10_500 | 500 | AC2 | I, 1.8V LVCMOS | SPI Master input Slave output. |
| D19 | SPI1_CS2(PMC_MIO7_500) | PMC_MIO7_500 | 500 | AG2 | O, 1.8V LVCMOS | SPI chip select2. |
| D20 | SPI1_CS1(PMC_MIO8_500) | PMC_MIO8_500 | 500 | AE2 | O, 1.8V LVCMOS | SPI chip select1. |
| D21 | SPI1_CS0(PMC_MIO9_500) | PMC_MIO9_500 | 500 | AD2 | O, 1.8V LVCMOS | SPI chip select0. |

### 2.6.9 CAN FD Interface

TheVersal AI Edge/Prime SOM supports one CAN FD (CAN Flexible Data-Rate) interfaces on Board-to-Board Connector2. The CAN FD1 controller of Versal's PS is used for CAN FD interface through PMC MIO pins. This CAN FD controller is compatible with CAN 2.0 frames specified in ISO specification 11898-1:2015 standards. And it supports flexible data rates up to 8Mb/s and normal data rates up to 1Mb/s.

For more details on CAN FD Interface pinouts on Board-to-Board Connector2, refer the below table.

**Table 20: CAN FD Interface Board to Board Connector2 Pinouts**

| B2B-1 Pin No | B2B Connector1 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| D28 | CANFD1_TX(PMC_MIO36_501) | PMC_MIO36_501 | 501 | AD7 | O, 1.8V LVCMOS | CAN FD Transmit data. |
| D27 | CANFD1_RX(PMC_MIO37_501) | PMC_MIO37_501 | 501 | AE7 | I, 1.8V LVCMOS | CAN FD Receive data. |

### 2.6.10JTAG Interface

The Versal AI Edge/Prime SOM supports JTAG interface on Board-to-Board Connector2. The JTAG interface is a multipurpose interface used for both boot and debug function. The Versal have their own TAP controller which are chained together inside the SoC. Versal support a 32-bit device identification register and a JTAG configuration register that adds additional readback and configuration JTAG capability

For more details on JTAG Interface pinouts on Board-to-Board Connector2, refer the below table.

**Table 21: JTAG Interface Board to Board Connector2 Pinouts**

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| A9 | JTAG_TCK | TCK_503 | 503 | AH10 | I, 1.8V LVCMOS/ 4.7K | JTAG Test Clock. |
| A12 | JTAG_TDI | TDI_503 | 503 | AG10 | I, 1.8V LVCMOS/ 4.7K | JTAG Test Data Input. |
| A11 | JTAG_TDO | TDO_503 | 503 | AF8 | O, 1.8V LVCMOS | JTAG Test Data Output. |
| A10 | JTAG_TMS | TMS_503 | 503 | AH9 | I, 1.8V LVCMOS/ 4.7K | JTAG Test Mode Select. |

### 2.6.11PL Interfaces

The interfaces which are supported in Board to Board Connector2 from Versal AI Edge, PL is explained in the following section.

### 2.6.12 GTYP High Speed Transceivers

The Versal AI Edge/Prime SOM supports 8 GTYP transceivers through Two transceiver Quad (Bank 103 & 104) with line rate from 1.2Gbps to 32 Gbps based on the speed grade of the SoC. These transceivers can be used to interface, multiple high-speed interface protocols. Each GTYP transceiver quad supports two dedicated reference clock input pairs.

**Table 22: GTYP Transceiver Speed Grade**

| Versal AI Edge Speed Grade | GTYP Transceiver line rate (min) | GTYP Transceiver line rate (max) |
|---|---|---|
| -1L Speed Grade | 1.2 Gbps | 25.78 Gbps |
| -2L Speed Grade | 1.2 Gbps | 32 Gbps |
| -1M Speed Grade | 1.2 Gbps | 26.56 Gbps |
| -2M Speed Grade | 1.2 Gbps | 32 Gbps |
| -2H Speed Grade | 1.2 Gbps | 32 Gbps |

*Note: For Backplane application, the transceiver maximum line rate may come down.*

The Versal AI Edge/Prime SOM Supports 8 GTYP transceivers along with the reference clock inputs (Bank 103& 104) from Board-to-Board Conenctor2 and each GTYP transceiver support a two dedicated reference clock input pair.

In Versal AI Edge SOM, On board reference clock 1 to the GTYP transceiver quad is provided. This is fed from the on-SOM clock synthesizer and also optional clock is fed from carrier board. The reference clock 0 to the GTYP transceiver quad is not supported from SOM. This must be fed from the carrier board based on the peripheral standards used on GTYP transceivers. This gives full flexibility to end user to select the required peripheral standards on GTYP transceivers.

For more details on GTYP transceiver pinouts on Board-to-Board Connector2, refer the below table.

**Table 23: GTYP Transceiver Board to Board Connector 2 Pinouts**

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| **Bank103 Transceiver Quad Pins** | | | | | | |
| A39 | GTYP_TXP0_103 | GTYP_TXP0_103 | 103 | N5 | O, DIFF | GTYP Bank103 channel0 High speed differential transmitter positive. |
| A40 | GTYP_TXN0_103 | GTYP_TXN0_103 | 103 | N4 | O, DIFF | GTYP Bank103 channel0 High speed differential transmitter negative. |
| A35 | GTYP_RXP0_103 | GTYP_RXP0_103 | 103 | P2 | I, DIFF | GTYP Bank103 channel0 High speed differential receiver positive. |
| A36 | GTYP_RXN0_103 | GTYP_RXN0_103 | 103 | P1 | I, DIFF | GTYP Bank103 channel0 High speed differential receiver negative. |
| B37 | GTYP_TXP1_103 | GTYP_TXP1_103 | 103 | L5 | O, DIFF | GTYP Bank103 channel1 High speed differential transmitter positive. |

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| B38 | GTYP_TXN1_103 | GTYP_TXN1_103 | 103 | L4 | O, DIFF | GTYP Bank103 channel1 High speed differential transmitter negative. |
| B33 | GTYP_RXP1_103 | GTYP_RXP1_103 | 103 | M2 | I, DIFF | GTYP Bank103 channel1 High speed differential receiver positive. |
| B34 | GTYP_RXN1_103 | GTYP_RXN1_103 | 103 | M1 | I, DIFF | GTYP Bank103 channel1 High speed differential receiver negative. |
| C39 | GTYP_TXP2_103 | GTYP_TXP2_103 | 103 | J5 | O, DIFF | GTYP Bank103 channel2 High speed differential transmitter positive. |
| C40 | GTYP_TXN2_103 | GTYP_TXN2_103 | 103 | J4 | O, DIFF | GTYP Bank103 channel2 High speed differential transmitter negative. |
| C35 | GTYP_RXP2_103 | GTYP_RXP2_103 | 103 | K2 | I, DIFF | GTYP Bank103 channel2 High speed differential receiver positive. |
| C36 | GTYP_RXN2_103 | GTYP_RXN2_103 | 103 | K1 | I, DIFF | GTYP Bank103 channel2 High speed differential receiver negative. |
| D37 | GTYP_TXP3_103 | GTYP_TXP3_103 | 103 | G5 | O, DIFF | GTYP Bank103 channel3 High speed differential transmitter positive. |
| D38 | GTYP_TXN3_103 | GTYP_TXN3_103 | 103 | G4 | O, DIFF | GTYP Bank103 channel3 High speed differential transmitter negative. |
| D33 | GTYP_RXP3_103 | GTYP_RXP3_103 | 103 | H2 | I, DIFF | GTYP Bank103 channel3 High speed differential receiver positive. |
| D34 | GTYP_RXN3_103 | GTYP_RXN3_103 | 103 | H1 | I, DIFF | GTYP Bank103 channel3 High speed differential receiver negative. |
| A31 | GTYP_REFCLK0P_103 | GTYP_REFCLKP0_103 | 103 | M7 | I, DIFF | GTYP Bank103 channel0 High speed differential reference clock0 positive. |
| A32 | GTYP_REFCLK0N_103 | GTYP_REFCLKN0_103 | 103 | M6 | I, DIFF | GTYP Bank103 channel0 High speed differential reference clock0 negative. |
| **Bank104 Transceiver Quad Pins** | | | | | | |
| A47 | GTYP_TXP0_104 | GTYP_TXP0_104 | 104 | E5 | O, DIFF | GTYP Bank104 channel0 High speed differential transmitter positive. |
| A48 | GTYP_TXN0_104 | GTYP_TXN0_104 | 104 | E4 | O, DIFF | GTYP Bank104 channel0 High speed differential transmitter negative. |
| A43 | GTYP_RXP0_104 | GTYP_RXP0_104 | 104 | F2 | I, DIFF | GTYP Bank104 channel0 High speed differential receiver positive. |
| A44 | GTYP_RXN0_104 | GTYP_RXN0_104 | 104 | F1 | I, DIFF | GTYP Bank104 channel0 High speed differential receiver negative. |
| B49 | GTYP_TXP1_104 | GTYP_TXP1_104 | 104 | D8 | O, DIFF | GTYP Bank104 channel1 High speed differential transmitter positive. |
| B50 | GTYP_TXN1_104 | GTYP_TXN1_104 | 104 | D7 | O, DIFF | GTYP Bank104 channel1 High speed differential transmitter negative. |
| B45 | GTYP_RXP1_104 | GTYP_RXP1_104 | 104 | D2 | I, DIFF | GTYP Bank104 channel1 High speed differential receiver positive. |
| B46 | GTYP_RXN1_104 | GTYP_RXN1_104 | 104 | D1 | I, DIFF | GTYP Bank104 channel1 High speed differential receiver negative. |

| B2B-2 Pin No | B2B Connector2 Signal Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| C47 | GTYP_TXP2_104 | GTYP_TXP2_104 | 104 | C5 | O, DIFF | GTYP Bank104 channel2 High speed differential transmitter positive. |
| C48 | GTYP_TXN2_104 | GTYP_TXN2_104 | 104 | C4 | O, DIFF | GTYP Bank104 channel2 High speed differential transmitter negative. |
| C43 | GTYP_RXP2_104 | GTYP_RXP2_104 | 104 | B2 | I, DIFF | GTYP Bank104 channel2 High speed differential receiver positive. |
| C44 | GTYP_RXN2_104 | GTYP_RXN2_104 | 104 | B1 | I, DIFF | GTYP Bank104 channel2 High speed differential receiver negative. |
| D49 | GTYP_TXP3_104 | GTYP_TXP3_104 | 104 | B8 | O, DIFF | GTYP Bank104 channel3 High speed differential transmitter positive. |
| D50 | GTYP_TXN3_104 | GTYP_TXN3_104 | 104 | B7 | O, DIFF | GTYP Bank104 channel3 High speed differential transmitter negative. |
| D45 | GTYP_RXP3_104 | GTYP_RXP3_104 | 104 | A5 | I, DIFF | GTYP Bank104 channel3 High speed differential receiver positive. |
| D46 | GTYP_RXN3_104 | GTYP_RXN3_104 | 104 | A4 | I, DIFF | GTYP Bank104 channel3 High speed differential receiver negative. |
| B41 | GTYP_REFCLK0P_104 | GTYP_REFCLKP0_104 | 104 | H7 | I, DIFF | GTYP Bank104 channel0 High speed differential reference clock0 positive. |
| B42 | GTYP_REFCLK0N_104 | GTYP_REFCLKN0_104 | 104 | H6 | I, DIFF | GTYP Bank104 channel0 High speed differential reference clock0 negative. |

### 2.6.13 Power, Reset & Control Signals

The Versal AI Edge SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin (pin B8) in Board-to-Board Connector2. Also, in Board-to-Board Connector2, Ground pins are distributed throughout the connector for better performance.

The Versal AI Edge SOM supports VCC_RTC coin cell power input from Board-to-Board Connector2 and connected to PMIC's VBBAT pin for real time clock backup voltage.

The Versal AI Edge SOM support an optional reference clock 1 input for GTYP Bank 103 & 104 from board-to-board connector 2 with a pins of C31, C32, D31, D42.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

**Table 24: Board to Board connector2 Control & Power Pins**

| B2B-2 Pin No | B2B Connector2 Pin Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| B8 | SOM_PWR_EN | NA | NA | NA | I, 5V | Active High SOM power enable.<br>*Important Note:*<br>*High – SOM power ON*<br>*Low – SOM Power OFF* |
| B10 | PMIC2_GEM0_B2B_RST | NA | NA | NA | O, 1.8V LVCMOS | Reset Pin |
| B11 | RESET_SW_IN | NA | NA | NA | I, 5V 10K PU | Active low reset input. |
| B30 | HS_PCIe_RSTN | IO_L10N_302 | 302 | A14 | IO, 1.8V LVCMOS | PCIe Reset for RP and EP Mode. |
| B13 | MSIO_PWRBTN# | NA | NA | NA | I, 5V 10K PU | Power-button input from Carrier Board |
| B12 | CONFIG_DONE | DONE_503 | 503 | AF5 | O, 1.8V LVCMOS/ 4.7K PU | Configuration done pin. |
| B14 | MSIO_1PPS_IN | NA | NA | NA | I, 1.8V LVCMOS | 1Hz clock input from Carrier Board |
| D12 | PS_MODE0 | MODE0_503 | 503 | AG8 | I, 1.8V LVCMOS | Boot Mode0 Select pin |
| D13 | PS_MODE1 | MODE1_503 | 503 | AG7 | I, 1.8V LVCMOS | Boot Mode1 Select pin |
| D14 | PS_MODE2 | MODE2_503 | 503 | AG6 | I, 1.8V LVCMOS | Boot Mode2 Select pin |
| C14 | ETH2_INT(PMC_MIO12_500) | PMC_MIO12_500 | 500 | AA3 | I, 1.8V LVCMOS | Ethernet 2 interrupt pin |
| C31 | B2B_GTYP_REFCLK1P_103 | GTYP_REFCLKP1_103 | 103 | K7 | I, DIFF | Optional Reference clock1 for GTYP Bank 103 |
| C32 | B2B_GTYP_REFCLK1N_103 | GTYP_REFCLKN1_103 | 103 | K6 | I, DIFF | Optional Reference clock1 for GTYP Bank 103 |
| D41 | B2B_GTYP_REFCLK1P_104 | GTYP_REFCLKP1_104 | 104 | F7 | I, DIFF | Optional Reference clock1 for GTYP Bank 104 |
| D42 | B2B_GTYP_REFCLK1N_104 | GTYP_REFCLKN1_104 | 104 | F6 | I, DIFF | Optional Reference clock1 for GTYP Bank 104 |
| D9 | VRTC_3V0 | NA | NA | NA | I, 3V Power | 3V backup coin cell input for RTC. |

| B2B-2 Pin No | B2B Connector2 Pin Name | SoC Pin Name | SoC Bank | SoC Pin No | Signal Type/ Termination | Description |
|---|---|---|---|---|---|---|
| A1, A2, A3, A4, A5 B1, B2, B3, B4, B5 C1, C2, C3, C4, C5 D1, D2, D3, D4, D5 | VCC_5V | NA | NA | NA | I, 5V | Supply Voltage. |
| A6, A7, A15, A18, A21, A24, A27, A30, A33, A34, A37, A38, A41, A42, A45, A46, A49, A50, A53, A54, A57, A58, B6, B7, B15, B22, B31, B32, B35, B36, B39, B40, B43, B43, B47, B48, B51, B52, B55, B56, B59,B60, C6, C7, C15, C22, C30, C33, C34, C37, C38, C41, C42, C45, C46, C49, C50, C53, C54,C57, C58, D6, D7, D15, D22, D31, D32, D35, D36, D39, D40, D43, D44, D47, D48, D51, D52, D55, D56, D59, D60 | GND | NA | NA | NA | Power | Ground |

### 2.7 Versal AI Edge PS Pin Multiplexing on Board to Board Connectors

The Versal AI Edge PS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of Versal AI Edge PS IO pins can be configured as GPIO if required. The below table provides the details of PS pin connections on Versal AI Edge SoC with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring PS I/O configuration in Xilinx Vivado Design Suite. To know the complete available alternate functions, refer the PS I/O configuration in the latest Vivado Design Suite

**Table 25: PS IOMUX on Versal AI Edge SOM**

| Interface/ Function | B2B PIN No. | SoC pin Name | GPIO | Function 1 | Function 2 | Function 3 | Function 4 | Function 5 | Function 6 | Function 7 | Function 8 | Function 9 | Function 10 | Function 11 | Function 12 | Function 13 | Function 14 | Function 15 | Function 16 | Function 17 | Function 18 | Function 19 | Function 20 | Function 21 | Function 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| On SOM Features from PS MIO | | | | | | | | | | | | | | | | | | | | | | | | | |
| **eMMC** | NA | PMC_MIO 38_501 | PMC_G PIO38 | SD0/EMMC 0_CLK | SD0/EMM C0_CLK | SD0/EMM C0_CLK | SD0/EMM C0_CLK | SD0/EMM C0_CLK | SD0/EMM C0: CLK | - | - | - | - | - | - | SMAP_IO[ 18] | - | GEM1: RGMII_TX _CLK | PMC_I2C _SCL | CANFD0_ RX | UART 1_TXD | SPI0_SCLK | LPD_I2C0 _SCL | SWDT0_C LK | TTC 1_CLK |
| | NA | PMC_MIO 39_501 | PMC_G PIO39 | SD0_DETEC T | SD0: DETECT | SD0: DETECT | - | - | - | - | - | - | - | - | - | SMAP_IO[ 19] | - | GEM1: RGMII_TX D[0] | PMC_I2C _SDA | CANFD0_ TX | UART 1_RXD | SPI0_SS2_ B | LPD_I2C0 _SDA | SWDT0_R ST | TTC 1_WAVE |
| | NA | PMC_MIO 40_501 | PMC_G PIO40 | SD0/EMMC 0_CMD | SD0/EMM C0_CMD | SD0/EMM C0_CMD | SD0/EMM C0_CMD | SD0/EMM C0_CMD | SD0/EMM C0: CMD | - | - | - | - | - | - | SMAP_IO[ 20] | - | GEM1: RGMII_TX D[1] | - | CANFD1_ TX | UART 1_RTS_B | SPI0_SS1_ B | LPD_I2C1 _SCL | SWDT0_R ST_PEND | TTC 0_CLK |
| | NA | PMC_MIO 41_501 | PMC_G PIO41 | SD0/EMMC 0_DATA[0] | SD0/EMM C0_DATA[ 0] | SD0/EMM C0_DATA[ 0] | SD0/EMM C0_DATA[ 0] | SD0/EMM C0_DATA[ 0] | SD0/EMM C0: DATA[0] | - | - | - | - | - | - | SMAP_IO[ 21] | - | GEM1: RGMII_TX D[2] | - | CANFD1_ RX | UART 1_CTS_B | SPI0_SS0_ B | LPD_I2C1 _SDA | SWDT0_I NT | TTC 0_WAVE |
| | NA | PMC_MIO 42_501 | PMC_G PIO42 | SD0/EMMC _DATA[1] | SD0/EMM C_DATA[1 ] | SD0/EMM C_DATA[1 ] | - | SD0/EMM C_DATA[1 ] | SD0/EMM C: DATA[1] | - | - | - | - | - | - | SMAP_IO[ 22] | - | GEM1: RGMII_TX D[3] | PMC_I2C _SCL | CANFD0_ RX | UART 0_RXD | SPI0_MSI O | LPD_I2C0 _SCL | SWDT0_ WS0 | TTC 3_CLK |
| | NA | PMC_MIO 43_501 | PMC_G PIO43 | SD0/EMMC 0_DATA[2] | SD0/EMM C0_DATA[ 2] | SD0/EMM C0_DATA[ 2] | - | SD0/EMM C0_DATA[ 2] | SD0/EMM C0: DATA[2] | - | - | - | - | - | - | SMAP_IO[ 23] | - | GEM1: RGMII_TX _CTL | PMC_I2C _SDA | CANFD0_ TX | UART 0_TXD | SPI0_MO SI | LPD_I2C0 _SDA | SWDT0_ WS1 | TTC 3_WAVE |
| | NA | PMC_MIO 44_501 | PMC_G PIO44 | SD0/EMMC 0_DATA[3] | SD0/EMM C0_DATA[ 3] | SD0/EMM C0_DATA[ 3] | - | SD0/EMM C0_DATA[ 3] | SD0/EMM C0: DATA[3] | - | - | - | - | - | - | SMAP_IO[ 24] | - | GEM1: RGMII_RX _CLK | - | CANFD1_ TX | UART 0_CTS_B | SPI1_SCLK | LPD_I2C1 _SCL | SWDT1_C LK | TTC 2_CLK |
| | NA | PMC_MIO 45_501 | PMC_G PIO45 | - | SD0/EMM C0_SEL/D ATA[4] | SD0/EMM C0_SEL/D ATA[4] | - | - | SD0/EMM C0: SEL/DATA [4] | - | - | - | - | - | - | SMAP_IO[ 25] | - | GEM1: RGMII_RX D[0] | - | CANFD1_ RX | UART 0_RTS_B | SPI1_SS2_ B | LPD_I2C1 _SDA | SWDT1_R ST | TTC 2_WAVE |
| | NA | PMC_MIO 46_501 | PMC_G PIO46 | - | SD0/EMM C0_DIR_C MD/DATA [5] | - | - | - | SD0/EMM C0: DIR_CMD /DATA[5] | - | - | - | - | - | - | SMAP_IO[ 26] | - | GEM1: RGMII_RX D[1] | PMC_I2C _SCL | CANFD0_ RX | UART 1_TXD | SPI1_SS1_ B | LPD_I2C0 _SCL | SWDT1_R ST_PEND | TTC 1_CLK |
| | NA | PMC_MIO 47_501 | PMC_G PIO47 | - | SD0/EMM C0_DIR0/ DATA[6] | - | - | - | SD0/EMM C0: DIR0/DAT A[6] | - | - | - | - | - | - | SMAP_IO[ 27] | - | GEM1: RGMII_RX D[2] | PMC_I2C _SDA | CANFD0_ TX | UART 1_RXD | SPI1_SS0_ B | LPD_I2C0 _SDA | SWDT1_I NT | TTC 1_WAVE |
| | NA | PMC_MIO 48_501 | PMC_G PIO48 | - | SD0/EMM C0_DIR1/ DATA[7] | - | - | - | SD0/EMM C0: DIR1/DAT A[7] | - | - | - | - | - | - | SMAP_IO[ 28] | - | GEM1: RGMII_RX D[3] | - | CANFD1_ TX | UART 1_RTS_B | SPI1_MSI O | LPD_I2C1 _SCL | SWDT1_ WS0 | TTC 0_CLK |
| | NA | PMC_MIO 49_501 | PMC_G PIO49 | SD0/EMMC 0_BUSPWR /RST | SD0/EMM C0_BUSP WR/RST | SD0/EMM C0_BUSP WR/RST | SD0/EMM C0_BUSP WR/RST | SD0/EMM C0_BUSP WR/RST | SD0/EMM C0: BUSPWR/ RST | - | - | - | - | - | - | SMAP_IO[ 29] | - | GEM1: RGMII_RX _CTL | - | CANFD1_ RX | UART 1_CTS_B | SPI1_MO SI | LPD_I2C1 _SDA | SWDT1_ WS1 | TTC 0_WAVE |
| **QSPI** | NA | PMC_MIO 0_500 | PMC_G PIO0 | QSPI0_CLK | QSPI0_CL K | QSPI0_CL K | QSPI0_CL K | QSPI0_CL K | QSPI0_CL K | QSPI0_CL K | OSPI_CLK | OSPI_CLK | SD1/EMM C1: CLK | SD1/EMM C1_CLK | SD1/EMM C1_CLK | SD1/EMM C1: CLK | SD1/EMM C1_CLK | SD1/EMM C1_CLK | - | CANFD0_ RX | UART 0_RXD | SPI0_SCLK | LPD_I2C1 _SCL | SWDT0_C LK | TTC3_CLK |
| | NA | PMC_MIO 1_500 | PMC_G PIO1 | QSPI0_IO[1] | QSPI0_IO[ 1] | QSPI0_IO[ 1] | QSPI: QSPI0_IO[ 1] | QSPI0_IO[ 1] | QSPI0_IO[ 1] | QSPI0_IO[ 1] | OSPI_IO[0 ] | OSPI_IO[0 ] | SD1_WP | SD1_WP | SD1: WP | - | - | - | - | CANFD0_ TX | UART 0_TXD | SPI0_SS2_ B | LPD_I2C1 _SDA | SWDT0_R ST | TTC3_WA VE |
| | NA | PMC_MIO 2_500 | PMC_G PIO2 | - | - | QSPI0_IO[ 2] | | QSPI0_IO[ 2] | QSPI0_IO[ 2] | QSPI0_IO[ 2] | OSPI_IO[1 ] | OSPI_IO[1 ] | SD1: DETECT | SD1_DETE CT | SD1: DETECT | - | - | - | PMC_I2C _SCL | CANFD1_ TX | UART 0_CTS_B | SPI0_SS1_ B | LPD_I2C0 _SCL | SWDT0_R ST_PEND | TTC 2_CLK |
| | NA | PMC_MIO 3_500 | PMC_G PIO3 | - | - | QSPI0_IO[ 3] | | QSPI0_IO[ 3] | QSPI0_IO[ 3] | QSPI0_IO[ 3] | OSPI_IO[2 ] | OSPI_IO[2 ] | SD1/EMM C1: CMD | SD1/EMM C1_CMD | SD1/EMM C1_CMD | SD1/EMM C1: CMD | SD1/EMM C1_CMD | SD1/EMM C1_CMD | PMC_I2C _SDA | CANFD1_ RX | UART 0_RTS_B | SPI0_SS0_ B | LPD_I2C0 _SDA | SWDT0_I NT | TTC 2_WAVE |

| Interface/ Function | B2B PIN No. | SoC pin Name | GPIO | Function 1 | Function 2 | Function 3 | Function 4 | Function 5 | Function 6 | Function 7 | Function 8 | Function 9 | Function 10 | Function 11 | Function 12 | Function 13 | Function 14 | Function 15 | Function 16 | Function 17 | Function 18 | Function 19 | Function 20 | Function 21 | Function 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | NA | PMC_MIO 4_500 | PMC_G PIO4 | QSPI0_IO[0] | QSPI0_IO[ 0] | QSPI0_IO[ 0] | QSPI0_IO[ 0] | QSPI0_IO[ 0] | QSPI0_IO[ 0] | QSPI0_IO[ 0] | OSPI_IO[3 ] | OSPI_IO[3 ] | SD1/EMM C1: DATA[0] | SD1/EMM C1_DATA[ 0] | SD1/EMM C1_DATA[ 0] | SD1/EMM C1: DATA[0] | SD1/EMM C1_DATA[ 0] | SD1/EMM C1_DATA[ 0] | - | CANFD0_ RX | UART 1_TXD | SPI0_MSI O | LPD_I2C1 _SCL | SWDT0_ WS0 | TTC 1_CLK |
| | NA | PMC_MIO 5_500 | PMC_G PIO5 | QSPI0_CS_B | QSPI0_CS _B | QSPI0_CS _B | QSPI0_CS _B | QSPI0_CS _B | QSPI0_CS _B | QSPI0_CS _B | OSPI_IO[4 ] | OSPI_IO[4 ] | SD1/EMM C1: DATA[1] | SD1/EMM C1_DATA[ 1] | SD1/EMM C1_DATA[ 1] | - | SD1/EMM C1_DATA[ 1] | SD1/EMM C1_DATA[ 1] | - | CANFD0_ TX | UART 1_RXD | SPI0_MO SI | LPD_I2C1 _SDA | SWDT0_ WS1 | TTC 1_WAVE |
| **USB 2.0** | NA | PMC_MIO 13_500 | PMC_G PIO13 | SD0/EMMC 0_DATA[0] | SD0/EMM C0_DATA[ 0] | SD0/EMM C0_DATA[ 0] | SD0/EMM C0_DATA[ 0] | SD0/EMM C0_DATA[ 0] | SD0/EMM C0_DATA[ 0] | USB_ULPI _RST | - | - | - | - | - | | - | - | - | CANFD0_ TX | UART 1_RXD | SPI0_SS2_ B | LPD_I2C1 _SDA | SWDT0_R ST | TTC 1_WAVE |
| | NA | PMC_MIO 14_500 | PMC_G PIO14 | SD0/EMMC 0_DATA[1] | SD0/EMM C0_DATA[ 1] | SD0/EMM C0_DATA[ 1] | - | SD0/EMM C0_DATA[ 1] | SD0/EMM C0_DATA[ 1] | USB_ULPI _DATA[0] | - | - | - | - | - | SMAP_IO[ 0] | - | - | PMC_I2C _SCL | CANFD1_ TX | UART 1_RTS_B | SPI0_SS1_ B | LPD_I2C0 _SCL | SWDT0_R ST_PEND | TTC 0_CLK |
| | NA | PMC_MIO 15_500 | PMC_G PIO15 | SD0/EMMC 0_DATA[2] | SD0/EMM C0_DATA[ 2] | SD0/EMM C0_DATA[ 2] | - | SD0/EMM C0_DATA[ 2] | SD0/EMM C0_DATA[ 2] | USB_ULPI _DATA[1] | - | - | - | - | - | SMAP_IO[ 1] | - | - | PMC_I2C _SDA | CANFD1_ RX | UART 1_CTS_B | SPI0_SS0_ B | LPD_I2C0 _SDA | SWDT0_I NT | TTC 0_WAVE |
| | NA | PMC_MIO 16_500 | PMC_G PIO16 | SD0/EMMC 0_DATA[3] | SD0/EMM C0_DATA[ 3] | SD0/EMM C0_DATA[ 3] | - | SD0/EMM C0: DATA[3] | SD0/EMM C0_DATA[ 3] | USB_ULPI _DATA[2] | - | - | - | - | - | SMAP_IO[ 2] | - | - | - | CANFD0_ RX | UART 0_RXD | SPI0_MSI O | LPD_I2C1 _SCL | SWDT0_ WS0 | TTC 3_CLK |
| | NA | PMC_MIO 17_500 | PMC_G PIO17 | SD0/EMMC 0_BUSPWR /RST | SD0/EMM C0_BUSP WR/RST | SD0/EMM C0_BUSP WR/RST | SD0/EMM C0_BUSP WR/RST | SD0/EMM C0_BUSP WR/RST | SD0/EMM C0_BUSP WR/RST | USB_ULPI _DATA[3] | - | - | - | - | - | SMAP_IO[ 3] | - | - | - | CANFD0_ TX | UART 0_TXD | SPI0_MO SI | LPD_I2C1 _SDA | SWDT0_ WS1 | TTC 3_WAVE |
| | NA | PMC_MIO 18_500 | PMC_G PIO18 | SD0/EMMC 0_CLK | SD0/EMM C0_CLK | SD0/EMM C0_CLK | SD0/EMM C0_CLK | SD0/EMM C0_CLK | SD0/EMM C0_CLK | USB_ULPI _CLK | - | - | - | - | - | SMAP_CL K | - | - | PMC_I2C _SCL | CANFD1_ TX | UART 0_CTS_B | SPI1_SCLK | LPD_I2C0 _SCL | SWDT1_C LK | TTC 2_CLK |
| | NA | PMC_MIO 19_500 | PMC_G PIO19 | - | SD0/EMM C0_SEL/D ATA[4] | SD0/EMM C0_SEL/D ATA[4] | - | - | SD0/EMM C0_SEL/D ATA[4] | USB_ULPI _DATA[4] | - | - | - | - | - | SMAP_CS _B | - | - | PMC_I2C _SDA | CANFD1_ RX | UART 0_RTS_B | SPI1_SS2_ B | LPD_I2C0 _SDA | SWDT1_R ST | TTC 2_WAVE |
| | NA | PMC_MIO 20_500 | PMC_G PIO20 | - | SD0/EMM C0_DIR_C MD/DATA [5] | - | - | - | SD0/EMM C0_DIR_C MD/DATA [5] | USB_ULPI _DATA[5] | - | - | - | - | - | SMAP_RD WR_B | - | - | - | CANFD0_ RX | UART 1_TXD | SPI1_SS1_ B | LPD_I2C1 _SCL | SWDT1_R ST_PEND | TTC 1_CLK |
| | NA | PMC_MIO 21_500 | PMC_G PIO21 | - | SD0/EMM C0_DIR0/ DATA[6] | - | - | - | SD0/EMM C0_DIR0/ DATA[6] | USB_ULPI _DATA[6] | - | - | - | - | - | SMAP_BU SY | - | - | - | CANFD0_ TX | UART 1_RXD | SPI1_SS0_ B | LPD_I2C1 _SDA | SWDT1_I NT | TTC 1_WAVE |
| | NA | PMC_MIO 22_500 | PMC_G PIO22 | - | SD0/EMM C0_DIR1/ DATA[7] | - | - | - | SD0/EMM C0_DIR1/ DATA[7] | USB_ULPI _DATA[7] | - | - | - | - | - | SMAP_IO[ 4] | - | - | PMC_I2C _SCL | CANFD1_ TX | UART 1_RTS_B | SPI1_MSI O | LPD_I2C0 _SCL | SWDT1_ WS0 | TTC 0_CLK |
| | NA | PMC_MIO 23_500 | PMC_G PIO23 | SD0/EMMC 0_CMD | SD0/EMM C0_CMD | SD0/EMM C0_CMD | SD0/EMM C0_CMD | SD0/EMM C0_CMD | SD0/EMM C0_CMD | USB_ULPI _DIR | - | - | - | - | - | SMAP_IO[ 5] | - | - | PMC_I2C _SDA | CANFD1_ RX | UART 1_CTS_B | SPI1_MO SI | LPD_I2C0 _SDA | SWDT1_ WS1 | TTC 0_WAVE |
| | NA | PMC_MIO 24_500 | PMC_G PIO24 | SD0_DETEC T | SD0_DETE CT | SD0_DETE CT | - | - | - | USB_ULPI _STP | - | - | - | - | - | SMAP_IO[ 6] | - | - | - | - | - | - | - | - | - |
| | NA | PMC_MIO 25_500 | PMC_G PIO25 | SD0_WP | SD0_WP | SD0_WP | - | - | - | USB_ULPI _NXT | - | - | - | - | - | SMAP_IO[ 7] | - | - | - | - | - | - | - | - | - |
| **GEM0** | NA | LPD_MIO0 _502 | LPD_GP IO0 | GEM0_TX_ CLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD1_ TX | UART 0_RXD | SPI0_SCLK | LPD_I2C1 _SCL | SWDT0_C LK | TTC 3_CLK |
| | NA | LPD_MIO1 _502 | LPD_GP IO1 | GEM0_TXD[ 0] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD1_ RX | UART 0_TXD | SPI0_SS2_ B | LPD_I2C1 _SDA | SWDT0_R ST | TTC 3_WAVE |
| | NA | LPD_MIO2 _502 | LPD_GP IO2 | GEM0_TXD[ 1] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD0_ RX | UART 0_CTS_B | SPI0_SS1_ B | LPD_I2C0 _SCL | SWDT0_R ST_PEND | TTC 2_CLK |
| | NA | LPD_MIO3 _502 | LPD_GP IO3 | GEM0_TXD[ 2] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD0_ TX | UART 0_RTS_B | SPI0_SS0_ B | LPD_I2C0 _SDA | SWDT0_I NT | TTC 2_WAVE |
| | NA | LPD_MIO4 _502 | LPD_GP IO4 | GEM0_TXD[ 3] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD1_ TX | UART 1_TXD | SPI0_MSI O | LPD_I2C1 _SCL | SWDT0_ WS0 | TTC 1_CLK |
| | NA | LPD_MIO5 _502 | LPD_GP IO5 | GEM0_TX_ CTRL | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD1_ RX | UART 1_RXD | SPI0_MO SI | LPD_I2C1 _SDA | SWDT0_ WS1 | TTC 1_WAVE |

| Interface/ Function | B2B PIN No. | SoC pin Name | GPIO | Function 1 | Function 2 | Function 3 | Function 4 | Function 5 | Function 6 | Function 7 | Function 8 | Function 9 | Function 10 | Function 11 | Function 12 | Function 13 | Function 14 | Function 15 | Function 16 | Function 17 | Function 18 | Function 19 | Function 20 | Function 21 | Function 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | NA | LPD_MIO6_502 | LPD_GPIO6 | GEM0_RX_CLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD0_RX | UART 1_RTS_B | SPI1_SCLK | LPD_I2C0_SCL | SWDT1_CLK | TTC 0_CLK |
| | NA | LPD_MIO7_502 | LPD_GPIO7 | GEM0_RXD[0] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD0_TX | UART 1_CTS_B | SPI1_SS2_B | LPD_I2C0_SDA | SWDT1_RST | TTC 0_WAVE |
| | NA | LPD_MIO8_502 | LPD_GPIO8 | GEM0_RXD[1] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD1_TX | UART 0_RXD | SPI1_SS1_B | LPD_I2C1_SCL | SWDT1_RST_PEND | TTC 3_CLK |
| | NA | LPD_MIO9_502 | LPD_GPIO9 | GEM0_RXD[2] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD1_RX | UART 0_TXD | SPI1_SS0_B | LPD_I2C1_SDA | SWDT1_INT | TTC 3_WAVE |
| | NA | LPD_MIO10_502 | LPD_GPIO10 | GEM0_RXD[3] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD0_RX | UART 0_CTS_B | SPI1_MSIO | LPD_I2C0_SCL | SWDT1_WS0 | TTC 2_CLK |
| | NA | LPD_MIO11_502 | LPD_GPIO11 | GEM0_RX_CTRL | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD0_TX | UART 0_RTS_B | SPI1_MOSI | LPD_I2C0_SDA | SWDT1_WS1 | TTC 2_WAVE |
| **Board to Board Connector Interfaces from PS MIO** | | | | | | | | | | | | | | | | | | | | | | | | | |
| **SPI** | D16 | PMC_MIO6_500 | PMC_GPIO6 | QSPI_LPBK | LOOPBACK CLK: QSPI_LPBK | LOOPBACK CLK: QSPI_LPBK | QSPI_LPBK | QSPI_LPBK | QSPI_LPBK | QSPI_LPBK | OSPI_DS | OSPI_DS | SD1/EMMC1: DATA[2] | SD1/EMMC1_DATA[2] | SD1/EMMC1_DATA[2] | - | SD1/EMMC1_DATA[2] | SD1/EMMC1_DATA[2] | PMC_I2C_SCL | CANFD1_TX | UART 1_RTS_B | SPI1_SCLK | LPD_I2C0_SCL | SWDT1_CLK | TTC 0_CLK |
| | D19 | PMC_MIO7_500 | PMC_GPIO7 | - | - | - | QSPI1_CS_B | QSPI1_CS_B | QSPI: QSPI1_CS_B | QSPI1_CS_B | OSPI_IO[5] | OSPI_IO[5] | SD1/EMMC1: DATA[3] | SD1/EMMC1_DATA[3] | SD1/EMMC1_DATA[3] | - | - | SD1/EMMC1_DATA[3] | PMC_I2C_SDA | CANFD1_RX | UART 1_CTS_B | SPI0_SS2_B | LPD_I2C0_SDA | SWDT1_RST | TTC 0_WAVE |
| | D20 | PMC_MIO8_500 | PMC_GPIO8 | - | - | - | - | - | - | QSPI1_IO[0] | OSPI_IO[6] | OSPI_IO[6] | - | SD1/EMMC1_SEL/DATA[4] | SD1/EMMC1_SEL/DATA[4] | - | - | SD1/EMMC1_SEL/DATA[4] | - | CANFD0_RX | UART 0_RXD | SPI1_SS1_B | LPD_I2C1_SCL | SWDT1_RST_PEND | TTC 3_CLK |
| | D21 | PMC_MIO9_500 | PMC_GPIO9 | - | - | - | - | - | - | QSPI1_IO[1] | OSPI_IO[7] | OSPI_IO[7] | - | SD1/EMMC1_DIR_CMD/DATA[5] | - | - | - | SD1/EMMC1_DIR_CMD/DATA[5] | - | CANFD0_TX | UART 0_TXD | SPI1_SS0_B | LPD_I2C1_SDA | SWDT1_INT | TTC 3_WAVE |
| | D18 | PMC_MIO10_500 | PMC_GPIO10 | - | - | - | - | - | - | QSPI1_IO[2] | OSPI0_CS_B | OSPI0_CS_B | - | SD1/EMMC1_DIR0/DATA[6] | - | - | - | SD1/EMMC1_DIR0/DATA[6] | PMC_I2C_SCL | CANFD1_TX | UART 0_CTS_B | SPI1_MSIO | LPD_I2C0_SCL | SWDT1_WS0 | TTC 2_CLK |
| | D17 | PMC_MIO11_500 | PMC_GPIO11 | - | - | - | - | - | - | QSPI1_IO[3] | - | OSPI1_CS_B | - | SD1/EMMC1_DIR1/DATA[7] | - | - | - | SD1/EMMC1_DIR1/DATA[7] | PMC_I2C_SDA | CANFD1_RX | UART 0_RTS_B | SPI1_MOSI | LPD_I2C0_SDA | SWDT1_WS1 | TTC 2_WAVE |
| **GPIO** | C14 | PMC_MIO12_500 | PMC_GPIO12 | - | - | - | - | - | - | QSPI1_CLK | - | - | SD1/EMMC1_BUSPWR/RST | SD1/EMMC1_BUSPWR/RST | SD1/EMMC1_BUSPWR/RST | SD1/EMMC1_BUSPWR/RST | SD1/EMMC1_BUSPWR/RST | SD1/EMMC1_BUSPWR/RST | - | CANFD0_RX | UART 1_TXD | SPI0_SCLK | LPD_I2C1_SCL | SWDT0_CLK | TTC 1_CLK |
| **SD1** | B23 | PMC_MIO26_501 | PMC_GPIO26 | - | - | - | - | - | - | SD1/EMMC1_CLK | SD1/EMMC1_CLK | SD1/EMMC1_CLK | SD1/EMMC1_CLK | SD1/EMMC1_CLK | SD1/EMMC1_CLK | | GEM0_TX_CLK | - | PMC_I2C_SCL | CANFD0_RX | UART 0_RXD | SPI0_SCLK | LPD_I2C0_SCL | SWDT0_CLK | TTC 3_CLK |
| | B21 | PMC_MIO27_501 | PMC_GPIO27 | - | - | - | - | - | - | | SD1/EMMC1_DIR1/DATA[7] | | | | SD1/EMMC1_DIR1/DATA[7] | | GEM0_TXD[0] | - | PMC_I2C_SDA | CANFD0_TX | UART 0_TXD | SPI0_SS2_B | LPD_I2C0_SDA | SWDT0_RST | TTC 3_WAVE |
| | B29 | PMC_MIO28_501 | PMC_GPIO28 | - | - | - | - | - | - | SD1: DETECT | SD1_DETECT | SD1_DETECT | | | | SMAP_IO[8] | GEM0_TXD[1] | - | - | CANFD1_TX | UART 0_CTS_B | SPI0_SS1_B | LPD_I2C1_SCL | SWDT0_RST_PEND | TTC 2_CLK |
| | B24 | PMC_MIO29_501 | PMC_GPIO29 | - | - | - | - | - | - | SD1/EMMC1_CMD | SD1/EMMC1_CMD | SD1/EMMC1_CMD | SD1/EMMC1_CMD | SD1/EMMC1_CMD | SD1/EMMC1_CMD | SMAP_IO[9] | GEM0_TXD[2] | - | - | CANFD1_RX | UART 0_RTS_B | SPI0_SS0_B | LPD_I2C1_SDA | SWDT0_INT | TTC 2_WAVE |
| | B25 | PMC_MIO30_501 | PMC_GPIO30 | - | - | - | - | - | - | SD1/EMMC1_DATA[0] | SD1/EMMC1_DATA[0] | SD1/EMMC1_DATA[0] | SD1/EMMC1_DATA[0] | SD1/EMMC1_DATA[0] | SD1/EMMC1_DATA[0] | SMAP_IO[10] | GEM0_TXD[3] | - | PMC_I2C_SCL | CANFD0_RX | UART 1_TXD | SPI0_MSIO | LPD_I2C0_SCL | SWDT0_WS0 | TTC 1_CLK |
| | B26 | PMC_MIO31_501 | PMC_GPIO31 | - | - | - | - | - | - | SD1/EMMC1_DATA[1] | SD1/EMMC1_DATA[1] | SD1/EMMC1_DATA[1] | | SD1/EMMC1_DATA[1] | SD1/EMMC1_DATA[1] | SMAP_IO[11] | GEM0_TX_CTRL | - | PMC_I2C_SDA | CANFD0_TX | UART 1_RXD | SPI0_MOSI | LPD_I2C0_SDA | SWDT0_WS1 | TTC 1_WAVE |
| | B27 | PMC_MIO32_501 | PMC_GPIO32 | - | - | - | - | - | - | SD1/EMMC1_DATA[2] | SD1/EMMC1_DATA[2] | SD1/EMMC1_DATA[2] | | SD1/EMMC1_DATA[2] | SD1/EMMC1_DATA[2] | SMAP_IO[12] | GEM0_RX_CLK | - | - | CANFD1_TX | UART 1_RTS_B | SPI1_SCLK | LPD_I2C1_SCL | SWDT1_CLK | TTC 0_CLK |

| Interface/ Function | B2B PIN No. | SoC pin Name | GPIO | Function 1 | Function 2 | Function 3 | Function 4 | Function 5 | Function 6 | Function 7 | Function 8 | Function 9 | Function 10 | Function 11 | Function 12 | Function 13 | Function 14 | Function 15 | Function 16 | Function 17 | Function 18 | Function 19 | Function 20 | Function 21 | Function 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | B28 | PMC_MIO 33_501 | PMC_G PIO33 | - | - | - | - | - | - | SD1/EMM C1_DATA[ 3] | SD1/EMM C1_DATA[ 3] | SD1/EMM C1_DATA[ 3] | | SD1/EMM C1_DATA[ 3] | SD1/EMM C1_DATA[ 3] | SMAP_IO[ 13] | GEM0_RX D[0] | - | - | CANFD1_ RX | UART 1_CTS_B | SPI1_SS2_ B | LPD_I2C1 _SDA | SWDT1_R ST | TTC 0_WAVE |
| **UART0** | A14 | PMC_MIO 34_501 | PMC_G PIO34 | - | - | - | - | - | - | - | SD1/EMM C1_SEL/D ATA[4] | SD1/EMM C1_SEL/D ATA[4] | | | SD1/EMM C1_SEL/D ATA[4] | SMAP_IO[ 14] | GEM0_RX D[1] | - | PMC_I2C _SCL | CANFD0_ RX | UART 0_RXD | SPI1_SS1_ B | LPD_I2C0 _SCL | SWDT1_R ST_PEND | TTC 3_CLK |
| | A13 | PMC_MIO 35_501 | PMC_G PIO35 | - | - | - | - | - | - | - | SD1/EMM C1_DIR_C MD/DATA [5] | - | - | - | SD1/EMM C1_DIR_C MD/DATA [5] | SMAP_IO[ 15] | GEM0_RX D[2] | - | PMC_I2C _SDA | CANFD0_ TX | UART 0_TXD | SPI1_SS0_ B | LPD_I2C0 _SDA | SWDT1_I NT | TTC 3_WAVE |
| **CANFD1** | D28 | PMC_MIO 36_501 | PMC_G PIO36 | - | - | - | - | - | - | - | SD1/EMM C1_DIR0/ DATA[6] | - | - | - | SD1/EMM C1_DIR0/ DATA[6] | SMAP_IO[ 16] | GEM0_RX D[3] | - | - | CANFD1_ TX | UART 0_CTS_B | SPI1_MSI O | LPD_I2C1 _SCL | SWDT1_ WS0 | TTC 2_CLK |
| | D27 | PMC_MIO 37_501 | PMC_G PIO37 | SD0: WP | SD0: WP | SD0: WP | - | - | - | | | - | - | - | - | SMAP_IO[ 17] | GEM0_RX _CTRL | - | - | CANFD1_ RX | UART 0_RTS_B | SPI1_MO SI | LPD_I2C1 _SDA | SWDT1_ WS1 | TTC 2_WAVE |
| **I2C** | C8 | PMC_MIO 50_501 | PMC_G PIO50 | GEM0_MDI O_CLK | GEM1_M DIO_CLK | GEM_TSU _CLK | - | - | - | SD1_WP | SD1_WP | SD1_WP | - | - | - | SMAP_IO[ 30] | GEM0_M DIO_CLK | GEM1_M DIO_CLK | PMC_I2C _SCL | - | - | - | - | - | - |
| | C9 | PMC_MIO 51_501 | PMC_G PIO51 | GEM0_MDI O_DATA | GEM1_M DIO_DAT A | GEM_TSU _CLK | - | - | - | SD1/EMM C1_BUSP WR/RST | SD1/EMM C1_BUSP WR/RST | SD1/EMM C1_BUSP WR/RST | SD1/EMM C1_BUSP WR/RST | SD1/EMM C1_BUSP WR/RST | SD1/EMM C1_BUSP WR/RST | SMAP_IO[ 31] | GEM0_M DIO_DAT A | GEM1_M DIO_DAT A | PMC_I2C _SDA | - | - | - | - | - | - |
| **GEM1** | C16 | LPD_MIO1 2_502 | LPD_GP IO12 | - | GEM1_TX _CLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD1_ TX | UART 1_TXD | SPI0_SCLK | LPD_I2C1 _SCL | SWDT0_C LK | TTC 1_CLK |
| | C17 | LPD_MIO1 3_502 | LPD_GP IO13 | - | GEM1_TX D[0] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD1_ RX | UART 1_RXD | SPI0_SS2_ B | LPD_I2C1 _SDA | SWDT0_R ST | TTC 1_WAVE |
| | C18 | LPD_MIO1 4_502 | LPD_GP IO14 | - | GEM1_TX D[1] | - | - | - | - | - | - | - | - | - | - | - | - | - | - | CANFD0_ RX | UART 1_RTS_B | SPI0_SS1_ B | LPD_I2C0 _SCL | SWDT0_R ST_PEND | TTC 0_CLK |
| | C19 | LPD_MIO1 5_502 | LPD_GP IO15 | | GEM1_TX D[2] | | | | | | | | | | | | | | | CANFD0_ TX | UART 1_CTS_B | SPI0_SS0_ B | LPD_I2C0 _SDA | SWDT0_I NT | TTC 0_WAVE |
| | C20 | LPD_MIO1 6_502 | LPD_GP IO16 | | GEM1_TX D[3] | | | | | | | | | | | | | | | CANFD1_ TX | UART 0_RXD | SPI0_MSI O | LPD_I2C1 _SCL | SWDT0_ WS0 | TTC 3_CLK |
| | C21 | LPD_MIO1 7_502 | LPD_GP IO17 | | GEM1_TX _CTRL | | | | | | | | | | | | | | | CANFD1_ RX | UART 0_TXD | SPI0_MO SI | LPD_I2C1 _SDA | SWDT0_ WS1 | TTC 3_WAVE |
| | C23 | LPD_MIO1 8_502 | LPD_GP IO18 | | GEM1_RX _CLK | | | | | | | | | | | | | | | CANFD0_ RX | UART 0_CTS_B | SPI1_SCLK | LPD_I2C0 _SCL | SWDT1_C LK | TTC 2_CLK |
| | C24 | LPD_MIO1 9_502 | LPD_GP IO19 | | GEM1_RX D[0] | | | | | | | | | | | | | | | CANFD0_ TX | UART 0_RTS_B | SPI1_SS2_ B | LPD_I2C0 _SDA | SWDT1_R ST | TTC 2_WAVE |
| | C25 | LPD_MIO2 0_502 | LPD_GP IO20 | | GEM1_RX D[1] | | | | | | | | | | | | | | | CANFD1_ TX | UART 1_TXD | SPI1_SS1_ B | LPD_I2C1 _SCL | SWDT1_R ST_PEND | TTC 1_CLK |
| | C26 | LPD_MIO2 1_502 | LPD_GP IO21 | | GEM1_RX D[2] | | | | | | | | | | | | | | | CANFD1_ RX | UART 1_RXD | SPI1_SS0_ B | LPD_I2C1 _SDA | SWDT1_I NT | TTC 1_WAVE |
| | C27 | LPD_MIO2 2_502 | LPD_GP IO22 | | GEM1_RX D[3] | | | | | | | | | | | | | | | CANFD0_ RX | UART 1_RTS_B | SPI1_MSI O | LPD_I2C0 _SCL | SWDT1_ WS0 | TTC 0_CLK |
| | C28 | LPD_MIO2 3_502 | LPD_GP IO23 | | GEM1_RX _CTRL | | | | | | | | | | | | | | | CANFD0_ TX | UART 1_CTS_B | SPI1_MO SI | LPD_I2C0 _SDA | SWDT1_ WS1 | TTC 0_WAVE |
| | C12 | LPD_MIO2 4_502 | LPD_GP IO24 | GEM0_MDI O_CLK | GEM0_M DIO_CLK | GEM_TSU _CLK | | | | | | | | | | | GEM0_M DIO_CLK | GEM1_M DIO_CLK | | CANFD1_ TX | | | LPD_I2C1 _SCL | | |
| | C13 | LPD_MIO2 5_502 | LPD_GP IO25 | GEM0_MDI O_DATA | GEM0_M DIO_DAT A | GEM_TSU _CLK | | | | | | | | | | | GEM0_M DIO_DAT A | GEM1_M DIO_DAT A | | CANFD1_ RX | | | LPD_I2C1 _SDA | | |
| **JTAG** | A9 | TCK_503 | - | JTAG_TCK | | | | | | | | | | | | | | | | | | | | | |
| | A12 | TDI_503 | - | JTAG_TDI | | | | | | | | | | | | | | | | | | | | | |
| | A11 | TDO_503 | - | JTAG_TDO | | | | | | | | | | | | | | | | | | | | | |
| | A10 | TMS_503 | - | JTAG_TMS | | | | | | | | | | | | | | | | | | | | | |

# 3. TECHNICAL SPECIFICATION

This section provides detailed information about the Versal AI Edge SOM technical specification with Electrical, Environmental and Mechanical characteristics.

## 3.1 Electrical Characteristics

### 3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Versal AI Edge SOM .

**Table 26: Power Input Requirement**

| Sl. No. | Power Rail | Min (V) | Typical (V) | Max(V) | Max Input Ripple |
|---|---|---|---|---|---|
| **1** | VCC_5V[1] | 4.75V | 5V | 5.25V | ±50mV |
| **2** | VRTC_3V0[2] | 0V | 3V | 3.15V | ±20mV |

*[1]Versal AI Edge SOM is designed to work with VCC_5V input power rail from Board-to-Board Connector2.*

*[2]Versal AI Edge SOM uses this voltage as backup power source to PMIC RTC when VCC_5V is off. This is an optional power and required only if RTC functionality is used.*

### 3.1.2 Power Input Sequencing

The Versal AI Edge SOM Power Input sequence requirement is explained below.

**Power up Sequence:**

- VRTC_3V0 must come up at the same time or before VCC_5V comes up.
- SOM_PWR_EN signal from Board-to-Board Connector2 must be high at the same time or after VCC_5V comes up.

**Power down Sequence:**

- SOM_PWR_EN signal from Board-to-Board Connector1 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_3V0 goes down.

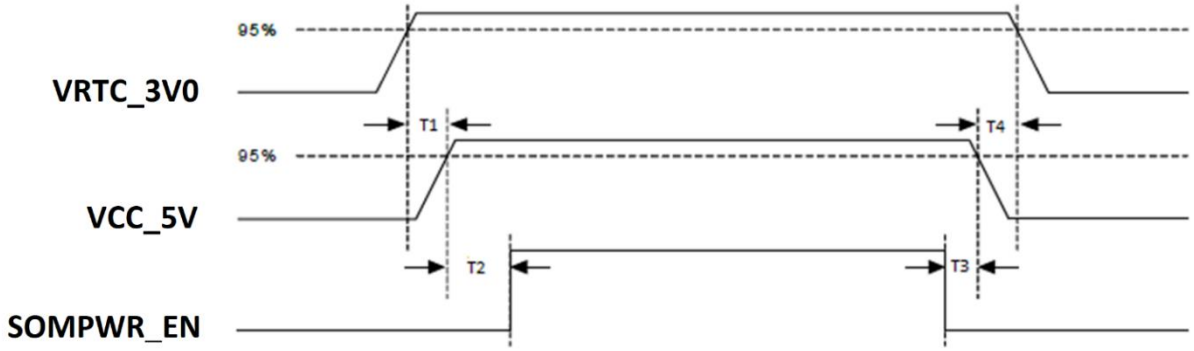


**Figure 6: Power Input Sequencing**

**Table 27: Power Sequence Timing**

| Item | Description | Value |
|---|---|---|
| T1 | VRTC_3V0[1] rise time to VCC_5V rise time | ≥ 0 ms |
| T2 | VCC_5V rise time to SOMPWR_EN rise time | ≥ 0 ms |
| T3 | SOMPWR_EN fall time to VCC_5V fall time | ≥ 0 ms |
| T4 | VCC_5V fall time to VRTC_3V0 fall time | ≥ 0 ms |

*[1] VRTC_3V0 is the RTC Battery backup supply. This is an optional power.*

### 3.1.3 Power Consumption

TBD

## 3.2 Environmental Characteristics

### 3.2.1 Temperature Specification

The below table provides the Environment specification of Versal AI Edge SOM

**Table 28: Temperature Specification**

| Parameters | Min | Max |
|---|---|---|
| Operating temperature range - Industrial[1] | -40°C | 85°C |
| Operating temperature range - Extended[1] | 0°C | 85°C |

*[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.*

### 3.2.2 RoHS2 Compliance

iWave's Versal AI Edge SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

### 3.2.3 Electrostatic Discharge

iWave's Versal AI Edge SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

## 3.3 Mechanical Characteristics

### 3.3.1 Versal AI Edge SOM Mechanical Dimensions

Versal AI Edge SOM PCB size is 50mm x 60mm x 1.83mm. SOM mechanical dimension is shown below.

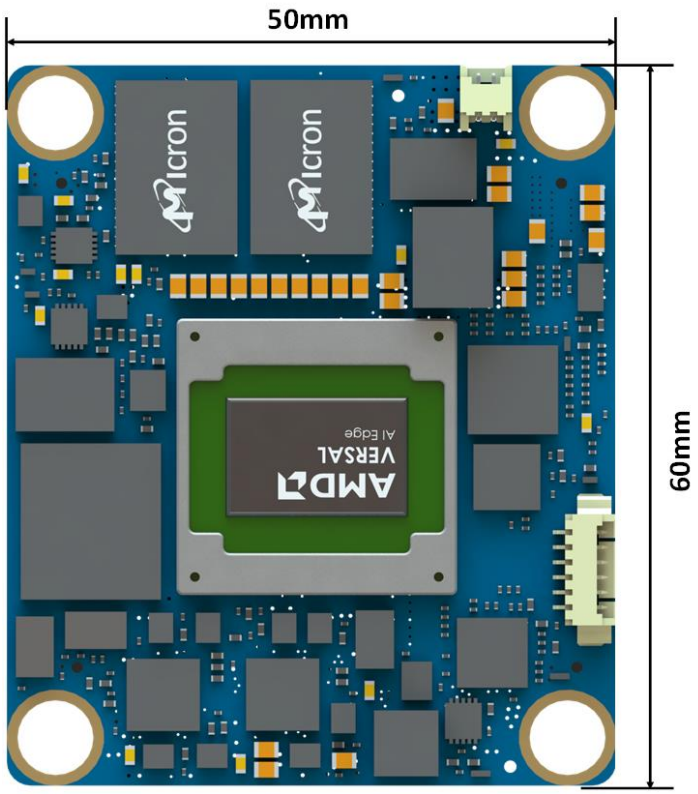


**Figure 7: Mechanical dimension of Versal AI Edge SOM SOM - Top View**

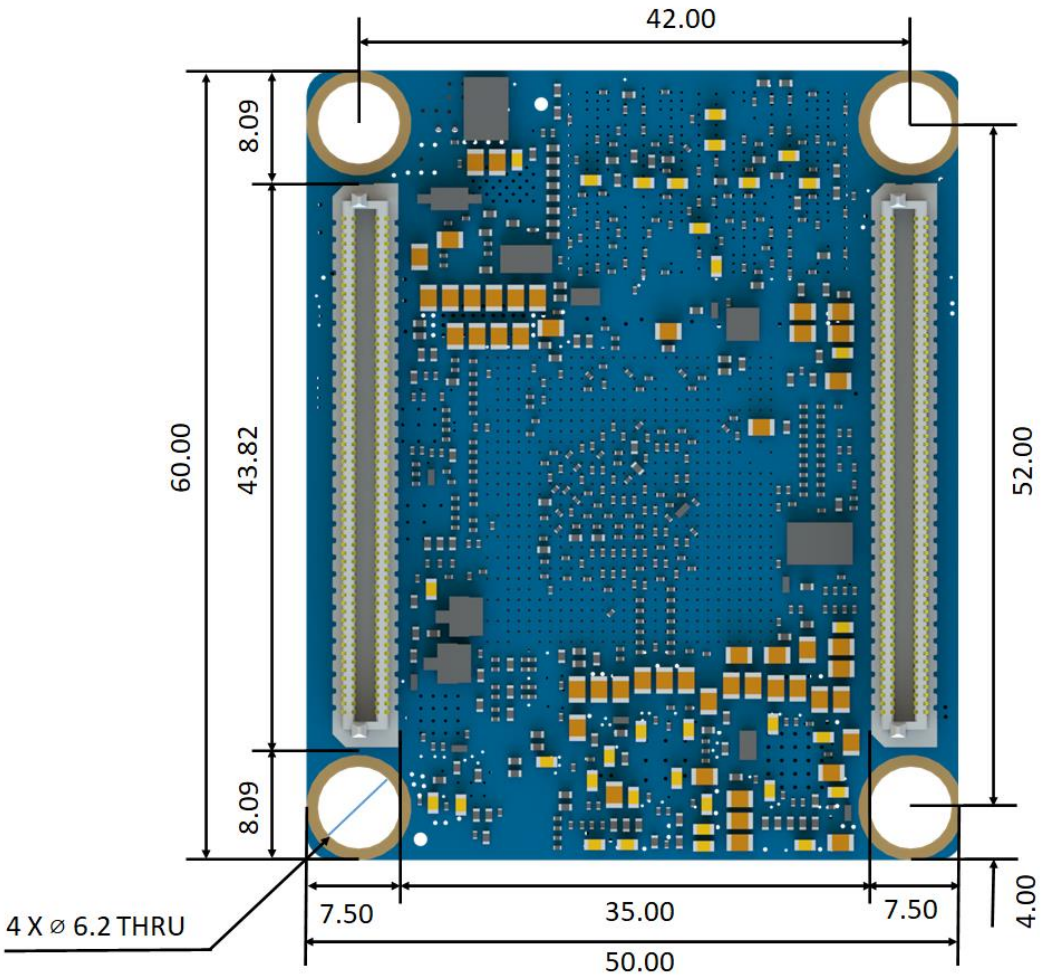


**Figure 8: Mechanical dimension of Versal AI Edge SOM - Bottom View**

Versal AI Edge SOM, PCB thickness is 1.83mm ±0.1mm, top side maximum height component is Fan header with height of 3.5mm and bottom side maximum height component is Board to Board connector 1 & 2 (4.1mm). Please refer the below figure which gives height details of Versal SOM.

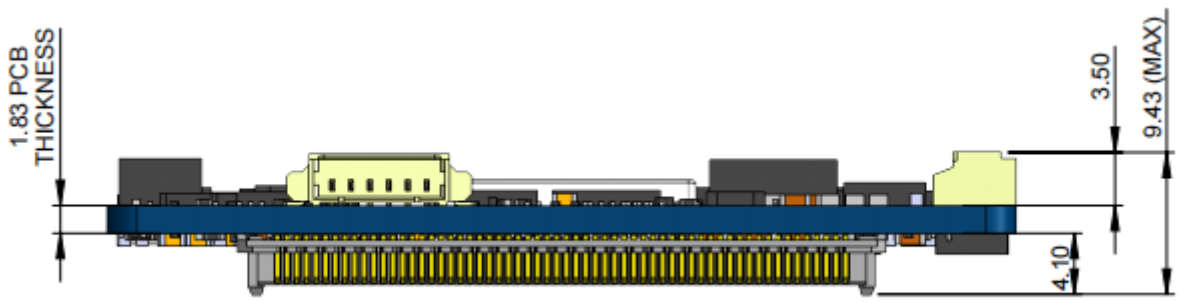


**Figure 9: Top and Bottom Maximum Heighted Component**

# 4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Versal AI Edge SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

**Table 29: Orderable Product Part Numbers**

| Product Part Number | Description | Temperature |
|---|---|---|
| **TBD** | | |

# 5. APPENDIX

## 5.1 Versal AI Edge SOM Development Platform

iWave Systems supports iW-RainboW-G57M– Versal AI Edge SOM Development Platform which is targeted for quick validation of Versal based SOM. iWave's Versal AI Edge Development Board incorporates Versal AI Edge SOM and High-performance Carrier board with complete BSP support.

Contact us for more details on Versal AI Edge SOM Development Platform.

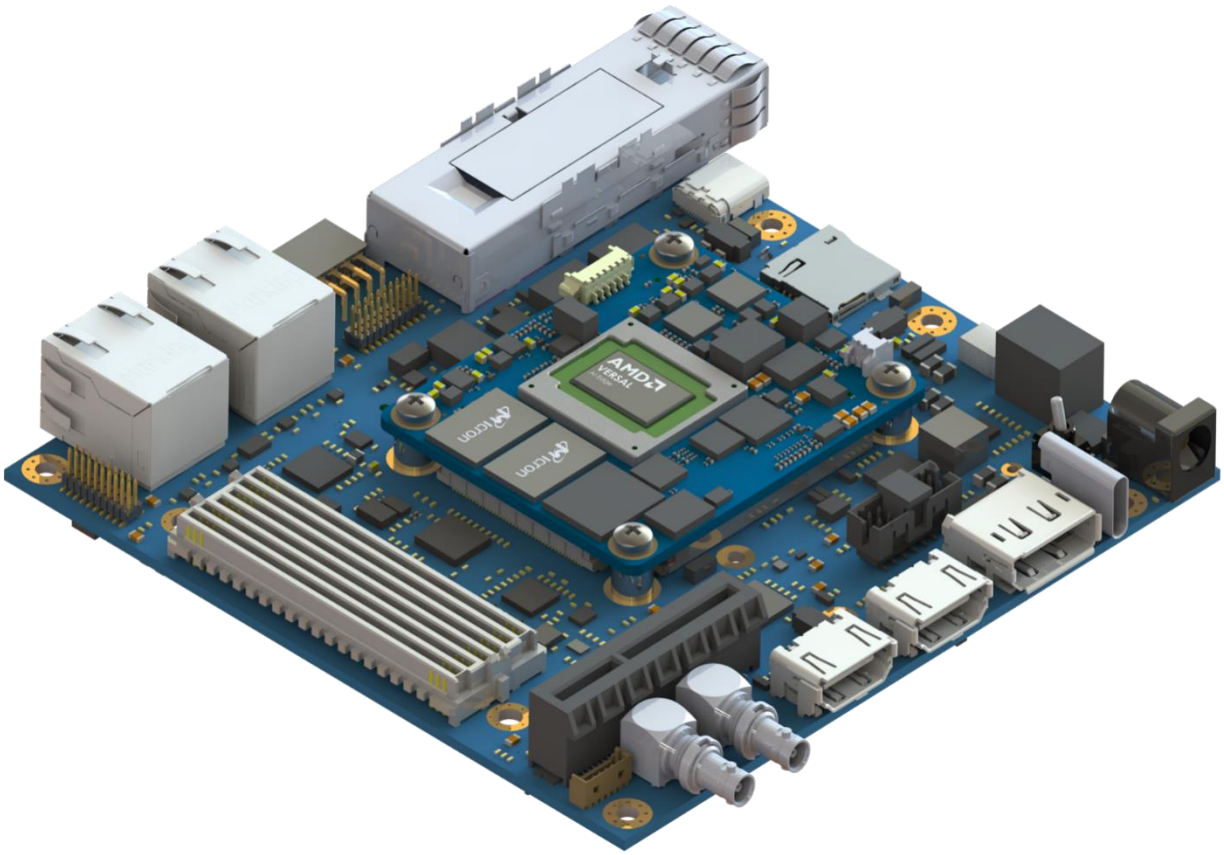

**Figure 10: Versal AI Edge Development Platform**


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