Key Design Features

- Synthesizable, technology independent IP Core for FPGA, ASIC and SoC
- Supplied as human-readable VHDL (or Verilog) source code
- Test patterns generated as an industry standard 20-bit 4:2:2 SMPTE stream
- YCbCr 4:2:2 output pixels
- All 720p, 1080p and 1080i video formats supported (SMPTE 296M and SMPTE 274M)
- Colour-bar output with choice off 8 different patterns
- All signals synchronous with the pixel clock
- Compatible with a wide range of video encoder ICs
- Tiny implementation size makes the core suitable for even the smallest FPGAs and CPLDs

Applications

- Digital video testing and prototyping
- Default output displays and simple 'screen savers'

Generic Parameters

Generic name	*Description*	*Type*	*Valid range*
hd_mode	Output video mode	integer	0: 720p 1: 1080p 2: 1080i

Pin-out Description

Pin name	*I/O*	*Description*	*Active state*
clk	in	Pixel clock (e.g. 148.5 MHz or 74.25 MHz depending on the required video stndard)	rising edge
reset	in	Asynchronous reset	low
tpg_type [2:0]	in	000 : bars 001 : blues 010 : reds 011 : greens 100 : yellows 101 : browns 110 : purples 111 : greys	data
video_ln [11:0]	out	Output video line number	data
video_y [9:0]	out	Y-channel video output	data
video_c [7:0]	out	C-channel video output	data
video_val	out	SMPTE output video stream valid	high

Block Diagram

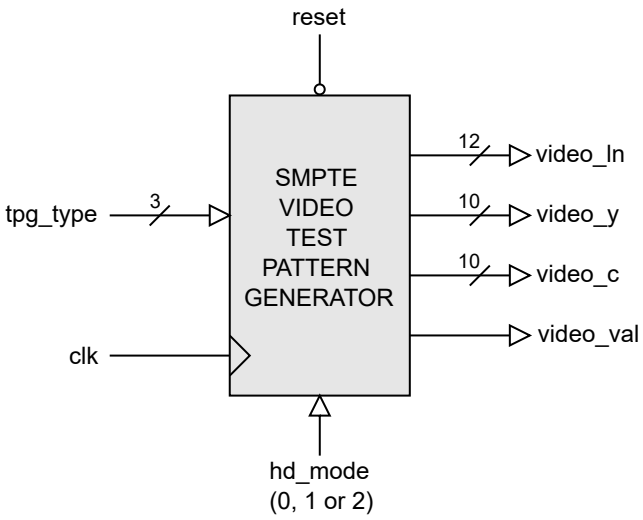

Figure 1: SMPTE Test pattern generator

General Description

The HD_SMPTE_TPG IP Core (Figure 1) is a versatile test pattern generator capable of producing a range of test patterns in 20-bit 4:2:2 format. The output stream format is compliant with the SMPTE standards 296M and 274M. The module is ideal for use in the prototyping stages of digital video systems or as a known good reference source for standard 720p, 1080p or 1080i video.

The video mode is controlled by the generic parameter *hd_mode* and the video test pattern can be set using the parameter *tpg_type*. In total there are 8 different test patterns to choose from.

The output video is a standard SMPTE 20-bit stream that is synchronous with the *clk* signal. The clock frequency should be set to the value that corresponds to the correct pixel clock frequency for the corresponding video mode. For instance, the clock frequency should be set to 74.25 MHz for 720p60, 1080p30 or 1080i60 modes. A clock frequency of 148.5 MHz should be chosen for 1080p60.

Test pattern type

By modifying the test pattern type, the colour and appearance of the test pattern may be controlled. Figure 2 on the following page gives a description of each pattern available[1].

The test pattern type may be programmed in real-time during normal operation. The images shown are for a single frame of a 720p60 video (SMPTE 296M). The video blanking regions are also shown. Note that the vertical blue lines are where the EAV and SAV codes are positioned in the video stream.

1 Additional test patterns may be provided on request. Please contact Zipcores for more information.

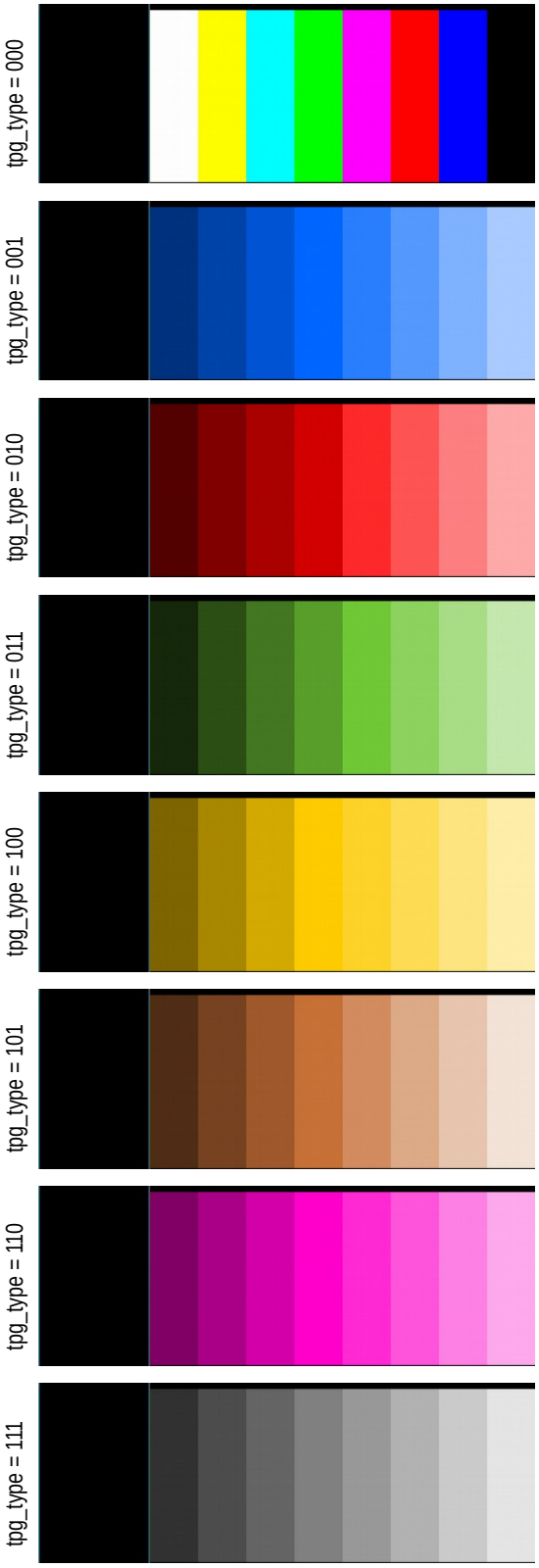

Figure 2: Different test pattern types. An SMPTE 296M (720p) output video stream is shown as an example

Functional Timing

An example output waveform is shown in Figure 3 below. The 20-bit Y/C output data is valid on the rising clock-edge of *clk* when *video_val* is high.

The *video_val* signal is active high one clock cycle after system reset. The current active line number is provided by the *video_ln* signal which is a value from 0 to N. So for example, a 720p format stream has 750 lines in total (including blanking). This means that the video line number will run from 0 to 749.

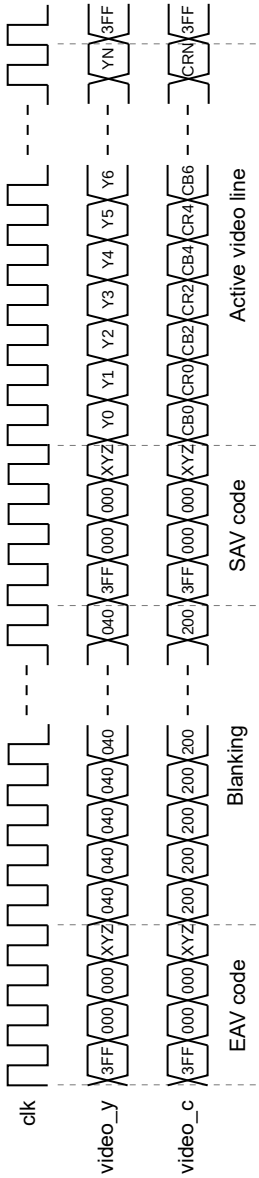

Figure 3: Typical SMPTE 296M/274M output stream

(Note: video_val and video_ln signals not shown)

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief explanation of each file.

Source file	Description
smpte_296m_tpg_720p.vhd	SMPTE 720 (progressive) core module
smpte_274m_tpg_1080i.vhd	SMPTE 1080 (interlaced) core module
smpte_274m_tpg_1080p.vhd	SMPTE 1080 (progressive) core module
hd_smpte_tpg.vhd	Top-level component
hd_smpte_tpg_bench.vhd	Top-level testbench

Functional Testing

An example VHDL test bench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. smpte_296m_tpg_720p.vhd
2. smpte_274m_tpg_1080i.vhd
3. smpte_274m_tpg_1080p.vhd
4. hd_smpte_tpg.vhd
5. hd_smpte_tpg_bench.vhd

The VHDL test bench instantiates the HD_SMPTE_TPG IP Core with the video format set to 720p60 and the output test pattern set to '000' (regular colour bars).

The simulation must be run for at least 20 ms during which time the outputs are captured to a text file called *smpte_out.txt.* This file contains the captured SMPTE stream with each 20-bit Y/C value captured on a consecutive line.

Synthesis and Implementation

The files required for synthesis and the design hierarchy is shown below:

- hs_smpte_tpg.vhd
  - smpte_296m_tpg_720p.vhd
  - smpte_274m_tpg_1080i.vhd
  - smpte_274m_tpg_1080p.vhd

The IP Core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx® 7-series FPGAs. Synthesis results for other FPGAs and technologies can be provided on request.

If the video_y and video_c output video signals are designed to be external signals, then we recommend placing these signals in the I/O or pads of the device. They should also be placed locally together to limit the timing skew between individual bits. Other than this, there are no special constraints required for synthesis. The IP Core is completely technology independent.

Trial synthesis results are shown with the generic *hd_mode* parameter set to '0' for 720p video.

The resource usage is specified after place and route.

XILINX® 7-SERIES FPGAS

Resource type	Artix-7	Kintex-7	Virtex-7
Slice Register	69	69	69
Slice LUTs	213	194	198
Block RAM	0	0	0
DSP48	0	0	0
Occupied Slices	65	58	61
Clock freq. (approx)	250 MHz	300 MHz	350 MHz

Revision History

Revision	Change description	Date
1.0	Initial revision	18/10/2019
1.1	First official release	08/11/2019